

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe TO-252 saves board space.
- Fast Switch Speed.
- High performance trench technology.

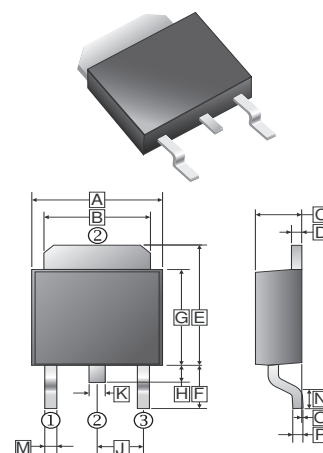
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

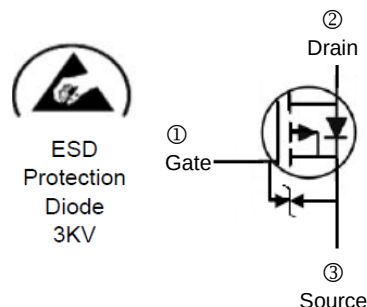
PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	J	2.30	REF.
B	5.20	5.50	K	0.64	0.90
C	2.15	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.65
E	6.8	7.5	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.25			
H	0.64	1.20			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	-36	A
Pulsed Drain Current @ $T_A=25^{\circ}\text{C}$ ²	I_{DM}	-40	A
Continuous Source Current (Diode Conduction) ¹	I_S	-30	A
Total Power Dissipation @ $T_A=25^{\circ}\text{C}$ ¹	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^{\circ}\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	50	$^{\circ}\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3	$^{\circ}\text{C} / \text{W}$

Notes :

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

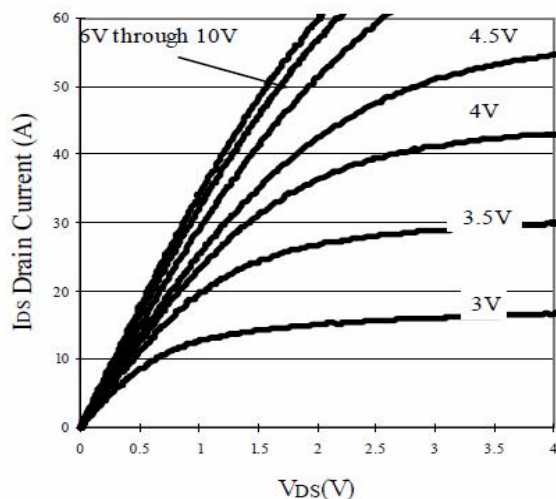
ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS} = V_{GS}$, $I_D = -250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0$, $V_{GS} = \pm 25\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -24\text{V}$, $V_{GS} = 0$
		-	-	-5		$V_{DS} = -24\text{V}$, $V_{GS} = 0$, $T_J = 55^{\circ}\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-41	-	-	A	$V_{DS} = -5\text{V}$, $V_{GS} = -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	30	m Ω	$V_{GS} = -10\text{V}$, $I_D = -36\text{A}$
		-	-	40		$V_{GS} = -4.5\text{V}$, $I_D = -29\text{A}$
Forward Transconductance ¹	g_{fs}	-	31	-	S	$V_{DS} = -15\text{V}$, $I_D = -36\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.7	-	V	$I_S = -41\text{A}$, $V_{GS} = 0$
Dynamic ²						
Total Gate Charge	Q_g	-	13.9	30	nC	$V_{DS} = -15\text{V}$ $V_{GS} = -4.5\text{V}$ $I_D = -36\text{A}$
Gate-Source Charge	Q_{gs}	-	5.2	20		
Gate-Drain Charge	Q_{gd}	-	5.8	20		
Input Capacitance	C_{iss}	-	1583	4000	pF	$V_{DS} = -15\text{V}$, $V_{GS} = 0$, $f = 1\text{MHz}$
Output Capacitance	C_{oss}	-	278	600		
Reverse Transfer Capacitance	C_{rss}	-	183	400		
Turn-on Delay Time	$T_{d(on)}$	-	15	-	nS	$V_{DD} = -15\text{V}$ $I_D = -41\text{A}$ $V_{GEN} = -10\text{V}$ $R_L = 15\Omega$ $R_G = 6\Omega$
Rise Time	T_r	-	12	-		
Turn-off Delay Time	$T_{d(off)}$	-	62	-		
Fall Time	T_f	-	46	-		

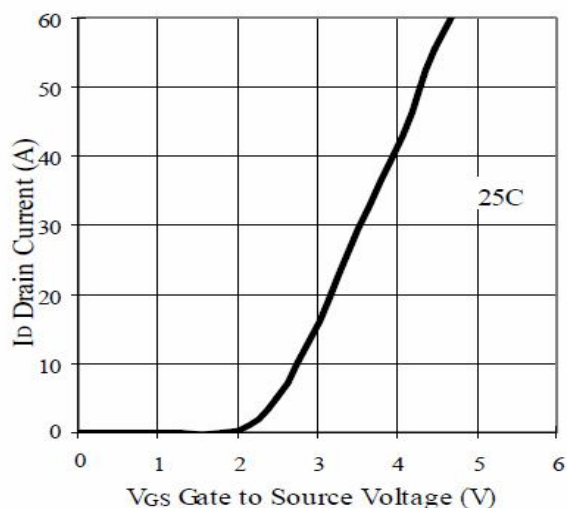
Notes:

1. Pulse test : Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

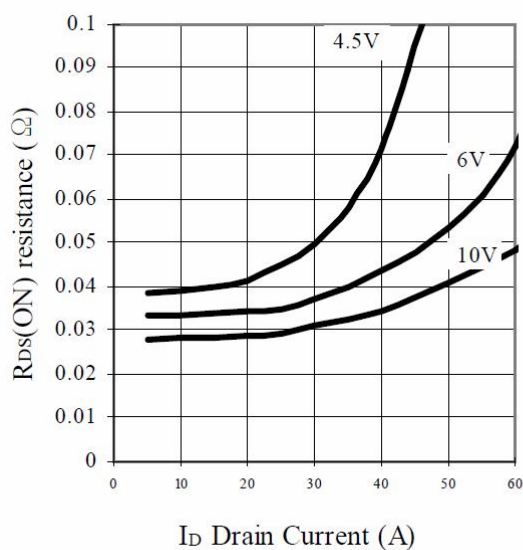
CHARACTERISTIC CURVES



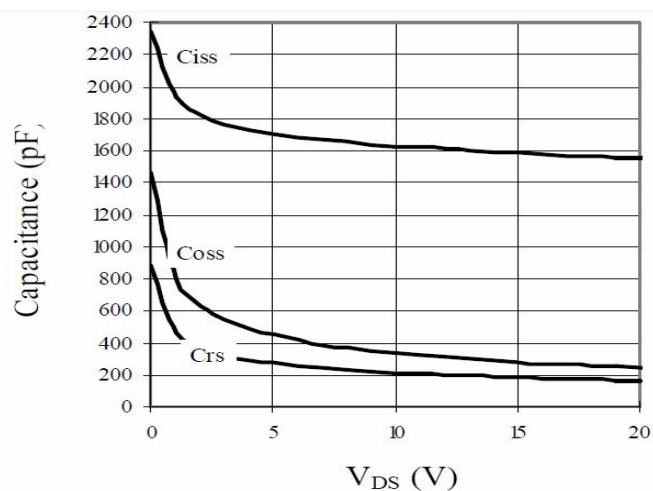
Output Characteristics



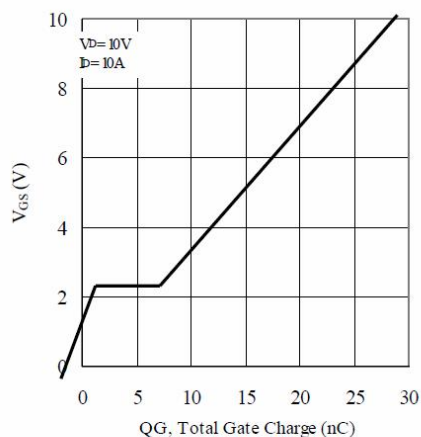
Transfer Characteristics



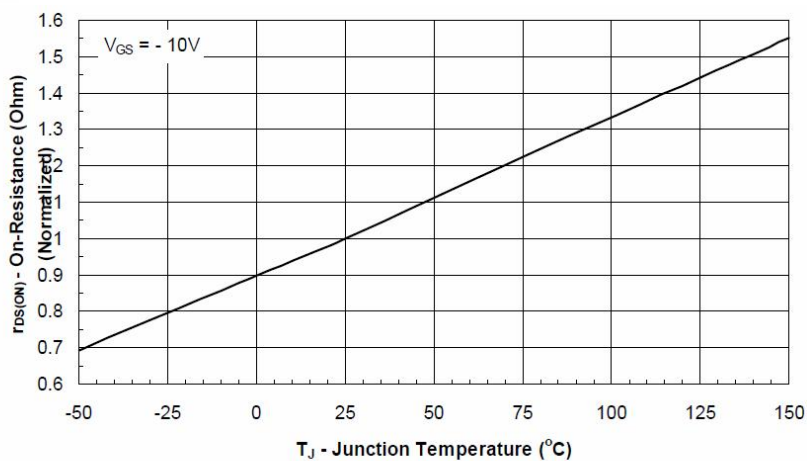
On Resistance Vs V_{GS} Voltage



Capacitance

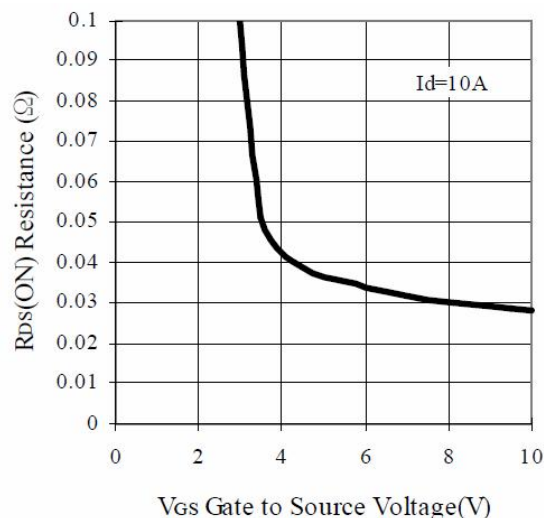
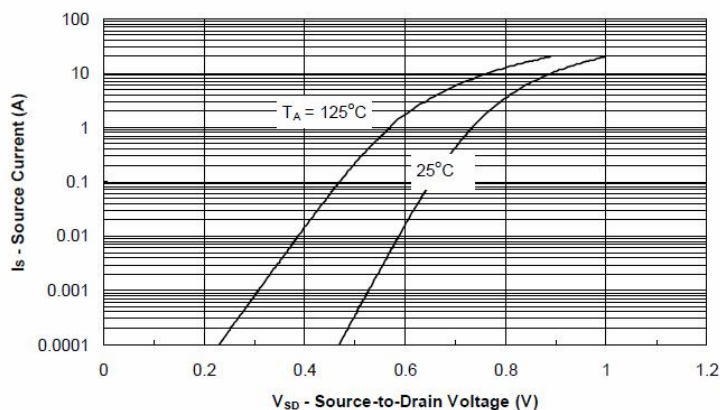


Gate Charge

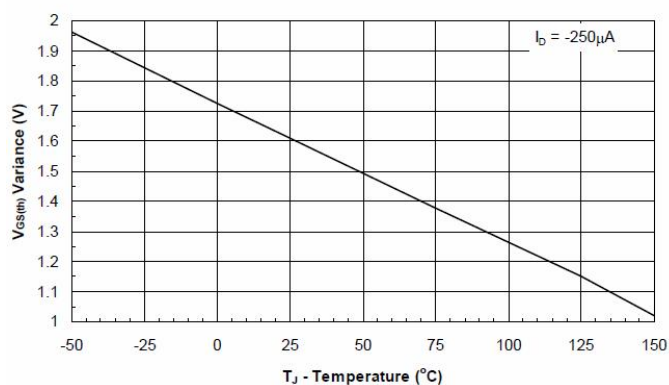


On-Resistance vs. Junction Temperature

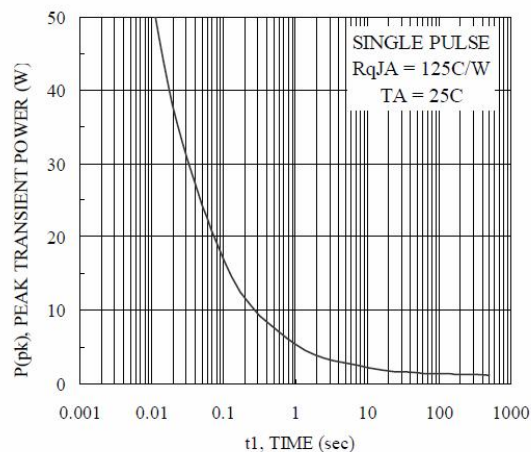
CHARACTERISTIC CURVES



Source-Drain Diode Forward Voltage



On-Resistance with Gate to Source Voltage



Threshold Voltage

Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

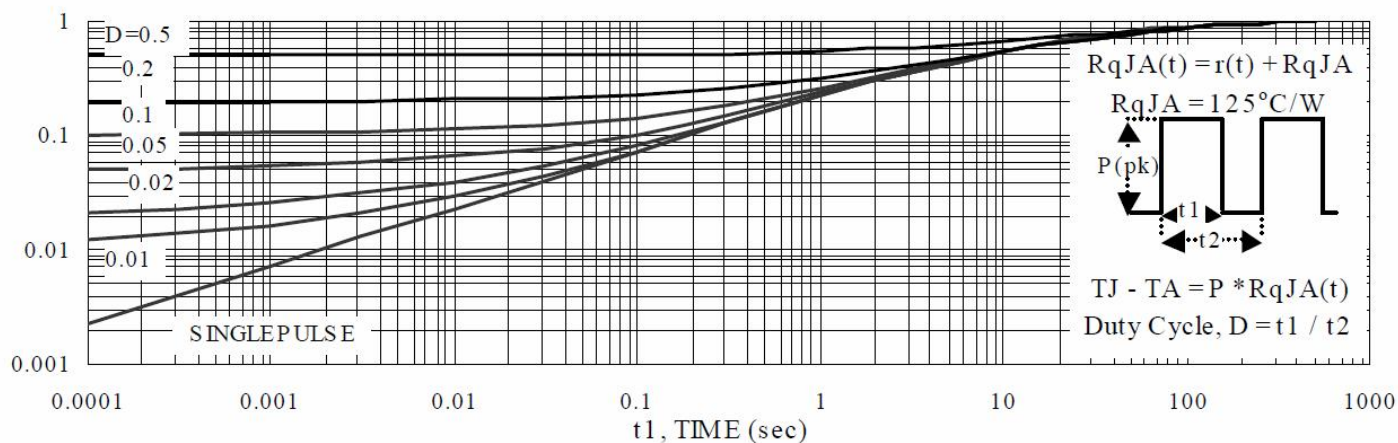


Figure 11. Transient Thermal Response Curve