



South Sea Semiconductor

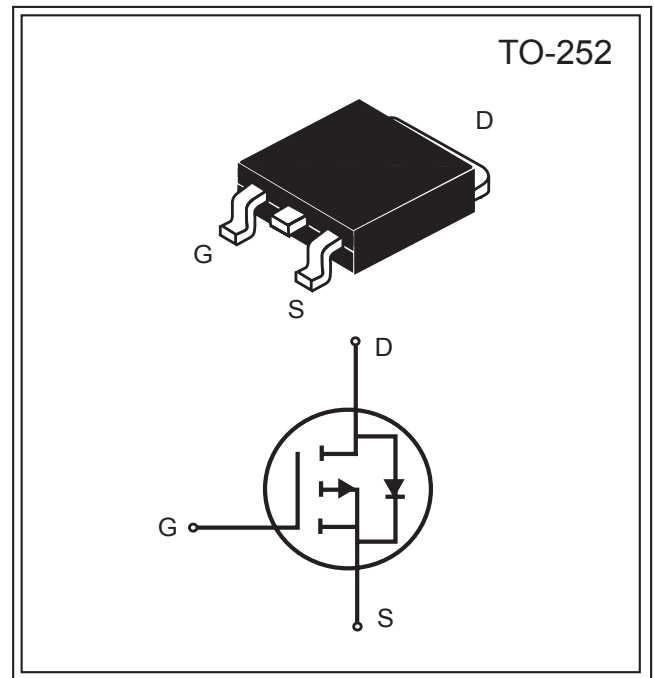
SSD3030P

P-Channel Enhancement Mode MOSFET

Product Summary		
V _{DS} (V)	I _D (A)	R _{DS(ON)} (mΩ) Max
-30V	-30A	25 @V _{GS} = -10V
		45 @V _{GS} = -5V
		55 @V _{GS} = -4.5V

FEATURES

- ◆ Super high density cell design for low R_{DS(ON)}.
- ◆ Rugged and reliable.
- ◆ TO-252 package.
- ◆ Pb free.



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±25	V
Drain Current-Continuous @ T _J = 125°C	I _D	-30	A
-Pulsed ^b	I _{DM}	-60	A
Drain-Source Diode Forward Current ^a	I _S	-1.7	A
Maximum Power Dissipation ^a	P _D	50	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	3	°C/W
Thermal Resistance, Junction-to-Ambient ^a	R _{θJA}	50	

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

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P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250 μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±25V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =-250 μA	-1	-1.9	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A			25	mΩ
		V _{GS} = -5V, I _D = -10A			45	
		V _{GS} =-4.5V, I _D =-10A			55	
On-State Drain Current	I _{D(ON)}	V _{DS} =-5V, V _{GS} =-10V	-40			A
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-5.3A		15		S
Input Capacitance	C _{ISS}	V _{DS} =-15V		1000	1200	pF
Output Capacitance	C _{OSS}	V _{GS} =0V		200		
Reverse Transfer Capacitance	C _{RSS}	f=1.0MHz		110	150	
Turn-On Delay Time	t _{D(ON)}	V _{DD} =-15V,		17.6		ns
Rise Time	t _r	I _D =-1A,		17.4		
Turn-Off Delay Time	t _{D(OFF)}	V _{GEN} =-10V,		169		
Fall Time	t _f	R _{GEN} =6Ω,		95.4		
Total Gate Charge	Q _g	V _{DS} =-15V, I _D = -8A, V _{GS} = -10V		20	25	nC
		V _{DS} =-15V, I _D = -8A, V _{GS} = -4.5V		11		
Gate-Source Charge	Q _{gs}	V _{DS} = -15V, I _D = -6A,		3.5		
Gate-Drain Charge	Q _{gd}	V _{GS} = -10V		6		
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D = -1A		-0.75	-1.2	V

Notes :

- Surface Mounted on FR4 Board, t ≤ 10 sec.
- Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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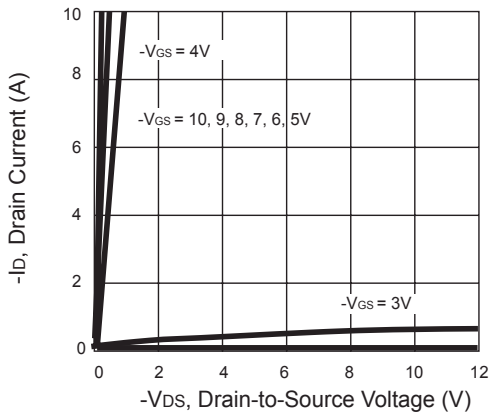


Figure 1. Output Characteristics

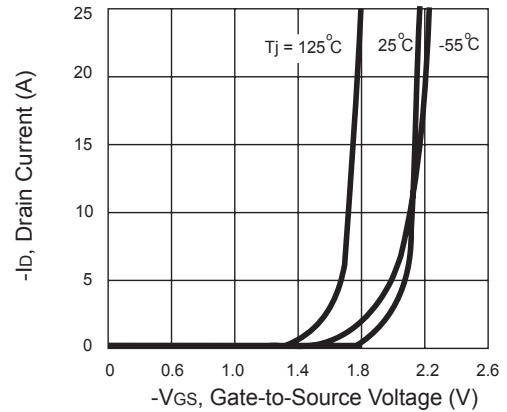


Figure 2. Transfer Characteristics

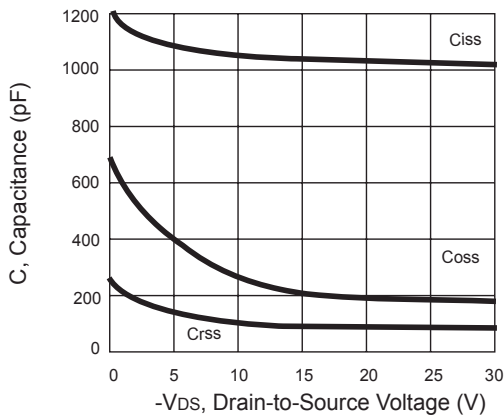


Figure 3. Capacitance

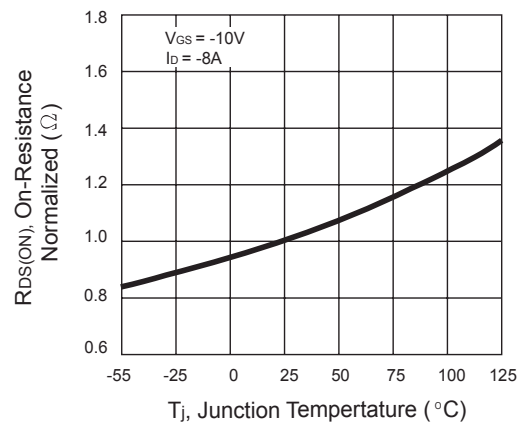


Figure 4. On-Resistance Variation with Temperature

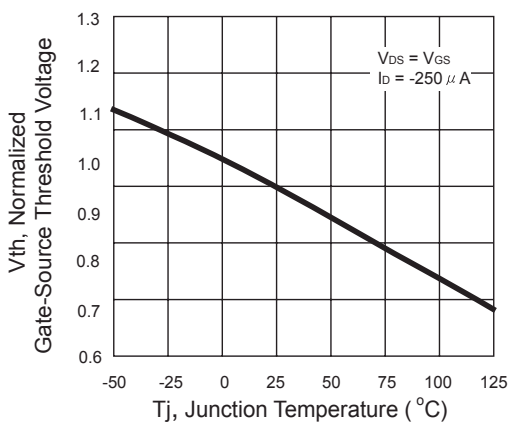


Figure 5. Gate Threshold Variation with Temperature

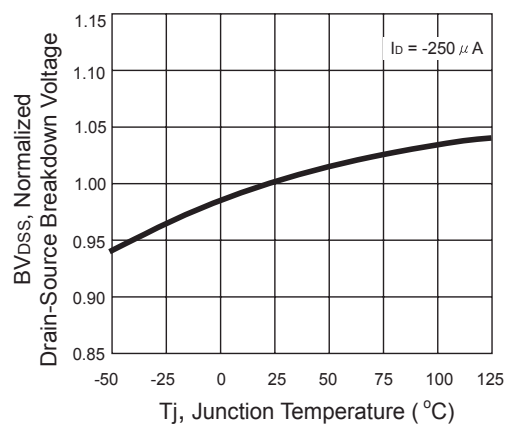


Figure 6. Breakdown Voltage Variation with Temperature

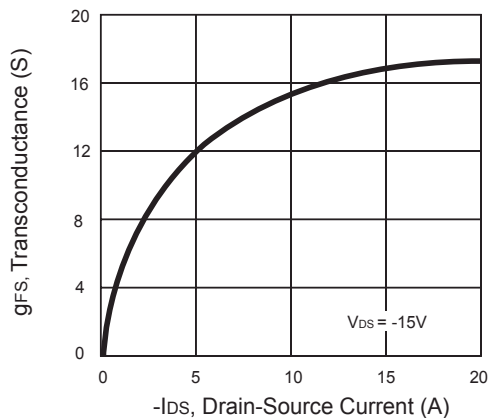


Figure 7. Transconductance Variation with Drain Current

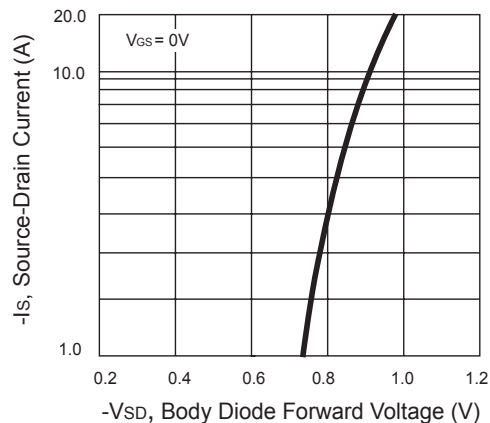


Figure 8. Body Diode Forward Voltage Variation with Source Current

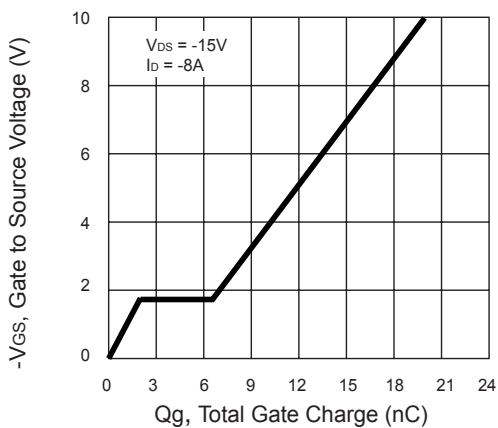


Figure 9. Gate Charge

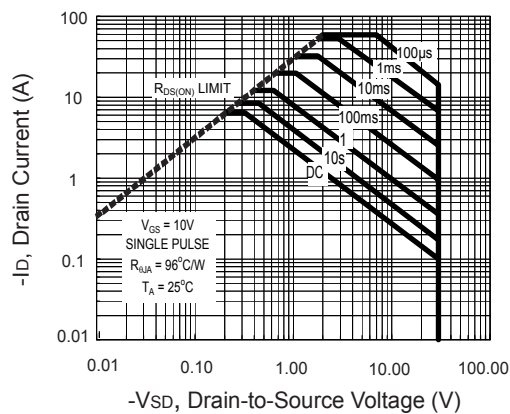


Figure 10. Maximum Safe Operating Area

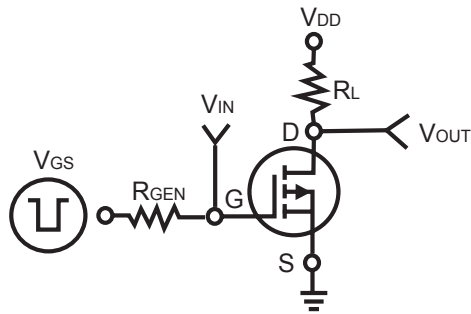


Figure 11. Switching Test Circuit

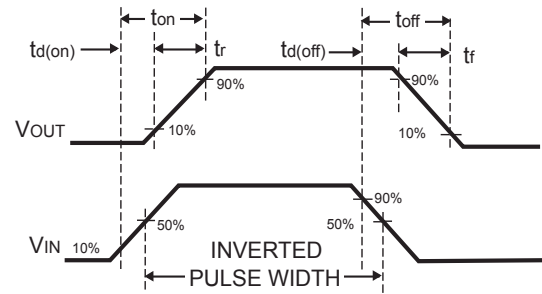


Figure 12. Switching Waveforms

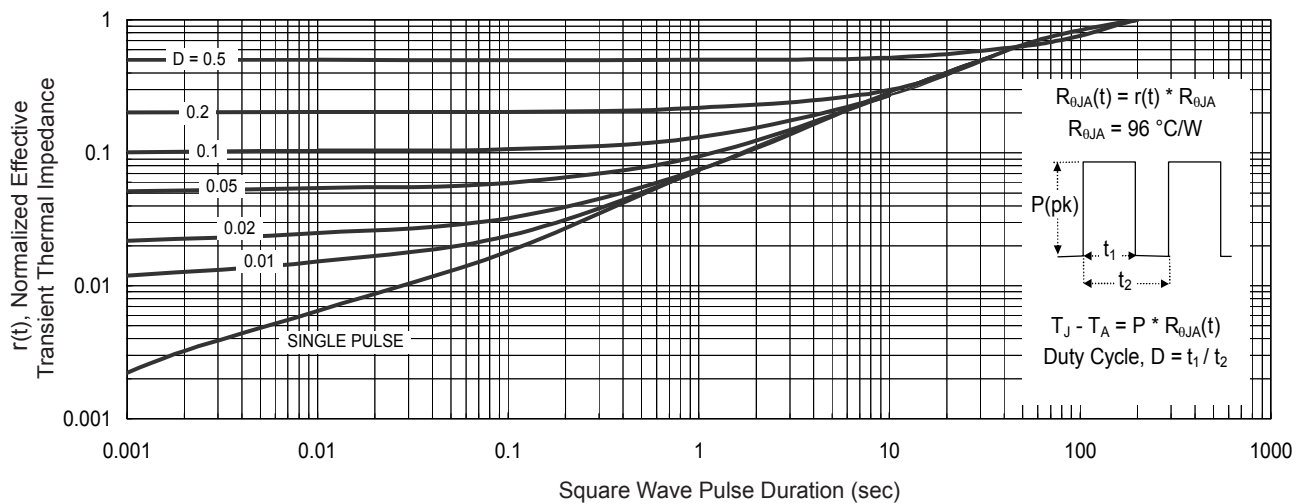


Figure 13. Normalized Thermal Transient Impedance Curve