

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

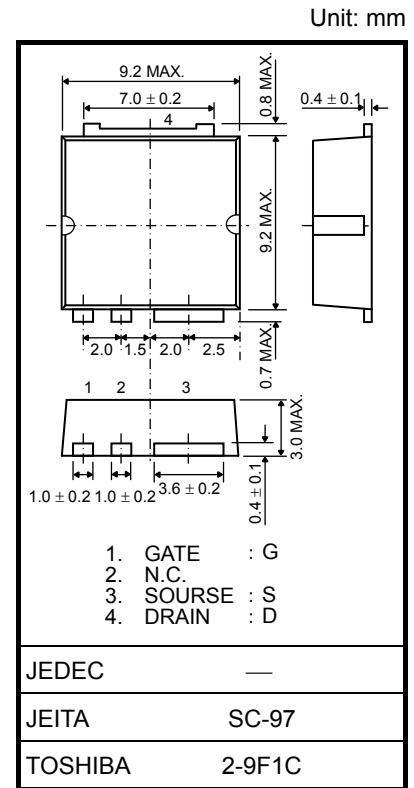
TK80X04K3

Switching Regulator, DC-DC Converter Applications
Motor Drive Applications

- Low drain-source ON-resistance: $R_{DS(ON)} = 2.7 \text{ m}\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 150 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 40 \text{ V}$)
- Enhancement mode: $V_{th} = 3.0 \text{ to } 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|--|----------------|-----------|------------|------------------|
| Drain-source voltage | | V_{DSS} | 40 | V |
| Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$) | | V_{DGR} | 40 | V |
| Gate-source voltage | | V_{GSS} | ± 20 | V |
| Drain current | DC (Note 1) | I_D | 80 | A |
| | Pulse (Note 1) | I_{DP} | 320 | |
| Drain power dissipation ($T_c = 25^\circ\text{C}$) | | P_D | 125 | W |
| Single pulse avalanche energy (Note 2) | | E_{AS} | 123 | mJ |
| Avalanche current | | I_{AR} | 80 | A |
| Repetitive avalanche energy (Note 3) | | E_{AR} | 12.5 | mJ |
| Channel temperature (Note 4) | | T_{ch} | 175 | $^\circ\text{C}$ |
| Storage temperature range (Note 4) | | T_{stg} | -55 to 175 | $^\circ\text{C}$ |



Weight: 0.74 g (typ.)

Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|-------------------------------------|----------------|-----|--------------------|
| Thermal resistance, channel to case | $R_{th(ch-c)}$ | 1.2 | $^\circ\text{C/W}$ |

Note 1: Ensure that the channel temperature does not exceed 175°C .

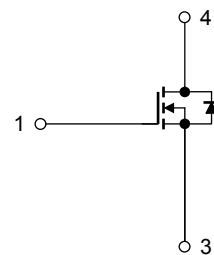
Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 20 \text{ }\mu\text{H}$, $I_{AR} = 80 \text{ A}$, $R_G = 25 \text{ }\Omega$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: The definitions of the absolute maximum channel temperature and storage temperatures are based on AEC-Q101.

Note 5: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



This transistor is an electrostatic-sensitive device. Handle with care.

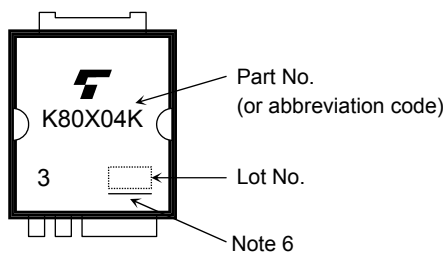
Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---------------|---------------|---|---|------|----------|------------------|
| Gate leakage current | | I_{GSS} | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | — | — | ± 10 | μA |
| Drain cut-off current | | I_{DSS} | $V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$ | — | — | 10 | μA |
| Drain-source breakdown voltage | | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$ | 40 | — | — | V |
| | | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$ | 20 | — | — | V |
| Gate threshold voltage | | V_{th} | $V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$ | 3.0 | — | 4.0 | V |
| Drain-source ON-resistance | | $R_{DS(ON)}$ | $V_{GS} = 10\text{ V}, I_D = 40\text{ A}$ | — | 2.7 | 3.5 | $\text{m}\Omega$ |
| Forward transfer admittance | | $ Y_{fs} $ | $V_{DS} = 10\text{ V}, I_D = 40\text{ A}$ | 75 | 150 | — | S |
| Input capacitance | | C_{iss} | $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | — | 4600 | — | pF |
| Reverse transfer capacitance | | C_{rss} | | — | 850 | — | |
| Output capacitance | | C_{oss} | | — | 1150 | — | |
| Switching time | Rise time | t_r | | — | 28 | — | ns |
| | Turn-on time | t_{on} | | — | 60 | — | |
| | Fall time | t_f | | — | 35 | — | |
| | Turn-off time | t_{off} | | Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$ | — | 90 | |
| Total gate charge (gate-source plus gate-drain) | | Q_g | $V_{DD} \approx 32\text{ V}, V_{GS} = 10\text{ V}, I_D = 80\text{ A}$ | — | 100 | — | nC |
| Gate-source charge | | Q_{gs} | | — | 60 | — | |
| Gate-drain ("miller") charge | | Q_{gd} | | — | 40 | — | |

Source-Drain Ratings and Characteristics (Ta = 25°C)

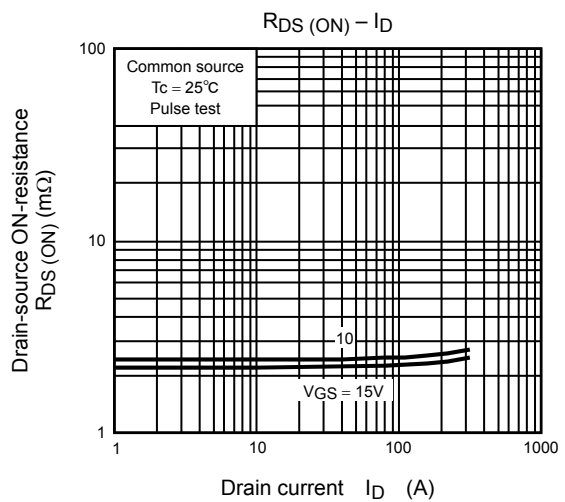
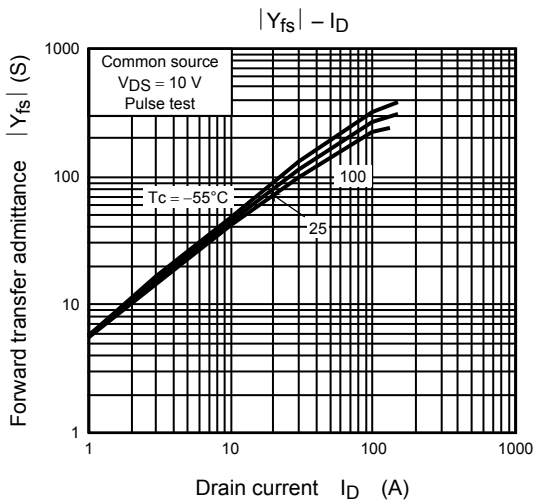
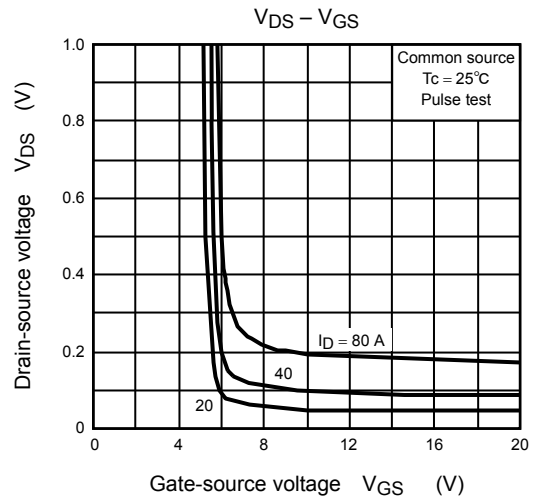
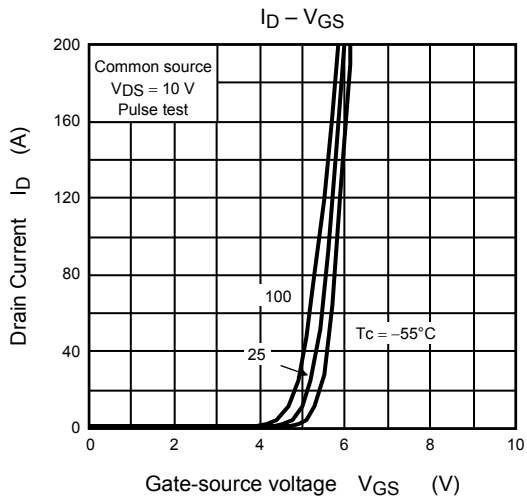
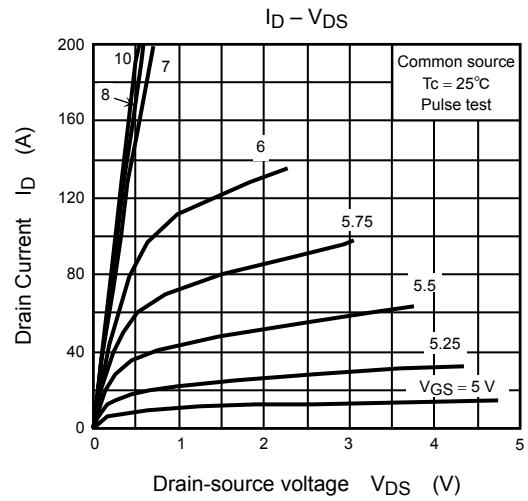
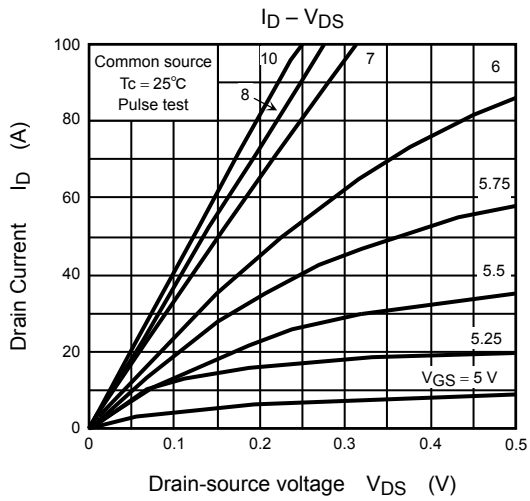
| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|----------------------------------|----------|-----------|---|-----|------|------|------|
| Continuous drain reverse current | (Note 1) | I_{DR} | — | — | — | 80 | A |
| Pulse drain reverse current | (Note 1) | I_{DRP} | — | — | — | 320 | A |
| Forward voltage (diode) | | V_{DSF} | $I_{DR} = 80\text{ A}, V_{GS} = 0\text{ V}$ | — | — | -1.5 | V |
| Reverse recovery time | | t_{rr} | $I_{DR} = 80\text{ A}, V_{GS} = 0\text{ V}, dI_{DR}/dt = 30\text{ A}/\mu\text{s}$ | — | 80 | — | ns |
| Reverse recovery charge | | Q_{rr} | | — | 60 | — | nC |

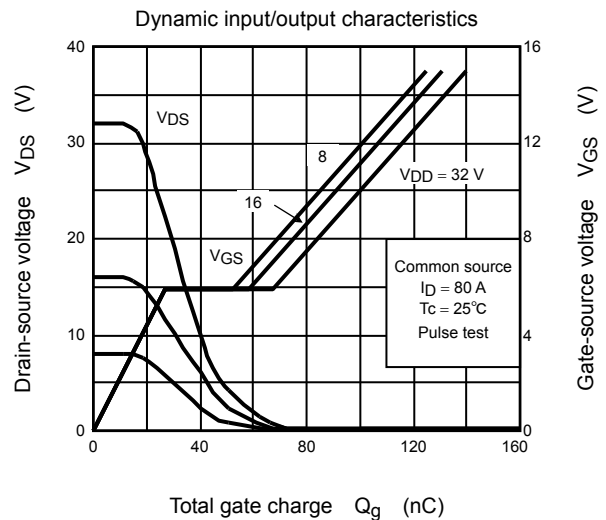
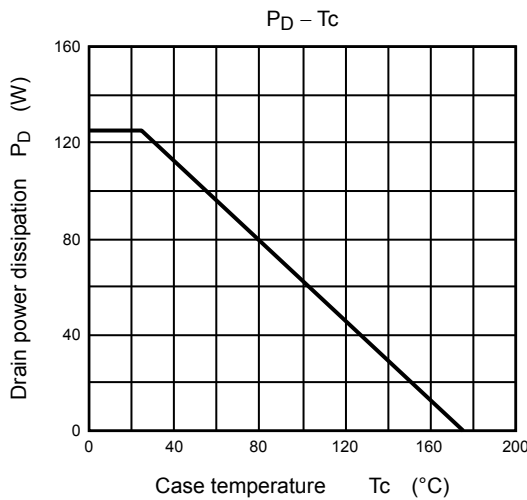
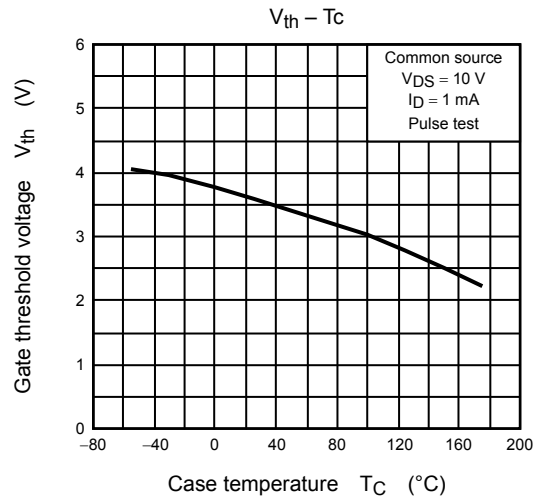
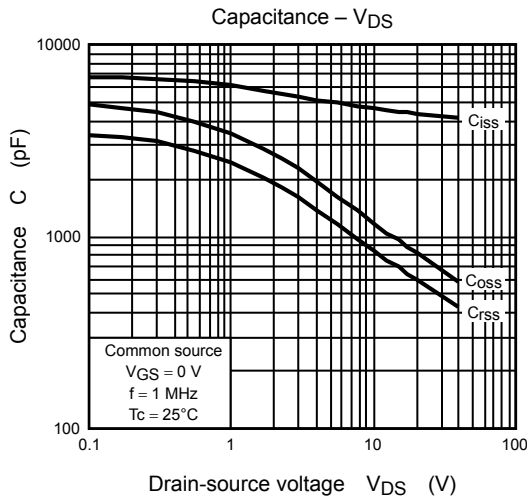
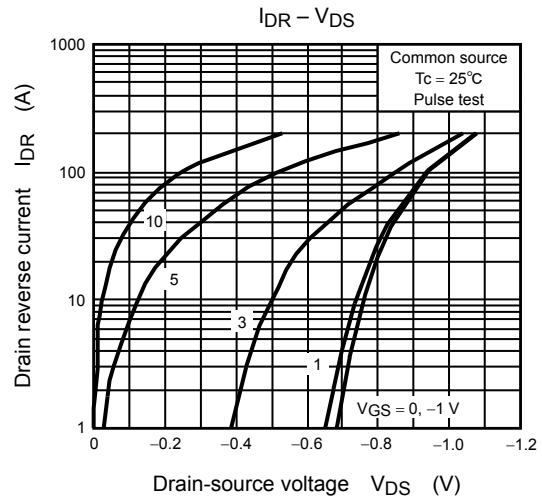
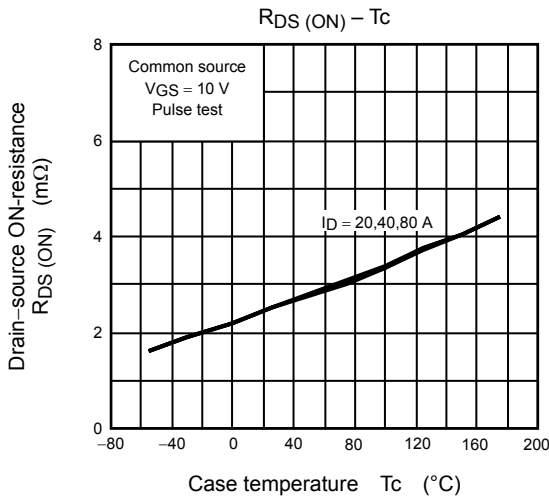
Marking

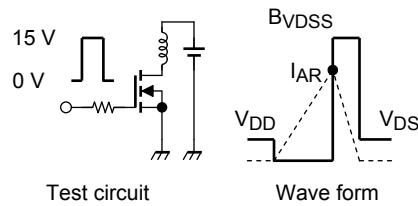
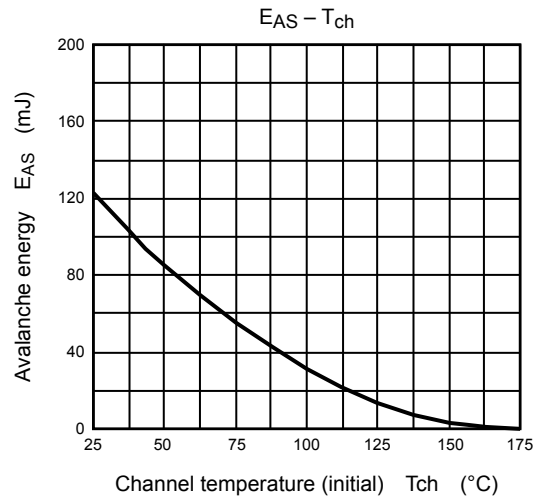
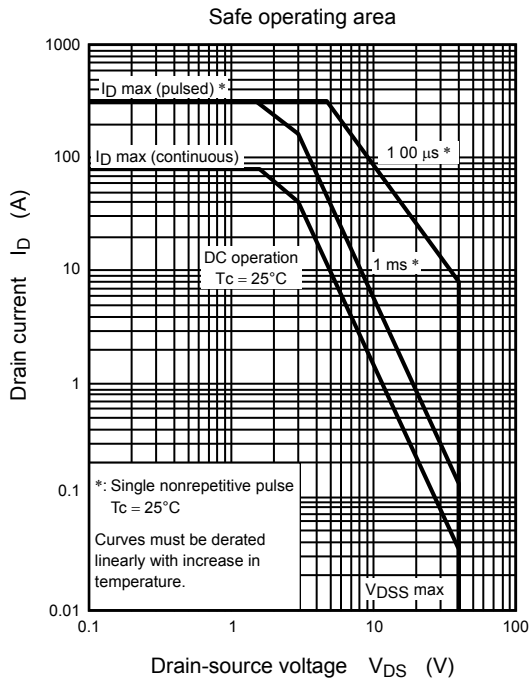
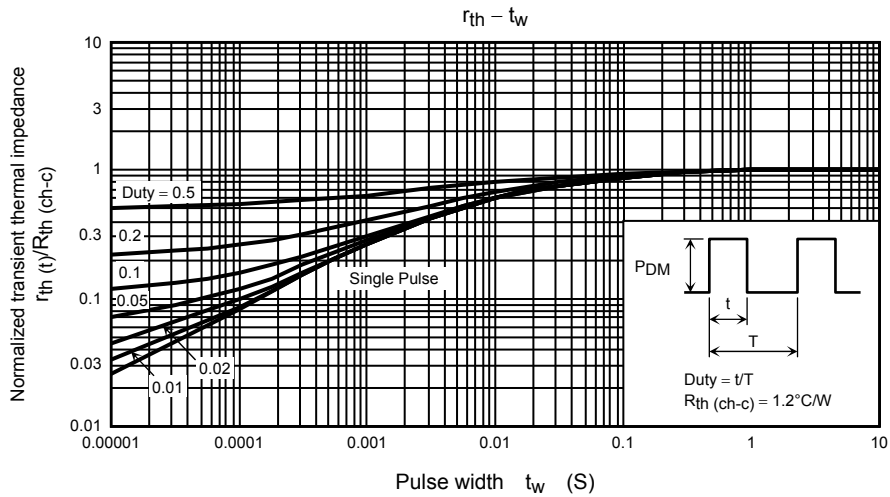


Note 6: A line under a Lot No. identifies the indication of product Labels [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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$R_G = 25 \Omega$
 $V_{DD} = 25 V, L = 20 \mu H$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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