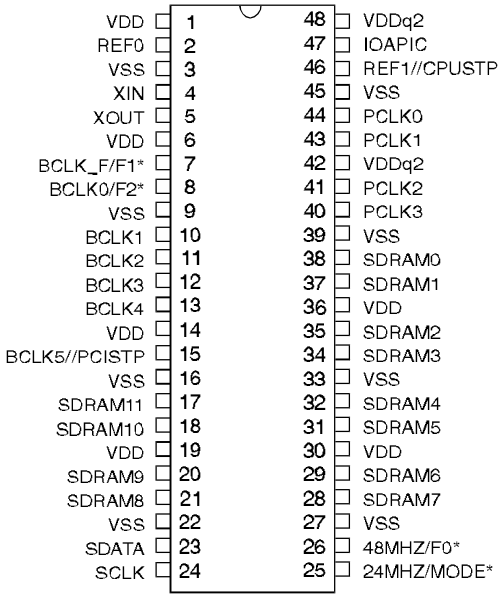
Pentium/SDRAM Clock Generator with Integrated Buffers

FEATURES

- Generates all clock frequencies for Pentium (II), AMD and Cyrix system requiring multiple CPU clocks.
- Supports up to16 Synchronous CPU clocks (4 CPU and 12 SDRAM) and 7 Synchronous PCI BUS clocks.
- Two 14.318Mhz reference clocks and one 2.5V IOAPIC
- One 24Mhz floppy clock and one 48Mhz USB clock.
- Power management control pins to stop CPU, SDRAM or PCI BUS clocks.
- Supports 2-wire I2C serial bus interface.
- 50% duty cycle with low jitter
- Mixed voltage support from 3.0 to 5V or (VDDq2=2.5V)
- Available in 300mil 48 pin SSOP.

PIN INFORMATION



PLL52C63-01

Note: F2,F1,F0 and MODE are selectable only during power-on. They are HIGH by default and LOW when 10K Ω Pull down is attached.

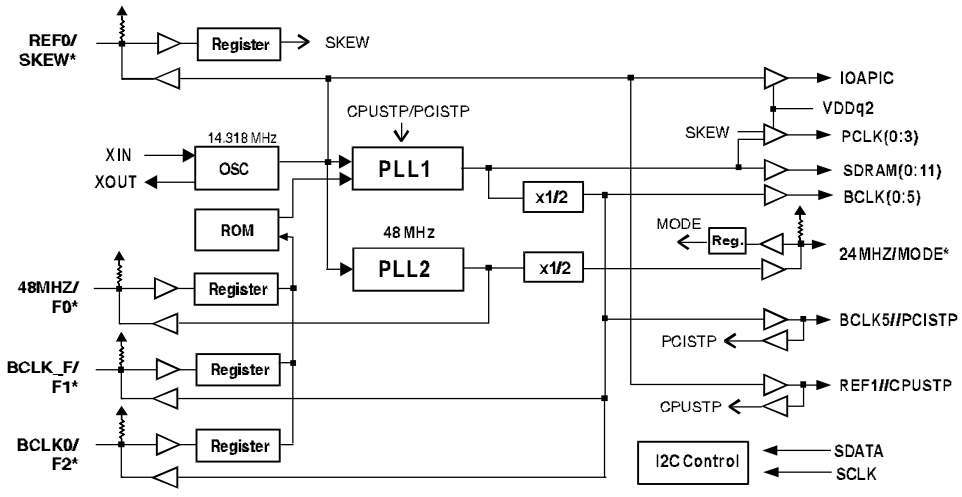
FREQUENCY SELECTION (MHz)

F2	F1	F0	PCLK/SDRAM	BCLK
0	0	0	50	25
0	0	1	100	50
0	1	0	83.3	41.6
0	1	1	68.5	34.2
1	0	0	55	27.5
1	0	1	75	37.5
1	1	0	60	30
1	1	1	66.6	33.3

I/O MODE CONFIGURATION

MODE	PIN15	PIN46
1 (OUTPUT)	BCLK5	REF1
0 (INPUT)	PCISTP	CPUSTP

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
VDD	1,6,14, 19,30,36	P	Power supply (3V ~ 5V)
VDDq2	42,48	P	Power supply 2.5V-5V
VSS	3,9,16,22 27,33,39,45	P	Ground
XIN	4	I	14.318Mhz crystal input to be connected to one end of the crystal. This input can also be connected directly to other available source of 14.318Mhz from the PC board.
XOUT	5	O	14.318Mhz crystal output
BCLK_F/F1* BCLK_0/F2* 48MHZ/F0*	7,8,26	B	At power-up, these pins are input pins and will determine the CPU clock frequency (see Frequency Selection Table). After input sampling, these pins will generate output clocks.
BCLK_F, BCLK(0:5)	7,8,10,11 12,13,15	O	PCI Bus clocks with frequencies defined by Frequency Table. These pins except BCLK_F will be LOW when PCISTP is LOW
PCLK(0:3)	44,43,41,40	O	CPU clocks with frequencies defined by Frequency Table for 2.5V and 3.3V. These pins are LOW when CPUSTP is LOW.
SDRAM(0:11)	38,37,35,34 32,31,29,28 21,20,18,17	O	SDRAM clocks with frequencies defined by Frequency Table for 3.3V. These pins are LOW when CPUSTP is LOW
SDATA	23	I	Serial data input for serial interface port
SCLK	24	I	Serial clock input for serial interface port
BCLK5//PCISTP	15	B	Multiplexed pin controlled by MODE signal (see I/O MODE configuration Table). PCISTP will stop PCI BUS clock except BCLK_F when LOW.
REF1//CPUSTP	46	B	Mulitplexed pin controlled by MODE signal (see I/O MODE configuration Table). CPUSTP will stop all PCLK and SDRAM clocks with glitch free.
48MHZ/F0*	26	B	48MHZ output for USB after input data latched during power-on.
24MHZ/MODE*	25	B	At power-on, MODE function is activated (see I/O Mode configuration table). It enables power management features . After input data latched, this pin will generate 24MHZ output for Super IO applications.
REF(0:1)	2,46	O	Buffered reference clock output
IOAPIC	47	O	2.5V 14.318Mhz Reference clock output for parallel processing.

I2C BUS CONFIGURATION SETTING

Address Assignment	A6 A5 A4 A3 A2 A1 A0 R/W 1 1 0 1 0 0 1 —
Slave/Receiver	Only Slave/receiver functionality is provided.
Data Transfer Rate	Standard mode at 100kbits/s
Serial Bits reading	The serial bits will be read by the clock driver in the following order Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
Data Protocol	This serial protocol is designed to allow only block writes from the controller. The bytes must be accessed in sequenctial order from lowest to highest byte. The block write begins with a slave address and a write condition (0xD2). Following the acknowledge of this address byte, two additional bytes must be sent but ignored by receiver : A: **Command Code byte**: 0x00 B: **Byte Count byte**: # of the additional bytes required for the transfer. (32 bytes Max) A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by controller.

I2C CONTROL REGISTERS

1. BYTE0: Functional and Frequency Select Clock Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	8	F2 (see Frequency Selection Table)
Bit 5	7	F1 (see Frequency Selection Table)
Bit 4	26	F0 (see Frequency Selection Table)
Bit 3		Frequency selection control bit. 1=Via I2C, 0=Via External jumper.
Bit 2	N/A	Reserved
Bit 1 Bit 0	N/A	**BIT1 BIT0** 1 1 Tristate Mode 1 0 (reserved) 0 1 Test Mode 0 0 Normal Operation (default)

2. BYTE1: CPU Clock Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	N/A	Reserved
Bit 5	N/A	Reserved
Bit 4	N/A	Reserved
Bit 3	40	PCLK3 (Active/Inactive)
Bit 2	41	PCLK2 (Active/Inactive)
Bit 1	43	PCLK1 (Active/Inactive)
Bit 0	44	PCLK0 (Active/Inactive)

3. BYTE2: PCI BUS Clock Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	7	BCLK_F (Active/Inactive)
Bit 5	15	BCLK5 (Active/Inactive)
Bit 4	13	BCLK4 (Active/Inactive)
Bit 3	12	BCLK3 (Active/Inactive)
Bit 2	11	BCLK2 (Active/Inactive)
Bit 1	10	BCLK1 (Active/Inactive)
Bit 0	8	BCLK0 (Active/Inactive)

4. BYTE3: SDRAM Clock Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	28	SDRAM7 (Active/Inactive)
Bit 6	29	SDRAM6 (Active/Inactive)
Bit 5	31	SDRAM5 (Active/Inactive)
Bit 4	32	SDRAMK4 (Active/Inactive)
Bit 3	34	SDRAM3 (Active/Inactive)
Bit 2	35	SDRAM2 (Active/Inactive)
Bit 1	37	SDRAM1 (Active/Inactive)
Bit 0	38	SDRAM0 (Active/Inactive)

Notes: 1. Inactive means outputs are STOPPED and held LOW.

5. BYTE4: SDRAM Clock Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	N/A	Reserved
Bit 5	N/A	Reserved
Bit 4	N/A	Reserved
Bit 3	17	SDRAM11 (Active/Inactive)
Bit 2	18	SDRAM10 (Active/Inactive)
Bit 1	20	SDRAM9 (Active/Inactive)
Bit 0	21	SDRAM8 (Active/Inactive)

6. BYTE5: Peripheral Clock Register (1=enable, 0=disable)

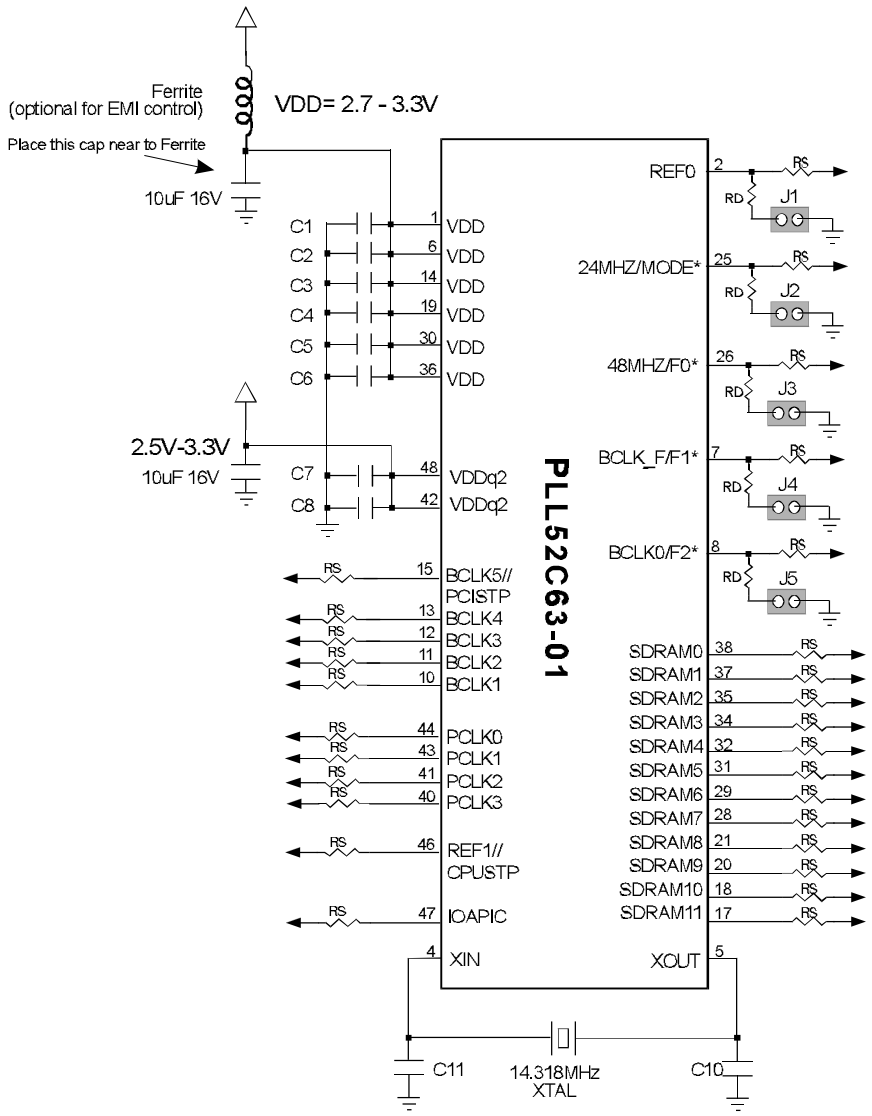
BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	N/A	Reserved
Bit 5	N/A	Reserved
Bit 4	47	IOAPIC (Active/Inactive)
Bit 3	N/A	Reserved
Bit 2	N/A	Reserved
Bit 1	46	REF1 (Active/Inactive)

7. BYTE6: Optional Register (1=enable, 0=disable)

BIT	PIN #	DESCRIPTION
Bit 7	N/A	Reserved
Bit 6	N/A	Reserved
Bit 5	N/A	Reserved
Bit 4	N/A	Reserved
Bit 3	N/A	Reserved
Bit 2	N/A	Reserved
Bit 1	N/A	Reserved
Bit 0	N/A	Reserved

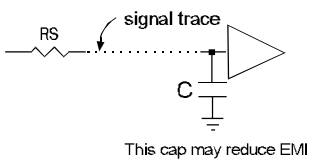
Notes: 1. Inactive means outputs are STOPPED and held LOW.

APPLICATION CIRCUITS



Notes:

1. J1:I/O Mode configuration jumper
2. J3-J5: Frequency selection jumpers
3. C10-C11: (optional) for fine tuning the crystal frequency.
4. RS: Series clock terminating resistor is recommended using 22 ohm resistor. To further reduce signal ringing and EMI, a capacitor could be placed near the receiving end of the clock line. (as the drawing shows)



5. C1-C9 are 0.1uF power bypass capacitors, should be placed as close to each VDD pin as physically possible.
6. RD=10K ohm resistor must place near to output pins.

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MAXIMUM RATINGS

SUPPLY VOLTAGE	VSS-0.5 TO 7V
INPUT VOLTAGE	VSS-0.5V to VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	0.75W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

AC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reference input clock rise time	T_{IR}	From 0.8 V to 2V			20	ns
Reference input clock fall time	T_{IF}	From 2V to 0.8V			20	ns
Duty cycle	D_T	15pF load.	45	50/50	55	%
Clock Skew (20pF load, @ 1.4V)	T_{SKW}	PCLK to PCLK		50	250	ps
		BCLK to BCLK		90	500	ps
		PCLK to SDRAM			250	ps
		PCLK to BCLK	1	2	5	ns
Jitter, Absolute (20pF load)	T_{JA}	PCLK, SDRAM, BCLK	-100		100	ps
Jitter, One Sigma (20pF load)	T_{JO}	PCLK, SDRAM, BCLK		50		ps

DC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Current	I_{DYN}	CPU at 66.6 MHZ no load		55	110	mA
Static Current	I_{STAT}	All internal circuitry off, XIN=0		25	50	µA
Input High Voltage	V_{IH}	All Inputs except XIN	2			V
Input Low Voltage	V_{IL}	All Inputs except XIN			0.8	V
Pull-up resistor	R_{Pu}	Pin 2,7,8,15,25,26,46		25		Kohm
Output Impedance	R_O	PCLK,SDRAM,BCLK		30		ohm
Output Low Current @VOL=0.4V	I_{OL}	XOUT	1			mA

BUFFER SPECIFICATIONS

TYPE 1 (=2.5V±5%) : PCLK(0:3) BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-27			mA
		VOUT=2.6V			-27	
Output Low Current	I_{OL}	VOUT=1.2V	27			mA
		VOUT=0.3V			27	
Output rise time	T_{OR}	From 0.4V to 2.0V, 10pf Load	1			V/ns
		From 0.4V to 2.0V, 20pf Load			4	
Output fall time	T_{OF}	From 2.0V to 0.4V, 10pf Load	1			V/ns
		From 2.0V to 0.4V, 20pf Load			4	

TYPE 2 (=2.5V±5%) : IOAPIC BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.4V	-36			mA
		VOUT=2.7V			-29	
Output Low Current	I_{OL}	VOUT=1.0V	36			mA
		VOUT=0.2V			28	
Output rise time	T_{OR}	From 0.4V to 2.0V, 10pf Load	1			V/ns
		From 0.4V to 2.0V, 20pf Load			4	
Output fall time	T_{OF}	From 2.0V to 0.4V, 10pf Load	1			V/ns
		From 2.0V to 0.4V, 20pf Load			4	

TYPE 3 (=3.3V±5%) : REF1,24Mhz,48Mhz BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-29			mA
		VOUT=3.135V			-23	
Output Low Current	I_{OL}	VOUT=1.95V	29			mA
		VOUT=0.4V			27	
Output rise time	T_{OR}	From 0.4V to 2.4V, 10pf Load	0.5			V/ns
		From 0.4V to 2.4V, 20pf Load			2	
Output fall time	T_{OF}	From 2.4V to 0.4V, 10pf Load	0.5			V/ns
		From 2.4V to 0.4V, 20pf Load			2	

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TYPE 4 (=3.3V±5%) : SDRAM(0:11), REF0 BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-54			mA
		VOUT=3.135V			-46	
Output Low Current	I_{OL}	VOUT=1.95V	54			mA
		VOUT=0.4V			53	
Output rise time	T_{OR}	From 0.4V to 2.4V, 20pf Load	1.5			V/ns
		From 0.4V to 2.4V, 30pf Load			4	
Output fall time	T_{OF}	From 2.4V to 0.4V, 20pf Load	1.5			V/ns
		From 2.4V to 0.4V, 30pf Load			4	

TYPE 5 (=3.3V±5%) : BCLK(0:5),BCLK_F BUFFER Characteristics						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Output High Current	I_{OH}	VOUT=1.0V	-33			mA
		VOUT=3.135V			-33	
Output Low Current	I_{OL}	VOUT=1.95V	30			mA
		VOUT=0.4V			38	
Output rise time	T_{OR}	From 0.4V to 2.4V, 15pf Load	1			V/ns
		From 0.4V to 2.4V, 30pf Load			4	
Output fall time	T_{OF}	From 2.4V to 0.4V, 15pf Load	1			V/ns
		From 2.4V to 0.4V, 30pf Load			4	

PACKAGE INFORMATION

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

45437 Warm Springs Blvd., Fremont, CA 94539, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
device number, package type and operating temperature range.

PLL52C63-01 X C

PART NUMB E R

TEMPERATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL

PACKAGE TYPE
X=SSOP