Elektronische Bauelemente

STT6405

-5.0 A, -30 V, $R_{DS(ON)}$ 50 mΩ
P-Channel Enhancement Mode Mos.FET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

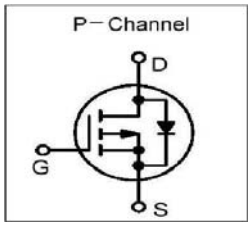
DESCRIPTION

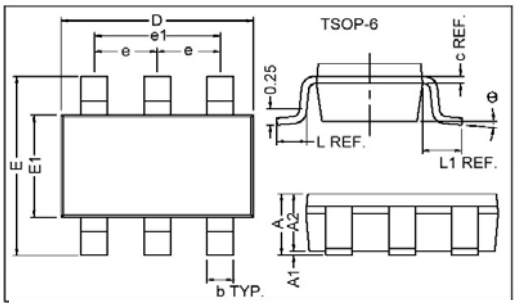
The STT6405 uses advanced trench technology to provide excellent on-resistance with low gate change. The device is suitable for use as a load switch or in PWM applications.

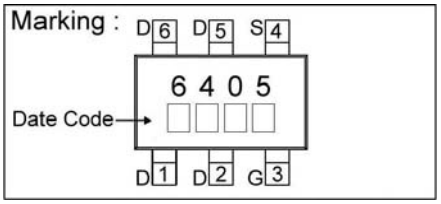
FEATURES

- N-Channel
- Lower Gate Charge
- Small Footprint & Low Profile Package

PACKAGE DIMENSIONS







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.10 Max		L	0.45 Ref	
A1	0	0.10	L1	0.60 Ref	
A2	0.70	1.00		0°	10°
c	0.12 Ref		b	0.30	0.50
D	2.70	3.10	e	0.95 Ref	
E	2.60	3.00	e1	1.90 Ref	
E1	1.40	1.80			

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (TJ=150℃)	I_D @TA=25℃ I_D @TA=70℃	-5.0 -4.2	A
Pulsed Drain Current	I_{DM}	-20	A
Power Dissipation	P_D @TA=25℃	2	W
Linear Derating Factor		0.016	W/℃
Operating Junction and Storage Temperature Range	Tj, Tstg	-55 ~ +150	℃

Parameter	Symbol	Ratings	Unit
Thermal Resistance- Junction to Ambient[3] Max.	RθJA	62.5	℃/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS} = 0, I_D= -250 uA
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-3.0	V	V_{DS} = V_{GS}, I_D= -250 uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS} = ±20 V
Drain-Source Leakage Current (Tj=25℃)	I_{DSS}	-	-	-1	uA	V_{DS} = -30 V, V_{GS} = 0
Drain-Source Leakage Current (Tj=55℃)		-	-	-5		V_{DS} = -24 V, V_{GS} = 0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	50	mΩ	V_{GS} = -10 V, I_D = -5.0 A
				75		V_{GS} = -4.5 V, I_D = -4.0 A
Forward Transconductance	g_{fs}	-	8.6	-	S	V_{DS} = -5V, I_D = -5.0A
Total Gate Charge[2]	Q_g	-	14.7	18	nC	I_D = -5.0 A V_{DS} = -15 V V_{GS} = -10 V
Gate-Source Charge	Q_{gs}	-	2	-		
Gate-Drain (“Miller”) Charge	Q_{gd}	-	3.8	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	8.3	-	ns	V_{DS} = -15 V V_{GS} = -10 V R_G = 3 Ω R_L = 3 Ω
Rise Time	T_r	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	29	-		
Fall Time	T_f	-	14	-		
Input Capacitance	Ciss	-	700	840	pF	V_{GS} = 0 V V_{DS} = -15 V f = 1.0 MHz
Output Capacitance	Coss	-	120	-		
Reverse Transfer Capacitance	Crss	-	75	-		
Gate Resistance	R_g	-	10	-	Ω	f=1.0 MHz

SOURCE-DRAIN DIODE

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	-1.0	V	I_S = -1.0 A, V_{GS}= -0 V
Reverse Recovery Time[2]	T_{rr}	-	23.5	-	ns	I_S = -5.0A, V_{GS}=0V, dI/dt=
Reverse Recovery Charge	Q_{rr}	-	13.4	-	nC	100A/us

Notes: 1. Pulse width limited by Max. junction temperature.
2. Pulse width≦300us, duty cycle≦2%.
3. Surface mounted on 1 in^2 copper pad of FR4 board; 156℃/W when mounted on Min. copper pad.

CHARACTERISTIC CURVES

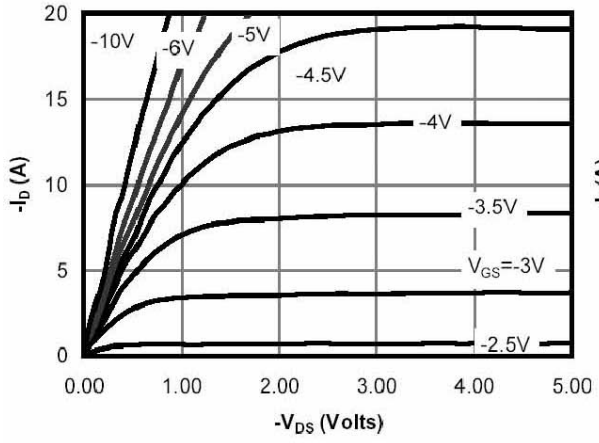


Fig 1. Typical Output Characteristics

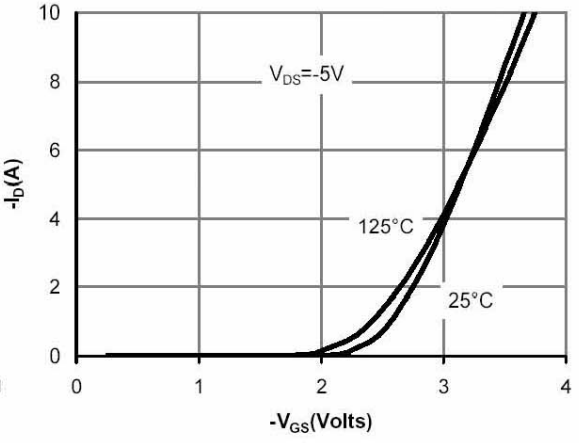


Fig 2. Transfer Characteristics

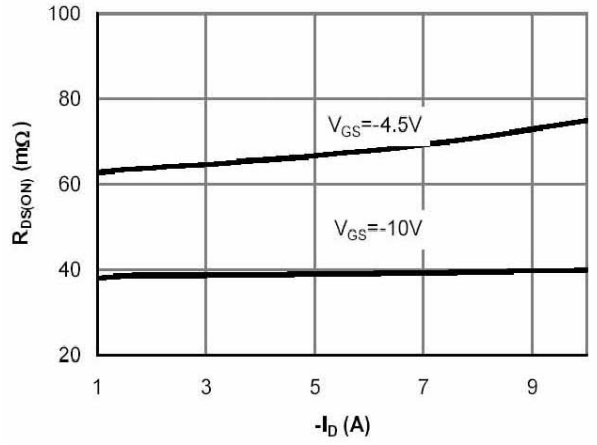


Fig 3. On-Resistance vs. Drain Current and Gate Voltage

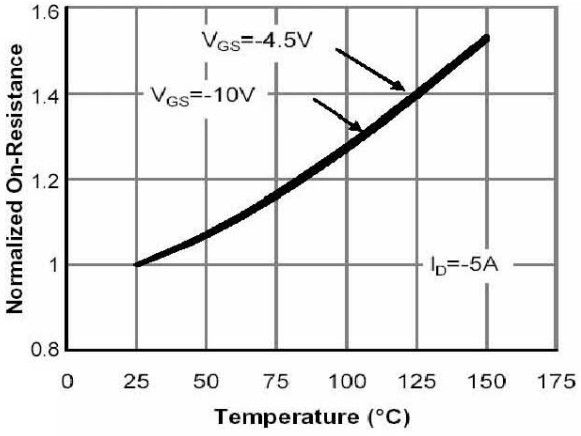


Fig 4. On-Resistance vs. Junction Temperature

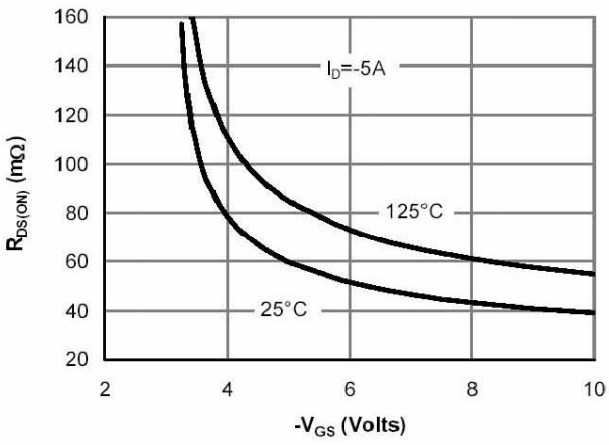


Fig 5. On-Resistance vs. Gate-Source Voltage

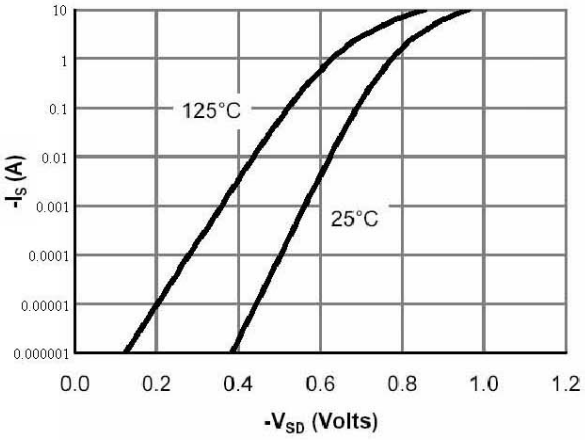


Fig 6. Body Diode Characteristics

CHARACTERISTIC CURVES

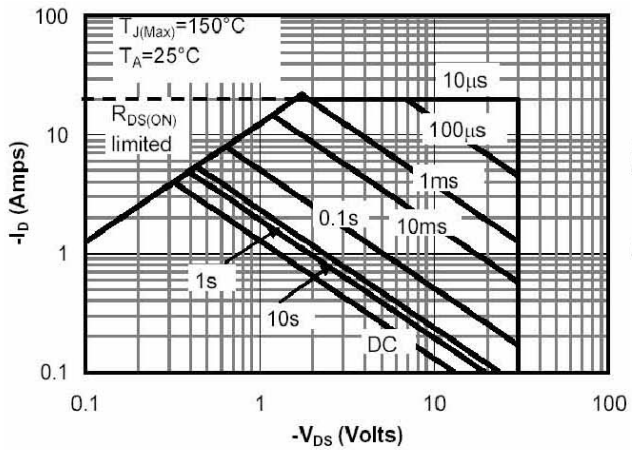


Fig 7. Maximum Safe Operating Area

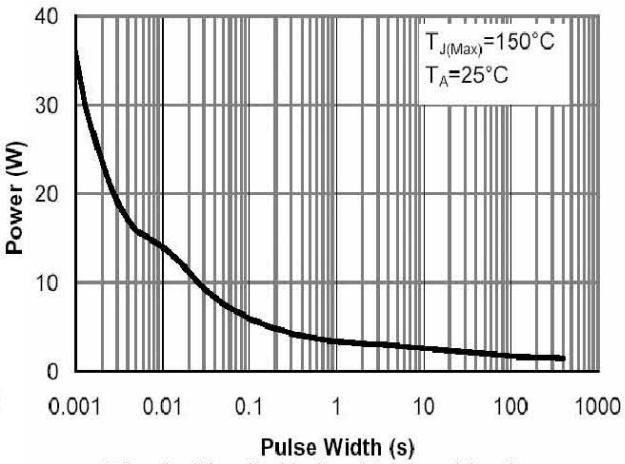


Fig 8. Single Pulse Power Rating Junction-to-Ambient

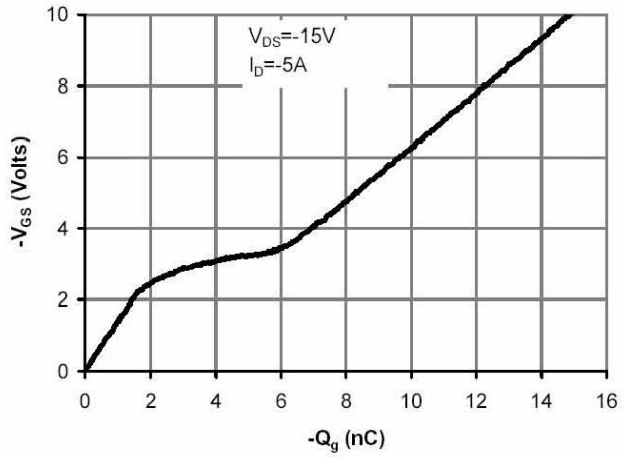


Fig 9. Gate Charge Characteristics

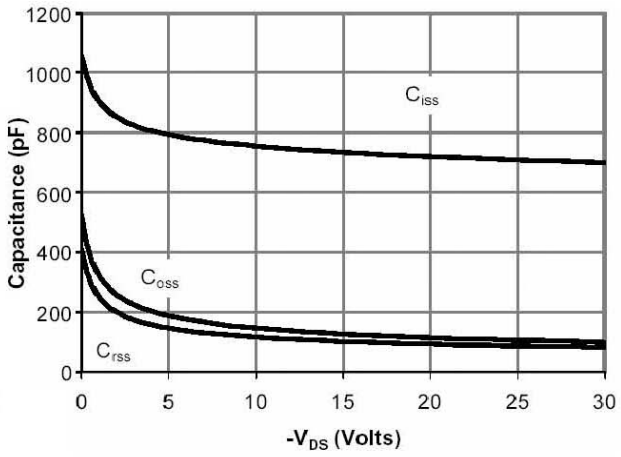


Fig 10. Typical Capacitance Characteristics

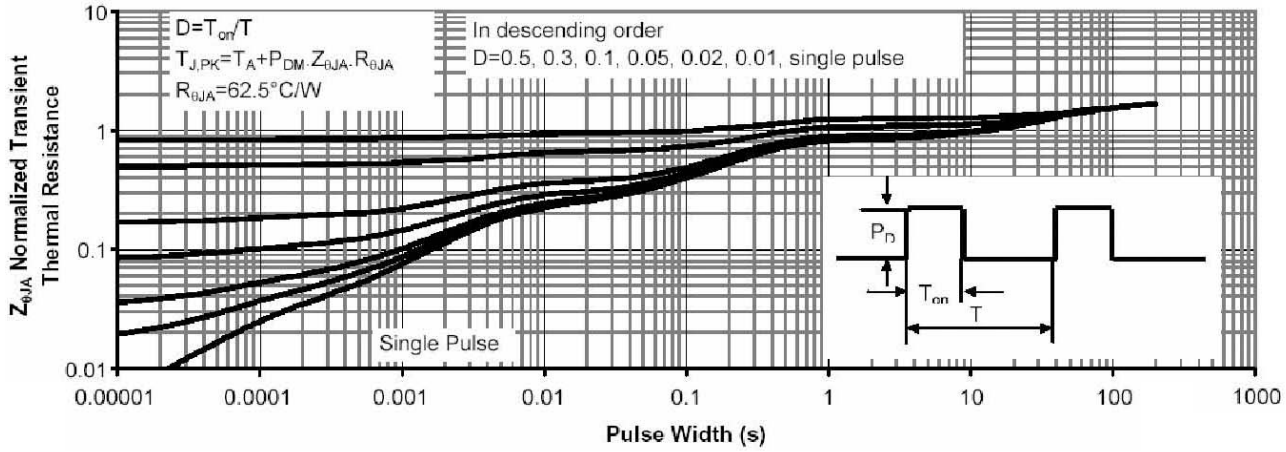


Fig 11. Normalized Maximum Transient Thermal Impedance