Elektronische Bauelemente

STT6802

3.3A , 30V , $R_{DS(ON)}$ 65 mΩ
N-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

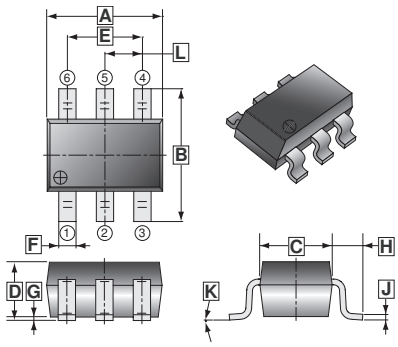
DESCRIPTION

STT6802 utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device. The TSOP-6 package is universally used for all commercial-industrial applications.

FEATURES

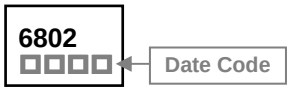
- Simple Drive Requirement
- Smaller Outline Package
- Surface mount package

TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60 REF.	
C	1.40	1.80	J	0.12 REF.	
D	1.10 MAX.		K	0°	10°
E	1.90 REF.		L	0.95 REF.	
F	0.30	0.50			

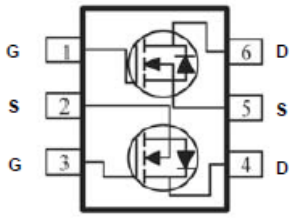
MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7 inch

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [3]	T_A=25℃	I_D	3.3	A
	T_A=70℃		2.6	
Pulsed Drain Current [1]		I_{DM}	10	A
Power Dissipation	T_A=25℃	P_D	1.14	W
Linear Derating Factor			0.01	W / ℃
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Maximum Junction to Ambient [3]		$R_{\theta JA}$	110	℃ / W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0
		-	-	25		V_{DS}=24V, V_{GS}=0, T_J=70°C
Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	-	65	mΩ	V_{GS}=10V, I_D=3A
		-	-	90		V_{GS}=4.5V, I_D=2A
Forward Transconductance	g_{fs}	-	4.0	-	S	V_{DS}=5V, I_D=3.0A
Dynamic						
Total Gate Charge[2]	Q_g	-	3.1	-	nC	V_{DS}=25V, V_{GS}=4.5V, I_D=3.0A
Gate-Source Charge	Q_{gs}	-	1.2	-		
Gate-Drain Charge	Q_{gd}	-	1.6	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	3.3	-	nS	V_{DS}=15V, V_{GS}=10V, R_{GEN}=3.3Ω, R_D=15Ω, I_D=1A
Rise Time	T_r	-	2.5	-		
Turn-off Delay Time	$T_{d(off)}$	-	13.2	-		
Fall Time	T_f	-	1.7	-		
Input Capacitance	C_{iss}	-	200	-	pF	V_{GS}=0,V_{DS}=25V,f=1.0MHz
Output Capacitance	C_{oss}	-	40	-		
Reverse Transfer Capacitance	C_{rss}	-	20	-		
Reverse Transfer Capacitance	R_g	-	2.3	3.0	Ω	f=1.0MHz
Source-Drain Diode						
Diode Forward Voltage [2]	V_{SD}	-	-	1.2	V	I_S=0.9A, V_{GS}=0V
Reverse Recovery Time	T_{RR}	-	14	-	ns	I_S=3.0A, V_{GS}=0V
Reverse Recovery Charge	Q_{RR}	-	7.0	-	nC	dI/dt=100A/μs

Notes:
1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in^2 copper pad of FR4 board, t≦5sec; 180℃/W when mounted on Min. copper pad.

CHARACTERISTIC CURVES

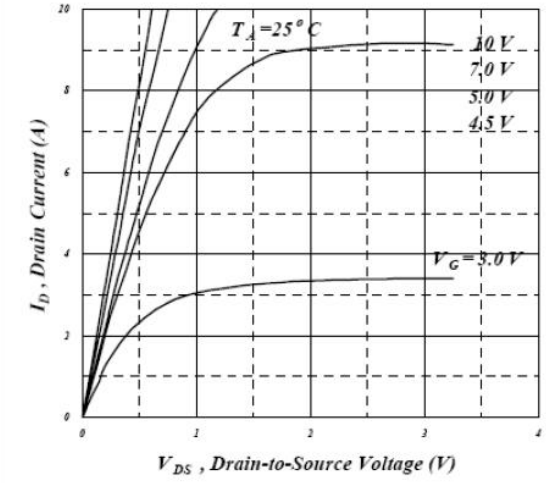


Fig 1. Typical Output Characteristics

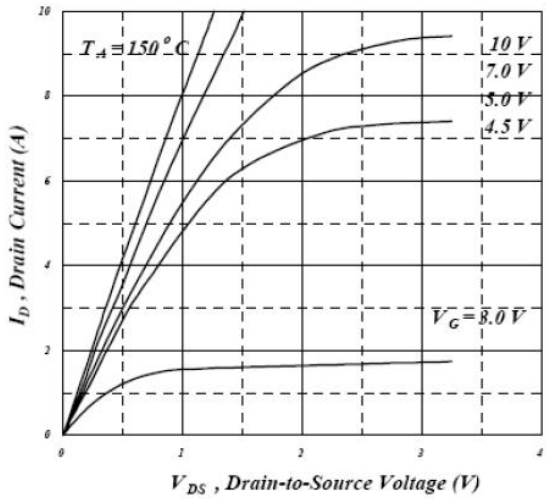


Fig 2. Typical Output Characteristics

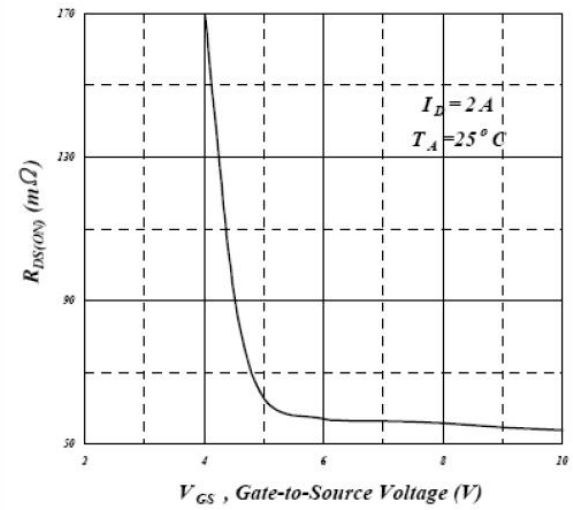


Fig 3. On-Resistance v.s. Gate Voltage

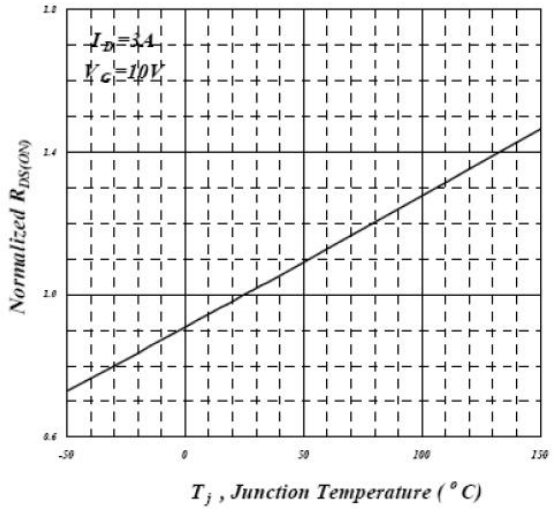


Fig 4. Normalized On-Resistance v.s. Junction Temperature

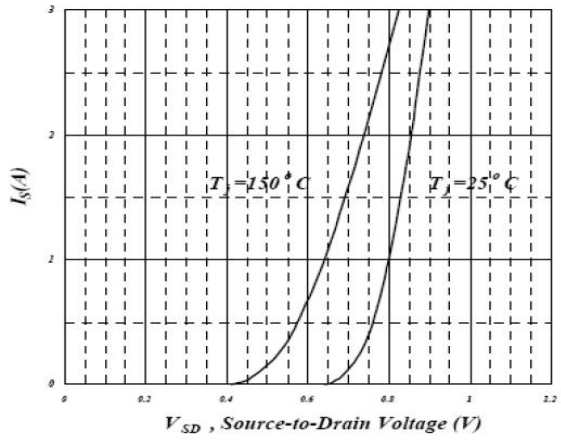


Fig 5. Forward Characteristic of Reverse Diode

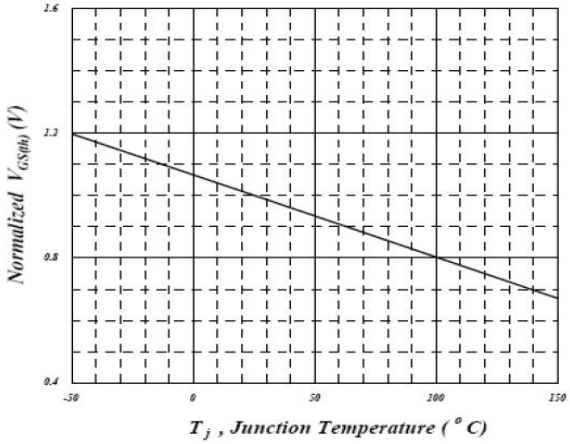


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVES

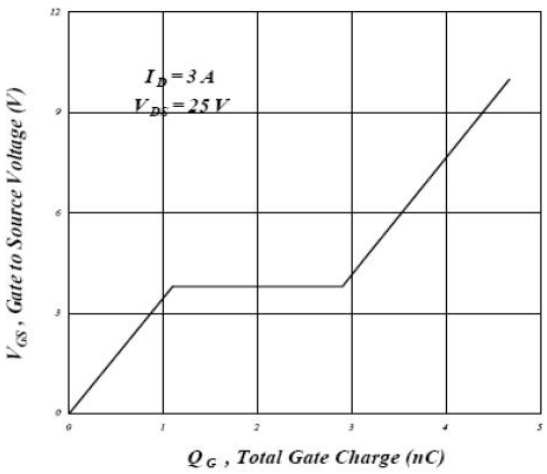


Fig 7. Gate Charge Characteristics

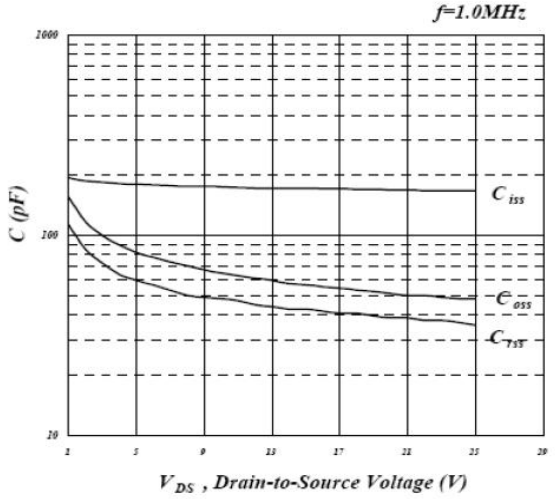


Fig 8. Typical Capacitance Characteristics

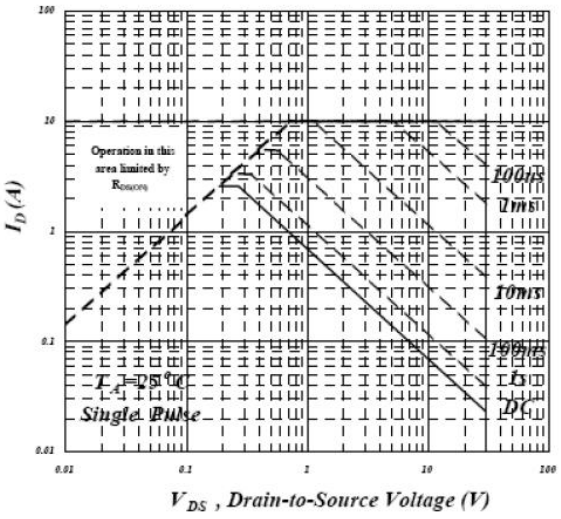


Fig 9. Maximum Safe Operating Area

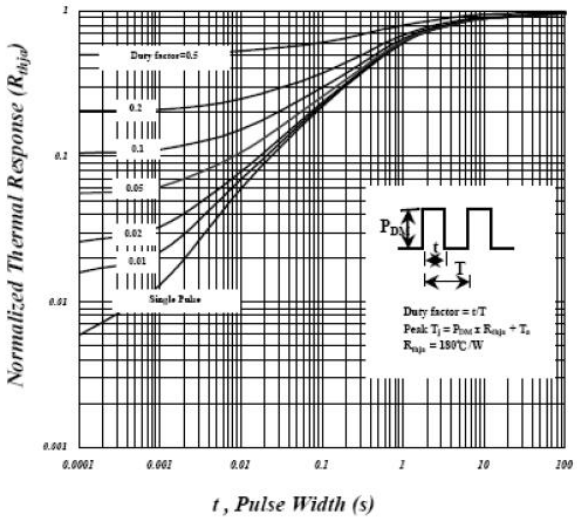


Fig 10. Effective Transient Thermal Impedance

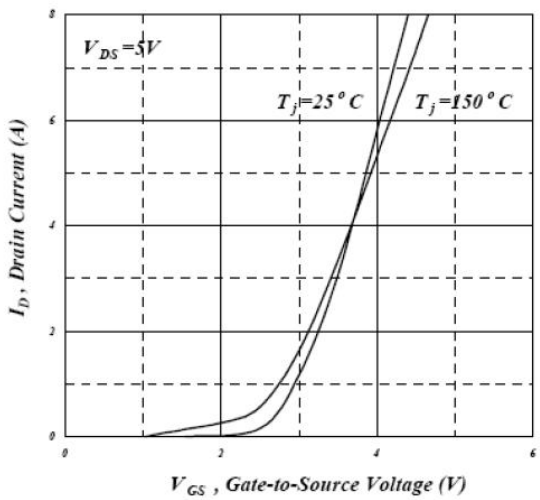


Fig 11. Transfer Characteristics

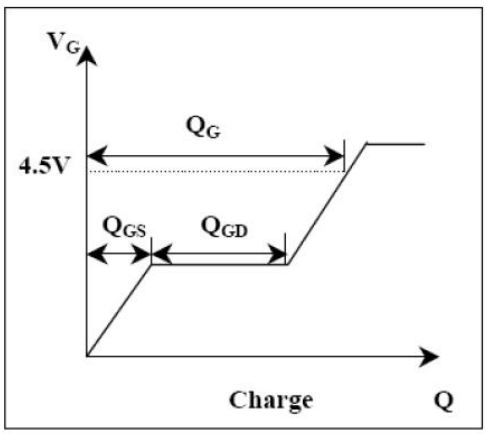


Fig 12. Gate Charge Waveform