11. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (T_a = 25°C)

Parameter	Symbol	Conditions	Rated Value	Unit
Supply voltage	V_{DD}		-0.3 to +7.0	V
	V_{LOAD}		V_{DD}-40 to V_{DD}+0.3	V
	V_{PRE}		V_{DD}-11 to V_{DD}+0.3	V
Input voltage	V_I		-0.3 to V_{DD}+0.3	V
Output voltage	V_O	Pins other than display output pins	-0.3 to V_{DD}+0.3	V
	V_{OD}	Display output pins	V_{DD}-40 to V_{DD}+0.3	V
High-level output current	I_{OH}	One of pins other than display output pins	-15	mA
		One pin of S0 to S9	-15	mA
		One pin of T0 to T15	-30	mA
		All pins other than display output pins	-20	mA
		Total of all display output pins	-120	mA
Low-level output current	I_{OL}	One pin	17	mA
		Total of all pins	60	mA
Total power dissipation(*1)	P_T	Plastic QFP	450	mW
		Plastic shrink DIP	600	mW
Operating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Operating supply voltage (T_a = -40°C to +85°C)

Item	Conditions	MIN.	MAX.	Unit
CPU(*2)		(*3)	6.0	V
Display controller		4.5	6.0	V
Timer/pulse generator		4.5	6.0	V
Hardware other than the above(*2)		2.7	6.0	V

*1 Method for calculating the total power dissipation

The uPD75217CW/GF dissipates power in the following places. The microcomputer shall be designed so that the sum of the values of power dissipation in these three places does not exceed the value of total power dissipation P_T. (NEC recommends that the microcomputer is used at 80% or less of the rated value.)

① Power dissipation at the CPU:
This value is calculated by V_{DD} (max.) x I_{DD1} (max.).

② Power dissipation at output pins:
There are two cases, normal output and display output. All the power dissipation values when the maximum current is applied to each output pin must be added.

③ Power dissipation at pull-down resistors:
Power dissipation at the pull-down resistors to be incorporated into each display output pin with the mask option

Example:

If the maximum current of 3 mA flows through each segment pin, 15 mA through the timing pin, and 10 mA through each LED output pin under the conditions of 4 LED outputs in 9_{SEG} x 11_{DIGIT}, V_{DD} = 5 V +10%, and 4.19 MHz oscillation, and if the voltage of the fluorescent display tube (the voltage V_{LOAD}) is -30 V and a little of power is dissipated at normal output:

① Power dissipation at the CPU: 5.5 V x 9.0 mA = 49.5 mW

② Power dissipation at pins:
Segment pins ... 2 V x 3 mA x 9 = 54 mW
Timing pin ..... 2 V x 15 mA = 30 mW

LED outputs $\ldots\ldots(\frac{10}{15} \times 2\ V) \times 10\ mA \times 4 = 53\ mW$

③ Power dissipation at pull-down resistors:

$$\frac{(30 + 5.5\ V)^2}{40\ k\Omega} \times 10 = 315\ mW$$

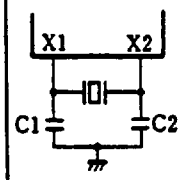
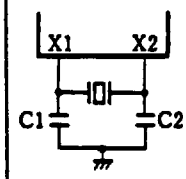
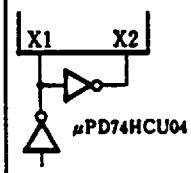
P_T = ① + ② + ③ = 501.5 mW

In this example, the power consumption of 501.5 mW is permitted because the total value of allowable power dissipation for the shrink DIP is 600 mW. The power consumption must be reduced for the QFP because the total value of allowable power dissipation is 450 mW. If the number of built-in pull-down resistors is reduced, power consumption can be reduced. In the example, built-in pull-down resisters only for eleven digit outputs and four segment outputs and external pull-down resistors for the remaining five segment outputs enables the power consumption to be limited to 344 mW.

*2 The CPU does not include the system clock oscillator, the display controller, and the timer/pulse generator.

*3 The range of the supply voltage at which the CPU can operate varies according to the cycle time. See the item of AC characteristics.

Characteristics of the main system clock oscillator
(T_a = -40°C to +85°C, V_{DD} = 2.7 to 6.0 V)

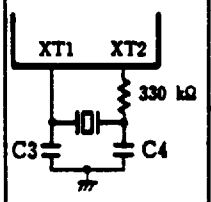
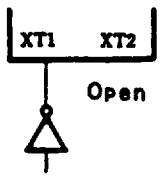
Resonator	Recommended constant	Parameter	Condition	MIN.	TYP.	MAX.	Unit
(*3) Ceramic resonator		(*1) Oscillator frequency (f_{XX})	V_{DD} = oscillation voltage range	2.0		5.0	MHz
		(*2) Oscillation stability time	After V_{DD} reaches MIN. of the oscillation voltage range			4	ms
(*3) Crystal resonator		(*1) Oscillator frequency (f_{XX})		2.0	4.19	5.0	MHz
		(*2) Oscillation stability time	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		(*1) X1 input frequency (f_X)		2.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

*1 The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

*2 The oscillation stability time means the time required for the oscillation to stabilize after V_{DD} is applied or after the STOP mode is released.

*3 NEC recommends the resonators shown in the table of DC characteristics.

Characteristics of the subsystem clock oscillator (T_a = -40°C to +85°C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Crystal resonator		(*1) Oscillator frequency (f_{XT})		32	32.768	35	kHz
		(*2) Oscillation stability time	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		(*1) XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		10		32	us

*1 The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

*2 The oscillation stability time means the time required for the oscillation to stabilize after V_{DD} is applied or after the STOP mode is released.

Capacitance (T_a = 25°C, V_{DD} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance		C_{IN}				15	pF
Output capacitance	Other than display output	C_{OUT}	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
	Display output					35	pF
I/O capacitance		C_{IO}				15	pF

Recommended oscillator constant

Main system clock: Ceramic resonator (T_a = -40°C to +80°C)

Manufacturer	Part number	Capacitance (pF) for connection		Oscillation voltage range (V)		Remarks
		C1	C2	Min.	Max.	
Kyocera Corporation	KBR-2.0MS KBR-4.0MS	47 33	47 33	2.7	6.0	
Murata Mfg. Co., Ltd.	CSA 2.00MG CSA 4.19MG	30	30	2.7	6.0	
	CST 2.00MG CST 4.19MG	-	-			Containing capacitor
Toko, Inc.	CRHF3.00 CRHF4.19	30	30	3.0	3.0	

-: Unrequired

Main system clock: Crystal resonator (T_a = -40°C to +85°C)

Manufacturer	Part number	Capacitance (pF) for connection		Oscillation voltage range (V)		Remarks
		C1	C2	Min.	Max.	
Kinseki,Ltd.	HC-49/U	22	22	2.7	6.0	

Subsystem clock: 32.768 kHz crystal reonator (T_a = -10°C to +60°C)

Manufacturer	Part number	Capacitance for connection			Oscillation voltage range		Remarks
		C3 (pF)	C4 (pF)	R (kΩ)	Min. (V)	Max. (V)	
Kinseki,Ltd.	P-3	15	22	330	2.7	6.0	

DC characteristics (T_a = -40°C to +85°C, V_{DD} = 2.7 to 6.0 V)

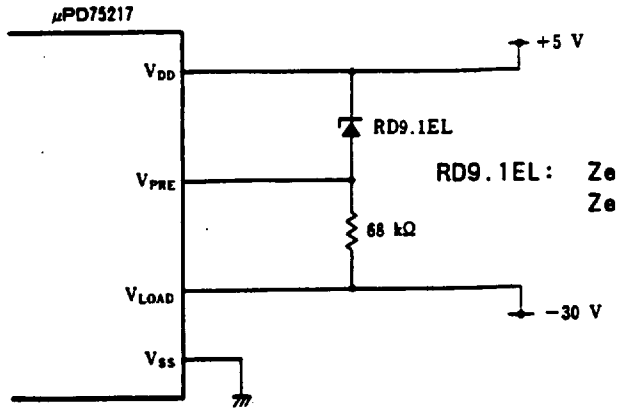
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Other than below		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0 and 1, and $\overline{RESET}$		0.75 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, and XT1		V_{DD} - 0.4		V_{DD}	V
	V_{IH4}	Port 6	V_{DD} = 4.5 to 6.0 V	0.65 V_{DD}		V_{DD}	V
				0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	Other than below		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, and 6, and $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, and XT1		0		0.4	V
High-level output voltage	V_{OH}	All output pins	V_{DD} = 4.5 to 6.0 V, I_{OH} = -1 mA	V_{DD} - 1.0			V
			I_{OH} = -100 uA	V_{DD} - 0.5			V
Low-level output voltage	V_{OL}	Ports 4 and 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		All output pins	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 uA			0.5	V
High-level input leakage voltage	I_{LIH1}	Other than X1, X2, and XT1	V_{IN} = V_{DD}			3	uA
	I_{LIH2}	X1, X2, and XT1				20	uA
Low-level input leakage voltage	I_{LIL1}	Other than X1, X2, and XT1	V_{IN} = 0 V			-3	uA
	I_{LIL2}	X1, X2, and XT1				-20	uA

(to be continued)

(Cont'd)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High-level output leakage voltage	I_{LOH}	All output pins	$V_{OUT} = V_{DD}$				3	uA
Low-level output leakage voltage	I_{LOL1}	Other than display output	$V_{OUT} = 0$ V				-3	uA
	I_{LOL2}	Display output	$V_{OUT} = V_{LOAD} = V_{DD} - 35$ V				-10	uA
Display output current	I_{OD}	S0 to S9	V_{DD} = 4.5 to 6.0 V	(*1) $V_{PRE} = V_{DD} - 9 \pm 1$ V	-3	-5.5		mA
			$V_{DD} = V_{DD} - 2$ V	$V_{PRE} = 0$ V	-1.5	-3.5		mA
		T0 to T15		(*1) $V_{PRE} = V_{DD} - 9 \pm 1$ V	-15	-22		mA
				$V_{PRE} = 0$ V	-7	-15		mA
Built-in pull-down resistor (mask option)	R_{PG}	Port G $V_{IN} = V_{DD}$	V_{DD} = 4.5 to 6.0 V		20	80	200	kΩ
					20		1000	kΩ
	R_L	Display output	$V_{DD} - V_{LOAD} = 35$ V		25	70	135	kΩ
(*2) Supply current	I_{DD1}	4.19 MHz Crystal resonance C1 = C2 = 15 pF	$V_{DD} = 5$ V ±10% (*3)			3.0	9.0	mA
			$V_{DD} = 3$ V ±10% (*4)			0.55	1.5	mA
	I_{DD2}		HALT mode	$V_{DD} = 5$ V ±10%		600	1800	uA
				$V_{DD} = 3$ V ±10%		200	600	uA
	I_{DD3}	(*5) 32 kHz Crystal resonator	$V_{DD} = 3$ V ±10%			40	120	uA
	I_{DD4}		HALT mode	$V_{DD} = 3$ V ±10%		5	15	uA
	I_{DD5}	XT1 = 0 V STOP mode	$V_{DD} = 5$ V ±10%			0.5	20	uA
			$V_{DD} = 3$ V ±10%			0.1	10	uA

*1 The following external circuits are recommended.



RD9.1EL: Zener diode (NEC)
Zener voltage = 8.29 to 9.30 V

*2 This current does not refer to the current which flows through the built-in pull-down resistors (mask option).

*3 Value when the processor clock control resistor (PCC) is set to 0011 and operated in the high-speed mode

*4 Value when the PCC is set to 0000 and operated in the low-speed mode

*5 Value when the system clock control resistor (SCC) is set to 1001, generation of the main system clock pulse is stopped, and the SCC is operated according to the subsystem clock pulse.

AC characteristics (T_a = -40°C to +85°C, V_{DD} = 2.7 to 6.0 V)

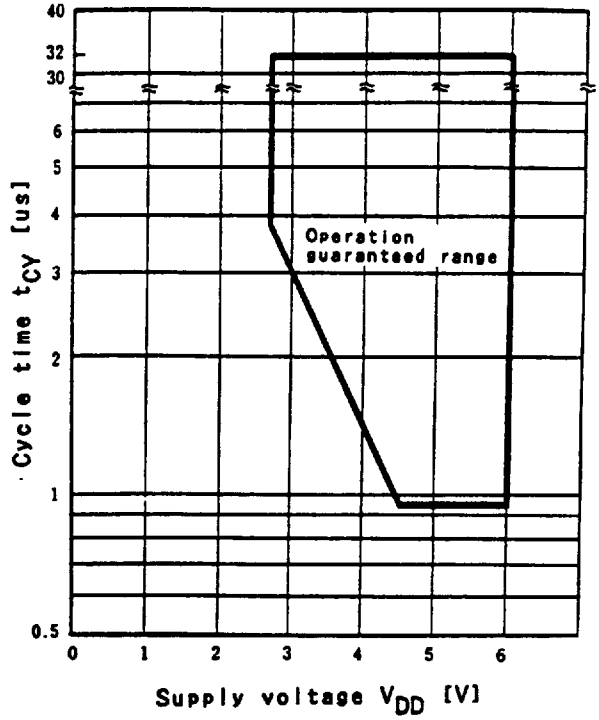
Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time) (*1)	t_{CY}	Operated by main system clock pulse	V_{DD} = 4.5 to 6.0 V		0.95		32	us
					3.8		32	us
		Operated by sub-system clock pulse			114	122	125	us
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V			0		0.6	MHz
					0		165	kHz
TI0 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V			0.83			us
					3			us
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 6.0 V		Input	0.8			us
				Output	0.95			us
				Input	3.2			us
				Output	3.8			us
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V		Input	0.4			us
				Output	$t_{KCY}/2-50$			ns
				Input	1.6			us
				Output	$t_{KCY}/2-150$			ns
SI setup time (referred to $\overline{SCK}$↑)	t_{SIK}				100			ns
SI hold time (referred to $\overline{SCK}$↑)	t_{KSI}				400			ns
$\overline{SCK}$↓→SO output delay time	t_{KSO}	V_{DD} = 4.5 to 6.0 V					300	ns
							1000	ns
Interrupt input high/low level width	t_{INTH}, t_{INTL}			INT0	(*2)			us
				INT1	$2t_{CY}$			us
				INT2,4	10			us
$\overline{RESET}$ low level width	t_{RSL}				10			us

*1 The cycle time (minimum instruction execution time) depends on the connected resonator frequency, the system clock control register (SCC), and the processor clock control register (PCC).

The following figure shows the cycle time t_{CY} characteristics for the supply voltage V_{DD} during main system clock operation.

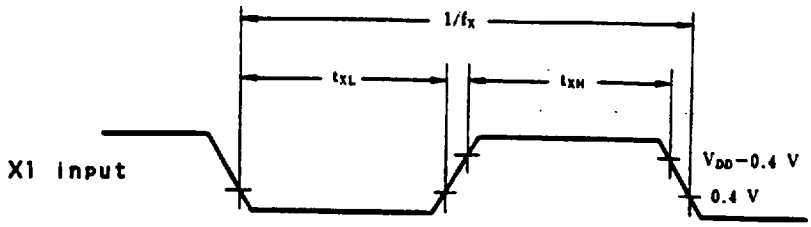
*2 This value becomes $2t_{CY}$ or $128/f_{XX}$ according to the setting of the interrupt mode register (IMO).

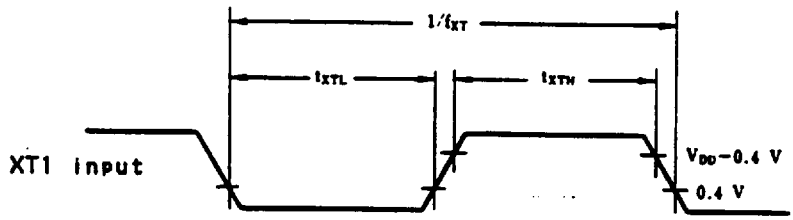
t_{CY} vs V_{DD}
(when the main system clock is operating)



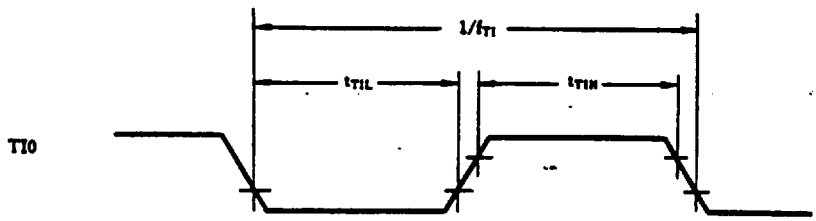
AC timing measurement points (excluding X1, and XT1 inputs)

Clock timing

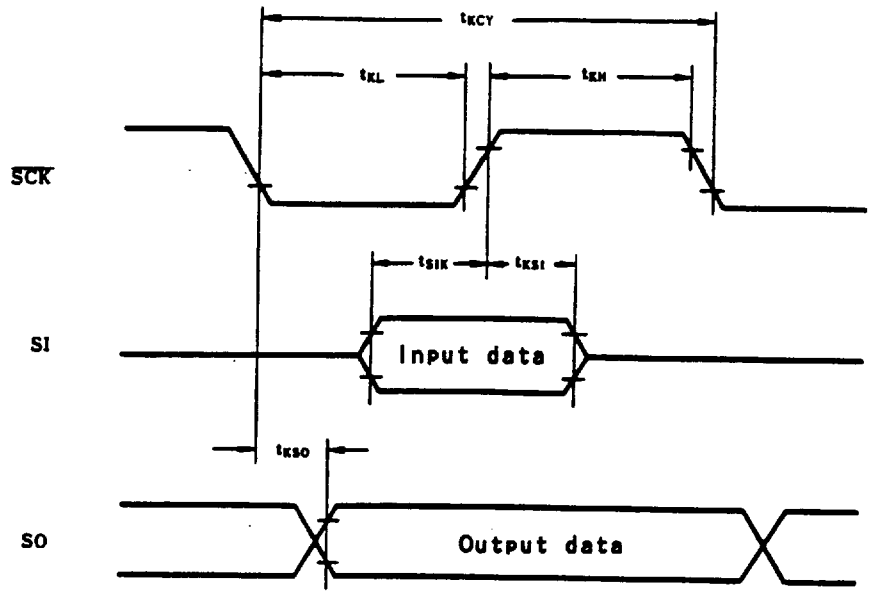




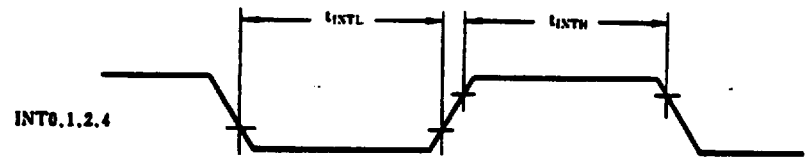
T10 timing



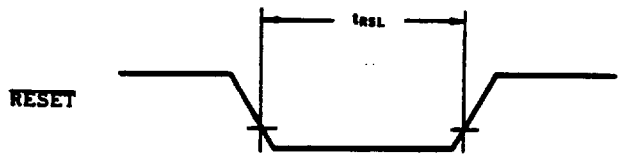
Serial transfer timing



Interrupt input timing



$\overline{\text{RESET}}$ input timing



Data hold characteristics by low supply voltage in data memory STOP mode (T_a = -40°C to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		2.0		6.0	V
(*1) Data hold supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	uA
Release signal setting time	t_{SREL}		0			us
(*2) Oscillation stability wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		(*3)		ms

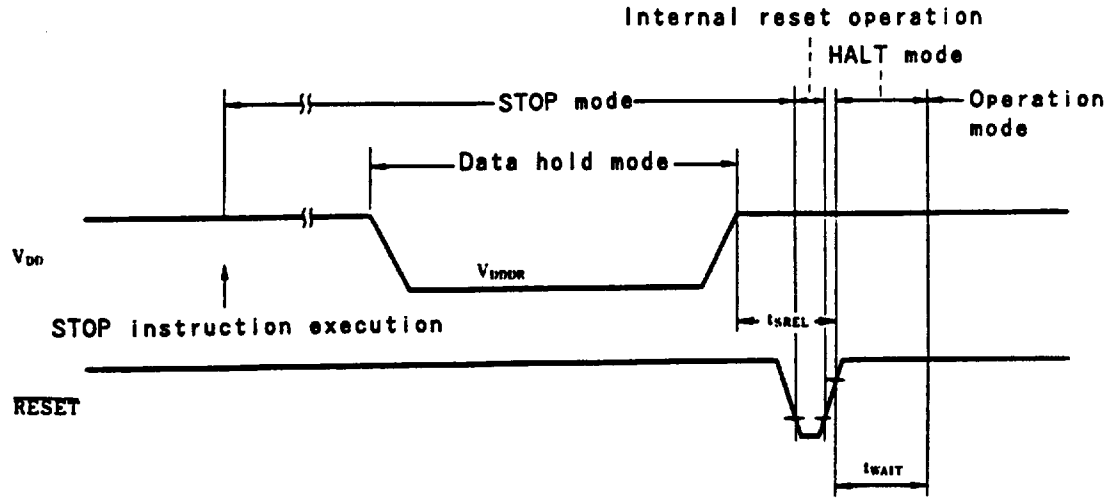
*1 Excluding the current which flows through the built-in pull-down resistors (mask option)

*2 CPU operation stop time for preventing unstable operation at the beginning of oscillation

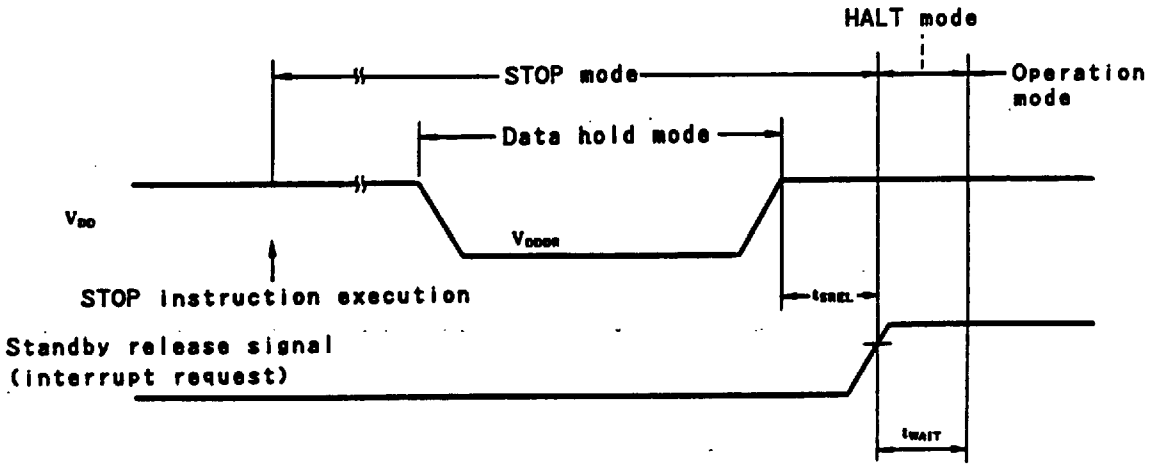
*3 This value depends on the settings of the basic interval timer mode register (BTM) shown below.

BTM3	BTM2	BTM1	BTM0	WAIT time: Value at f_{XX} = 4.19 MHz is enclosed in ( ).
–	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

Data hold timing (STOP mode release by $\overline{\text{RESET}}$)

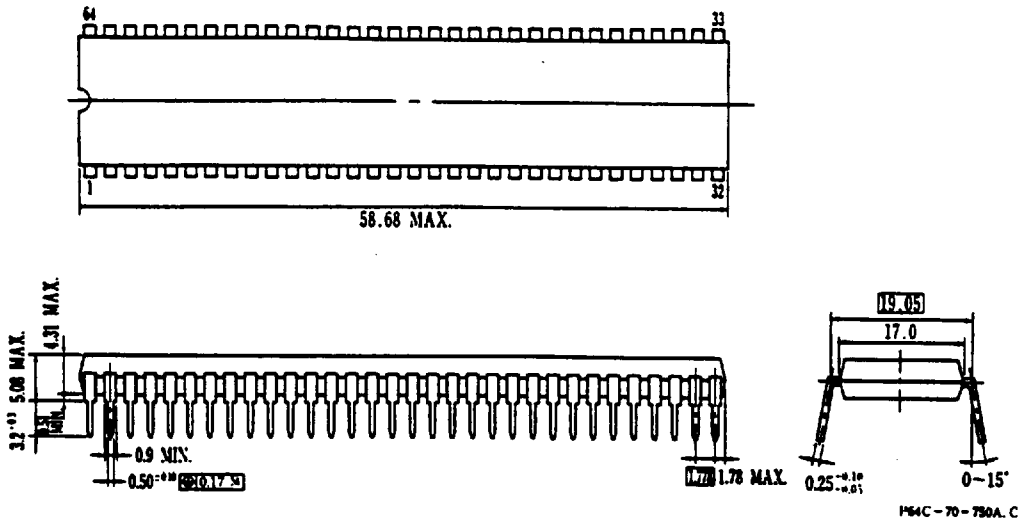


Data hold timing (standby release signal: STOP mode release by interrupt signal)

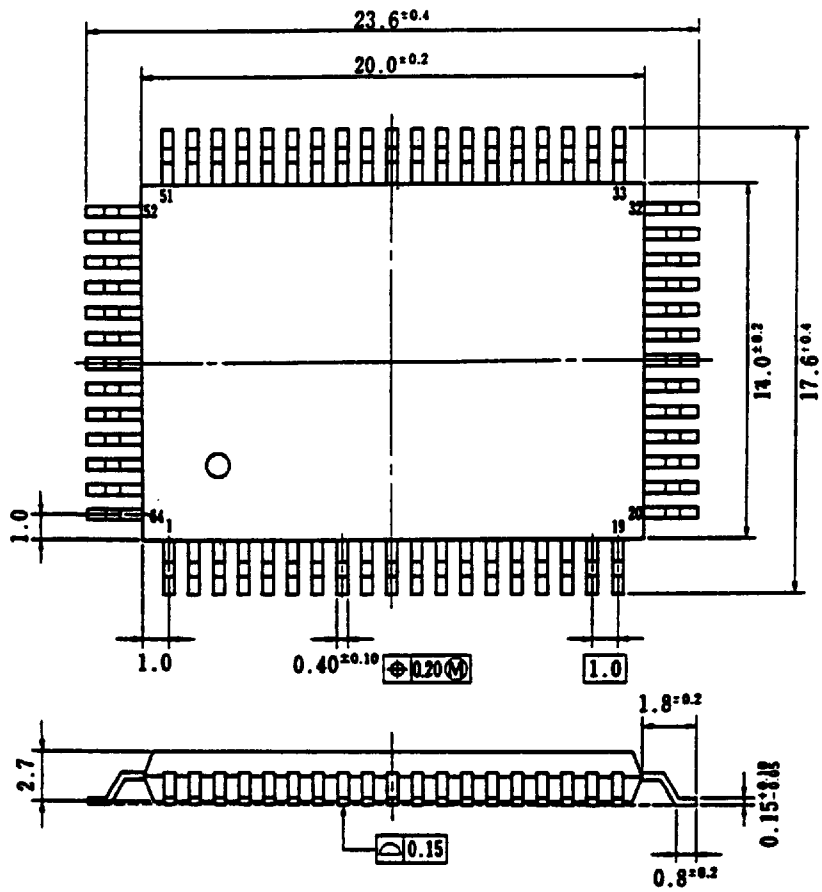


12. OUTSIDE DIMENSIONS

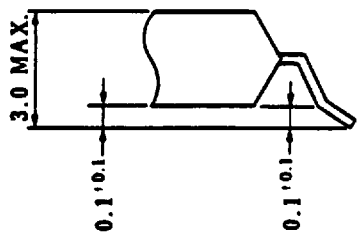
64-pin plastic shrink DIP (750 mil) outside dimensions (mm)



64-pin plastic QFP outside dimensions (mm)

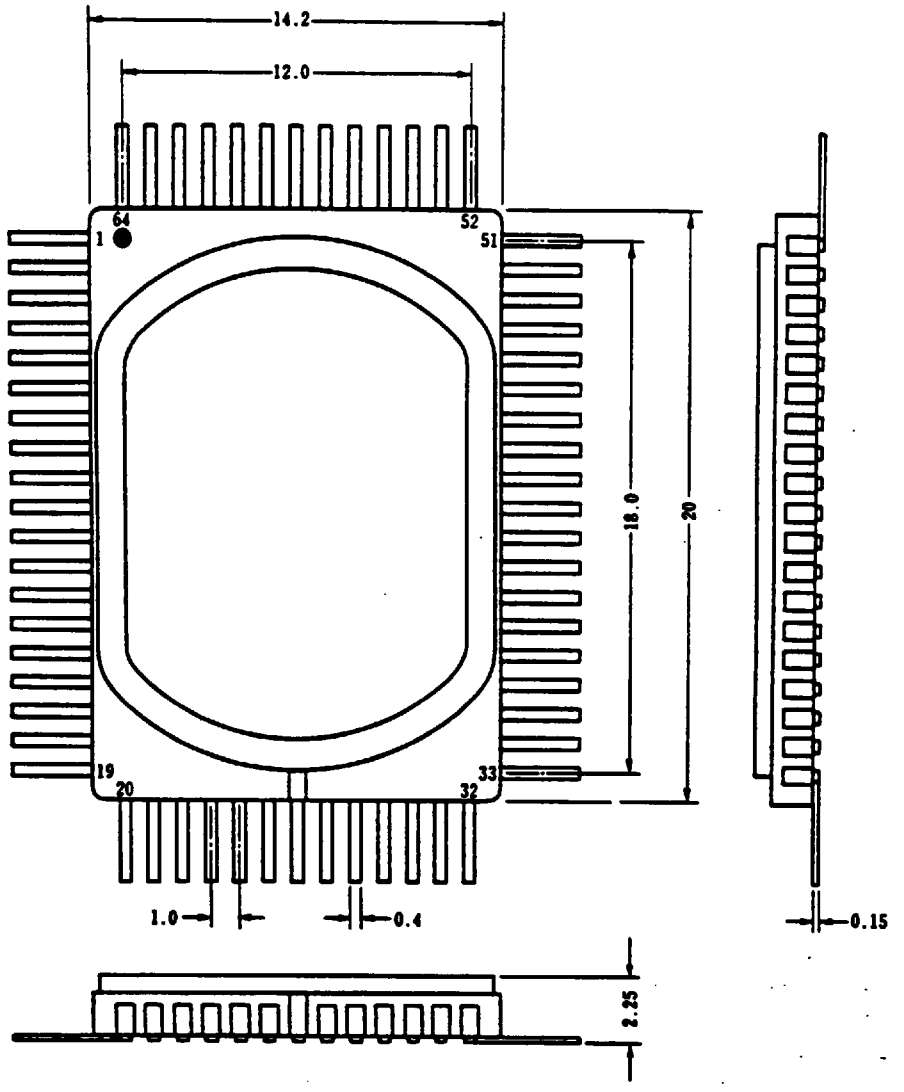


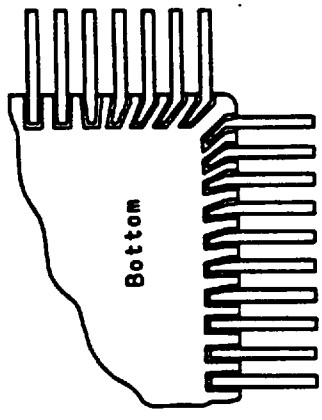
Details of Pin Tip Shape



P64GF-100-3B8,3BE-1

Outside dimensions (mm) of 64-pin ceramic QFP for ES (ref. dwg.)





Notes 1: Care must be taken because the metal cap connected to 26 pins reaches positive power level.

2: Care must be taken because the underside leads are bent as shown in the figure.

3: The length of a lead is not specified because the process of cutting the lead tip is not managed.