SLG8SP513

Clock Synthesizer for Intel Mobile PCI-Express Chipset

Features

- Low Power CK505 compatible clock synthesizer
- SLG8SP513 is a cost reduced CK505 with integrated voltage regulator for mobile applications
- Scalable Low Voltage VDD I/O (3.3V to 1.05V) to reduce power consumption
- Low Power differential outputs with integrated series termination resistors (50 ohm resistor to GND and 33 ohm series resistor not needed)
- Integrated CK_SSCD function to provide additional Spread Spectrum support for GMCH
- CLK_REQ# inputs to support SRC clock power management
- 64 pin QFN Package

Output Summary

- 2- differential CPU clock outputs @ 0.7V
- 1 - selectable differential CPU/SRC clock output @ 0.7V
- 1 - selectable differential DOT96/SRC clock output @ 0.7V
- 8 - differential Serial Reference Clock (SRC) clock outputs @ 0.7V
- 1 - selectable LCDCLK/27M clock output
- 1 - single-ended 48MHz clock output @ 3.3V
- 6 - single-ended 33MHz clock outputs @ 3.3V
- 1 - single-ended 14.318MHz clock output @ 3.3V

Table 1. Frequency Select Table (FS_C, FS_B, FS_A)

FS_C	FS_B	FS_A	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT_96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Table 2. LCDCLK & 27M_SS Spread Spectrum Table

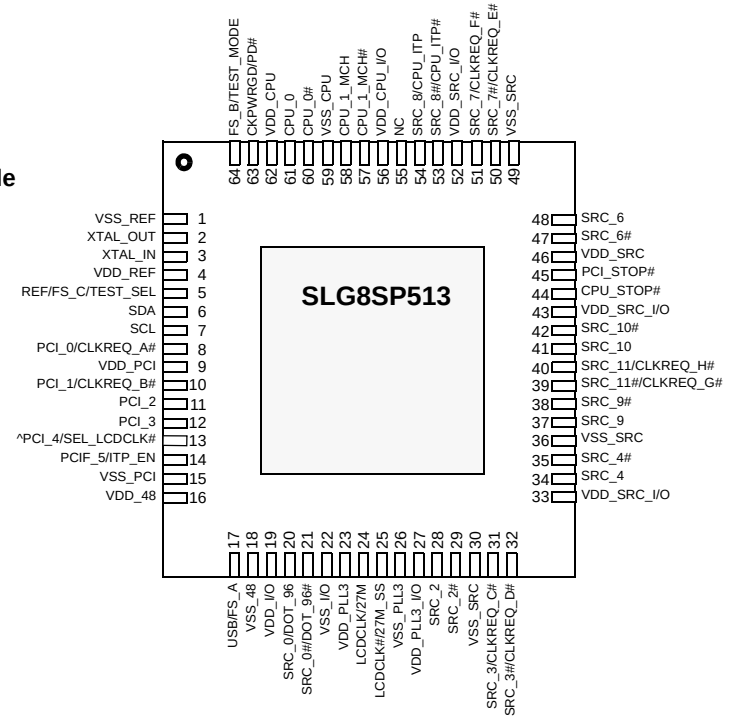
B1b5	B1b3	B1b2	B1b1	Spread Spectrum %
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	-0.50% SS
0	0	1	1	-1.00% SS
0	1	0	0	-1.50% SS
0	1	0	1	-2.00% SS
0	1	1	0	-2.50% SS
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	+/-0.25% SS
1	0	1	1	+/-0.50% SS
1	1	0	0	+/-0.75% SS
1	1	0	1	+/-1.00% SS
1	1	1	0	+/-1.25% SS
1	1	1	1	Reserved

Table 3. SEL_LCDCLK# Input Functional Table

SEL_LCDCLK#	Pin 20/21	Pin 24/25
0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

Pin Configuration

(Top View)



^ This pin has internal pull-down to GND

64-Pin QFN
9.0 x 9.0mm body, 0.50mm pitch

Pin Description

Pin #	Name	Type	Description
1	VSS_REF	GND	Ground for outputs.
2	XTAL_OUT	O, SE	14.318MHz crystal output.
3	XTAL_IN	I	14.318MHz crystal input.
4	VDD_REF	PWR	3.3V power supply for outputs.
5	REF/FS_C/TEST_SEL	I/O, SE	14.318 reference clock output. When FS_C/TEST_SEL input is pulled to 3.3V during CKPWRGD assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold. After CKPWRGD assertion, this pin will be configured as REF output.
6	SDA	I/O, SE	Serial Interface bus data input and output.
7	SCL	I	Serial Interface bus clock input.
8	PCI_0/CLKREQ_A#	I/O, SE	Configurable PCI clock output or CLKREQ input.
9	VDD_PCI	PWR	3.3V power supply for outputs.
10	PCI_1/CLKREQ_B#	I/O, SE	Configurable PCI clock output or CLKREQ input.
11	PCI_2	O, SE	PCI clock output.
12	PCI_3	O, SE	PCI clock output.
13	PCI_4/SEL_LCDCLK#	I/O, SE	PCI clock output. 3.3V input to select output function of pin 20/21 and 24/25. 0 = LCDCLK & DOT_96 for internal graphic controller support 1 = 27M & 27M_SS & SRC_0 for external graphic controller support
14	PCIF_5/ITP_EN	I/O, SE	Free running PCI clock output. When ITP_EN input is sampled HIGH during CKPWRGD assertion, it will configure CPU_ITP/SRC_8 as CPU output.
15	VSS_PCI	GND	Ground for outputs.
16	VDD_48	PWR	3.3V power supply for outputs.
17	USB/FS_A	I/O, SE	USB clock output. Frequency Select input to determine CPU output frequency.
18	VSS_48	GND	Ground for outputs.
19	VDD_I/O	PWR	Low voltage I/O power supply for outputs.
20	SRC_0/DOT_96	O, DIF	Configurable SRC or 96 MHz DOT clock output.
21	SRC_0#/DOT_96#	O, DIF	Configurable SRC or 96 MHz DOT clock output.
22	VSS_I/O	GND	Ground for outputs.
23	VDD_PLL3	PWR	3.3V power supply for outputs.
24	LCDCLK/27M	O, DIF/SE	Clock output for graphic contoller.
25	LCDCLK#/27M_SS	O, DIF/SE	Clock output for graphic contoller.
26	VSS_PLL3	GND	Ground for outputs.
27	VDD_PLL3_I/O	PWR	Low voltage I/O power supply for outputs.
28	SRC_2	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
29	SRC_2#	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
30	VSS_SRC	GND	Ground for outputs.

Pin Description (continued)

Pin #	Name	Type	Description
31	SRC_3/CLKREQ_C#	I/O	Configurable differential SRC clock output or CLKREQ input.
32	SRC_3#/CLKREQ_D#	I/O	Configurable differential SRC clock output or CLKREQ input.
33	VDD_SRC_I/O	PWR	Low voltage I/O power supply for outputs.
34	SRC_4	O, DIF	Differential Serial Reference Clock output.
35	SRC_4#	O, DIF	Differential Serial Reference Clock output.
36	VSS_SRC	GND	Ground for outputs.
37	SRC_9	O, DIF	Differential Serial Reference Clock output.
38	SRC_9#	O, DIF	Differential Serial Reference Clock output.
39	SRC_11#/CLKREQ_G#	I/O	Configurable differential SRC clock output or CLKREQ input.
40	SRC_11/CLKREQ_H#	I/O	Configurable differential SRC clock output or CLKREQ input.
41	SRC_10	O, DIF	Differential Serial Reference Clock output.
42	SRC_10#	O, DIF	Differential Serial Reference Clock output.
43	VDD_SRC_I/O	PWR	Low voltage I/O power supply for outputs.
44	CPU_STOP#	I	3.3V LVTTL input for CPU_STOP#.
45	PCI_STOP#	I	3.3V LVTTL input for PCI_STOP#.
46	VDD_SRC	PWR	3.3V power supply for outputs.
47	SRC_6#	O, DIF	Differential Serial Reference Clock output.
48	SRC_6	O, DIF	Differential Serial Reference Clock output.
49	VSS_SRC	GND	Ground for outputs.
50	SRC_7#/CLKREQ_E#	I/O	Configurable differential SRC clock output or CLKREQ input.
51	SRC_7/CLKREQ_F#	I/O	Configurable differential SRC clock output or CLKREQ input.
52	VDD_SRC_I/O	PWR	Low voltage I/O power supply for outputs.
53	SRC_8#/CPU_ITP#	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
54	SRC_8/CPU_ITP	O, DIF	Selectable differential CPU or SRC output. It will configure as CPU clock when ITP_EN is sampled HIGH. It will configure as SRC clock when ITP_EN is sampled LOW.
55	NC	I	No connect.
56	VDD_CPU_I/O	PWR	Low voltage I/O power supply for outputs.
57	CPU_1_MCH#	O, DIF	Differential CPU Clock output. This CPU output will be active during Intel AMT M1 mode.
58	CPU_1_MCH	O, DIF	Differential CPU Clock output. This CPU output will be active during Intel AMT M1 mode.
59	VSS_CPU	GND	Ground for outputs.
60	CPU_0#	O, DIF	Differential CPU Clock output.

Pin Description (continued)

Pin #	Name	Type	Description
61	CPU_0	O, DIF	Differential CPU Clock output.
62	VDD_CPU	PWR	3.3V power supply for outputs.
63	CKPWRGD/PD#	I	CKPWRGD is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After CKPWRGD assertion, it becomes a real time input for asserting power down (active high).
64	FS_B/TEST_MODE	I	Frequency Select input to determine CPU output frequency. When in test mode, FS_B/TEST_MODE will configure outputs to run at REF or Hi-Z. 0 = Hi-Z, 1 = REF

Block Diagram

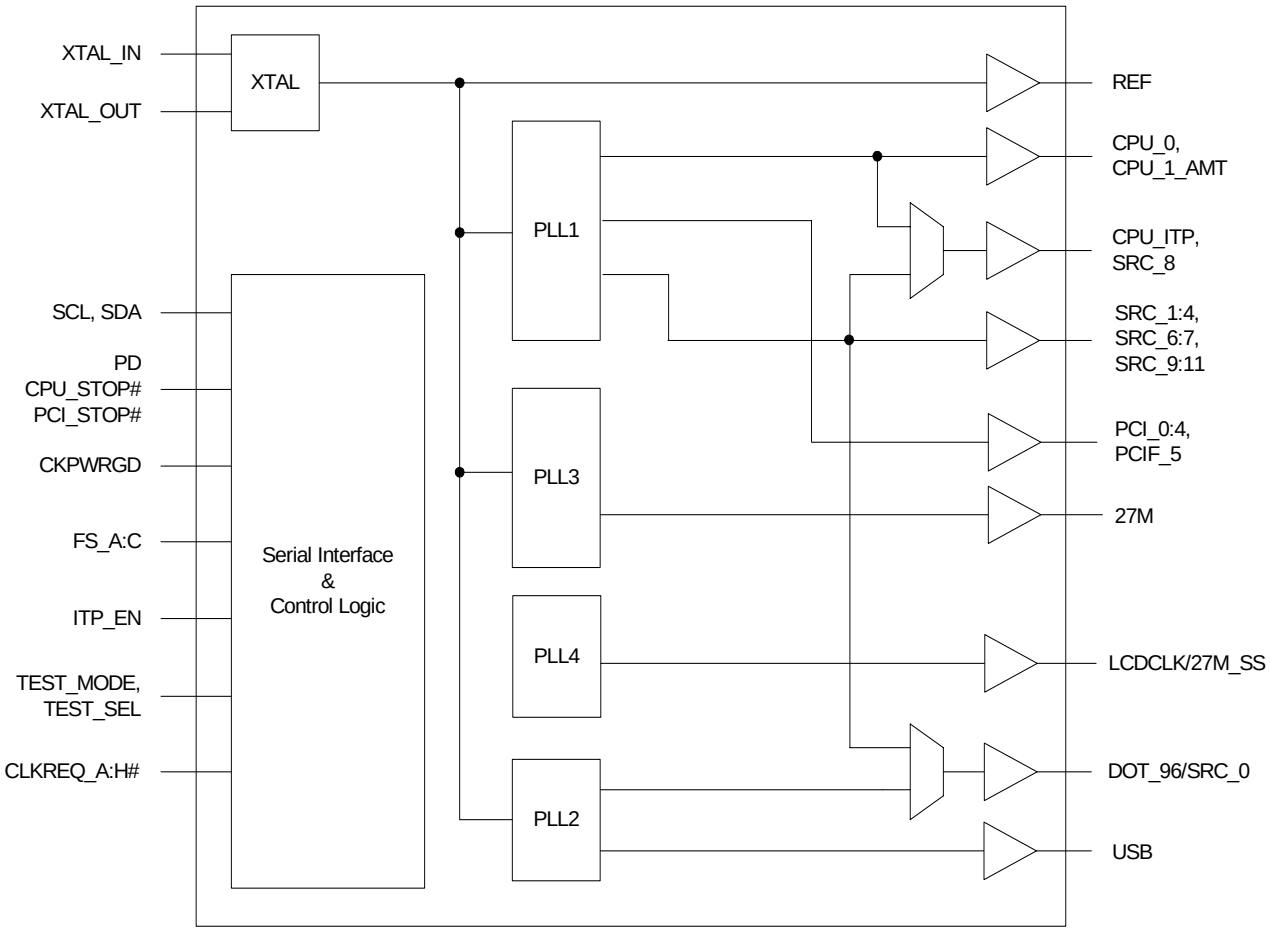


Figure 1. Simplified Block Diagram

Enhanced Scalable VDD type “SR” differential output buffer for mobile applicaiton

The CK505 utilizes a new output buffer for all differential clocks. The low power type SR buffer is a departure from the type X buffer used in previous CK410 clock generators. The Silego enhanced SR buffer uses custom drivers powered off from a scalable voltage power supply ranging from 1.05V to 3.3V, offering reduction in implementation cost and power consumption. It also improves edge rate performance, and cross point voltage control. In addition, the Silego enhanced SR buffer integrates the 33 ohm series termination resistors, which simplifies board layout and eliminates 20 passive components.

Low Voltage VDD_I/O Implementation Note (VDD_I/O = 1.05V)

The scalable VDD_I/O architecture in the SLG8SP513 is designed to accommodate a variety of low power mobile configurations. One such example is when the clock chip VDDIO is sourced from very low voltages such as 1.05V. Designed this way, significant power savings can be realized.

The CK505 Clock Synthesizer Specification already anticipates and allows for aggressive low power implementations. When using the SLG8SP513 with VDDIO=1.05V, some rounding of the waveform top edges are expected to occur. Because of variation in trace length and loading, the resulting slew rate can be somewhat affected. The SLG8SP513 has additional compensation available for those applications. Design engineers can set Control Register 9, Bits 2:0 to ‘111’ if additional slew rate is desired.

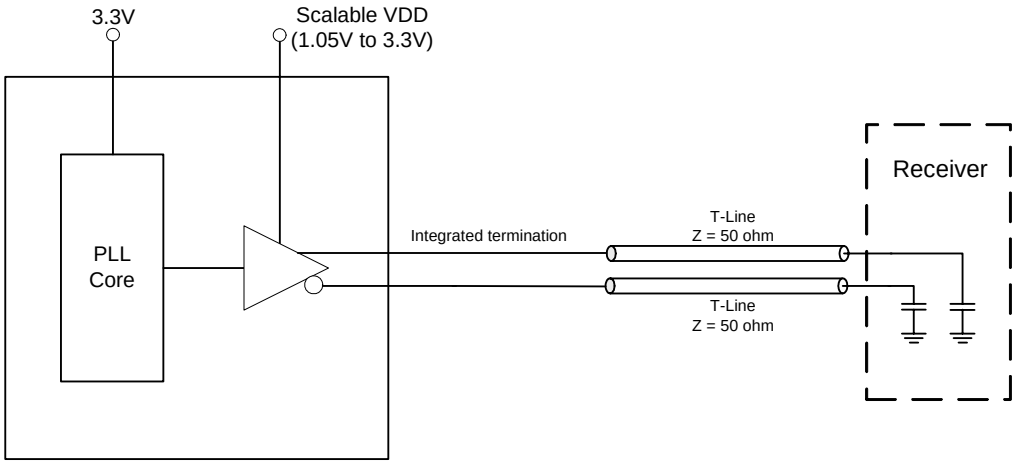


Figure 2. Type SR Differential Output Buffer

Silego CK505 with Integrated Linear Regulator

The SLG8SP513 eliminates the need of external pass element such as a common 2N3904 (SOT23) NPN transistor or a BSS138 MOSFET. The highly integrated CK505 drivers from Silego supports SR type output buffers with a scalable VDD_I/O power supply ranging from 1.05V to 3.3V. It simplifies layout, reduce implementation cost and BOM cost.

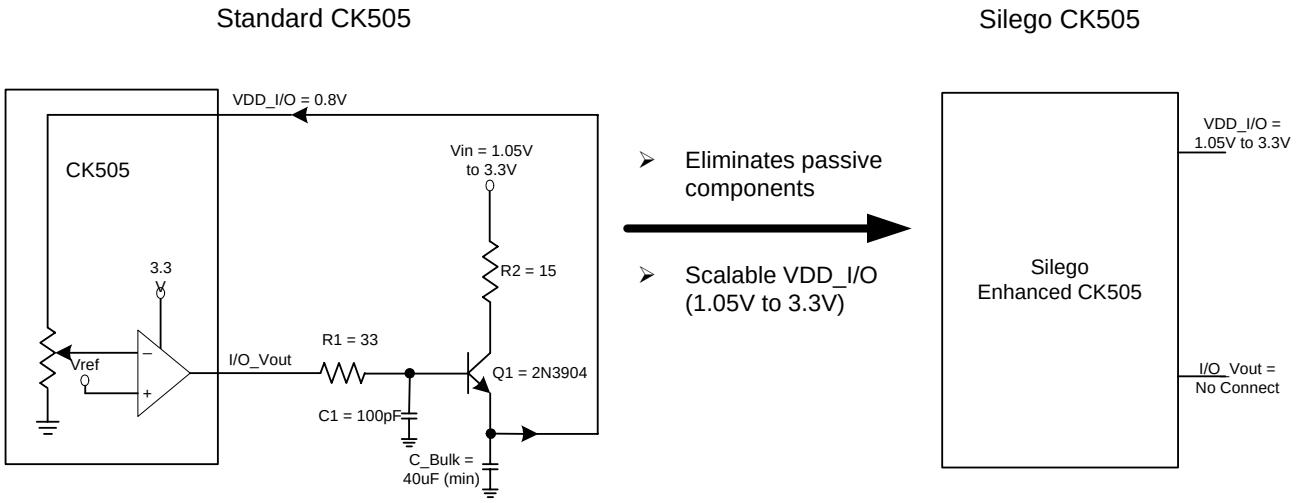


Figure 3. Silego CK505 with Integrated Linear Regulator

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 4*. The slave receiver address is 11010010 (D2h).

Table 4. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	R	Reflected the value of FS_C pin sampled on power up	X
6	R	Reflected the value of FS_B pin sampled on power up	X
5	R	Reflected the value of FS_A pin sampled on power up	X
4	RW	iAMT Enable 0 = Legacy Mode 1 = iAMT Mode Note: Once this bit is set, it cannot be disabled or cleared by writing a “0”. This bit can only be cleared by a power-on-reset.	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Configuration control for power down mode 0 = Upon assertion of PD#, the clock generator will initiate a full reset. Under this condition, the clock generator will emulate a cold power on reset internally and re-latch the FS input pins 1 = Legacy PD# input mode	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	PLL1 (CPU PLL) center spread enable 0 = down spread 1 = center spread	0
5	RW	LCDCLK & 27M_SS clock center spread enable 0 = down spread 1 = center spread	0
4	RW	Reserved	0
3:1	RW	LCD_CLK or 27M_SS spread spectrum magnitude control 000 = Reserved 001 = Reserved 010 = 0.5% 011 = 1.0% 100 = 1.5% 101 = 2.0% 110 = 2.5% 111 = Reserved	010
0	RW	Reserved	0

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	REF Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 2 (continued)

Bit	Type	Description/Function	Power up condition
6	RW	48MHz Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	PCIF_5 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	PCI_4 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	PCI_3 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	PCI_2 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PCI_1 Output Enabled 0 = Disabled 1 = Enabled	1
0	RW	PCI_0 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	SRC_11 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	SRC_10 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	SRC_9 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	SRC_8/CPU_ITP Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	SRC_7 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	SRC_6 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	Reserved	1
0	RW	SRC_4 Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	SRC_3 Output Enabled 0 = Disabled 1 = Enabled	1
6	RW	SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	LCDCLK Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	SRC_0/DOT_96 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	CPU_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PLL1 (CPU PLL) Spread Spectrum enable 0 = Disabled 1 = Enabled	1
0	RW	LCDCLK or 27M_SS Spread Spectrum enable 0 = Disabled 1 = Enabled	1

Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_A# enable 0 = Configure pin 8 as PCI_0 output 1 = Configure pin 8 as CLKREQ_A# input	0
6	RW	CLKREQ_A# mapping 0 = SRC_0 1 = SRC_2	0
5	RW	CLKREQ_B# enable 0 = Configure pin 10 as PCI_1 output 1 = Configure pin 10 as CLKREQ_B# input	0
4	RW	CLKREQ_B# mapping 0 = LCDCLK 1 = SRC_4	0
3	RW	CLKREQ_C# enable 0 = Configure pin 31 as SRC_3 output 1 = Configure pin 31 as CLKREQ_C# input Note: To configure this pin as CLKREQ_C# input, SRC_3 needs to be disabled by clearing Byte[4], bit[7] to “0” before setting this bit.	0
2	RW	CLKREQ_C# mapping 0 = SRC_0 1 = SRC_2	0

Control Register 5 (continued)

Bit	Type	Description/Function	Power up condition
1	RW	CLKREQ_D# enable 0 = Configure pin 32 as SRC_3# output 1 = Configure pin 32 as CLKREQ_D# input Note: To configure this pin as CLKREQ_D# input, SRC_3 needs to be disabled by clearing Byte[4], bit[7] to “0” before setting this bit.	0
0	RW	CLKREQ_D# mapping 0 = LCDCLK 1 = SRC_4	0

Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	CLKREQ_E# enable 0 = Configure pin 50 as SRC_7# output 1 = Configure pin 50 as CLKREQ_E# input to control SRC_6 output Note: To configure this pin as CLKREQ_E# input, SRC_7 needs to be disabled by clearing Byte[3], bit[3] to “0” before setting this bit.	0
6	RW	CLKREQ_F# enable 0 = Configure pin 51 as SRC_7 output 1 = Configure pin 51 as CLKREQ_F# input to control SRC_8 output Note: To configure this pin as CLKREQ_F# input, SRC_7 needs to be disabled by clearing Byte[3], bit[3] to “0” before setting this bit.	0
5	RW	CLKREQ_G# enable 0 = Configure pin 39 as SRC_11# output 1 = Configure pin 39 as CLKREQ_G# input to control SRC_9 output Note: To configure this pin as CLKREQ_G# input, SRC_11 needs to be disabled by clearing Byte[3], bit[7] to “0” before setting this bit.	0
4	RW	CLKREQ_H# enable 0 = Configure pin 40 as SRC_11 output 1 = Configure pin 40 as CLKREQ_H# input to control SRC_10 output Note: To configure this pin as CLKREQ_H# input, SRC_11 needs to be disabled by clearing Byte[3], bit[7] to “0” before setting this bit.	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	PCI_STOP# control for LCD_CLK output 0 = Free-running 1 = LCD_CLK clock are stopped when PCI_STOP# is active	0
0	RW	PCI_STOP# control for SRC outputs 0 = Free-running 1 = SRC clock are stopped when PCI_STOP# is active	0

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0

Control Register 7 (continued)

Bit	Type	Description/Function	Power up condition
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7:4	R	Reserved	0001
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	27M output enable 0 = Disabled 1 = Enabled	1
0	RW	27M_SS output enable 0 = Disabled 1 = Enabled	1

Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	PCI_STOP# control for PCIF_5 0 = Free-running 1 = PCIF_5 is stopped when PCI_STOP# is active	0
6	R	Reserved	X
5	RW	REF output drive strength control 0 = 1x (2 loads) 1 = 2x (3 loads)	1
4	RW	REF or Tristate Select for Test Mode 0 = Tristate 1 = REF	0
3	RW	Test Clock Mode Entry Control 0 = Normal operation 1 = REF or Tristate mode	0
2:0	RW	IO_VOUT control 000 = 0.3V 001 = 0.4V 010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V 110 = 0.9V 111 = 1.0V	101

Control Register 10

Bit	Type	Description/Function	Power up condition
7	R	SEL_LCDCLK# input status	X
6:2	RW	Reserved	00000
1	RW	Allow control of CPU_1_AMT with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1
0	RW	Allow control of CPU_0 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1

Control Register 11

Bit	Type	Description/Function	Power up condition
7:1	RW	Reserved	0000000
0	RW	Vendor Manufacturing/Production Test Mode. Please write with “1”	1

Control Register 12

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	00
5:0	RW	Byte count register for block read operation Note: The default value is 13. To read more than 13 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	001101

Control Register 13 (Manufacturing Test Control)

Bit	Type	Description/Function	Power up condition
7:2	RW	Reserved	00000
1:0	RW	Reserved	00

Control Register 14 (Reserved)

Bit	Type	Description/Function	Power up condition
7	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	0
6:0	RW	Reserved	XXXXXX

Control Register 15 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Control Register 16 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Control Register 17

Bit	Type	Description/Function	Power up condition
7:6	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	00
5:3	RW	Reserved	000
2	RW	LCDCLK output frequency selection 0 = 100MHz 1 = 96MHz	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 18 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	0000110

Control Register 19

Bit	Type	Description/Function	Power up condition
7:3	RW	Reserved	00000
2:1	RW	Reserved	00
0	RW	Reserved	0

Control Register 20

Bit	Type	Description/Function	Power up condition
7	RW	48MHz clock drive strength control 0 = Normal 1 = High	0
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	PCIF_5 output drive strength 0 = Normal 1 = High	0
3	RW	Reserved	1
2	RW	PCI_3:4 output drive strength 0 = Normal 1 = High	0
1	RW	Reserved	1
0	RW	PCI_0:2 output drive strength 0 = Normal 1 = High	0

Control Register 21

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	0000000
0	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	0

Control Register 22 to 28 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Crystal Recommendations

The SLG8SP513 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG8SP513 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 6. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Max VDD Supply Voltage (VDD_3.3):.....4.6V

Max VDD_I/O Supply Voltage (VDD_I/O):.....4.6V

Max Input Voltage (Vih):.....4.6V

Min Input Voltage (Vil):.....-0.5V

Storage Temperature::..... –65°C to + 150°C

Operating Temperature (Ambient, no airflow): . 0°C to +70°C

ESD Protection (Min):..... 2000V

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDD_3.3	3.3V Supply Voltage	±5%	3.135		3.465	V
Vih	Input High Voltage (SE)		2.0		VDD+0.3	V
Vil	Input Low Voltage (SE)		VSS-0.3		0.8	V
Vih_FS_Test	Input High Voltage (SE)		2.0		VDD+0.3	V
Vih_FS_Normal	Input High Voltage (FS)		0.7		1.5	V
Vil_FS_Normal	Input Low Voltage (FS)		VSS-0.3		0.35	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Voh	Output High Voltage (SE)	Ioh = -1mA	2.4			V
Vol	Output Low Voltage (SE)	Iol = 1mA			0.4	V
VDD_I/O	Low Voltage Differential I/O Supply Voltage		1.050		3.465	V
Cin	Input Pin Capacitance		1.5		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_3.3V	Operating Supply Current, default configuration				250	mA
Idd_IO_0.8V	Differential I/O current, all output enabled		25		80	mA
Idd_PD_3.3V	Powerdown Supply Current, 3.3V				1.0	mA
Idd_PD_0.8V	Powerdown Supply Current, 0.8V				0.1	mA
Idd_M1_3.3V	M1 Mode Supply Current, 3.3V				25	mA
Idd_M1_0.8V	M1 Mode Supply Current, 0.8V				8.0	mA

AC Electrical Characteristics

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccurracy	Long term accuracy		300	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC disabled)	7.497751	7.502251	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC disabled)	5.998201	6.001801	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC disabled)	4.998500	5.001500	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC disabled)	3.748875	3.751125	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC disabled)	2.999100	3.000900	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC disabled)	2.499250	2.500750	ns	Average period over 1 us
Tperiod	Average CPU Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.497751	7.539950	ns	Average period over 1 us
Tperiod	Average CPU Period (166MHz, SSC enabled)	5.998201	6.031960	ns	Average period over 1 us
Tperiod	Average CPU Period (200MHz, SSC enabled)	4.998500	5.026634	ns	Average period over 1 us
Tperiod	Average CPU Period (266MHz, SSC enabled)	3.748875	3.769975	ns	Average period over 1 us
Tperiod	Average CPU Period (333MHz, SSC enabled)	2.999100	3.015980	ns	Average period over 1 us
Tperiod	Average CPU Period (400MHz, SSC enabled)	2.499250	2.513317	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC disabled)	9.997001	10.003000	ns	Average period over 1 us
Tperiod	Average SRC Period (100MHz, SSC enabled)	9.997001	10.05327	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (100, SSC disabled)	9.912001	10.08800	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.412751	7.587251	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC disabled)	5.913201	6.086801	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC disabled)	4.913500	5.086500	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC disabled)	3.663875	3.836125	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC disabled)	2.914100	3.085900	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC disabled)	2.414250	2.585750	ns	
Tabs	Absolute Min/Max CPU Period (100, SSC enabled)	9.912001	10.13827	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.412751	7.624950	ns	
Tabs	Absolute Min/Max CPU Period (166, SSC enabled)	5.913201	6.116960	ns	
Tabs	Absolute Min/Max CPU Period (200, SSC enabled)	4.913500	5.111634	ns	
Tabs	Absolute Min/Max CPU Period (266, SSC enabled)	3.663875	3.854975	ns	
Tabs	Absolute Min/Max CPU Period (333, SSC enabled)	2.914100	3.100980	ns	
Tabs	Absolute Min/Max CPU Period (400, SSC enabled)	2.414250	2.598317	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC disabled)	9.872001	10.12800	ns	
Tabs	Absolute Min/Max SRC Period (100, SSC enabled)	9.872001	10.17827	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16354	10.66979	ns	

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Slew_rise	Rising slew rate[1]	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_fall	Falling slew rate[1]	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_var	Slew rate matching		20	%	1. Use 'average' acquisition mode of the scope 2. Measurement taken from single ended waveform 3. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculation
V_swing	Differential output swing	300		mV	Measurement taken from differential waveform
V_cr	Crossing point voltage	300	550	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. Only applies to the differential rising edge (i.e. Clock rising and Clock# falling)
V_cr_dlt	Variation of V_cr		140	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. V_cross delta is defined as the total variation of all crossing voltages of rising Clock and falling Clock#
Tccjitter	Cycle to Cycle Jitter (CPU)		85	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew (CPU_0 & CPU_1)		100	ps	
Tskew	Pin-to-Pin Skew (CPU_2)		150	ps	
Tskew	Pin-to-Pin Skew (all SRC outputs)		3	ns	

Note: [1] May require programming IOVOUT when VDD_IO = 1.05V and certain loading conditions.

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 33.333333MHz
Tperiod	Average Period (SSC disabled)	29.99100	30.00900	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tperiod	Average Period (SSC enabled, -0.5%)	29.99100	30.15980	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period (SSC disabled)	29.49100	30.50900	ns	
Tabs	Absolute Min/Max Period (SSC enabled, -0.5%)	29.49100	30.65980	ns	
Thigh	CLK high time	12	N/A	ns	
Tlow	CLK low time	12	N/A	ns	

PCI Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		500	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V
Tskew	Pin-to-Pin Skew		1000	ps	

USB_48 Timing Characteristics

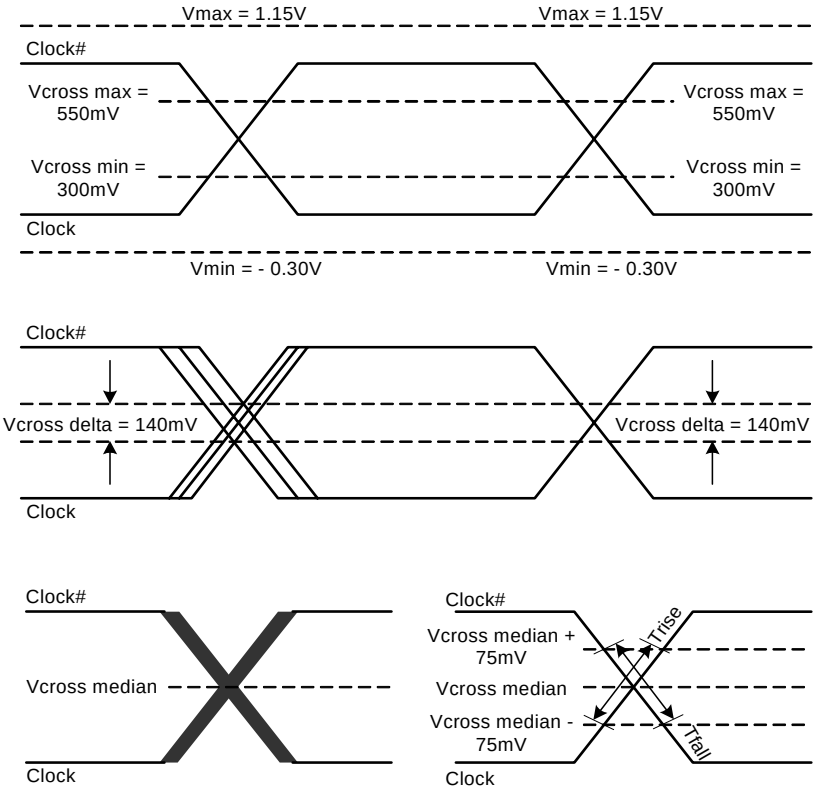
Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 48.000000MHz
Tperiod	Average Period	20.83125	20.83542	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	20.48125	21.18542	ns	
Thigh	CLK high time	8.094	10.036	ns	
Tlow	CLK low time	7.694	9.836	ns	
Edge Rate	Rising edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	2.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		350	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

REF Timing Characteristics

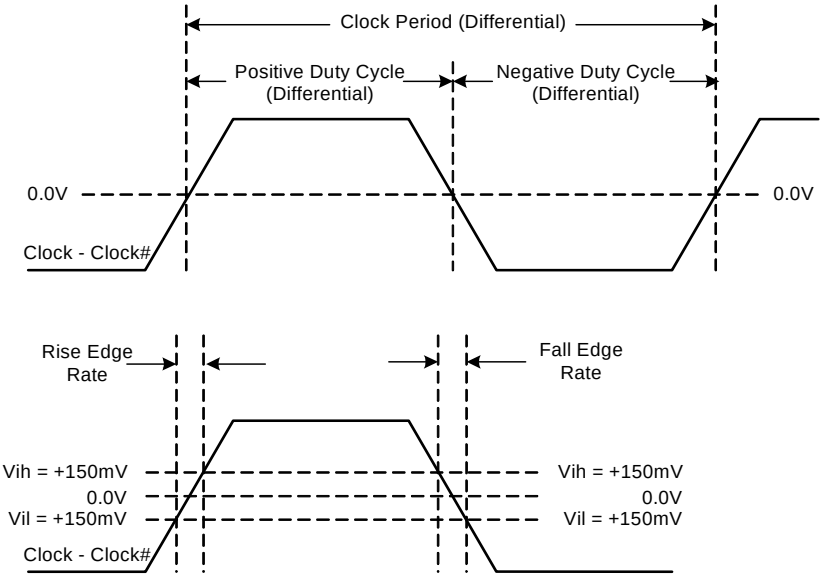
Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 14.318180MHz
Tperiod	Average Period	69.82033	69.86224	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	68.82033	70.86224	ns	
Thigh	CLK high time	TBD	TBD	ns	
Tlow	CLK low time	TBD	TBD	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

Measurement Points for Differential Clocks

Single ended (SE) measurement waveforms



Differential (DIFF) measurement waveforms

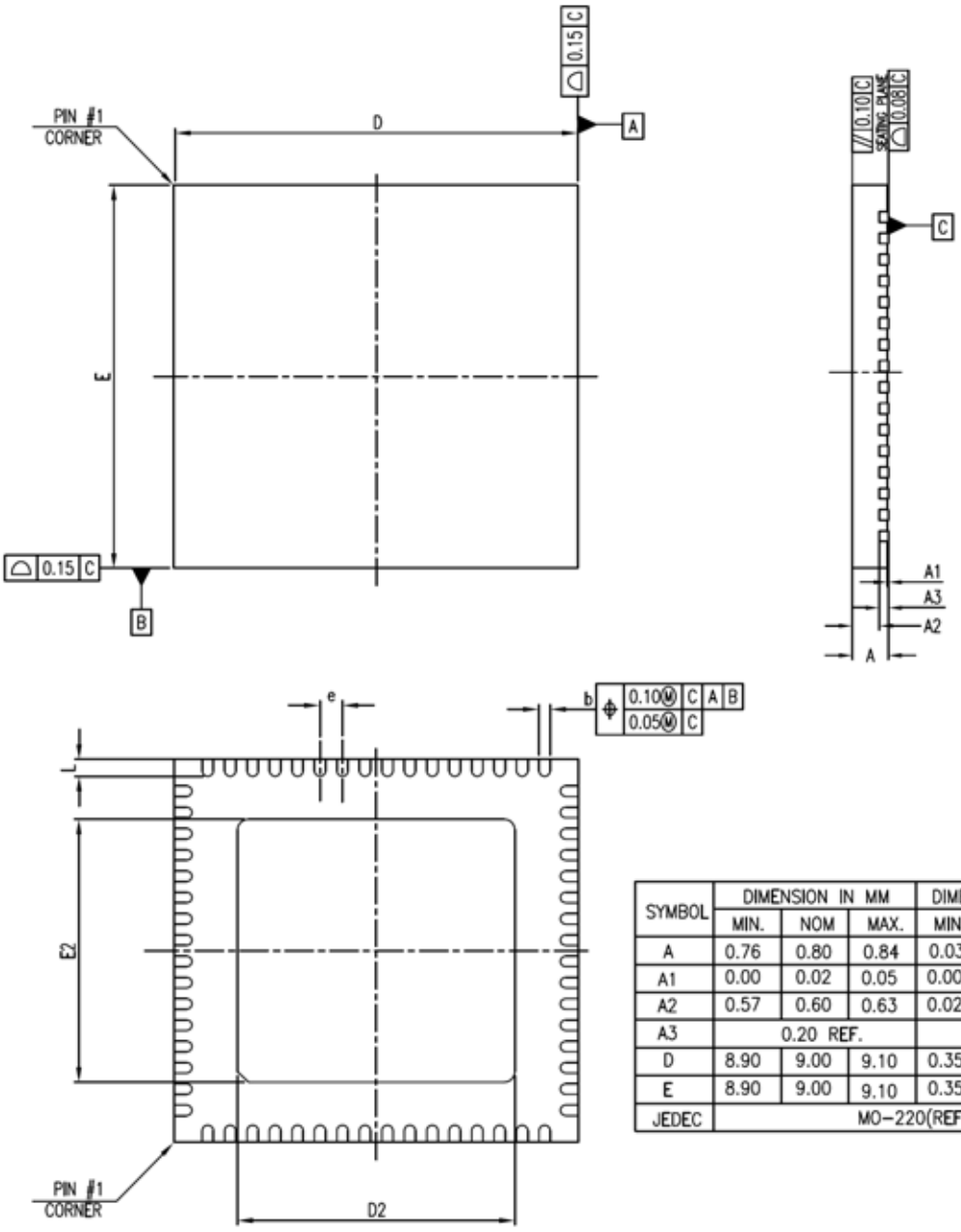


Ordering Information

Part Number	Package Type	Temperature Range
SLG8SP513V	64 Lead Green Package QFN	Commercial, 0° to 70°C
SLG8SP513VTR	64 Lead Green Package QFN - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

64 Lead QFN Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.05	0.000	0.0008	0.0020
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
JEDEC	MO-220(REF.)					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
64L	0.20	0.25	0.30	6.13	6.18	6.23	6.13	6.18	6.23	0.500 BSC	0.35	0.40	0.45	MO-220WMMD