



# Product Specification

AU OPTRONICS CORPORATION

(✓) Preliminary Specifications

( ) Final Specifications

<b>Module</b>	<b>17.3" (17.26) HD+ 16:9 Color TFT-LCD with LED Backlight design</b>
<b>Model Name</b>	B173RTN 01.1 (H/W:0A)
<b>Note</b> (  )	<b>LED Backlight with driving circuit design, eDP 1.1</b>

<b>Customer</b>	<b>Date</b>
<b>Checked &amp; Approved by</b>	<b>Date</b>
_____	_____
<p>Note: This Specification is subject to change without notice.</p>	

<b>Approved by</b>	<b>Date</b>
<u>Trista</u>	2012/7/31
<b>Prepared by</b>	<b>Date</b>
<u>Donald</u>	2012/07/31
<p><b>NBBU Marketing Division / AU Optronics corporation</b></p>	

## 2. General Description

B173RTN01.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD+ (1600(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP (display port) interface compatible.

B173RTN01.1 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

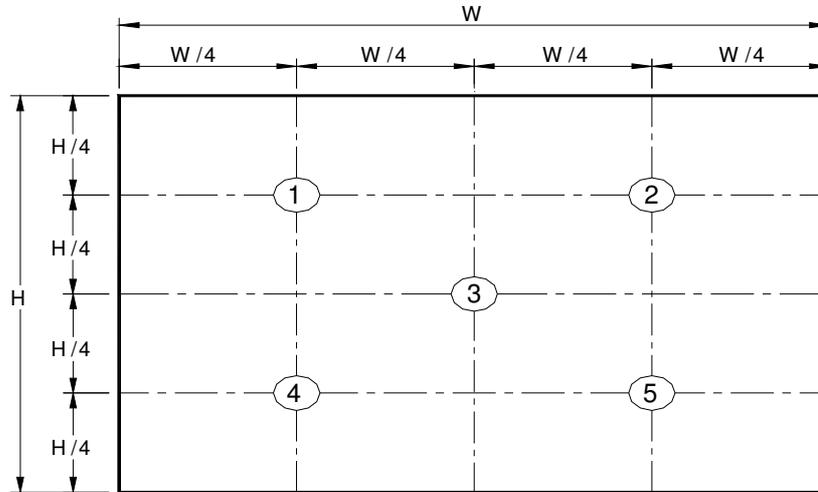
Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3"(17.26)			
Active Area	[mm]	382.08 X 214.92			
Pixels H x V		1600x3(RGB) x 900			
Pixel Pitch	[mm]	0.2388X0.2388			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance ( <b>I<sub>LED</sub>=20mA</b> ) <b>(Note: I<sub>LED</sub> is LED current)</b>	[cd/m <sup>2</sup> ]	220 typ. (5 points average) 187 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500:1 typ			
Response Time	[ms]	8 typ/16max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	TBD			
Weight	[Grams]	570 max.			
Physical Size <b>Without inverter, bracket.</b>	[mm]		Min.	Typ.	Max.
		Length	397.6	398.1	398.6
		Width	232.3	232.8	233.3
		Thickness	-	-	5.8
Electrical Interface		1 channel Display Port			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare			
Support Color		262K colors ( RGB 6-bit )			
Temperature Range	Operating	[°C]	0 to +50		
	Storage (Non-Operating)	[°C]	-20 to +60		
RoHS Compliance		RoHS Compliance			

## 2.2 Optical Characteristics

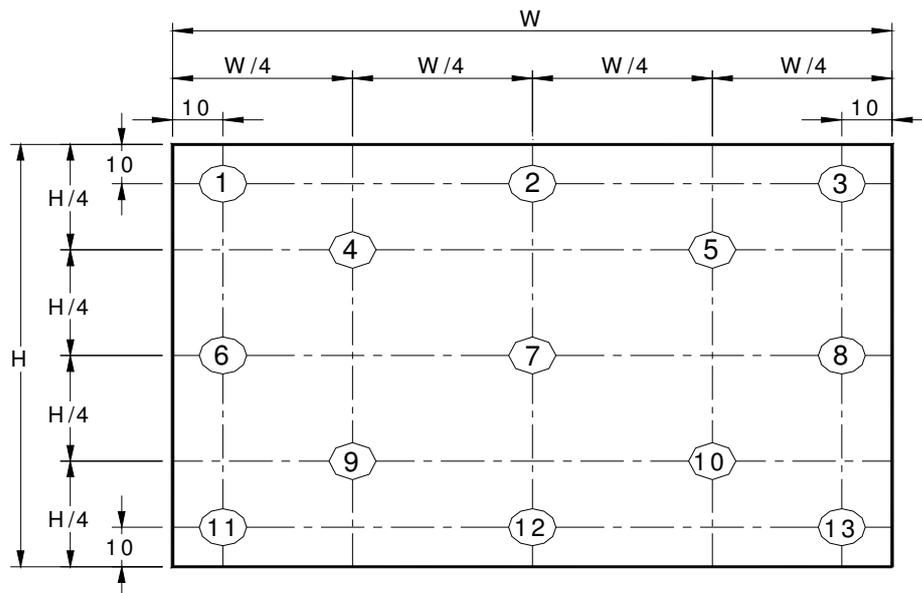
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note		
White Luminance ILED=20mA		5 points average	187	220	-	cd/m <sup>2</sup>	1, 4, 5.		
Viewing Angle	$\theta_R$	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9		
	$\theta_L$		40	45	-				
	$\psi_H$	Vertical (Upper) CR = 10 (Lower)	10	15	-				
	$\psi_L$		30	35	-				
Luminance Uniformity	$\delta_{5P}$	5 Points	-	-	1.25		1, 3, 4		
Luminance Uniformity	$\delta_{13P}$	13 Points	-	-	1.6		2, 3, 4		
Contrast Ratio	CR		300	400	-		4, 6		
Cross talk	%				4		4, 7		
Response Time	$T_{RT}$	Rising + Falling	-	8	16				
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.585	0.615	0.645	4		
		Ry		0.317	0.347	0.377			
	Green	Gx		0.288	0.318	0.348			
		Gy		0.579	0.609	0.639			
	Blue	Bx		0.120	0.150	0.180			
		By		0.084	0.114	0.144			
	White	Wx		0.283	0.313	0.343			
		Wy		0.299	0.329	0.359			
	NTSC	%			-	60		-	

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

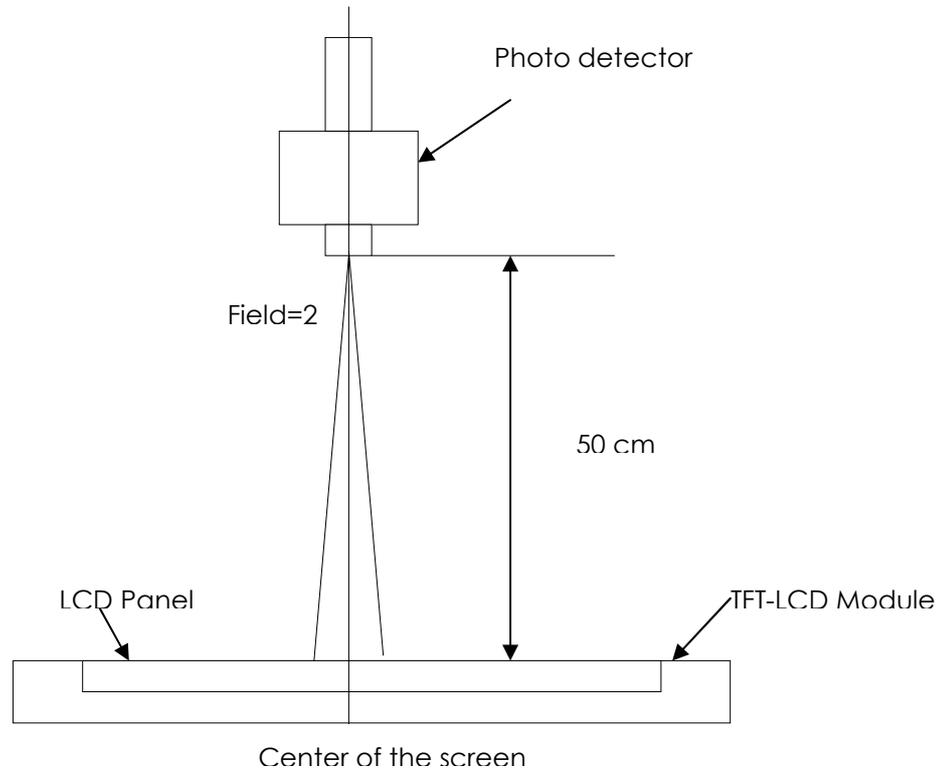
$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should

be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ·  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

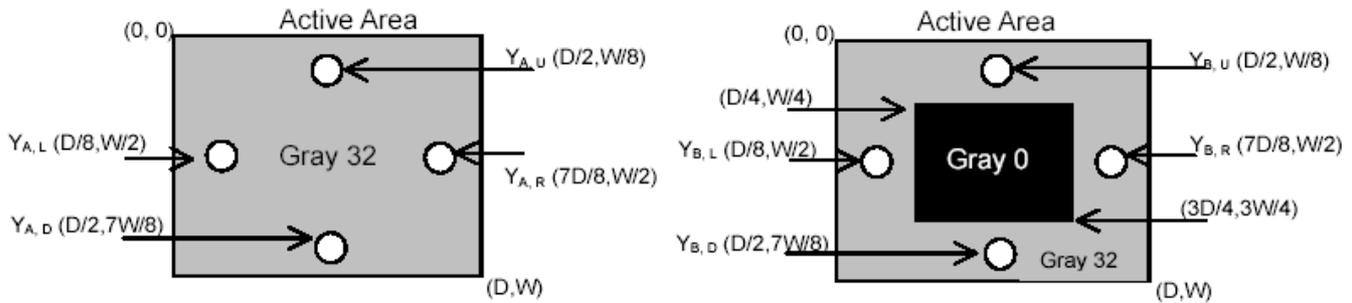
**Note 7 :** Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

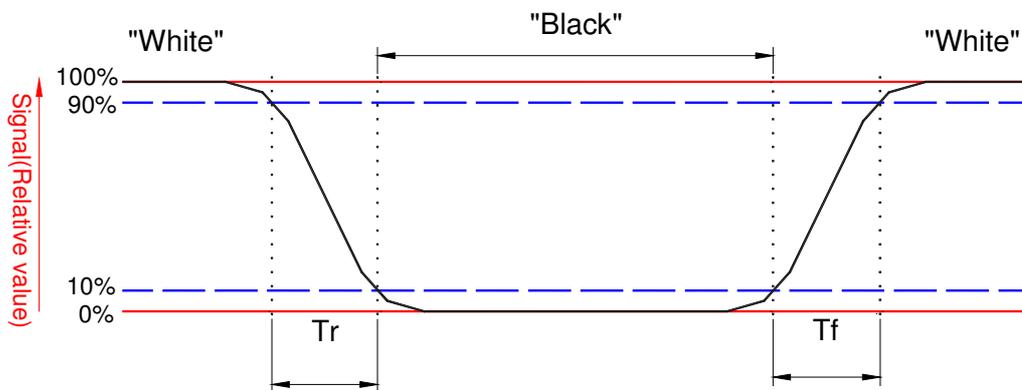
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



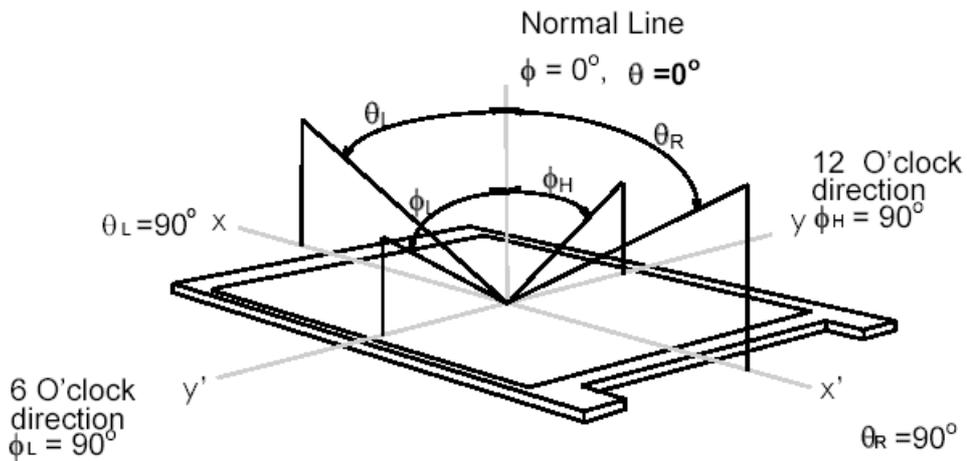
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



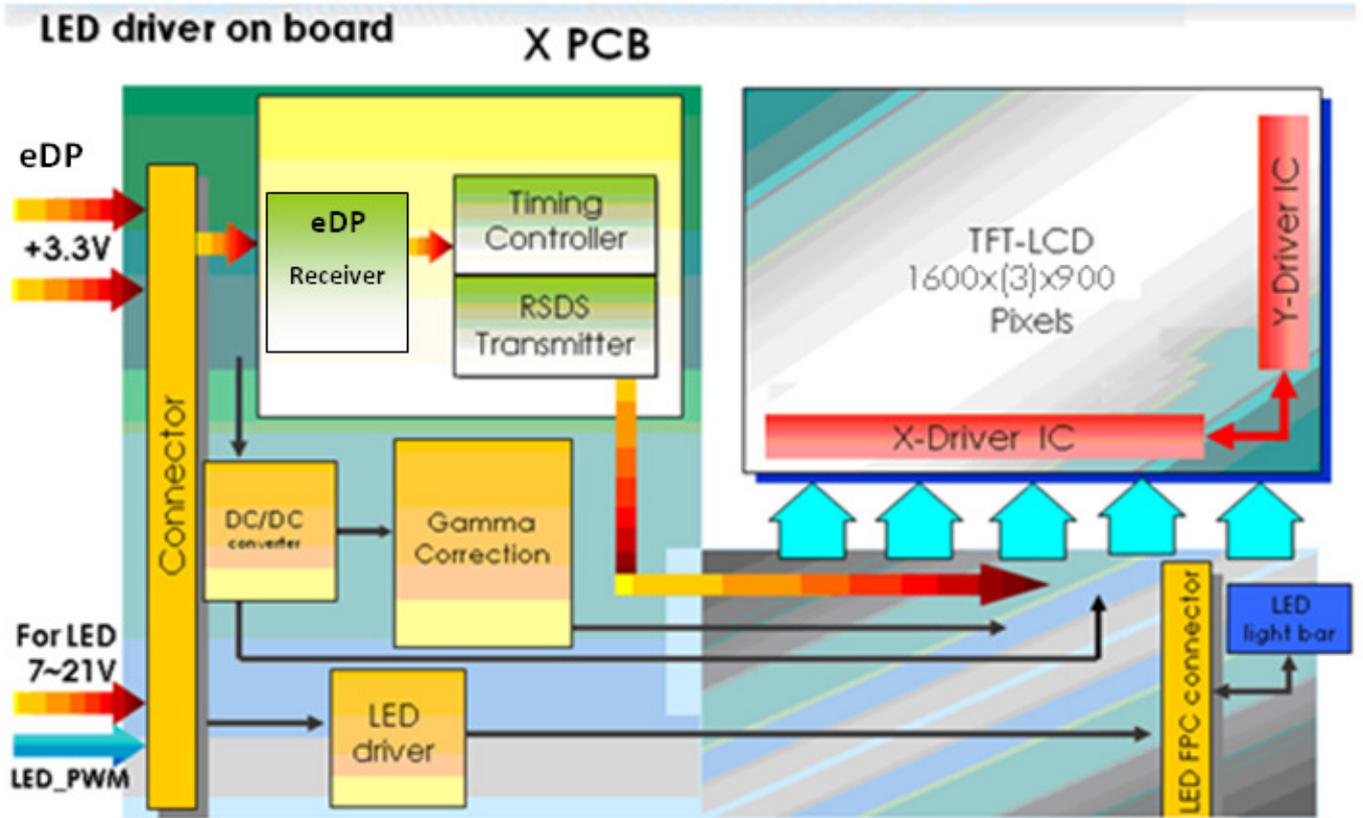
**Note 9.** Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 30 Pin.



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

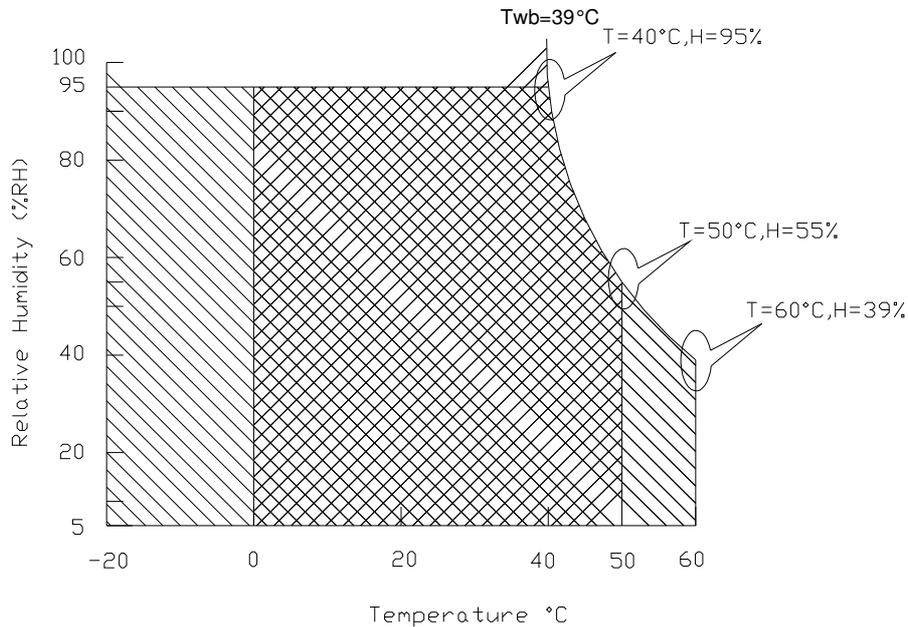
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

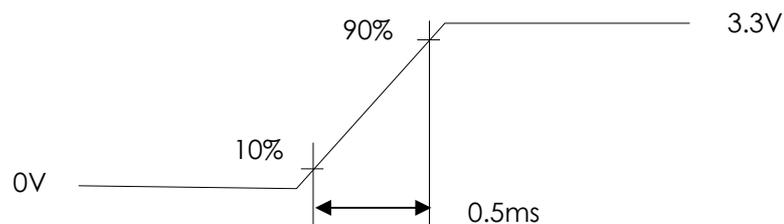
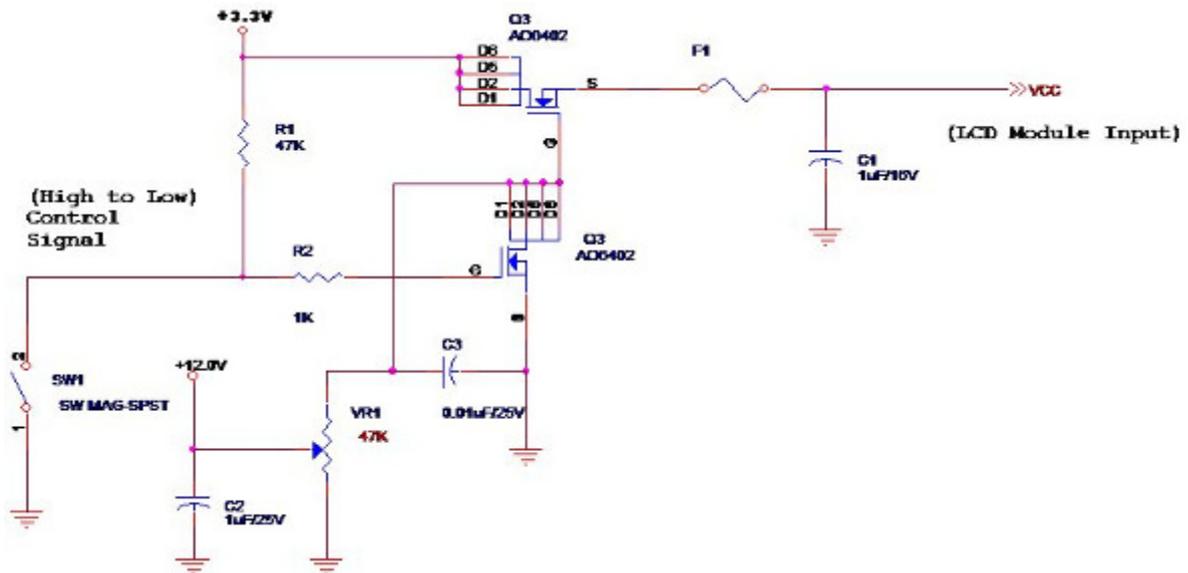
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	TBD	[Watt]	Note 1/2
IDD	IDD Current	-	TBD	TBD	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



Vin rising time

## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

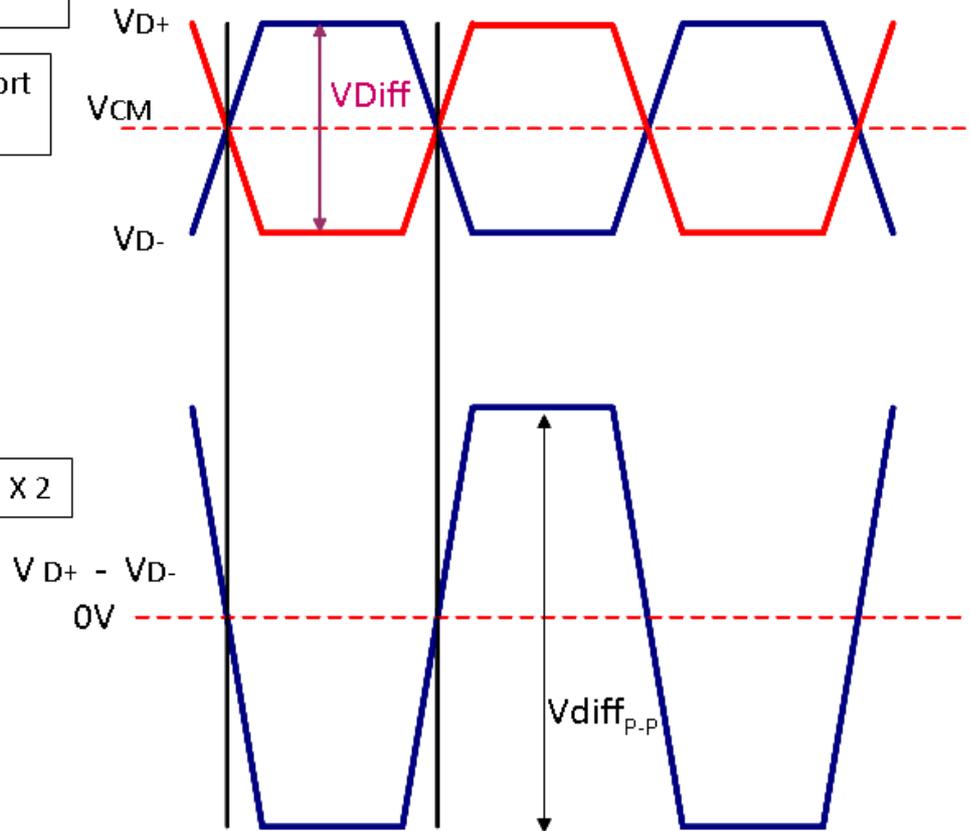
Signal electrical characteristics are as follows;

### Display Port main link signal:

Differential pair VD+ , VD-  
Which is one Display port  
Main link

VCM of Display port  
Main link

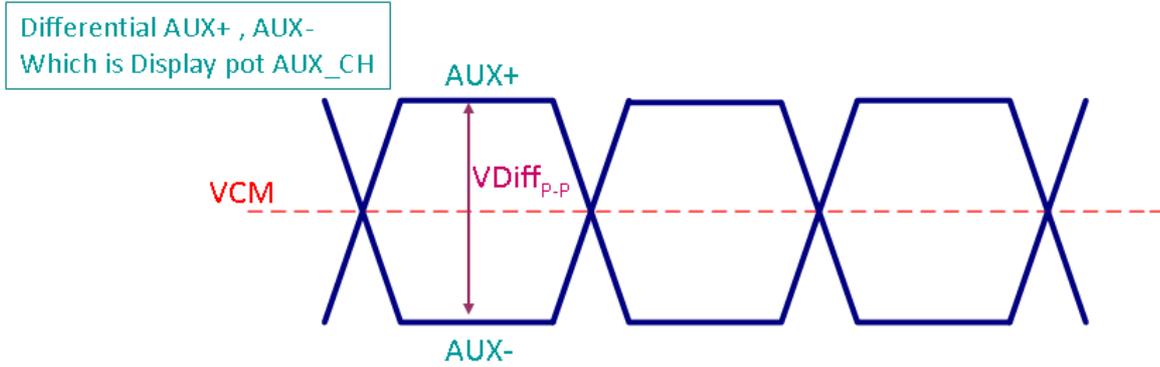
$$V_{diff_{P-P}} = [(VD+) - (VD-)] \times 2$$



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff <sub>p-p</sub>	Peak-to-peak Voltage at a receiving Device	120		1320	mV

Fallow as VESA display port standard V1.1a.

## Display Port AUX\_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>p-p</sub>	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

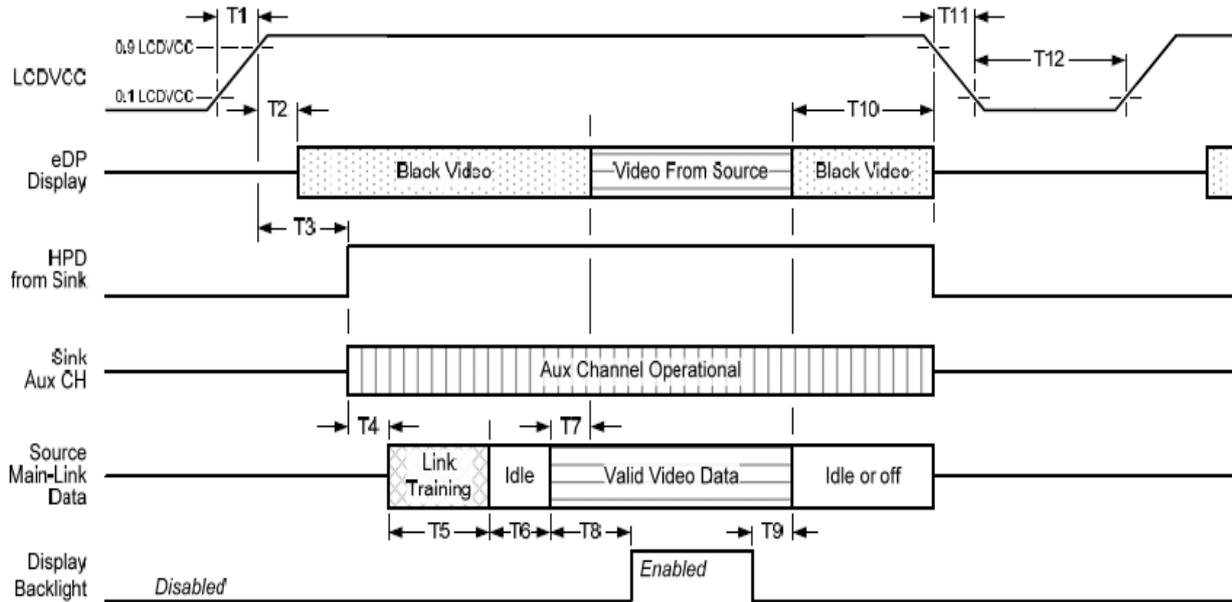
Fallow as VESA display port standard V1.1a.

## Display Port VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD voltage	2.25		3.6	V

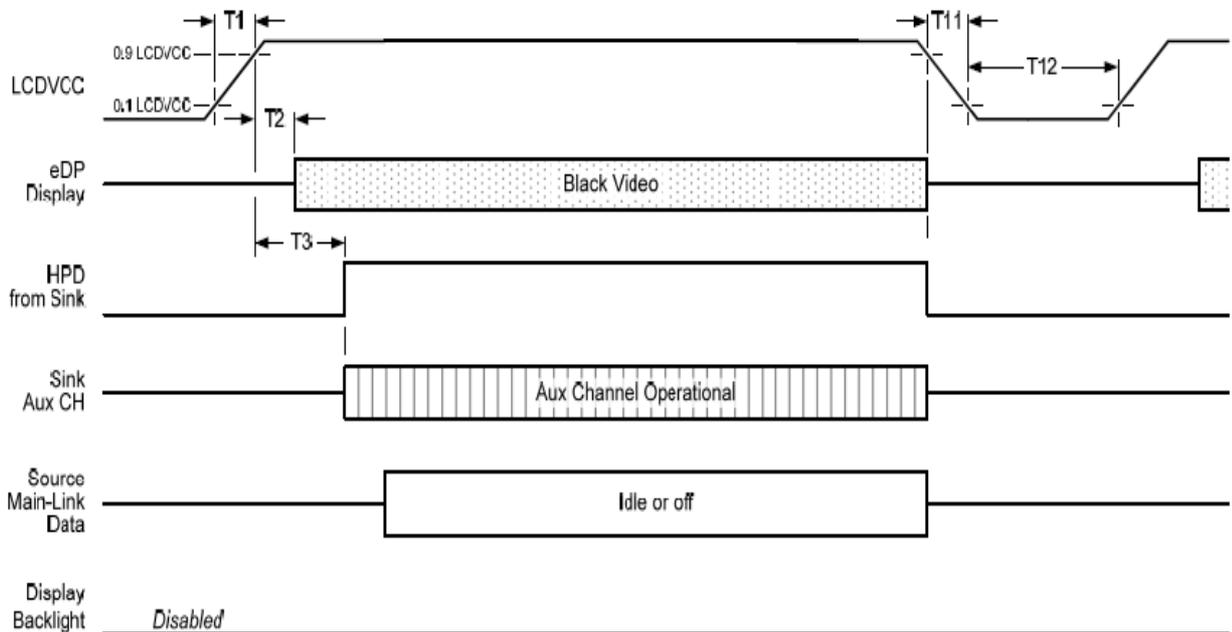
Fallow as VESA display port standard V1.1a.

## Display Port panel power sequence:



## Display port interface power up/down sequence, normal system operation

## Display Port AUX\_CH transaction only:



## Display port interface power up/down sequence, AUX\_CH transaction only



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## Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

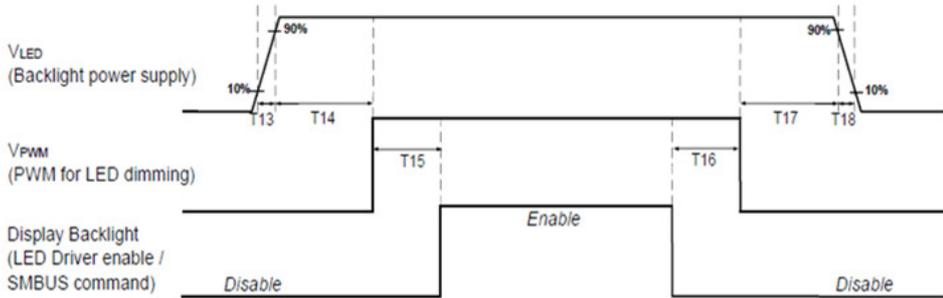
-upon LCDVDD power on (with in T2 max)-when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

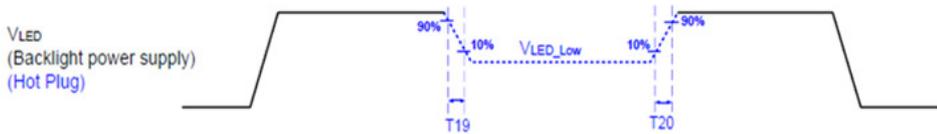
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.

## Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change:  $T19/T20 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/PWM \text{ Frequency}$

## 5.2 Backlight Unit

### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	4.8	5.0	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = VF$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

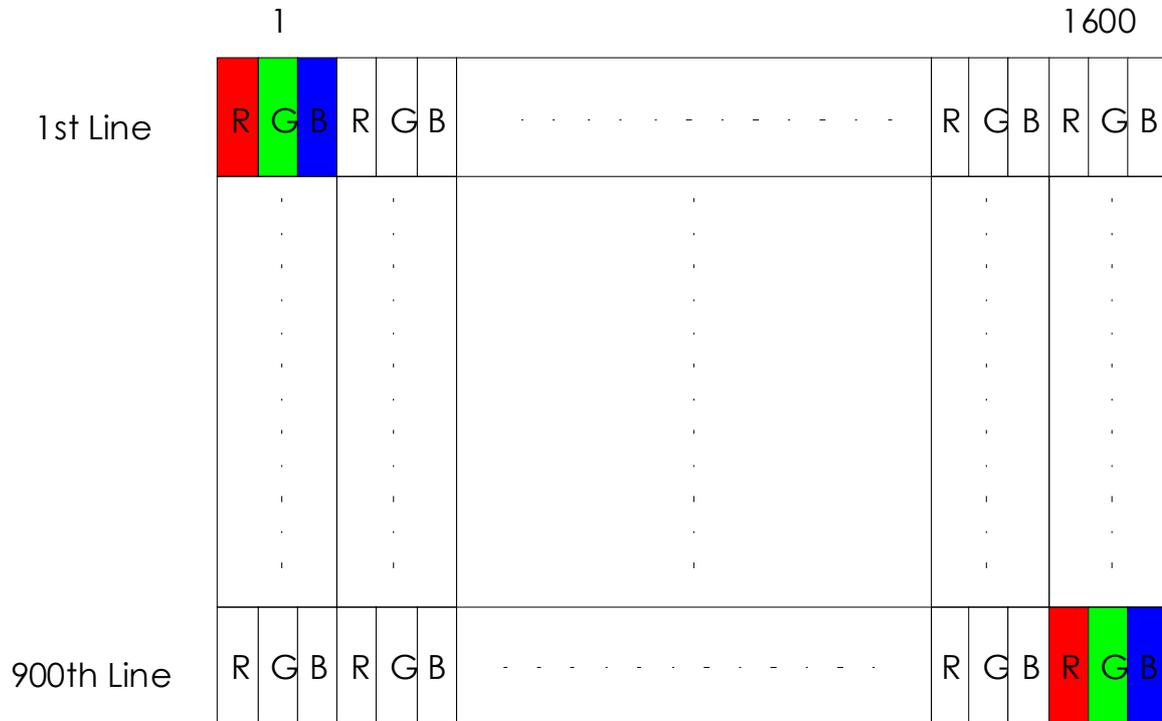
### 5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7	--	21	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	3	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	3	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	1K	20k	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

## 6. Signal Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





## 6.2 Integration Interface and Pin Assignment

### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

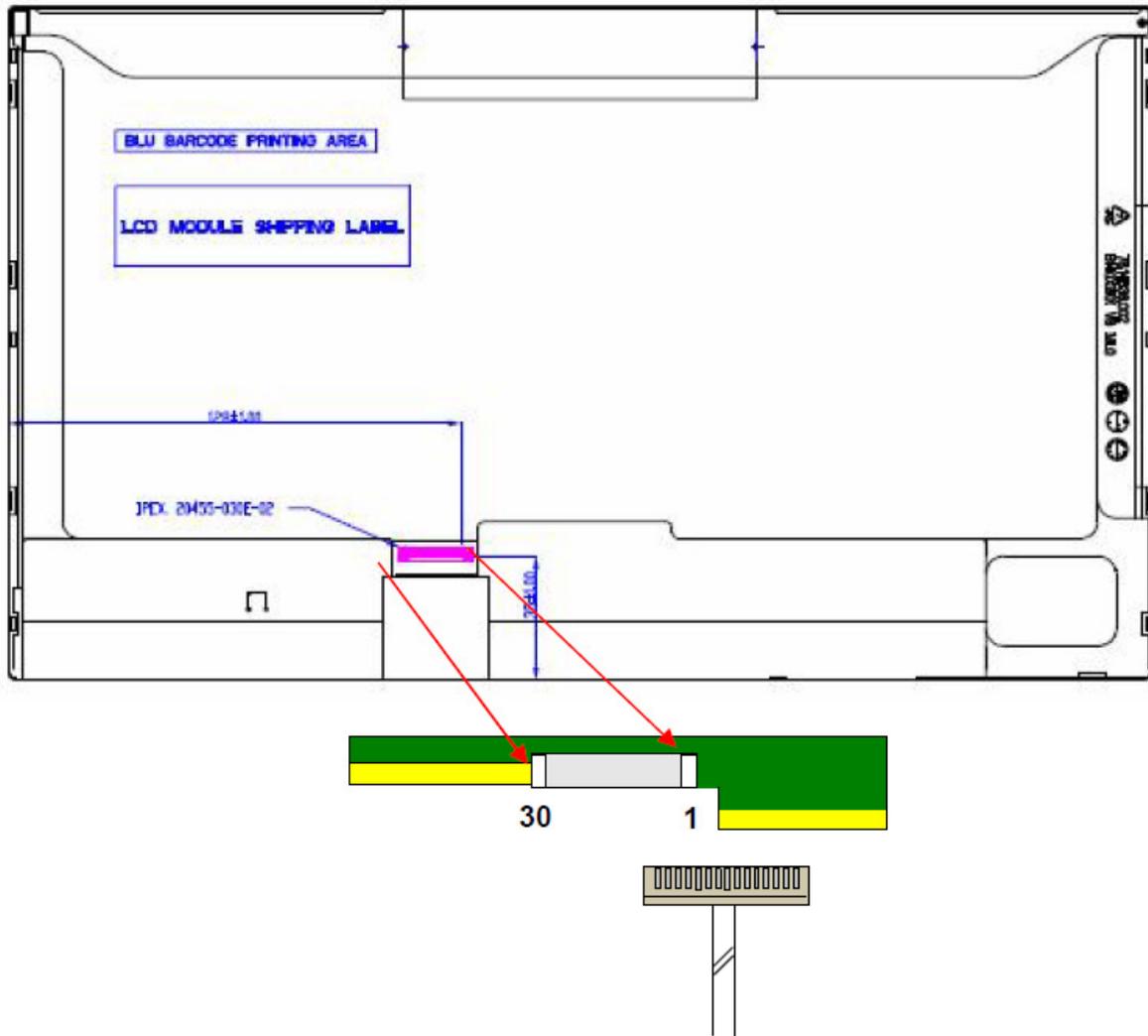
<b>Connector Name / Designation</b>	<b>For Signal Connector</b>
Manufacturer	IPEX or compatible
Type / Part Number	I-PEX 20455-030E-12 or compatible
Mating Housing/Part Number	I-PEX 20453-030T-11 or compatible



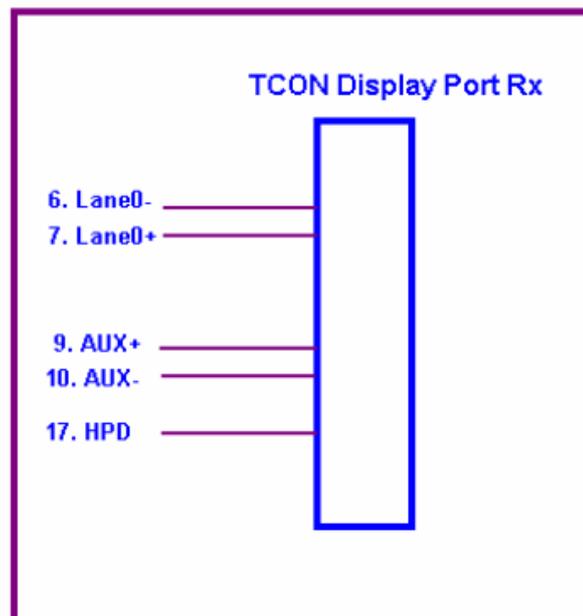
## 6.2.2 Pin Assignment

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	NC	
4	NC	
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	Reverse for AUO TEST only
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect

Note1: Start from right side



Note2: Input signals shall be low or High-impedance state when VDD is off.  
internal circuit of eDP inputs are as following.



## 6.3 Interface Timing

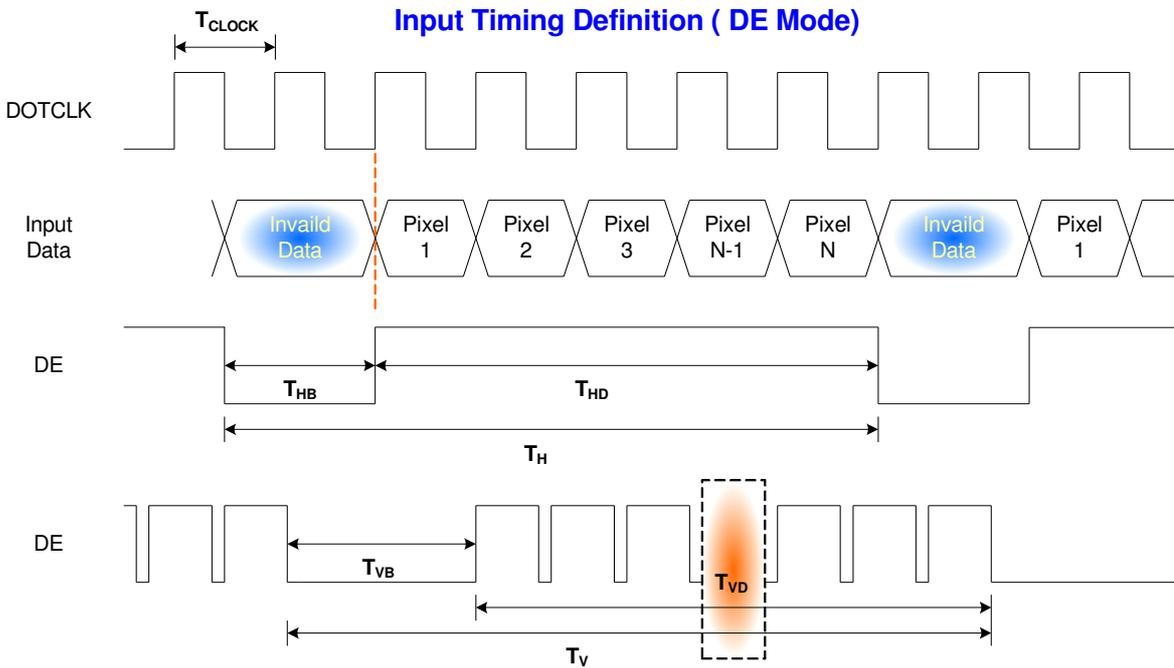
### 6.3.1 Timing Characteristics

Basically, interface timings should match the 1600x900 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-		60	-	Hz	
Clock frequency	$1/T_{\text{Clock}}$		100		MHz	
Vertical Section	Period	$T_V$	908	926	1100	$T_{\text{Line}}$
	Active	$T_{VD}$	900			
	Blanking	$T_{VB}$	8	26	200	
Horizontal Section	Period	$T_H$	1778	1798	1968	$T_{\text{Clock}}$
	Active	$T_{HD}$	1600			
	Blanking	$T_{HB}$	178	198	368	

Note : DE mode only

## 6.4 Timing diagram





## 7. Vibration and Shock Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test Spec:

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 35%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 300h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

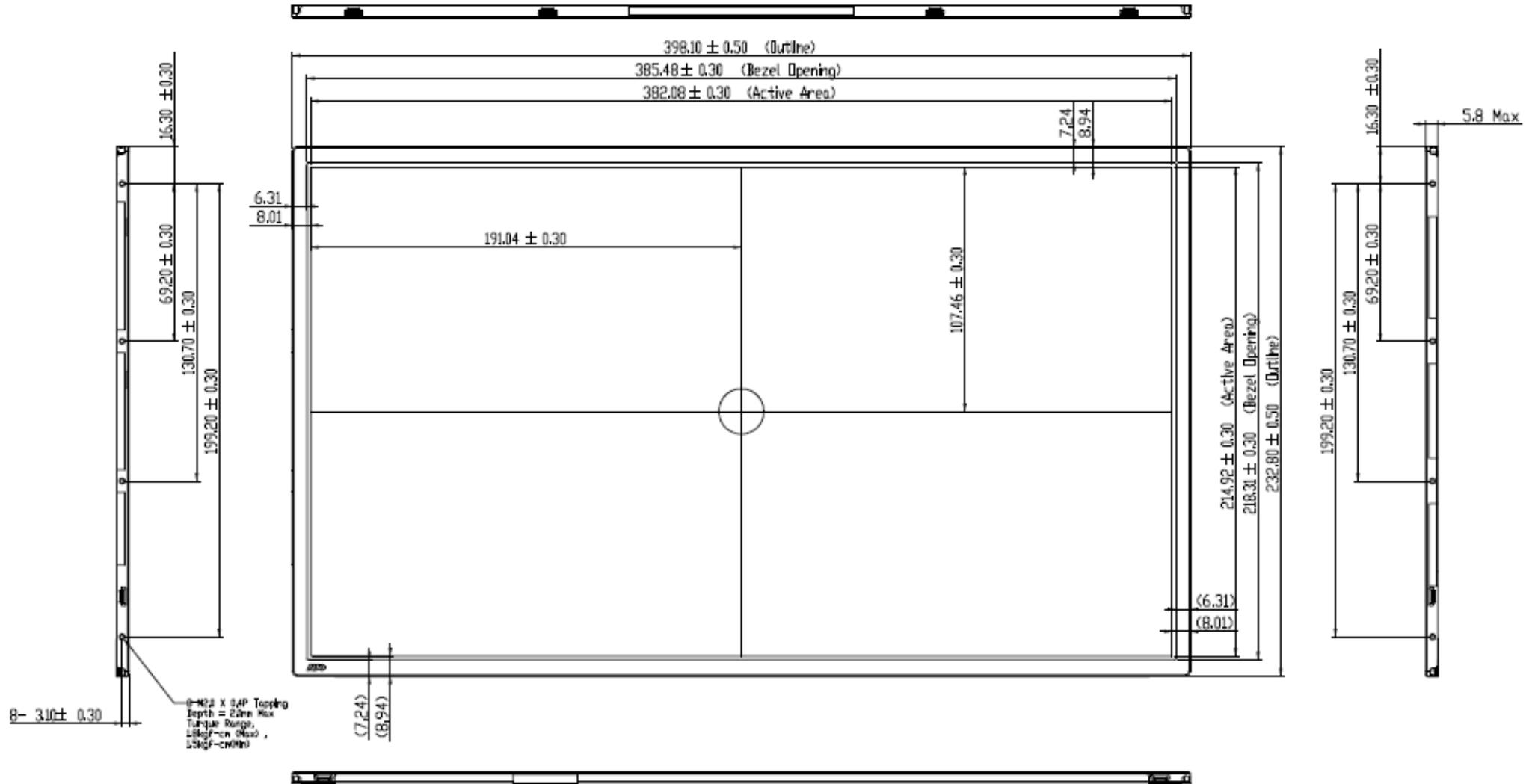


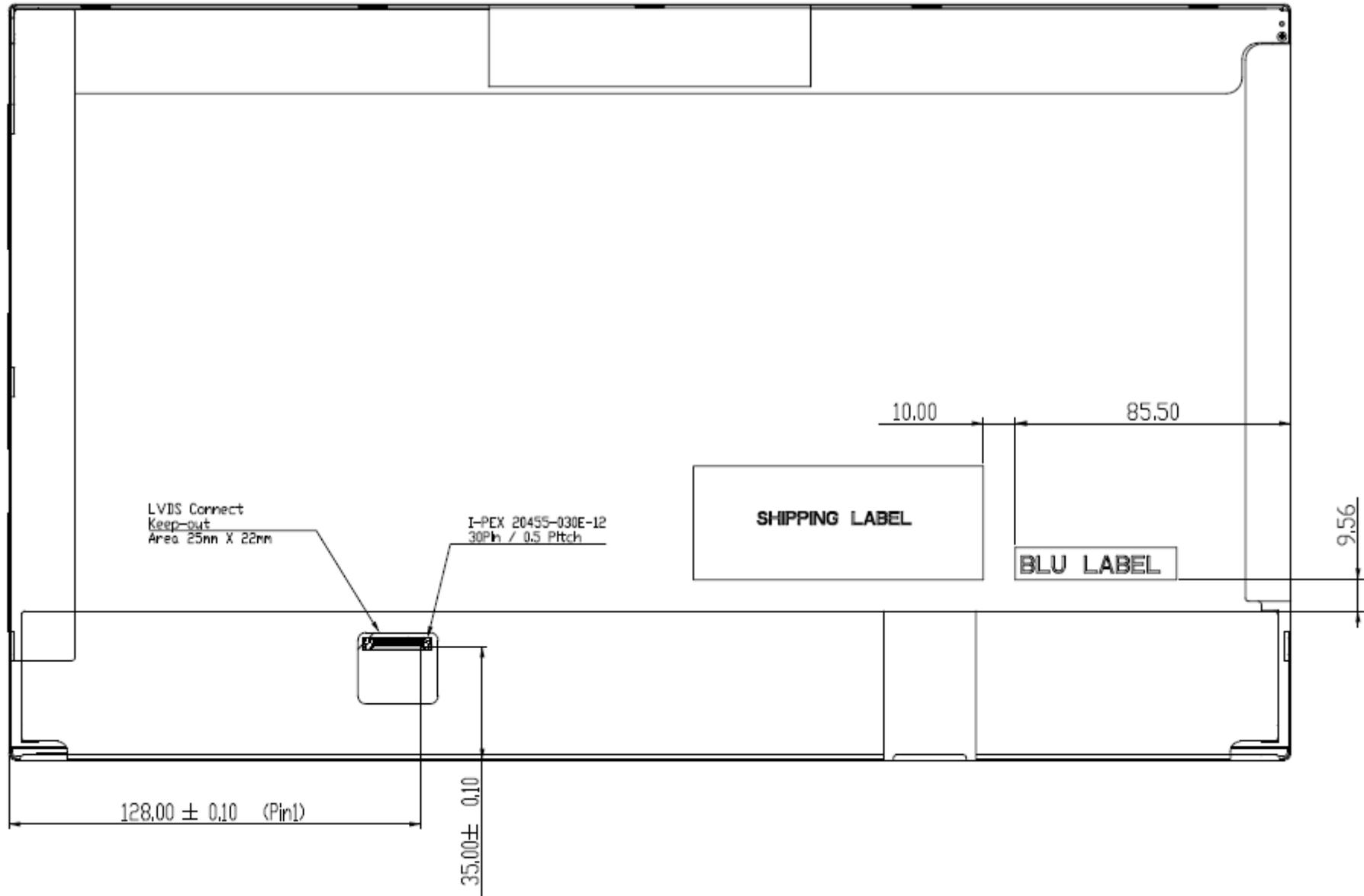
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## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension





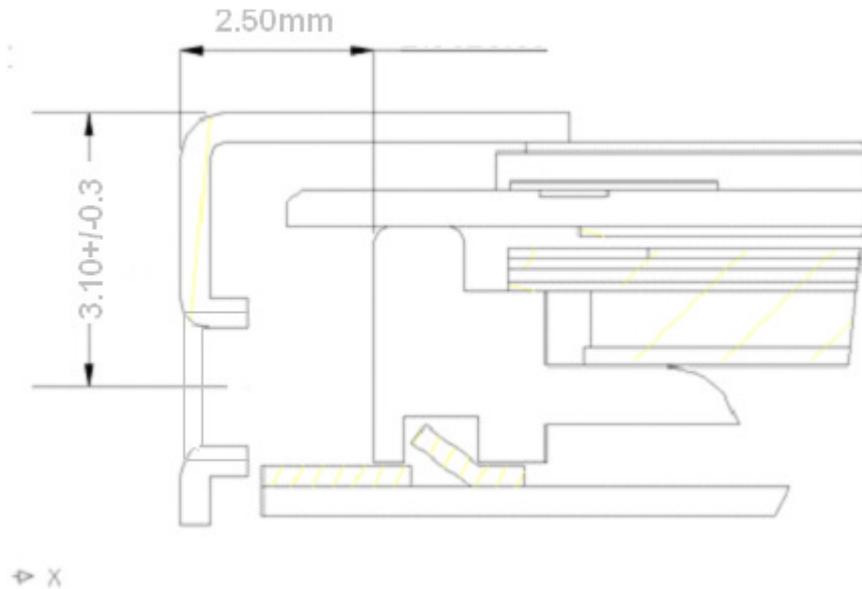
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

## 8.2 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is 2.5mm (See drawing)

Screw hole center location, from front surface =  $3.10 \pm 0.3\text{mm}$  (See drawing)

Screw Torque: Maximum 2.5 kgf-cm

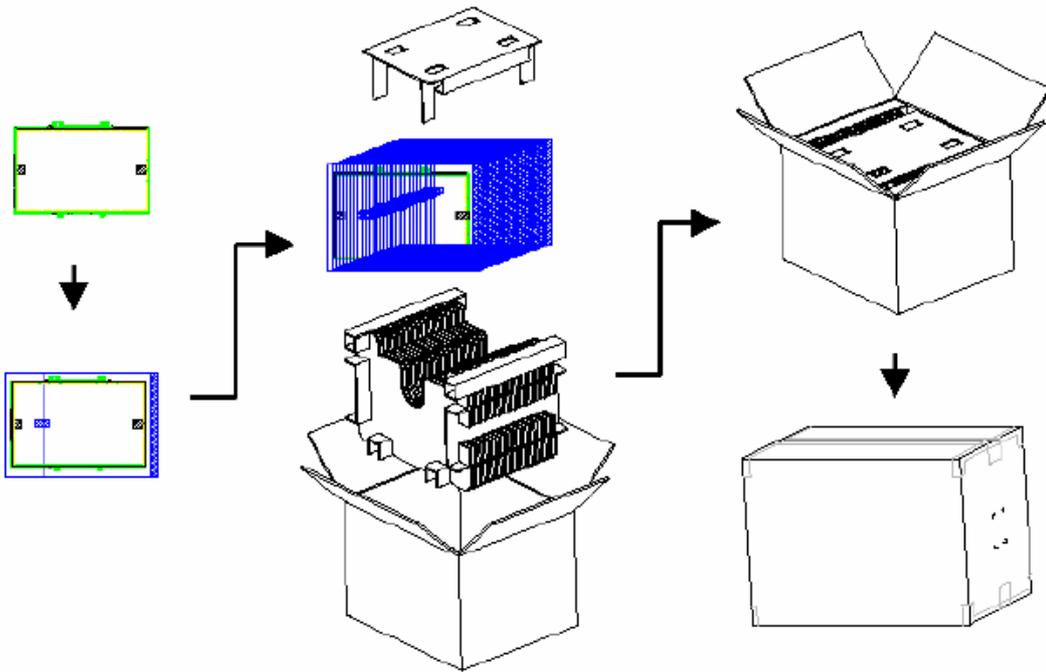


## 9. Shipping and Package

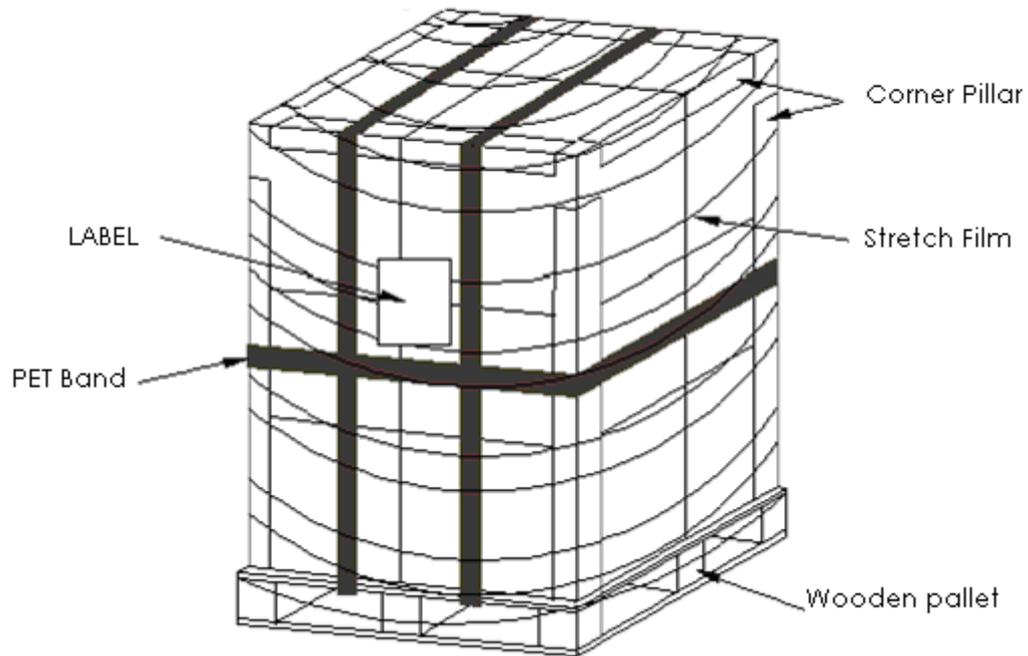
### 9.1 Shipping Label Format



### 9.2. Carton package



## 9.3 Shipping package of palletizing sequence





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## 10. Appendix: EDID description

### B173RTN01 1 EDID Code

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	9E	10011110	158
0B	hex, LSB first	11	00010001	17
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	2B	00101011	43
11	Year of manufacture	15	00010101	21
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	<b>Video input def.</b> ( <i>digital I/P, non-TMDS, CRGB</i> )	90	10010000	144
15	<b>Max H image size</b> ( <i>rounded to cm</i> )	26	00100110	38
16	<b>Max V image size</b> ( <i>rounded to cm</i> )	15	00010101	21
17	<b>Display Gamma</b> ( <i>=(gamma*100)-100</i> )	78	01111000	120
18	<b>Feature support</b> ( <i>no DPMS, Active OFF, RGB, tmg Blk#1</i> )	02	00000010	2
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	EE	11101110	238
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	85	10000101	133
1B	Red x ( <b>Upper 8 bits</b> )	9E	10011110	158
1C	Red y/ highER 8 bits	59	01011001	89
1D	Green x	50	01010000	80
1E	Green y	9D	10011101	157
1F	Blue x	26	00100110	38
20	Blue y	1D	00011101	29
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1



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28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	10	00010000	16
37	Pixel Clock/10000 USB	27	00100111	39
38	Horz active <b>Lower 8bits</b>	40	01000000	64
39	Horz blanking <b>Lower 8bits</b>	C6	11000110	198
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	60	01100000	96
3B	Vertical Active <b>Lower 8bits</b>	84	10000100	132
3C	Vertical Blanking <b>Lower 8bits</b>	1A	00011010	26
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	30	00110000	48
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	36	00110110	54
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	00000000	0
42	Horizontal Image Size <b>Lower 8bits</b>	7E	01111110	126
43	Vertical Image Size <b>Lower 8bits</b>	D6	11010110	214
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	00010000	16
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0



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54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	37	00110111	55
74	Manufacture P/N	33	00110011	51
75	Manufacture P/N	52	01010010	82
76	Manufacture P/N	54	01010100	84
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	31	00110001	49
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	31	00110001	49
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	68	01101000	104



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