Model Name: T550QVN01.1

Issue Date : 2013/06/11

( )Preliminary Specifications
(＊)Final Specifications

Customer Signature	Date	AUO	Date
Approved By		Approval By PM Director Jacky Su	
Note		Reviewed By RD Director Eugene CC Chen Reviewed By Project Leader Chia Hsuan Lin	
		Prepared By PM Joe JJ Shih	

CONTENTS

RECORD OF REVISION

Version	Date	Page	Description
0.0	2013/06/11		First release

1. GENERAL DESCRIPTION

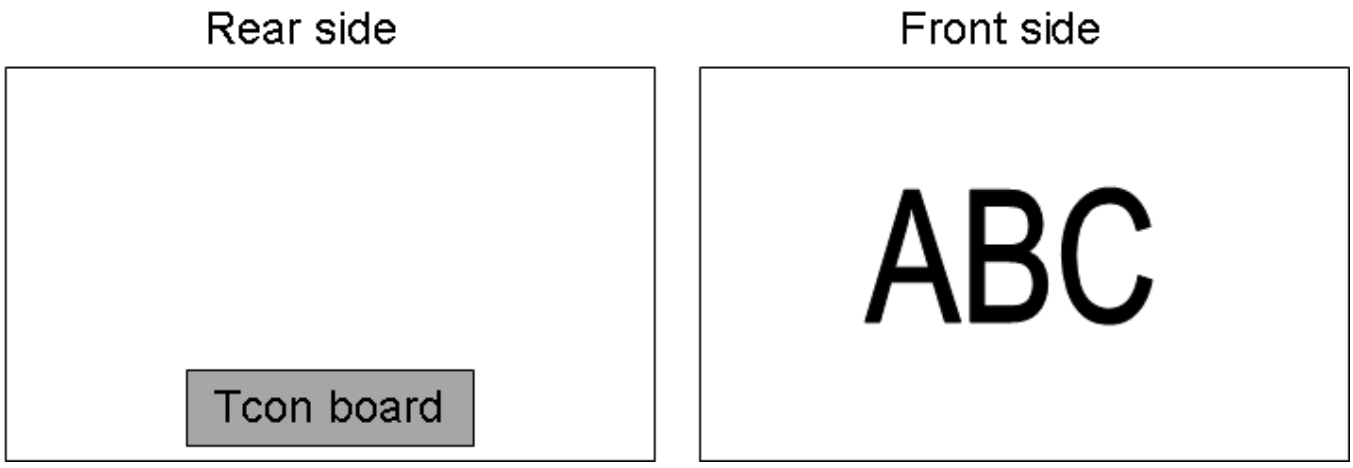
This specification applies to the 55inch Color TFT-LCD SKD model T550QVN01.1. This Open Cell Unit has a TFT active matrix type liquid crystal panel 3,840x2,160 pixels, and diagonal size of 55 inch. This Open Cell Unit supports 3,840x2,160 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	55	inch	
Display Area	1209.6(H) x 680.4(V)	mm	
Outline Dimension	1229.5(H) x 701.49(V) x 2.077(D)	mm	D: cell thickness (含 protective film)
Driver Element	a-Si TFT active matrix		
Bezel Opening	1218.6(H) x 689.4(V)	mm	Recommend
Display Colors	10 bit,	Colors	
Number of Pixels	3840 x 3 x 2160	Pixel	
Pixel Pitch	0.315(H) x 0.315(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 2H		Haze=1%
Weight	3400	g	
Rotate Function	Unachievable		Note 1
Display Orientation	Signal input with “ABC”		Note 2

Note 1: Rotate Function refers to LCD display could be able to rotate.

Note 2: LCD display as below illustrated when signal input with “ABC”.



2. ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	$[Volt]_{DC}$	Note 1
Input Voltage of Signal	Vin	-0.3	4	$[Volt]_{DC}$	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3
Electro Statistic Voltage	ESD		±2	[KV]	Note 4

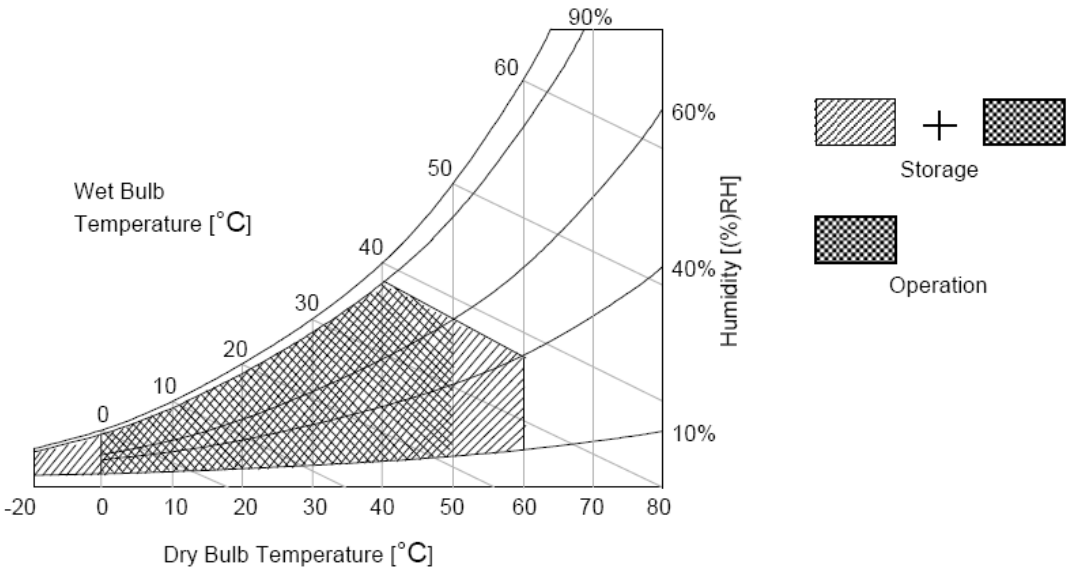
Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition

Note 4: ESD protection procedure must be applied during production process; especially polarizer protection films remove process. Please directly contact AUO if module process advice is required.



3. ELECTRICAL SPECIFICATION

The T550QVN01.1 Open Cell Unit requires power input which is employed to power the LCD electronics and to drive the TFT array and liquid crystal.

3.1 ELECTRICAL CHARACTERISTICS

3.1.1 DC CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V_{DC}	
Power Supply Input Current		I_{DD}	--	1	3.5	A	1
Power Consumption		P_C	--	12	42	Watt	1
Inrush Current		I_{RUSH}	--	--	7	A	2
Permissible Ripple of Power Supply Input Voltage		V_{RP}	--	--	V_{DD} * 5%	mV_{pk-pk}	3
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.4	--	3.3	V_{DC}	5
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	5
V-by-one Interface	CML Differential Input High Threshold	V_{RTH}	+50	--	--	mV_{DC}	
	CML Differential Input Low Threshold	V_{RTL}	--	--	-50	mV_{DC}	
	CML Common mode Bias Voltage	V_{RCT}	0.8	0.9	1.0	V_{DC}	

3.1.2 AC CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
V-by-one Interface	VRXINP/N input each bit Period	T_{RRIP} (UI)	413	--	505	ps	8bit 6
			310	--	379	ps	10bit 6
	CDR lock time(CDR training)	T_{RLCK0}	--	--	1.0	ms	6
	ALN Training	T_{RALN}	--	30720	--	UI	8bit 6
			--	40960	--	UI	10bit 6
	PDX active to hot plug enable	T_{RHPD0}	--	--	1.0	us	6
	Intra-pair skew	T_{INTRA}	--	--	0.3	UI	7
	Inter-pair skew	T_{INTER}	--	--	5	UI	8
	Inter-block skew	T_{INTER_BLK}	--	--	0.5	DE	9
I2C Interface	SCL clock frequency	F_{SCL}	0	--	400	KHZ	
	I2C clock high level	T_{SCHi}	0.6	--	--	us	
	I2C clock low level	T_{SCLo}	1.2	--	--	us	
	I2C data setup time	T_{SDS}	100	--	--	ns	
	I2C data hold time	T_{SDH}	0	--	900	ns	
	SDA and SCL rise time	T_R	--	--	1000	ns	
	SDA and SCL fall time	T_F	--	--	300	ns	

3.1.3 DRIVER CHARACTERISTICS

Item	Symbol	Min	Max	Unit	condition
Driver Surface Temperature	DST		100	[℃]	Note

Note : Any point on the driver surface must be less than 100℃ under any conditions.

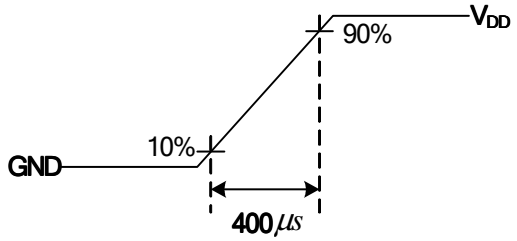
Note :

1. Test Condition:

(1) V_{DD} = 12.0V
(2) Fv = 120Hz
(3) Fclk= 74.25MHz
(4) Temperature = 25 ℃
(5) Typ. Input current : White Pattern
Max. Input current: Heavy loading pattern defined by AUO

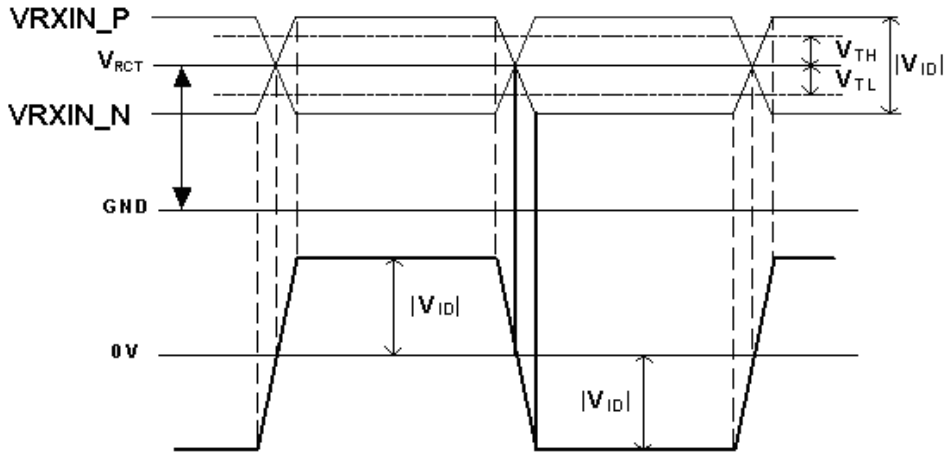
>> refer to "Section:3.3 Signal Timing Specification, Typical timing"

2. Measurement condition : Rising time = 400us



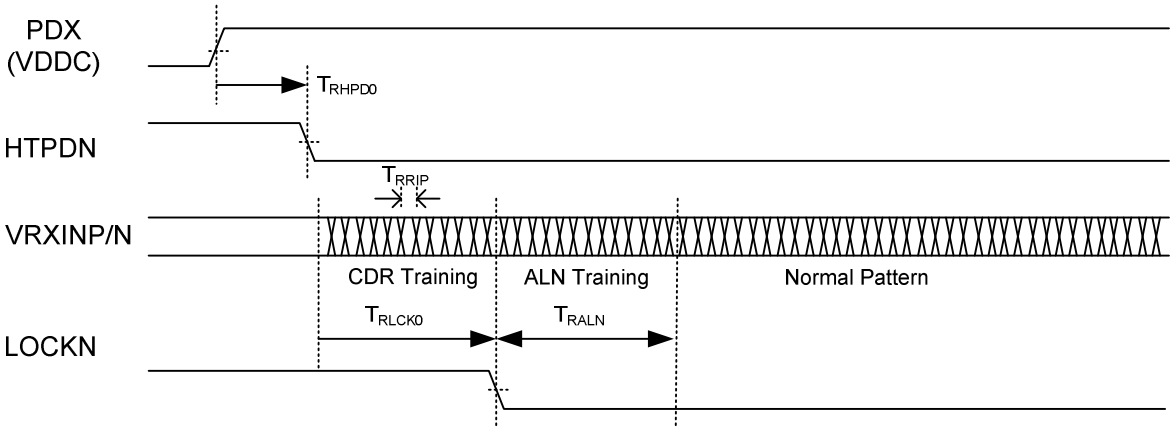
3. Test Condition:
(1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
(2) Under Max. Input current spec. condition.

4. V_{RCT} = 0.9V

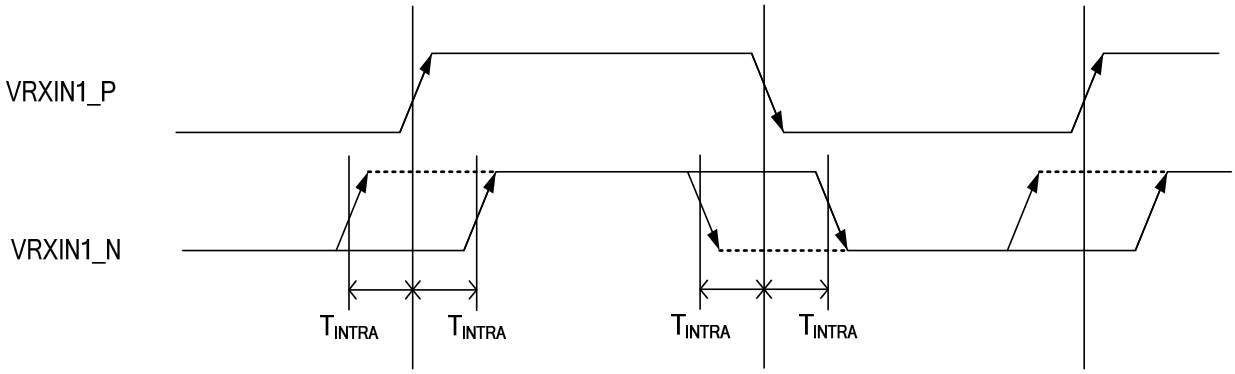


5. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.

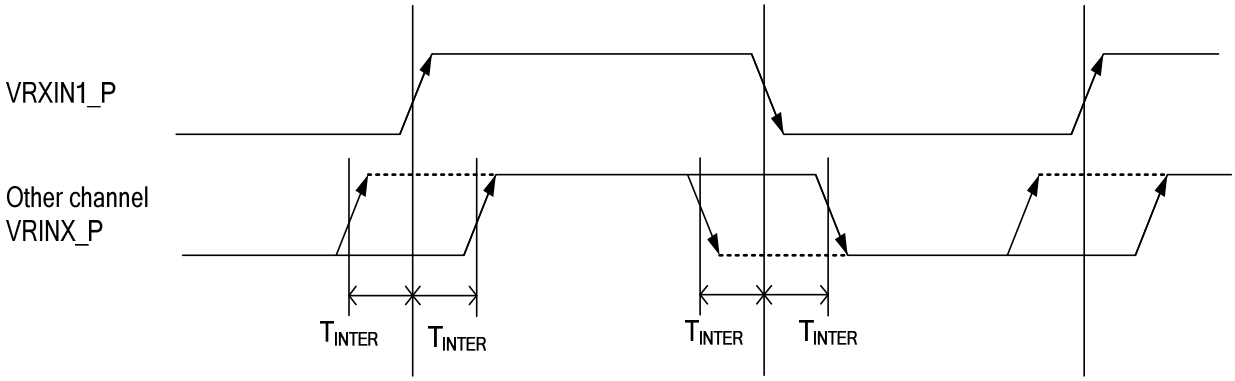
6. V-by-one Receiver start up timing waveform



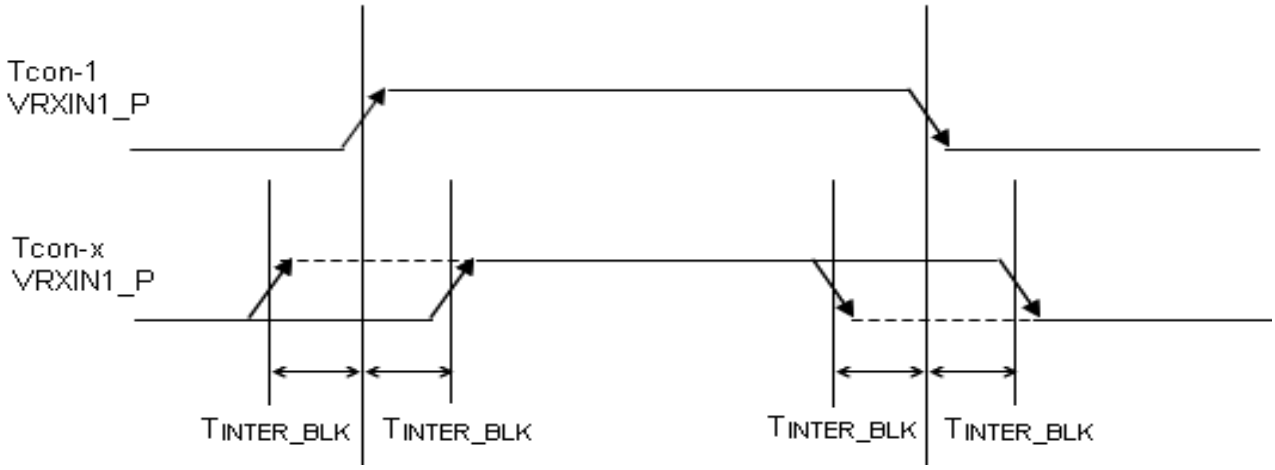
7. V-by-one Intra-pair Skew



8. V-by-one Inter-pair Skew



9. V-by-one Inter-block Skew



DE is H total (Th)

>> Th refer to “Section: 3.3 Signal Timing Specification

INTERFACE CONNECTIONS

3.2.1 T-CON BOARD PIN MAP

- LCD connector: FI-RE51S-HF (JAE) or compatible

	Symbol	Description	PIN	Symbol	Description
1	NC	NC PIN	26	GND	CML Ground
2	NC	NC PIN	27	Rx2n	V-by-One HS Data Lane 2
3	WP**	EEPROM write protect	28	Rx2p	V-by-One HS Data Lane 2
4	NC	NC PIN	29	GND	CML Ground
5	NC	NC PIN	30	GND	CML Ground
6	NC	NC PIN	31	Rx3n	V-by-One HS Data Lane 3
7	NC	NC PIN	32	Rx3p	V-by-One HS Data Lane 3
8	NC	AUO Internal Use Only	33	GND	CML Ground
9	NC	AUO Internal Use Only	34	GND	CML Ground
10	NC	NC PIN	35	Rx4n	V-by-One HS Data Lane 4
11	GND	Ground	36	Rx4p	V-by-One HS Data Lane 4
12	GND	Ground	37	GND	CML Ground
13	GND	Ground	38	GND	CML Ground
14	GND	Ground	39	Rx5n	V-by-One HS Data Lane 5
15	GND	Ground	40	Rx5p	V-by-One HS Data Lane 5
16	HTPDN	Hot plug detect	41	GND	CML Ground
17	LOCKN	Lock detect	42	GND	CML Ground
18	GND	CML Ground	43	Rx6n	V-by-One HS Data Lane 6
19	Rx0n	V-by-One HS Data Lane 0	44	Rx6p	V-by-One HS Data Lane 6
20	Rx0p	V-by-One HS Data Lane 0	45	GND	CML Ground
21	GND	CML Ground	46	GND	CML Ground
22	GND	CML Ground	47	Rx7n	V-by-One HS Data Lane 7
23	Rx1n	V-by-One HS Data Lane 1	48	Rx7p	V-by-One HS Data Lane 7
24	Rx1p	V-by-One HS Data Lane 1	49	GND	CML Ground
25	GND	CML Ground	50	NC	AUO Internal Use Only
			51	NC	AUO Internal Use Only

- LCD connector: FI-RE41S-HF (JAE) or compatible

PIN	Symbol	Description	PIN	Symbol	Description
1	GND	Ground	21	Rx11n	V-by-One HS Data Lane 11
2	GND	Ground	22	Rx11p	V-by-One HS Data Lane 11
3	GND	Ground	23	GND	CML Ground
4	GND	Ground	24	GND	CML Ground
5	GND	Ground	25	Rx12n	V-by-One HS Data Lane 12
6	SCL*	I2C CLK	26	Rx12p	V-by-One HS Data Lane 12
7	SDA*	I2C Data	27	GND	CML Ground
8	GND	CML Ground	28	GND	CML Ground
9	Rx8n	V-by-One HS Data Lane 8	29	Rx13n	V-by-One HS Data Lane 13
10	Rx8p	V-by-One HS Data Lane 8	30	Rx13p	V-by-One HS Data Lane 13
11	GND	CML Ground	31	GND	CML Ground
12	GND	CML Ground	32	GND	CML Ground
13	Rx9n	V-by-One HS Data Lane 9	33	Rx14n	V-by-One HS Data Lane 14
14	Rx9p	V-by-One HS Data Lane 9	34	Rx14p	V-by-One HS Data Lane 14
15	GND	CML Ground	35	GND	CML Ground
16	GND	CML Ground	36	GND	CML Ground
17	Rx10n	V-by-One HS Data Lane 10	37	Rx15n	V-by-One HS Data Lane 15
18	Rx10p	V-by-One HS Data Lane 10	38	Rx15p	V-by-One HS Data Lane 15
19	GND	CML Ground	39	GND	CML Ground
20	GND	CML Ground	40	NC	AUO Internal Use Only
			41	NC	AUO Internal Use Only

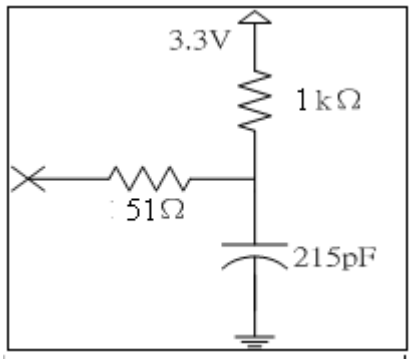
- LCD Power connector:

  Power CN (12Pin) : SM12B-PAHS-TBT (JST) or SM12B-PASS-TBT(LF)(SN) (JST)

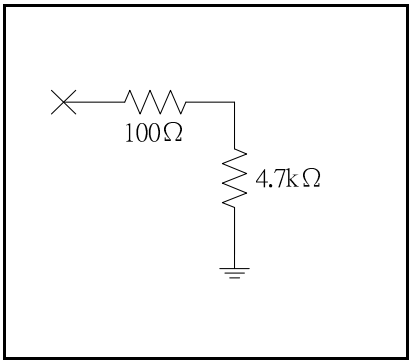
PIN	Symbol	Description
1	Power V12 IN	PWR Power V12 IN
2	Power V12 IN	PWR Power V12 IN
3	Power V12 IN	PWR Power V12 IN
4	Power V12 IN	PWR Power V12 IN
5	Power V12 IN	PWR Power V12 IN
6	NC	NC PIN
7	NC	NC PIN
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground

- FFC connector(80Pin): 196225-80041 (P-TWO) or 106C80-100000-G2-R(CHIEF LAND)

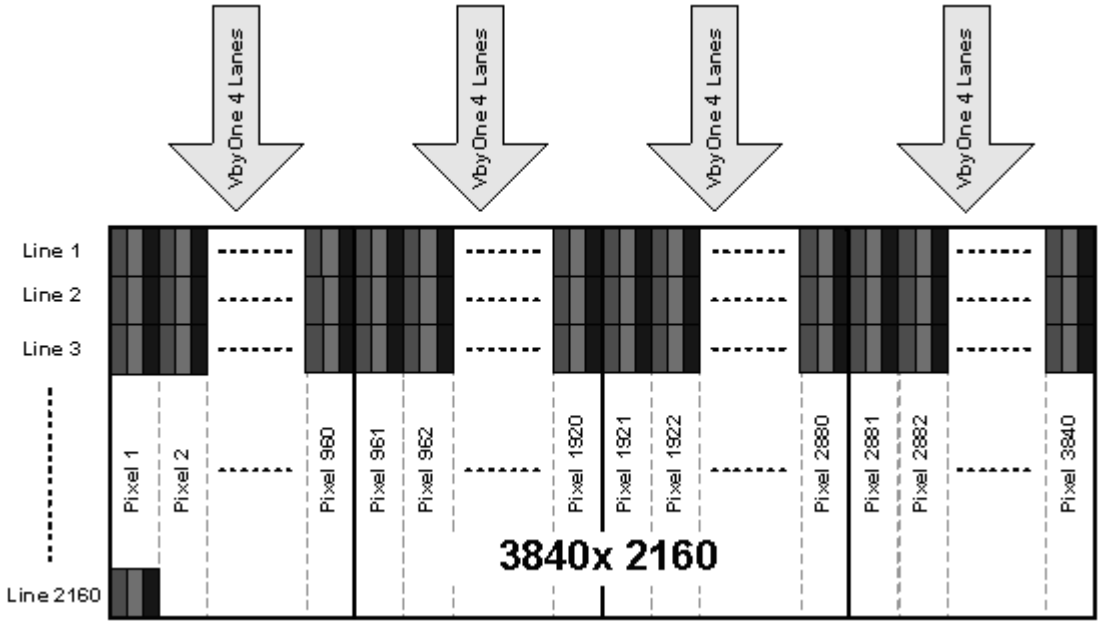
Note * : SCL/SDA



Note ** : WP



3.2.2 4K2K Input Data Format



Note: Normal pixel data mapping

	Pixel Mapping					Pixel Mapping					Pixel Mapping					Pixel Mapping			
Lane 0	1	5	…	957	Lane 4	961	965	…	1917	Lane 8	1921	1925	…	2877	Lane 12	2881	2885	…	3837
Lane 1	2	6	…	958	Lane 5	962	966	…	1918	Lane 9	1922	1926	…	2878	Lane 13	2882	2886	…	3838
Lane 2	3	7	…	959	Lane 6	963	967	…	1919	Lane 10	1923	1927	…	2879	Lane 14	2883	2887	…	3839
Lane 3	4	8	…	960	Lane 7	964	968	…	1920	Lane 11	1924	1928	…	2880	Lane 15	2884	2888	…	3840

2DMode Pixel Mapping:

Pixel No	Pixel 1			Pixel 2			Pixel 3			~		Pixel 3840		
Line 1	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 3	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 4	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 5	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 6	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
:	:	:	:	:	:	:	:	:	:	:	~	:	:	:
Line 2158	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2159	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840
Line 2160	R1	G1	B1	R2	G2	B2	R3	G3	B3	R4	~	R3840	G3840	B3840

3.3 SIGNAL TIMING SPECIFICATION

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	2180	2250	2715	Th
	Active	Tdisp (v)		2160		
	Blanking	Tblk (v)	20	90	555	Th
Horizontal Section	Period	Th	274	275	300	Tclk
	Active	Tdisp (h)		240		
	Blanking	Tblk (h)	34	35	60	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	75	MHz
Vertical Frequency	Frequency	Fv	94	120	122	Hz
Horizontal Frequency	Frequency	Fh	240	270	278.4	KHz

Notes:

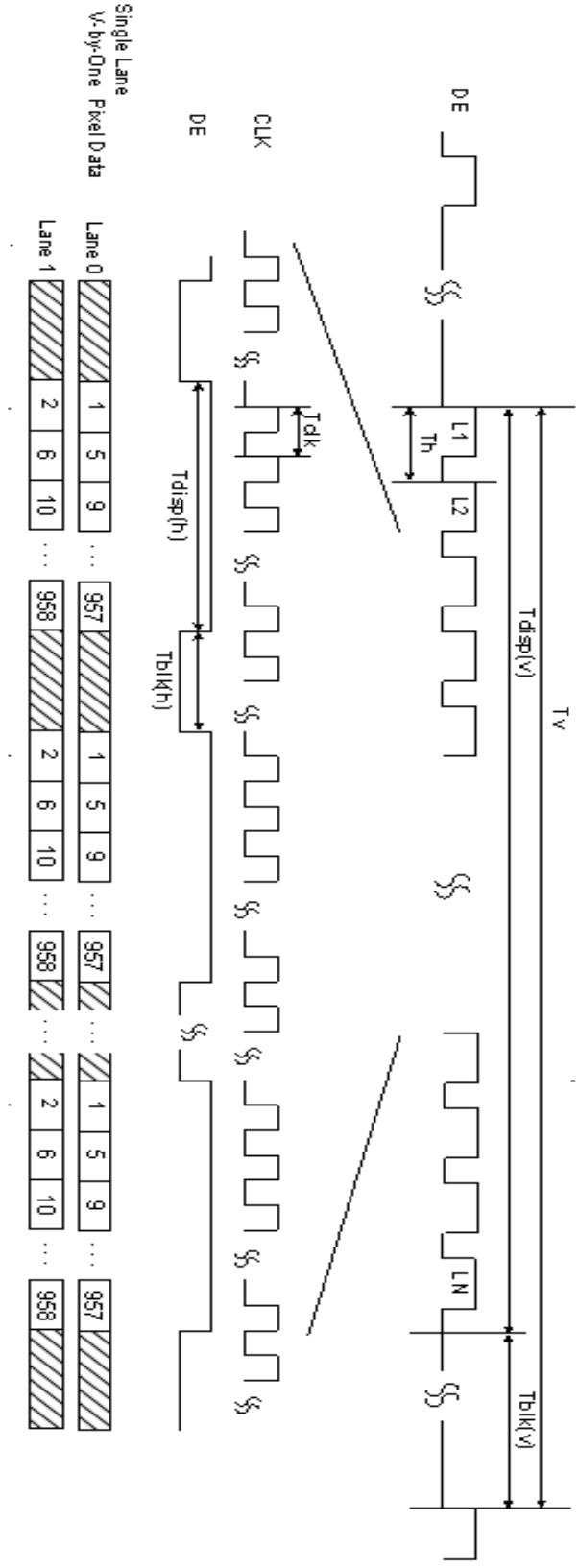
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2)Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3)If a period of DE “High” is less than 3840 DCLK or less than 2160 lines, the rest of the screen displays black.

(4)The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3.4 SIGNAL TIMING WAVEFORMS



3.5 COLOR INPUT DATA REFERENCE

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

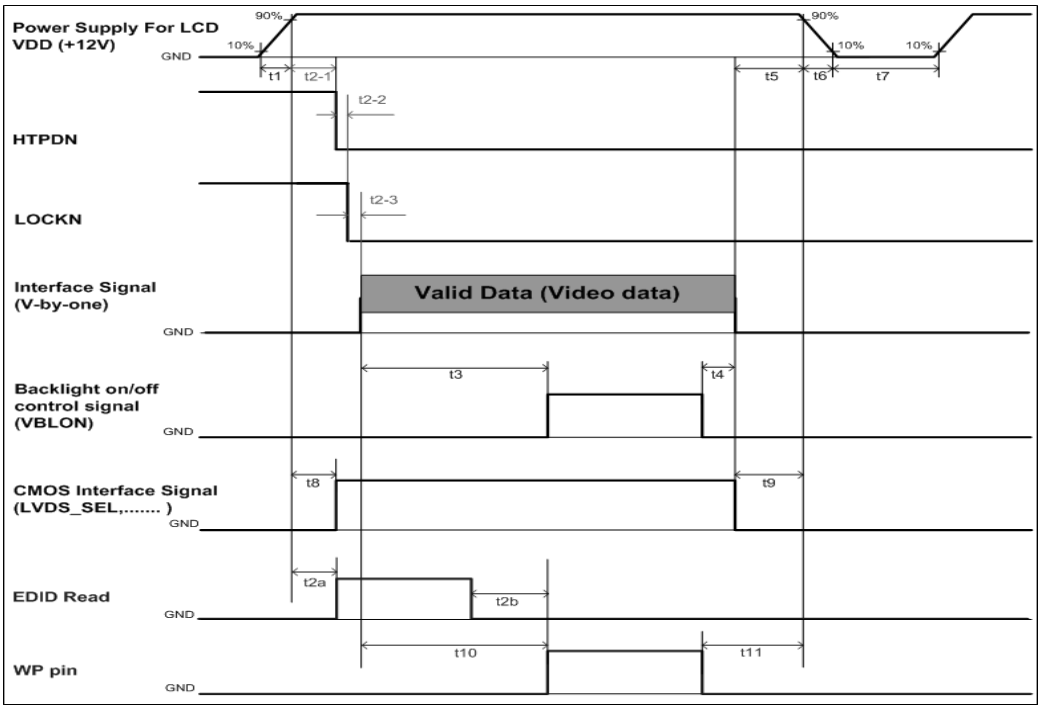
Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3.6 POWER SEQUENCE FOR LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2-1	150	---	200	ms
t2-2	---	---	---*1	ms
t2-3	---	---	1	ms
t3	450	---	---	ms
t4	0*2	---	---	ms
t5	0	---	---	ms
t6	---	---	---*3	ms
t7	500	---	---	ms
t8	10*4	---	50	ms
t9	0	---	---	ms
t10	450	---	---	ms
t11	150	---	---	ms
t2a	10	---	---	ms
t2b	10	---	---	ms

Note:

(1) t2-2 : V by One training time after power-on. The timing of HTPDN falling edge to LOCKN falling edge decided by customer system.

(2) t4=0 : concern for residual pattern before BLU turn off.

(3) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

(4) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

(5) t2-1: VDD rising(90%) to HTPDN falling edge

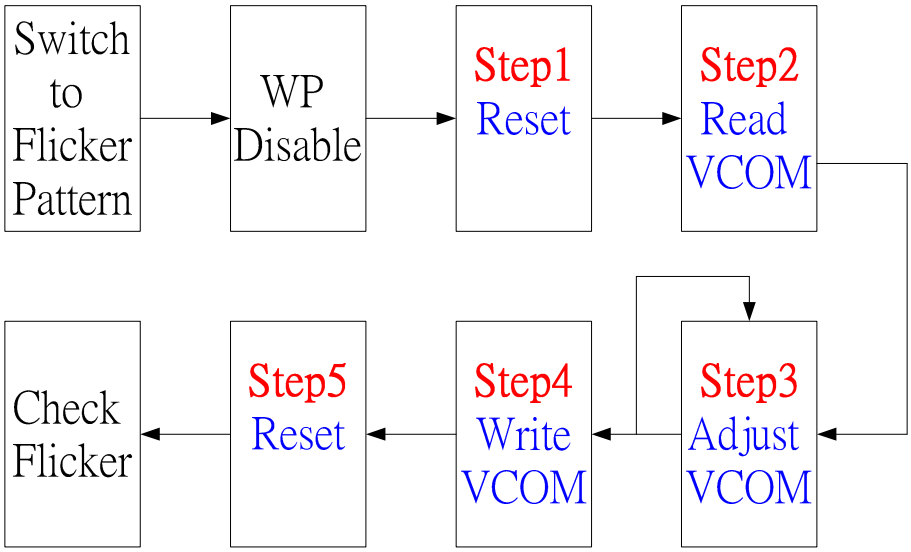
t2-2: CDR lock time (CDR training)

t2-3: ALN training

3.7 VCOM ADJUST SOP

If you need below pattern or more detail information, please directly contact AUO for engineer service.

3.7.1 VCOM I2C TUNING STEP



3.7.2 FLICKER PATTERN

3.7.3 WP (WRITE PROTECT) DISABLE

Disable	Enable	Default (NC)
H	L	L

3.7.4 ADJUST SOP

Step1 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

Step2 Read VCOM

* Data = 7Bits

S	Slave Address	W	A	Index Address 1	A	S	Slave Address	R	A	DATA	NA	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 1			1 1 1 0 1 0 0 1			X X X X X X X X		
	0xE8			0x01			0xE9					
	Device Address + W			VCOM Address			Device Address + R			Data		

Step3 Adjust VCOM

* DVCOM = 8Bits

S	Slave Address	W	A	Index Address 1	A	DVCOM	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 1		0000000X~1111111X		
	0xE8			0x01		0x00~0xFF		
	Device Address + W			VCOM Address		VCOM value		

Step4 Write VCOM

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 0 1 0 1 0		
	0xE8			0x00		0x0A		
	Device Address + W			Control Address		Write DAC to NVM+ OUT_EN		

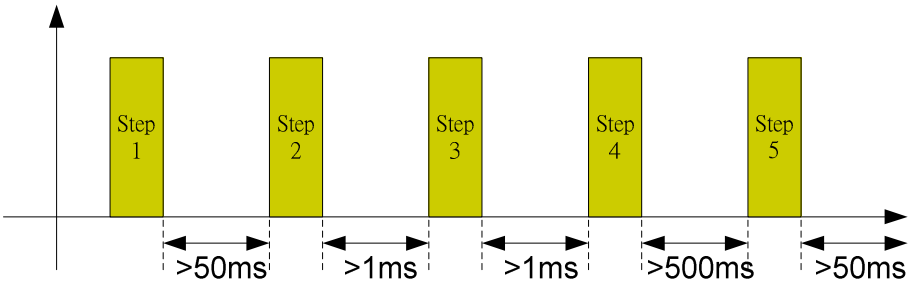
Step5 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

3.7.5 INTERVAL OF STEP TO STEP

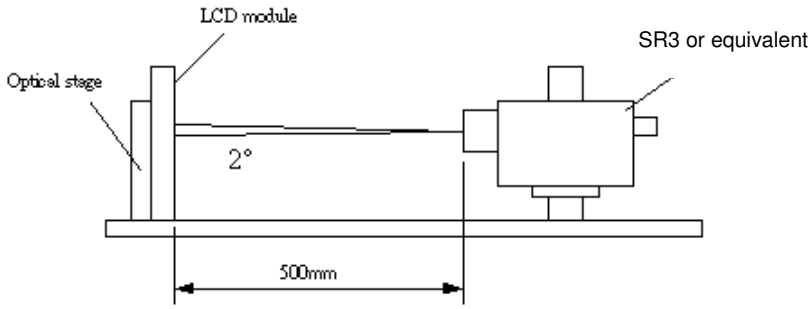
Step to step interval must follow below figure



4 OPTICAL SPECIFICATION

Optical characteristics are determined after the open cell unit and light source has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



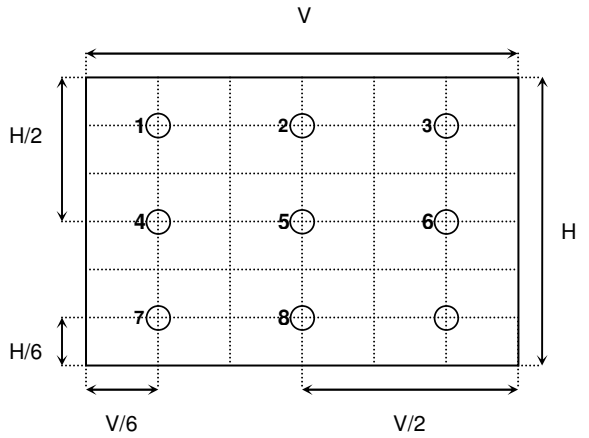
Parameter		Symbol	Condition	Values			Unit	Notes
				Min.	Typ.	Max		
Contrast Ratio		CR	With AUO Module	3200	4000	--		1, 2
White Variation		$\delta_{WHITE(9P)}$		--	--	1.33		1, 3
Response Time (G to G)		Tγ		--	6.5	--	ms	4
Center Transmittance		T%		--	4.2		%	1, 7
Color Chromaticity			With CS-1000T Standard light source "C"					5
	Red	R_X		Typ.-0.03	0.657	Typ.+0.03		
		R_Y			0.327			
	Green	G_X			0.270			
		G_Y			0.584			
	Blue	B_X			0.139			
		B_Y			0.089			
	White	W_X			0.289			
		W_Y			0.340			
Viewing Angle			With AUO Module					1, 6
2D	x axis, right(φ=0°)	θ_r		--	89	--	degree	
	x axis, left(φ=180°)	θ_l		--	89	--	degree	
	y axis, up(φ=90°)	θ_u		--	89	--	degree	
	y axis, down (φ=270°)	θ_d		--	89	--	degree	

1. Light source here is the BLU of AUO T550QVD01.0 module.
2. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

3. The white variation, δWHITE is defined as:

$\delta_{WHITE(9P)}$= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})

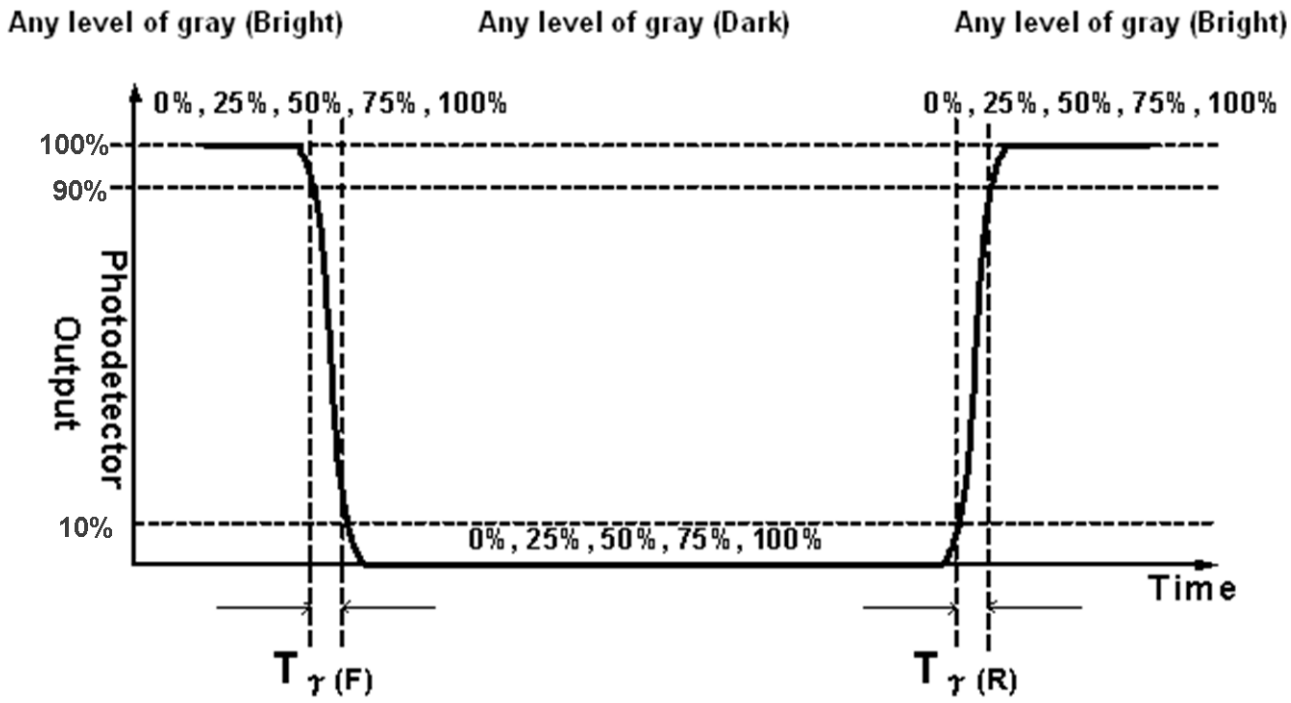


4. Response time T_Y is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on F_V=120Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

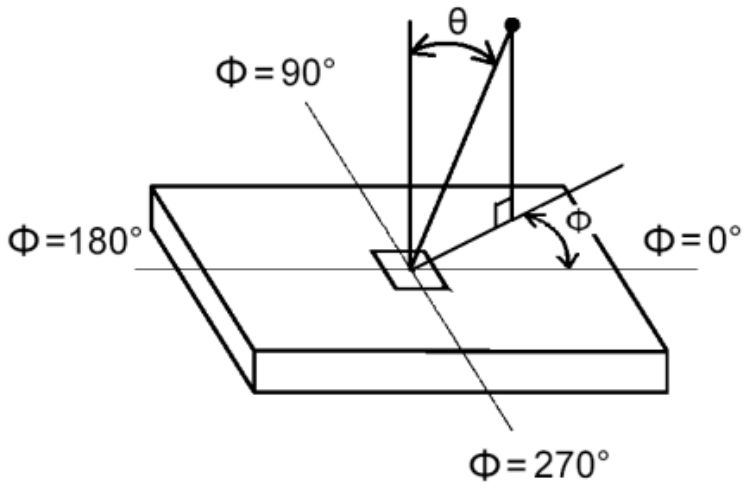
The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray (bright) "and "any level of gray (dark)".

FIG.3 Response Time



5. Light source here is the standard light source “C” which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：
   A. Measure the “Module” and “BLU” optical spectrums (W, R, G, B).
   B. Calculate cell spectrum from “Module” and “BLU” spectrums.
   C. Calculate color chromaticity by using cell spectrum and the spectrum of standard light source “C”.
6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG.4 Viewing Angle

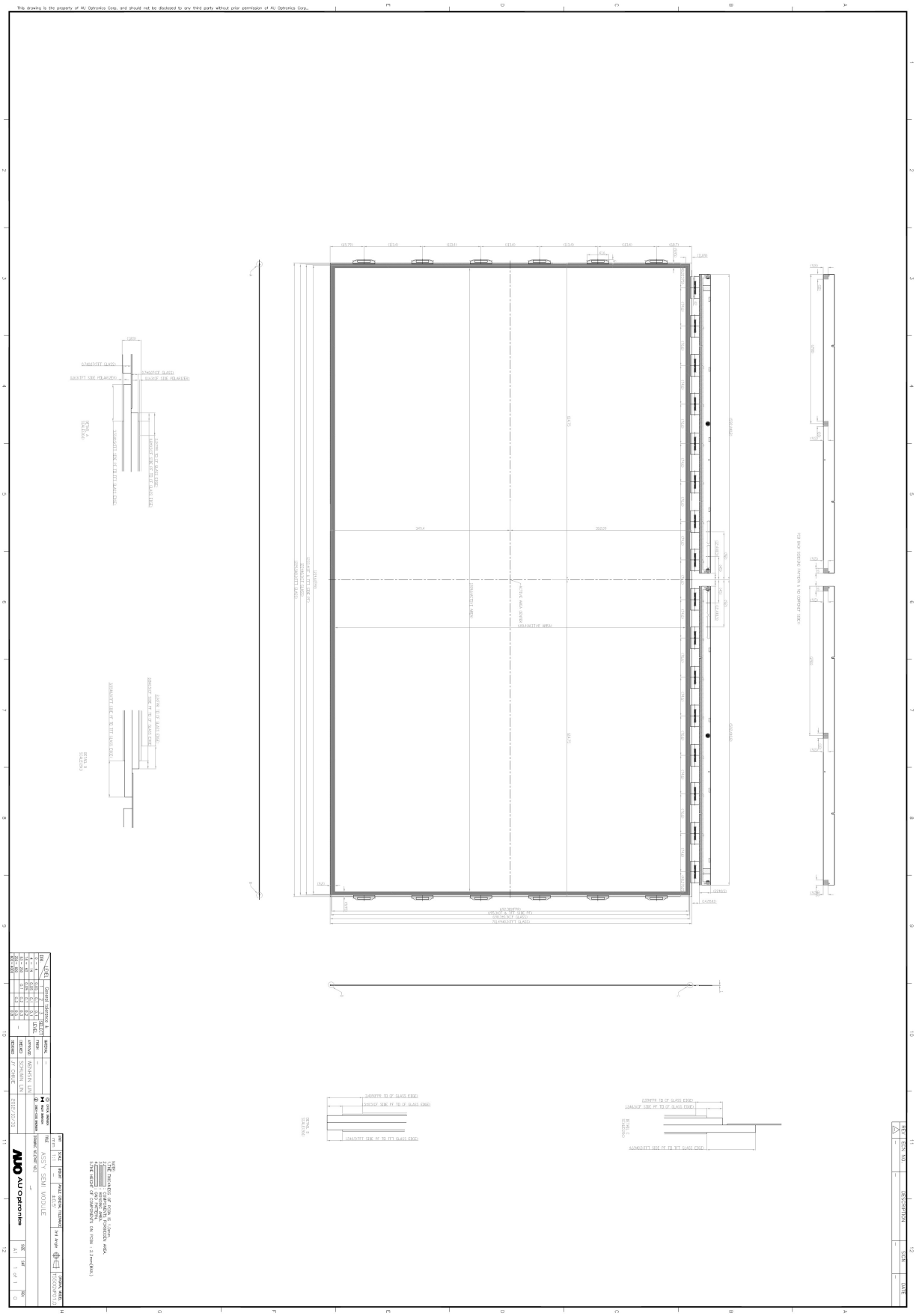


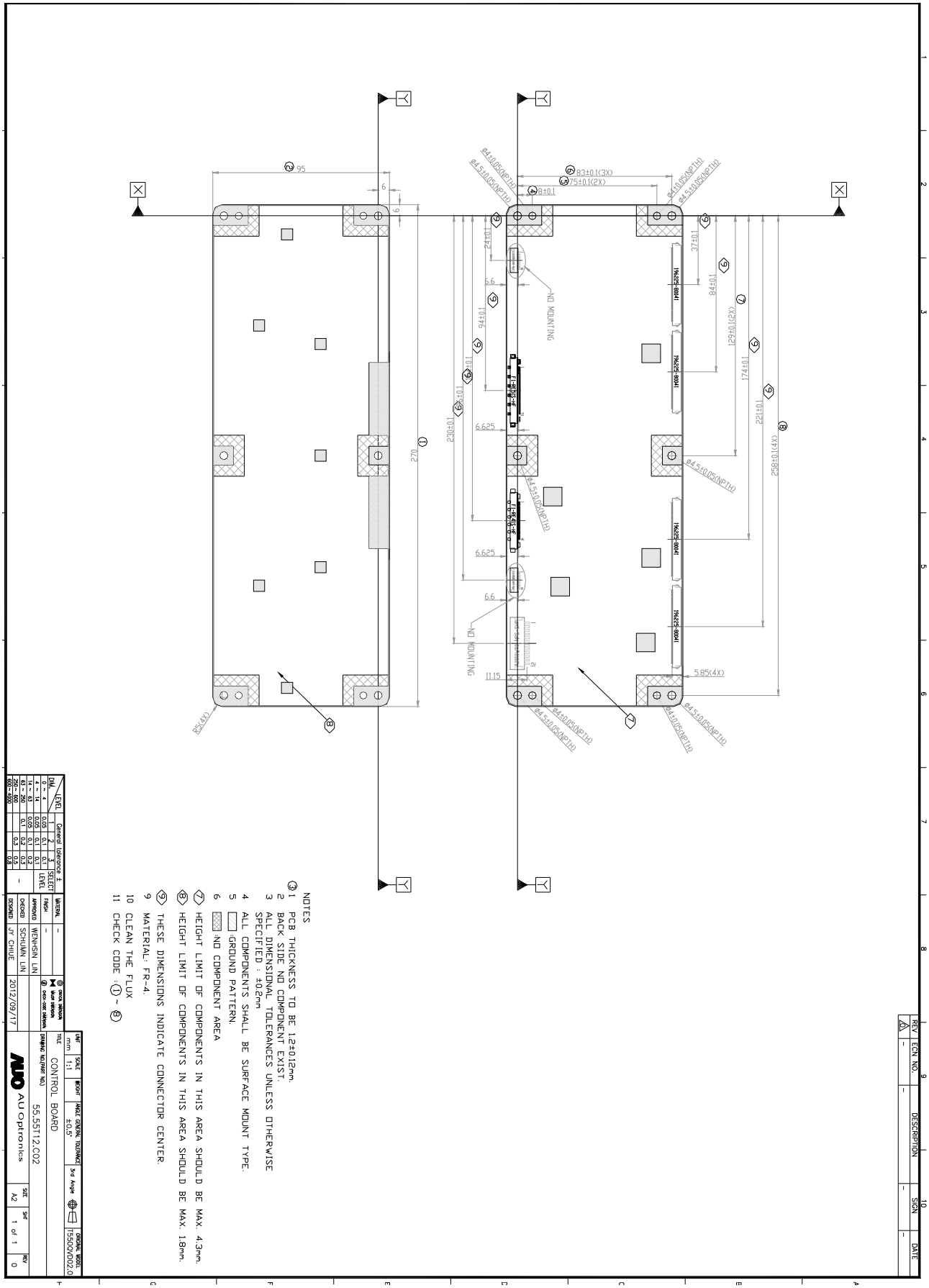
7. Definition of Transmittance (T%):

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

During transmittance measurement, the backlight of LCD module contains no brightness enhancement film. Two diffuser sheets which diffuse the light source uniformly are suggested to use for transmittance measurement.

5 MECHANICAL CHARACTERISTICS




NOTES
1 PCB THICKNESS TO BE 1.2±0.12mm.
2 BACK SIDE NO COMPONENT EXIST.
3 ALL DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED : ±0.2mm
4 ALL COMPONENTS SHALL BE SURFACE MOUNT TYPE.
5 GROUND PATTERN.
6 NO COMPONENT AREA
7 HEIGHT LIMIT OF COMPONENTS IN THIS AREA SHOULD BE MAX. 4.3mm.
8 HEIGHT LIMIT OF COMPONENTS IN THIS AREA SHOULD BE MAX. 1.8mm.
9 THESE DIMENSIONS INDICATE CONNECTOR CENTER.
9 MATERIAL: FR-4.
10 CLEAN THE FLUX
11 CHECK CODE : 1 - 8
NO MOUNTING
AU Optronics
CONTROL BOARD
55.55T12.C02
T550QVD02.0
2012/09/17

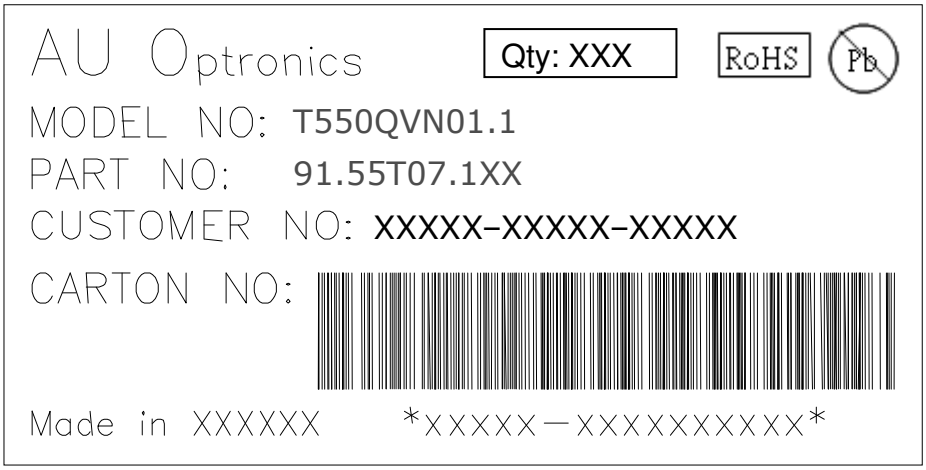
6 PACKING

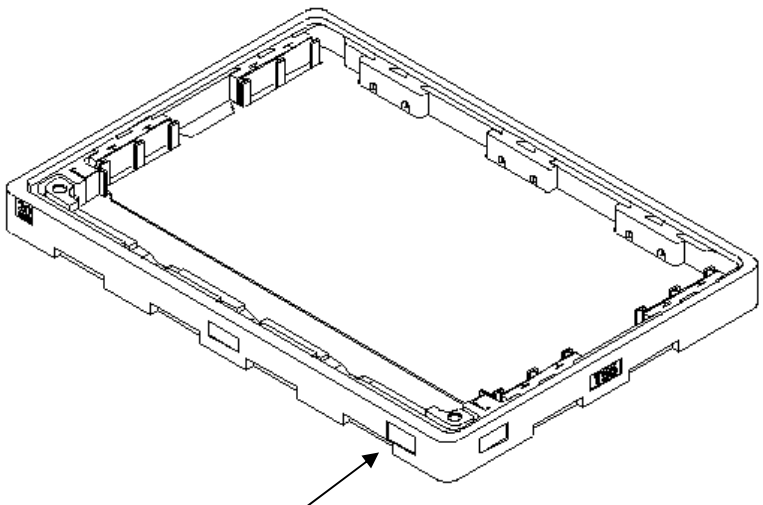
6-1. DEFINITION OF LABELS:

Open cell shipping label (35*7mm)

1. S/N Number
2. AUO internal use
3. Manufactured week
4. Model name

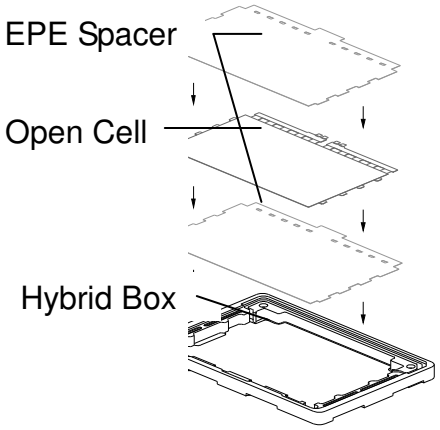
Carton Label for Open Cell Box:





Carton label location

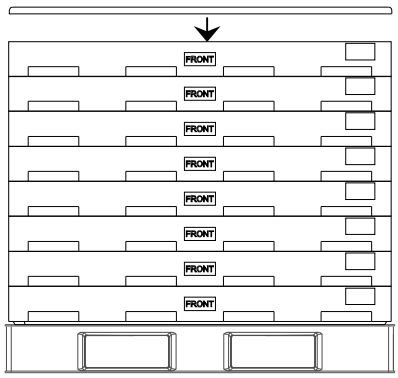
6-2 Packing Process:



1Box for **7 pcs** cells & **8 pcs** spacers

7 Pcs/Box,

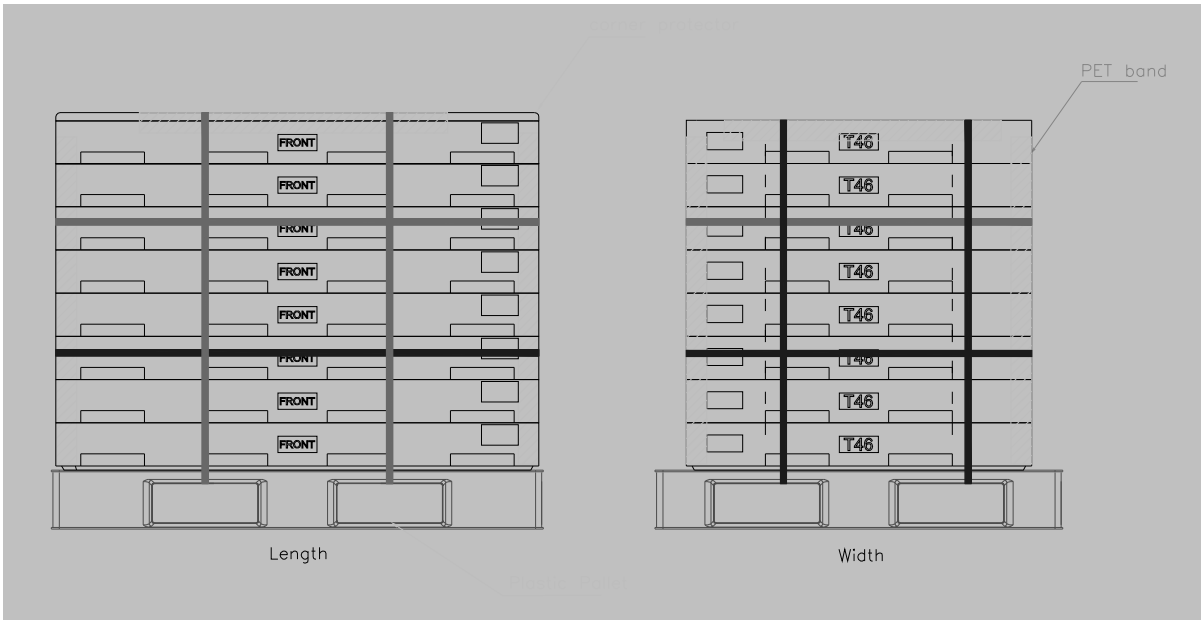
EPP Top Cover



Pallet Dimension:1420*1120*150 mm
8 Boxes/Pallet, after stack 8 boxes, then put EPP top cover on it.

6-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	7 pcs/box	1400(L)mm*990(W)mm*116(H)mm	32	
2	Pallet	1	1420(L)mm*1120(W)mm*150(H)mm	15	
3	Boxes per Pallet	8 boxes/Pallet (By Air) ; 8 Boxes/Pallet*Double Pallet (By Sea)			
4	Panels per Pallet	56 pcs/pallet(By Air) ; 56 pcs/Pallet*Double Pallet (By Sea)			
5	Pallet after packing	56(by Air)	1420(L)mm*1120(W)mm*1028(H)mm (by Air)	271(by Air)	
		112(by Sea)	1420(L)mm*1120(W)mm*2056(H)mm (by Sea)	542(by Sea)	40ft HQ



7 PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD Open Cell unit and strongly recommended to contact AUO if module process advice is required.

7.1 MOUNTING PRECAUTIONS

(1) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the cell. And the frame on which a cell is mounted should have sufficient strength so that external force is not transmitted directly to the cell.

(2) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Do not open the case because inside circuits do not have sufficient strength.

7.2 OPERATING PRECAUTIONS

(1) The open cell unit listed in the product specification sheets was designed and manufactured for TV application

(2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage:
V=±200mV(Over and under shoot voltage)

(3) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(4) Brightness/transmittance depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(6) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

7.3 ELECTROSTATIC DISCHARGE CONTROL

Since a open cell unit is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

7.4 PRECAUTIONS FOR STRON LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

7.5 STORAGE

When storing open cell units as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the open cell unit to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

7.6 HANDLING PRECAUTIONS FOR PROTECTION FILM OF POLARIZER

The protection film of polarizer is still attached on the surface as you receive open cell units. When the protection film is peeled off, static electricity is easily generated on the polarizer surface. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

