GPS

locate, communicate, accelerate

UC530M

Fastrax Multi-GNSS antenna module

Data Sheet

Highlights:

- Hybrid Multi-GNSS engine for combined GPS, GLONASS and QZSS
- Embedded GPS/GNSS Antenna
- Extremely small form factor and low power consumption
- Self-Assistance for 3 days
- Superior Sensitivity
- Connectivity for external GPS/GNSS antenna
- Easy migration from UC530
- LCC package for reliable and cost effective manufacturing

www.u-blox.com

Document Information	
Title	UC530M
Subtitle	Fastrax Multi-GNSS antenna module
Document type	Data Sheet
Document number	FTX-HW-12007-A
Document status	Preliminary

Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
UC530M	UC530M-0	Flash	N/A

Contents

1 Overview

1.1 General

The Fastrax UC530M is an OEM GNSS receiver module variant based on Fastrax UC530 with the Mediatek MT3333 chip that supports All-in-One GNSS hybrid navigation. The Fastrax UC530M receiver provides extremely low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations in navigation with hybrid solution using signals from both GPS + Glonass GNSS systems. Future GNSS systems like Galileo or Beidou can be supported with future firmware upgrade in GPS + Galileo or GPS + Beidou modes.

The UC530M provides complete signal processing from embedded antenna to host port UART and location data output is in NMEA protocol. The module requires a main and a backup power supply. The host port is configurable to UART during power up. Host data and I/O signal levels are 2.8V CMOS compatible and inputs are 3.6V tolerable. The host interface equals to the UC530 module variant excluding TIMER output signal (open drain), which is now FORCE_ON input signal; the external power switch used with UC530 low power modes is now embedded in to UC530M.

The UC530M supports a new feature called AlwaysLocate™, which is an intelligent controller of the UC530M power saving mode. Depending on the environment and motion conditions, the module can adaptively adjust the navigation activity in order to achieve a balance in positioning accuracy, fix rate and power consumption.

The module also supports autonomous A-GPS. It is self-assisted since the EASY™ (Embedded Assist System, also called as) ephemeris extension is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days.

The UC530M contains also an AIC (Active Interference Cancellation), which provides state-of-art narrow band (CW) interference and jamming elimination up to 12 CW jammers < -80dBm.

The module also supports a logging feature called LOCUS, which enables automatic logging of position data to internal flash memory. The logging capacity is >16 hrs typ. @ 15 sec storage interval.

The UC530M module supports also external active antenna connectivity with excellent out-of-band blocking rejection and which can provide also 3V antenna bias supply and automatic RF signal path switching.

This document describes the electrical connectivity and main functionality of the Fastrax UC530M OEM GPS Receiver module.

1.2 Block diagram

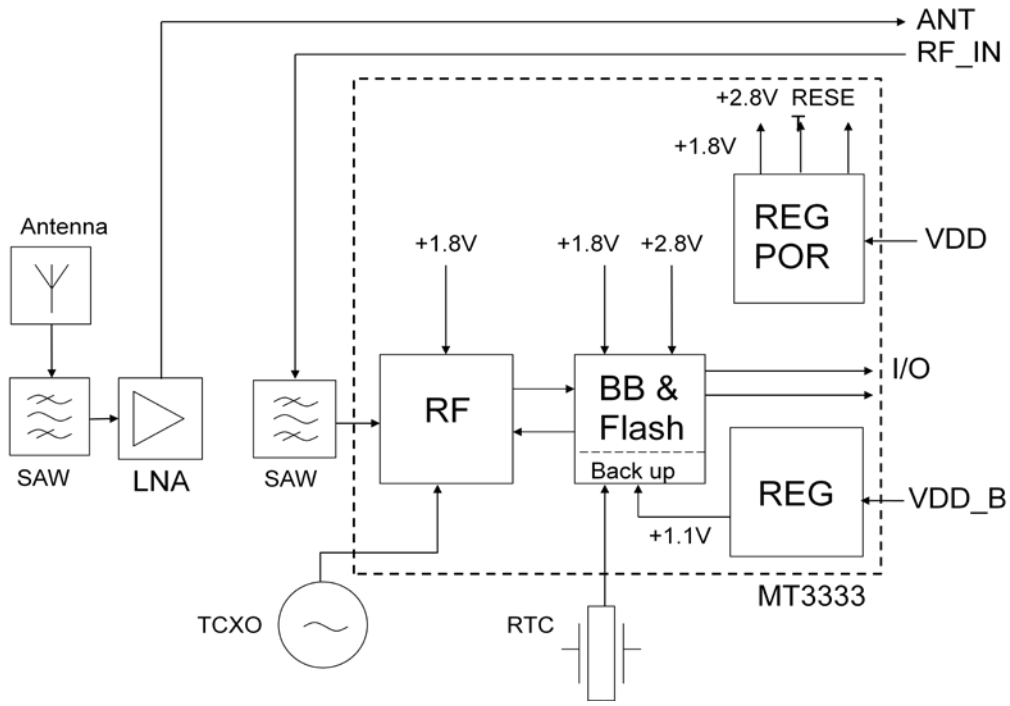

Figure 1: Block diagram

1.3 Frequency Plan

Clock frequencies generated internally in the Fastrax UC530M receiver:

- Switched Mode Power Supply (in PWM and PFM modes)
- 32,768 Hz Real Time Clock (RTC)
- 16.368 MHz Master Clock (TCXO)
- 3177.2 MHz Local Oscillator (LO) of the RF down-converter (GPS+Glonass mode)
- LO/2, i.e. 1588.6 MHz of the RF down-converter (GPS+Glonass mode)

1.4 General Specifications

Feature	Specification
Receiver	GNSS L1 C/A-code, SPS of GPS + Glonass, Galileo or Beidou
Chip set	Mediatek MT3333
Channels	99/33 (search/track)
Tracking sensitivity	-165 dBm typ.
Navigation sensitivity	-165 dBm typ.
Navigation sensitivity, re-acq.	-160 dBm typ.
Navigation sensitivity, cold acq.	-148 dBm typ.
Update rate	1 Hz (configurable up to 10 Hz)
Position accuracy (note 1)	3.0 m (67%) typ. Horizontal 5.0 m (67%) typ. Vertical 0.02 m/s (50%) typ. Velocity
Max altitude/velocity	<60,000 ft/<1,000 knots
Differential GPS	SBAS (WAAS, EGNOS, MSAS, GAGAN, QZSS), RTCM
Time to First Fix, cold acq.	23 s typ. (note 1)
Time to First Fix, warm acq.	23 s typ. (note 1)
Time to First Fix, hot acq.	1 s typ. (note 1)
Supply voltage, main VDD	+3.0 … +4.3 V
Supply voltage, backup VDD_B	+2.0 … +4.3 V
Power consumption, Full Power	66 mW typ. @ 3.3 V (note 2)
Power consumption, AlwaysLocate™	10 mW typ. @ 3.3 V
Power consumption, Backup state	30 µW typ. @ VDD_B 3.0 V
Optional External RF amplifier net gain range	+10… +30 dB
Storage temperature	-40°C…+85°C
Operating temperature	-40°C…+85°C
Host port configuration	UART
Host port protocol	NMEA-0183 rev. 3.01
Serial data format (UART)	8 bits, no parity, 1 stop bit
Serial data speed (UART)	115,200 baud (configurable 4,800... 921,600 baud)
PPS output	200 ms high pulse, rising edge +/-1 µs (note 1)

Table 1: General specifications

Note 1: With nominal GNSS signal levels -130dBm.

Note 2: @ 1Hz navigation, GPS+Glonass mode, SBAS enabled, average over 24h

2 Operation

2.1 Operating Modes

After power up the UC530M module boots from the internal ROM to Navigation Mode. Modes of operation:

- Navigation Mode (Full Power)
  - Power management system modes
- Standby Mode
- Backup State/Mode
- Reset State

2.2 Full Power Mode

The module will enter Full Power (aka Navigation Mode) after first power up with factory configuration settings. Power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This Mode is also referenced as *Full On, Full Power* or *Navigation* Mode.

Navigation is available and any configuration settings are valid as long as the main VDD and backup VDD_B power supplies are active. When the main VDD and backup VDD_B supply is powered off, settings are reset to factory configuration and receiver performs a cold start on next power up.

Suggestion is to keep the backup supply VDD_B active all the time in order to sustain on time, position and ephemeris in the backup RTC and RAM. The main VDD supply can be used to control the module activity, i.e. when VDD is switched off, the module operation is stopped.

Navigation fix rate can be configured by a NMEA command, see *NMEA Manual for Fastrax IT500 Series GPS receivers* [1]. Note that baud rate must be set high enough or message payload low enough in order to pass through all messages pending.

2.2.1 Host port configuration

Default host port is configured to UART Port 0 by leaving GPIO9 and GPIO10 floating (not connected) during power up. UART Port1 is reserved for DGPS/RTCM protocol.

Default protocol for host communication is NMEA at 115,200 baud. Details on NMEA protocol can be found in *NMEA Manual for Fastrax IT500 Series GPS receivers* [1]. Default NMEA message output configuration: $GPGGA, $GNGSA, $GPGSV, $GPRMC, $GPVTG and $GLGSV rate every second. The module also supports proprietary $PMTK input commands. The message consists of $PMTK<cmd_id>,<data_field(s)>*<chk_sum><CR><LF>. Sample command: $PMTK000*32<CR><LF>. For clarity <CR><LF> are not displayed in the following example messages but should be added to the payload at host.

2.2.2 Fix rate configuration

The host can configure navigation rate from 0.1 Hz to 10 Hz by sending NMEA message $PMTK300, i.e. $PMTK300,<fix_interval>,0,0,0,0*<chk_sum> ; <fix_interval> has valid range 100…. 10,000 ms. E.g. 5 Hz navigation rate is set by command: $PMTK300,200,0,0,0,0*2F.

2.3 Power Management Modes

The UC530M module supports also low power operating modes for reduced power consumption by using embedded power switch:

1. Standby Mode: In this Mode the receiver stops navigation and internal processor enters standby state; current drain at main supply VDD is reduced to 0.4 mA typ. Standby Mode is entered by sending NMEA command: $PMTK161,0*28. Host can wake up the module from Standby Mode to Full Power Mode by sending any byte via host port.

2. Backup Mode: In this mode the receiver is configured to enter autonomously to Backup State; the main power supply VDD shall be still active but supply is controlled internally on/off. In this mode the receiver stays in Backup state (VDD and backup supply VDD_B active) and VDD current is reduced to 3 µA typ. Backup Mode is entered by sending NMEA command: $PMTK225,4*2F. Host can wake up the module via host control signal FORCE_ON signal toggle to high state, t>800 ms.

3. Periodic Mode: This mode allows autonomous power on/off with reduced fix rate to reduce average power consumption, see figure below; the main power supply VDD is kept active but it is controlled on/off internally by an embedded power switch. Periodic Mode is entered by sending the following NMEA command: $PMTK225,<Type>,<Run_time>,<Sleep_time>,<2nd_run_time>,<2nd_sleep_time>*<checksum><CR><LF>, where Type=1 for Periodic Backup Mode; Run_time = Full Power period (ms); Sleep_time = Standby/Backup period (ms); 2nd_run_time = Full Power period (ms) for extended acquisition in case GNSS acquisition fails during the Run_time; 2nd_sleep_time = Standby/Backup period (ms) for extended sleep in case GNSS acquisition fails during the Run_time. Example: $PMTK225,1,3000,12000,18000,72000*16 for periodic Mode with 3 sec Navigation and 12 sec sleep in Backup state. Acknowledge response for the command is $PMTK001,225,3*35. The module can exit Periodic Mode by command $PMTK225,0*2B sent just after the module has been wake up from previous sleep cycle.

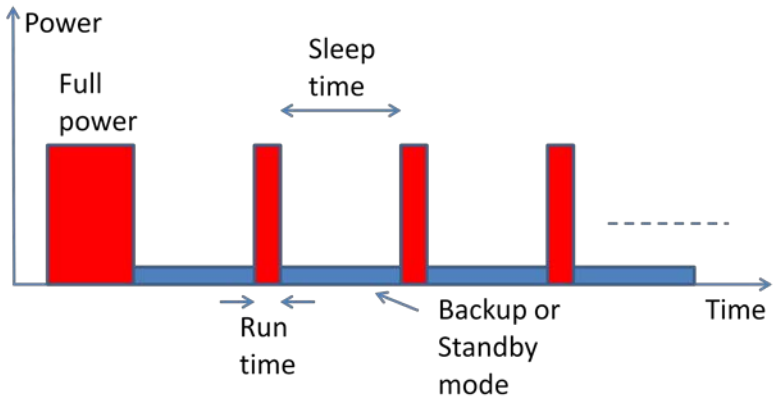

Figure 2: Periodic Mode

4. AlwaysLocate™ is an intelligent controller of the Periodic Mode, which controls the fix interval autonomously. Depending on the environment and motion conditions, the module can adaptively adjust the parameters of the Periodic Mode, e.g. on/off ratio and fix rate to achieve a balance in positioning accuracy and power consumption. The average power drain can vary based on conditions; typical average power is 10 mW. Associated profiles are: High and Low Speed, Walking, Outdoor Static and Indoor. AlwaysLocate™ Mode is entered by sending the following NMEA command: $PMTK225,<Mode>*<checksum><CR><LF>, where Mode=9 for AlwaysLocate™ in Backup Mode. Example: $PMTK225,9*22. Acknowledge response for the command is $PMTK001,225,3*35. The module can exit AlwaysLocate™ Mode by command $PMTK225,0*2B sent just after the module has been wake up from previous sleep cycle.

The module can control the embedded VDD power switch autonomously when the IT530M is set to Backup, Periodic or to AlwaysLocate™ mode by a NMEA command.

Note also that first fix position accuracy can be somewhat degraded in Power Management Modes when compared to Full Power operation. User can improve the position accuracy by taking the 2nd or 3rd fix after waking up.

User can exit low power Modes 3… 4 to Full Power by sending NMEA command $PMTK225,0*2B just after the module has woke up from previous sleep cycle or by toggling FORCE_ON signal for wake up.

2.4 Autonomous A-GPS, Self-Assistance EASY™ usage

The UC530M module self-assistance uses EASY™ (Embedded Assist System) GPS satellite ephemeris extension, which is embedded in the software without any resources required from the host. The EASY™ data is stored on internal flash memory and allows fast TTFF typ. 3 seconds over 3 days and is enabled by default.

Allow the receiver to navigate at least for 5 minutes with good GPS satellite visibility in order to collect broadcast ephemeris and to process necessary information.

2.5 Logger LOCUS usage

The UC530M module supports embedded logger function called LOCUS and when enabled it can log position information to internal flash memory; default log interval is 15 seconds that provides typically > 16 h log capacity. The LOCUS can be enabled by NMEA command $PMTK185,0*22. For details on Locus usage, see *LOCUS manual for Fastrax IT500 Series* [3].

2.6 DGPS usage

By default DGPS/SBAS navigation mode is enabled. The search for suitable SBAS satellite signal is automatic.

The host may either enable DGPS/RTCM navigation mode by sending command 'Set DGPS Data Source to RTCM' $PMTK301,1*2D. The UART Port1 is used for RTCM message input at 9600 baud.

Note that DGPS usage is only supported at 1Hz navigation rate in Full Power mode. Note also that acquiring necessary DGPS correction parameters may take up to 1 minute prior DGPS fix status is achieved, which is indicated in the $GPGGA message, Fix Valid Indicator. Note also that DGPS corrections do not provide corrections against multipath errors that are local; thus accuracy is not necessary improved in urban environments.

2.7 Backup State

Backup State means a low quiescent (10 µA typ. at VDD_B) power state where receiver operation is stopped; only the backup supply VDD_B is powered on while the main supply VDD is switched off by host (or autonomously by embedded power switch of UC530M, see also chapter 0. Waking up from Backup State to Full Power is controlled by host by switching on the VDD supply.

After waking up the receiver will use all internal aiding like GPS time, Ephemeris, Last Position etc. resulting to a fastest possible TTFF in either Hot or Warm start modes.

During Autonomous Backup Mode or Backup State the I/O block is powered off; thus suggestion is that host shall force it's outputs to low state or to high-Z state during Backup state to minimize small leakage currents (<10 µA typ.) at receiver's input signals.

2.8 Reset State

Reset State stops all internal operations and it is entered internally at power up after which internal reset state is relaxed when 167 ms (typ.) has elapsed and module operations begin. The power on reset level is 2.7 +/- 0.1 V at VDD. Host can also override Reset State via RESET_N input, which is low state active. Normally external reset override is not required and RESET_N signal can be left floating (not connected).

3 Connectivity

3.1 Signal Assignments

The I/O signals are available as soldering (castellated) pads on the bottom side of the module. These pads are also used to attach the module on the motherboard. All digital I/O signal levels are 2.8V CMOS compatible (except FORCE_ON and 32K/DR_INT that are 1.2V CMOS) and inputs are 3.6V tolerable. All unconnected I/O signals can be left unconnected when not used, unless instructed to use external pull up/down resistor.

Contact	Signal	I/O type Full Power, Standby	I/O type Backup	I/O type Reset	Signal description
1	32K/DR_INT	C1V1,B	C1V1,B	C1V1,B	- Reserved for wake-up interrupt (DR_INT default), PD. Can be left unconnected when not used. - Optionally 32678 Hz RTC clock output
2	UI_FIX	C,B	HZ	C,B	- Fix indicator output (default). Can be left unconnected when not used. - GPIO6
3	TX1	C,B	HZ	C,B	UART Port1 TX data transmit. Can be left unconnected when not used.
4	GND	G	G	G	Ground
5	GND	G	G	G	Ground
6	RX1	C,B	HZ	C,B	UART Port1 RX data receive (RTCM), PU. Can be left unconnected when not used.
7	EINT1	C,B	HZ	C,B	- Standby Mode control input (not supported). Can be left unconnected when not used. - GPIO13
8	VDD_B	P,I	P,I	P,I	Backup power input +3.0 V nom. De-couple externally with e.g. 1 uF low ESR ceramic capacitor.
9	VDD	P,I	-	P,I	Power supply input +3.3 V nom. De-couple externally with e.g. 4.7 uF low ESR ceramic capacitor.
10	GND	G	G	G	Ground
11	GND	G	G	G	Ground
12	GND	G	G	G	Ground
13	GND	G	G	G	Ground
14	GND	G	G	G	Ground
15	GND	G	G	G	Ground
16	ANT	A,O	-	-	Embedded Antenna Output (50 ohm)
17	RF_IN	A,I	-	-	Antenna Signal Input (50 ohm)
18	GND	G	G	G	Ground
19	GND	G	G	G	Ground
20	GPIO9	C,B	HZ	C,B	Reserved for future usage, leave floating.
21	GND	G	G	G	Ground
22	GND	G	G	G	Ground
23	RESET_N	C,I,PU	C,I,PU	C,I,PU	External reset input, active low. Can be left unconnected when not used.
24	GPIO10	C,B	HZ	C,B	Reserved for future usage, leave floating.
25	TX0	C,B	HZ	C,B	UART Port0 TX data transmit (NMEA)
26	RX0	C,B	HZ	C,B	UART Port0 RX data receive (NMEA), PU. Can be left unconnected when not used.
27	GND	G	G	G	Ground
28	FORCE_ON	C1V1,I	C1V1,I	C1V1,I	Power control input used to force wake up from low power modes. When not used connect to Ground externally.

Contact	Signal	I/O type Full Power, Standby	I/O type Backup	I/O type Reset	Signal description
29	PPS	C,B	HZ	C,B	- PPS Time Mark output signal (default) - GPIO7
30	WAKEUP	P,O	-	P,O	2.8V power output for optional control of external LNA bias switch, active high = LNA bias on. Max load current drain 2 mA. Can be left unconnected when not used.
31	GND	G	G	G	Ground

Table 2: Signal assignment

Legend: A=Analogue, B=Bidirectional, C=CMOS 2.8 V, C1V1=CMOS 1.1 V, G=Ground, HZ=High Impedance, I=Input, O=Output, OD=Output Open Drain, P=Power, PU=Internal Pull Up resistor, PD=Internal Pull Down resistor. Note that with Birectional I/O the firmware has control for input vs. output I/O type depending on the firmware function.

3.2 Power supply

The Fastrax UC530M module requires two separate power supplies: VDD_B for non-volatile back up block (RTC/Backup RAM) and the VDD for digital parts and I/O. VDD can be switched off when navigation is not needed but if possible keep the backup supply VDD_B active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Main power supply VDD current varies according to the VDD level, to the processor load, to the number of satellites is track and to the rate of satellite re-acquisition. Typical VDD peak current is 35 mA (typ.) during GNSS acquisition after power up and typical average 20 mA @ VDD 3.3 V over 24 h during good sky visibility. Note that average current drain will also increase during following features:

- 20 mA average (typ.) @1 Hz navigation, GPS+Glonass mode, good sky visibility
- +6 mA @ during first 5 minutes after cold and warm start due to increased frequency of acquisition and EASY background CPU load
- +5 mA @ 5 Hz navigation rate
- +10 mA @ 10 Hz navigation rate
- +1 mA @ Jammer Remover AIC usage

The following picture shows average current and power drain variation vs. VDD supply voltage.

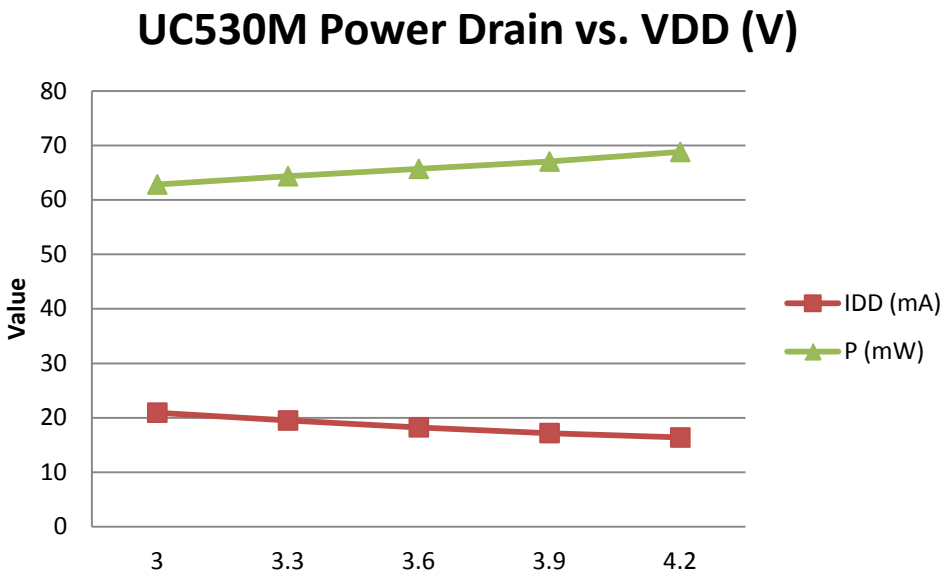

Figure 3: UC530M Power Drain (typ.) vs. VDD (V) @ 1 Hz

Back up supply VDD_B draws 10 µA typ. current in Backup State. During Full Power Mode VDD_B current typically peaks up to 60 µA and is on the average 40 µA.

☞ Backup supply VDD_B has to be active whenever Main supply VDD is active.

By-pass the VDD supply input by a low ESR ceramic de-coupling capacitor (e.g. 4.7 uF) placed nearby VDD pin to ensure low ripple voltage at VDD.

☞ De-couple the VDD input externally with e.g. 4.7uF low ESR ceramic capacitor connected to GND. The module has also internal a low ESR (~0.01 ohm) by-pass capacitor at VDD supply input. Ensure that the external regulator providing VDD and VDD_B supply is compatible with low ESR load capacitors.

3.3 Host port configuration

Default host port is UART and selected by leaving GPIO 9 and 10 signals floating (not connected) after power up. Other host port configurations are not supported.

3.4 Host port UART

UART Port 0 is normally used for GPS data reports and receiver control. Serial data rates are configurable from 4,800 baud to 921,600 baud by $PMTK251,<baud>*<checksum><CR><LF> command; ensure also that message payload fits in selected baud rate. Default baud rate is 115,200 baud; protocol is NMEA. RX signal is pulled up internally and can be left floating (not connected) when not used.

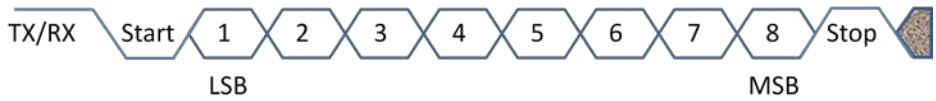

Figure 4: UART timing

Secondary UART Port 1 is configured to RTCM differential GPS data input at 9600 baud.

3.5 Reset input

The RESET_N (active low) signal provides external override of the internally generated power up/down reset. Normally external control of RESET_N is not necessary.

When RESET_N signal is used, it will force volatile RAM data loss. Note that Non-Volatile Backup RAM content is not cleared and thus fast TTFF is possible. The input has internal pull up resistor 75 kohm typ. and the signal can be left floating (not connected) if not used. Non-Volatile Backup RAM content can be cleared with NMEA command 'Factory Reset' $PMTK104*37<CR><LF>.

3.6 FORCE_ON input

The FORCE_ON signal provides input that can be used to force wakeup from low power modes. The signal is active high and shall be at high state at least > 800 ms for wakeup.

3.7 Antenna input

The module has an embedded GNSS antenna and the signal is further amplified by internal Low Noise Amplifier (LNA), which is available at ANT output. The antenna signal ANT shall be connected externally to RF_IN Antenna Input signal via a short trace between pads. The ANT signal is internally AC-coupled; max DC voltage at ANT

signal is +3.6 V. Note that RF_IN signal provides DC-path to ground and thus do not apply any bias voltage to RF_IN signal; max DC voltages at RF_IN signal is 0V and thus use an external series DC-block capacitor when needed.

The RF input signal path contains first a SAW band-pass filter before LNA, which provides excellent protection against out-of-band GPS blocking caused by possible near-by wireless transmitters.

3.8 External GPS antenna connectivity

The customer may use an external active GNSS antenna connected via an external RF-switch. It is suggested that the active antenna has a net gain *including cable loss* in the range from +10 dB to +30 dB. Specified sensitivity is measured with external low noise (NF≤1dB, G≥15dB) amplifier. The antenna shall provide simultaneous reception of both GPS 1575 MHz and Glonass bands 1598… 1606 MHz.

An active antenna requires an external antenna switch in order to select path between RF_IN input and external GPS antenna signal. For a reference example, see the application circuit diagram in chapter 6.2 Fastrax support can also provide other antenna switch reference circuits using discrete components.

The switch shall detect external active antenna presence for switching antenna signal path to external antenna by using e.g. the active antenna bias current detection. Second option is to use a suitable RF-connector with build-in switching operation. The external antenna switch must also provide a bias supply to the external active antenna and suggestion is also to add an external short circuit and ESD protection for antenna signal.

When the module is in Standby or Backup state, the antenna switch and bias can be switched off externally by using WAKEUP signal output, see e.g. Application Circuit Diagram.

3.8.1 Jamming Remover

Jamming Remover is an embedded HW block called AIC (Active Interference Cancellation) that tracks and removes up to 12 pcs CW (Carrier Wave) type signals up to -80 dBm (total power signal levels). By default the AIC is disabled and usage requires an NMEA command $PMTK286,1*23<CR><LF> to enable.

Jamming Remover can be used for solving EMI problems in the customer's system and it is effective against e.g. narrow band clock harmonics. When enabled, Jammer Remover will increase current drain by about 1 mA and impact on GNSS performance is low at modest jamming levels; however at high jammer levels -90… -80 dBm the RF signal sampling (ADC) starts to get saturated after which GPS signal levels start to reduce.

Note that Jamming Remover is not effective against wide band noise (e.g. from host CPU memory bus), which cannot be separated from thermal noise floor. Wide band Jamming signal increases effective noise floor and eventually reduces GNSS signal levels.

3.9 PPS output

The PPS output signal provides pulse-per-second output pulse signal for timing purposes. Pulse length (high state) is 100 ms and it has 1 us accuracy synchronized at rising edge to full UTC second with nominal GPS signal levels. The PPS will output PPS after a few seconds from first fix after the fix epoch is synchronized to full second.

The PPS output is valid when navigation is valid and will also continue 'freewheel' after valid fix is lost by a certain navigation DR timeout, typ. 10 seconds. User can also enable NMEA $GPZDA message that is sent right after the PPS pulse just sent.

3.10 Wakeup output

The WAKEUP output voltage provides indication to host that the module is active. Polarity is active high = module active.

WAKEUP output is intended to drive only CMOS inputs; do not load WAKEUP signal with current exceeding 2mA. Only loads with steady state current drain is allowed (i.e. loads with ripple currents are prohibited).

☞ Do not load WAKEUP output with current exceeding 2mA. Only loads with steady state current drain is allowed, i.e. loads with ripple currents are prohibited.

3.11 Interrupt input EINT1

The default EINT1 function is Standby mode control but the function is not supported; leave signal floating (not connected).

3.12 UI_FIX signal

The default UI_FIX function is valid fix indicator output. Without a valid fix the signal is at low state; during valid fix condition the signal outputs 0.1 s pulses every 1 second.

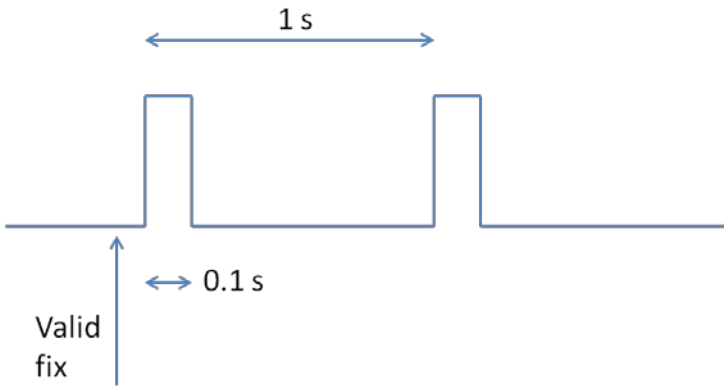

Figure 5: UI_FIX valid fix indicator timing

3.13 32K/DR_INT signal

The 32K/DR_INT signal is reserved for future usage as wake up interrupting input.

Optionally the signal can be configured to 32768 Hz RTC clock signal output with a custom firmware. The 32K/DR_INT signal has CMOS 1.1V logic levels and when input, the signal is +3.6V tolerable.

3.14 Mechanical Dimensions

Module size is 9.6 mm (width), 14.0 mm (length) and 1.95 mm (height, 2.25 mm max). General tolerance is ±0.3 mm. Note pin 1 polarity mark on the corner on the shield.

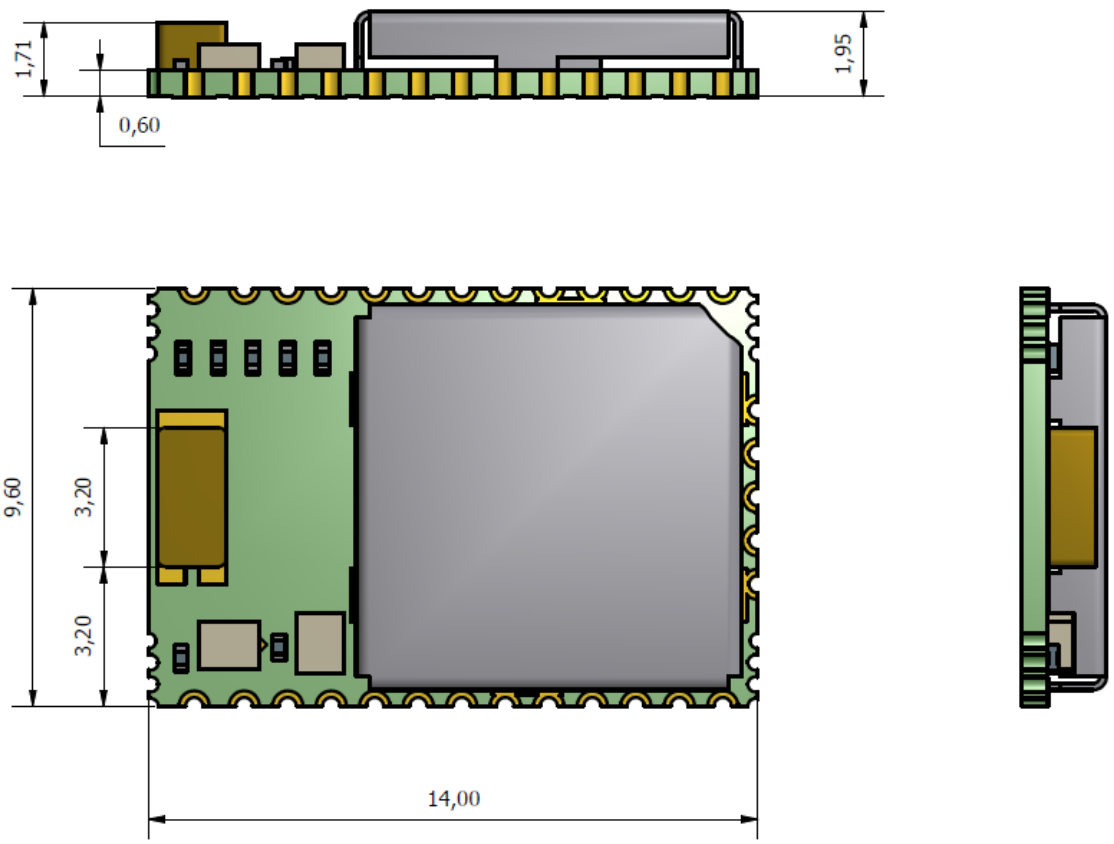

Figure 6: Mechanical dimensions

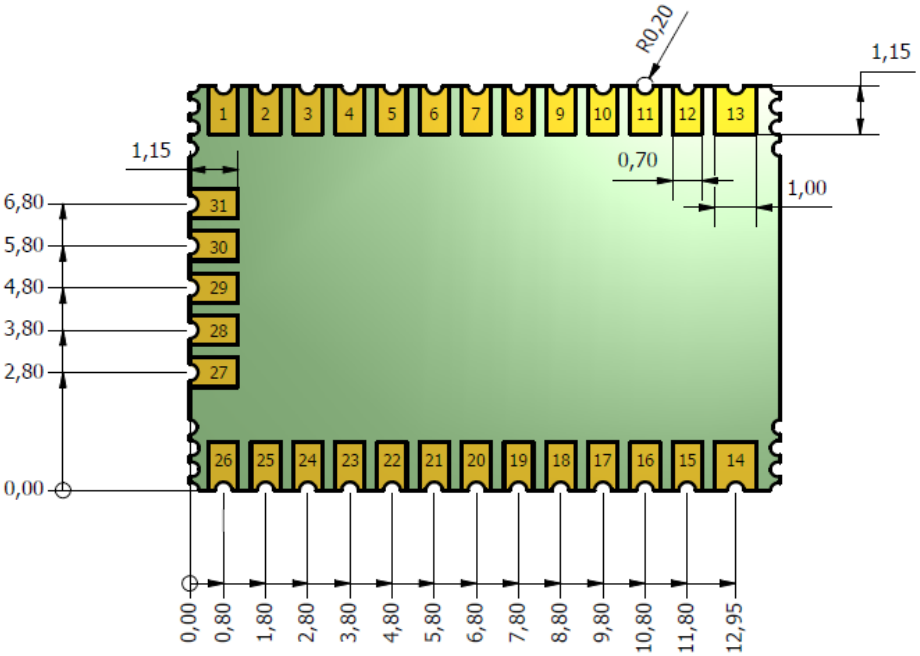

Figure 7: Pin numbering and dimensions, bottom view

3.15 Suggested pad layout

Suggested paste mask openings equal to pad layout. Note the keepout (void area) 4.8x7.2mm for copper & trace & components for all layers under the embedded antenna.

☞ See chapter 6.3 for layout suggestions to ensure proper embedded antenna operation, which requires solid ground plane around the module.

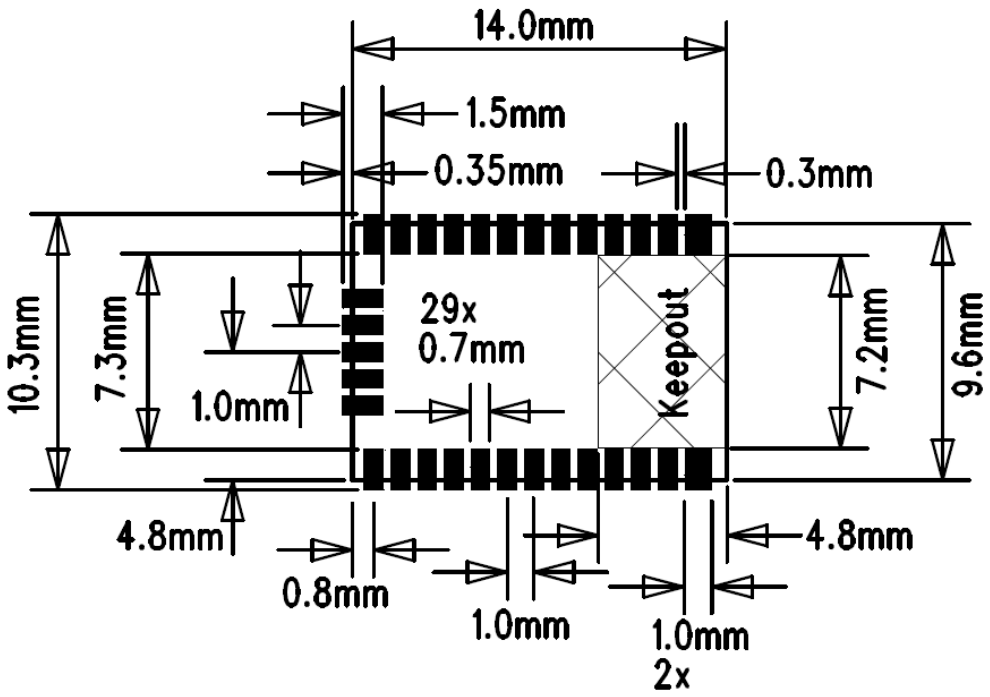

Figure 8: Suggested pad layout and occupied area, top view

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. Operation beyond the DC Electrical Specifications is not recommended and extended exposure beyond the Recommended Operating Conditions can affect device reliability.

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating and storage temperature	-40	+85	°C
P_{DIS}	Power dissipation	-	200	mW
VDD	Supply voltage input	-0.3	+4.3	V
VDD_B	Supply voltage input, Backup	-0.3	+4.3	V
V_{RF_IN}	DC Voltage at RF_IN input signal	-	0	V
V_{ANT}	DC Voltage at ANT output signal	-0.5	+3.6	V
V_{IO}(ESD)	I/O ESD voltage	-1000	+1000	V
P_{RF}	RF_IN input power (in band 1565… 1616 MHz)	-	-40	dBm
P_{RF}	RF_IN input power (out of band <1460 MHz or >1710 MHz)	-	+15	dBm

Table 3: Absolute Maximum Ratings

Note that module is an Electrostatic Sensitive Device (ESD).

4.2 DC Electrical specifications

Operating conditions are T_{AMB} =+25°C, VDD =+3.3 V, VDD_B =+3.0 V unless stated otherwise; navigation at 1 Hz.

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Operating temperature *(note 1)*	-40	+25	+85	°C
VDD	Supply voltage input	+3.0	+3.3	+4.3	V
VDD_B	Supply voltage input, Backup	+2.0	+3.0	+4.3	V
I_{VDD} (peak)	Supply current VDD, peak acq.		35		mA
I_{VDD} (ave)	Supply current VDD average, tracking		20		mA
I_{VDD} (Backup)	Supply current VDD, Backup Mode		3		µA
I_{VDD_B} (peak)	Supply current VDD_B, peak		60		µA
I_{VDD_B} (ave)	Supply current VDD_B, average		40		µA
I_{VDD_B} (Backup)	Supply current VDD_B, Backup State		10		µA
I_I(LEAK)	Leakage current, Digital Input	-10		+10	µA
V_{OL}	Low level output voltage, IOL 2 mA	-0.3		+0.4	V
V_{OH}	High level output voltage, IOH 2 mA	+2.4	+2.8	+3.1	V
V_{IL}	Low level input voltage	-0.3		+0.8	V
V_{IH}	High level input voltage	+2.1		+3.6	V
R_{PU}	Internal Pull Up resistor	40	85	190	kohm
R_{PD}	Internal Pull Down resistor	40	85	190	kohm

Table 4: DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Low level output voltage, IOL 0.9 mA			+0.165	V
V_{OH}	High level output voltage, IOH 0.9 mA	+0.78			V
V_{IL}	Low level input voltage	-0.3		+0.275	V
V_{IH}	High level input voltage	+0.935		+3.6	V
R_{PU}	Internal Pull Up resistor	130		560	kohm
R_{PD}	Internal Pull Down resistor	130		560	kohm

Table 5: DC electrical characteristics, 1.1 V CMOS domain (FORCE_ON & 32K/DR_INT)

4.3 AC Electrical characteristics

Operating conditions are T_{AMB} =+25°C and VDD =+1.8 V unless stated otherwise.

Symbol	Parameter	Min	Typ	Max	Unit
t_{PPS}	PPS cycle time		1		s
$t_{PPS,H}$	PPS, high state pulse length		200		ms
Δt_{PPS}	PPS accuracy, rising edge (note 1)	-1		+1	µs
f_{RTC}	RTC output (32K/DR_INT) frequency (note 2)		32.768		kHz

Table 6: AC electrical characteristics

Note 1: with nominal GNSS signal levels -130dBm.
Note 2: when enabled by I/O configuration.

5 Manufacturing

5.1 Assembly and Soldering

The UC530M module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150… 180°C for 60… 120 sec. Suggested peak reflow temperature is 235… 245°C (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260°C. For details, see Fastrax document *Reflow Soldering Profile* [2].

☞ Note that module is Electrostatic Sensitive Device (ESD).

Avoid also ultrasonic exposure due to internal crystal and SAW components.

The UC530M module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

5.2 Moisture sensitivity

UC530M module is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag self life is 1 year; thus it is suggested to assemble modules prior self life expiration. If the moisture barrier bad self life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

5.3 Marking

Module marking includes type code, batch code and serial number.

Type code is e.g. **UC530Mrbbbb** (may vary)**,** where

- **UC530M** is module type code
- **r** is incremental firmware revision (e.g. **A,** may vary)
- **bbbb** is BOM (Bill-of-Materials) revision code (e.g. **4355**, may vary)

Batch code is e.g.**120208** (may vary)**,** where

- **1** is factory code
- **2** is last digit of the year (e.g. 201**2**)
- **02** is month (e.g. February)
- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, Julian date code and incremental number.

5.4 Tape and reel

Reel is packed in 500 pcs per reel.

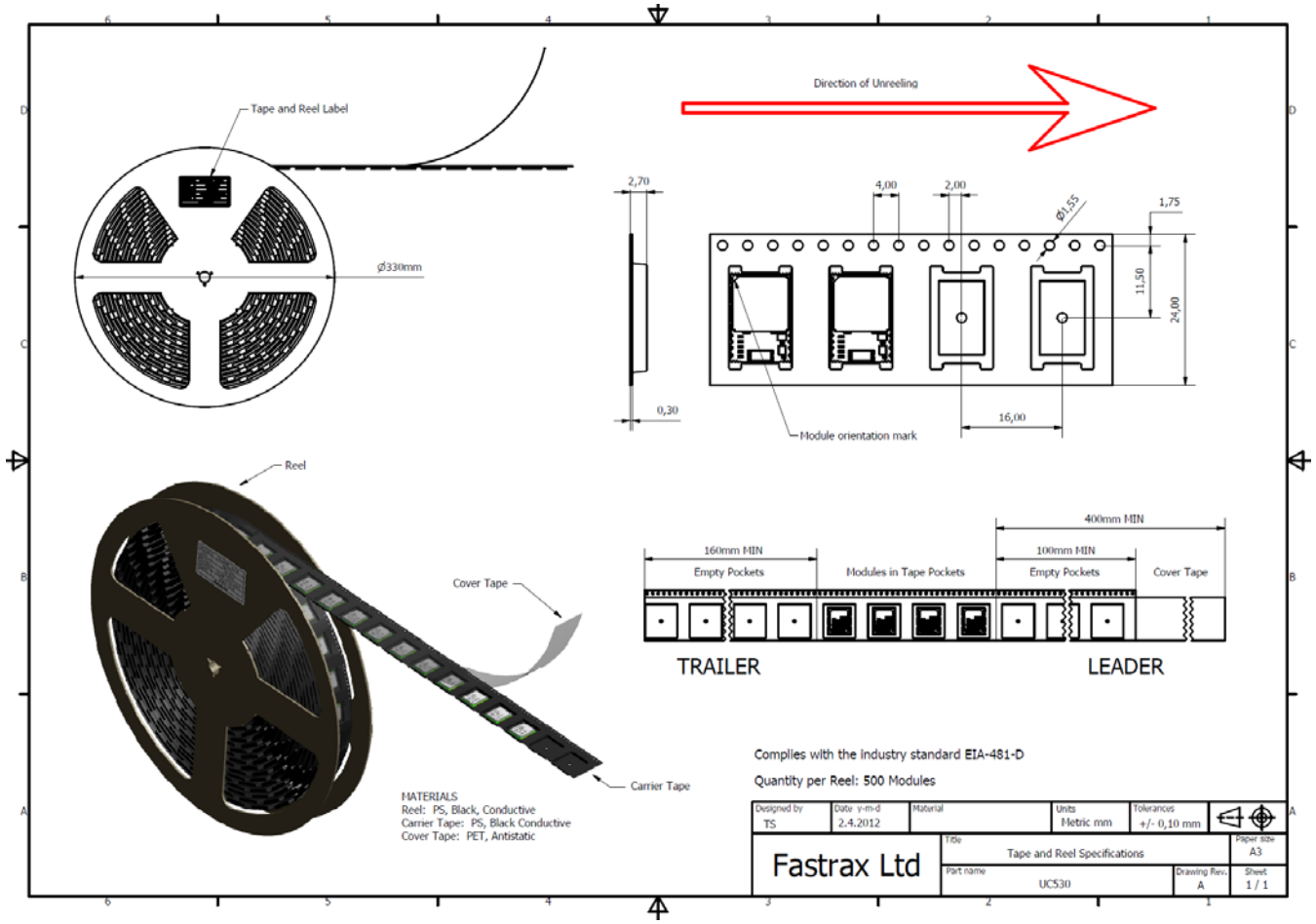

Figure 9: Tape and reel specification

5.5 Environmental Specification

The UC530M module shall be qualified for environmental stresses with the following test series:

Test	Condition	Standard
Temperature Cycle	Test: +85°C (20min) / -40°C (20min), Ramp Slope: 10°C/min, Test Cycles: 300 Cycles	JESD22A104
High Temperature Storage	Temperature +85°C , Test Time: 1,000hr	JESD22A103C
Temperature Humidity Test	Temperature +85°C , 85% R.H., Test Time: 1,000hr	JESD22A101
Vibration Test	10G, 10… 1,000Hz, 1 Octave/min (amplitude 1.0mm max @ <70Hz)	JESD22B103
Shock Test	100G pulse, duration 2ms, 5 Shock 2 directions 3 Axis = 30 Shocks	JESD22B110

Table 7: Environmental tests

6 Reference design

The idea of the reference design is to give a guideline for the applications using the OEM GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GPS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

6.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the UC530M module, which is powered by the main VDD supply (+3.3 V typ.) and backup supply VDD_B (+3.0V typ) powered by battery BT1. The external by-pass capacitor C1 and C2 is used to de-couple the supply inputs placed close to the pin.

Suggestion is to keep the backup supply VDD_B active all the time and host may use the VDD supply to control module activity between Full Power and Backup operation modes. When needed the VDD can be connected directly to a LiPo battery but in this case the backup battery BT1 must be charged from a separate 3V supply.

Embedded Antenna Signal (ANT) must be routed to RF-input (RF_IN) via a short trace between pads 16 and 17.

The host port is configured to UART by keeping GPIO 9 & 10 floating. Serial port TX output is connected to host UART input. RX input connection to host UART output is required when sending commands to UC530M. UART signals are decoupled with series resistors R1 and R2 in order to minimize risk for internal EMI.

The reference circuit supports also connectivity to UC530 (GPS only) module variant for optional Backup/Periodic modes of operation: with UC530 the external power switch U1, R8 and D2 shall be assembled while omitting by-pass resistor R7 & R9 (0R). The U1 power switch is controlled autonomously by the TIMER signal from UC530; for details see also UC530 datasheet. This way user may share the same electrical design with both UC530 and UC530M module variants.

Optional connectivity to host includes PPS, UI_FIX, 32K/DR_INT signals. UART Port 1 RX1 signal can be used optionally as input for RTCM differential GPS messages.

Note that all I/O signal levels are CMOS 2.8V compatible (excluding FORCE_ON and 32K/DR_INT signals that have 1.2 V CMOS domain) and inputs are 3.6 V tolerable.

Some I/O signals have series resistors 47… 220 ohm, which are intended for RF-decoupling purposes to improve rejection to internally generated EMI that may leak to embedded GPS antenna.

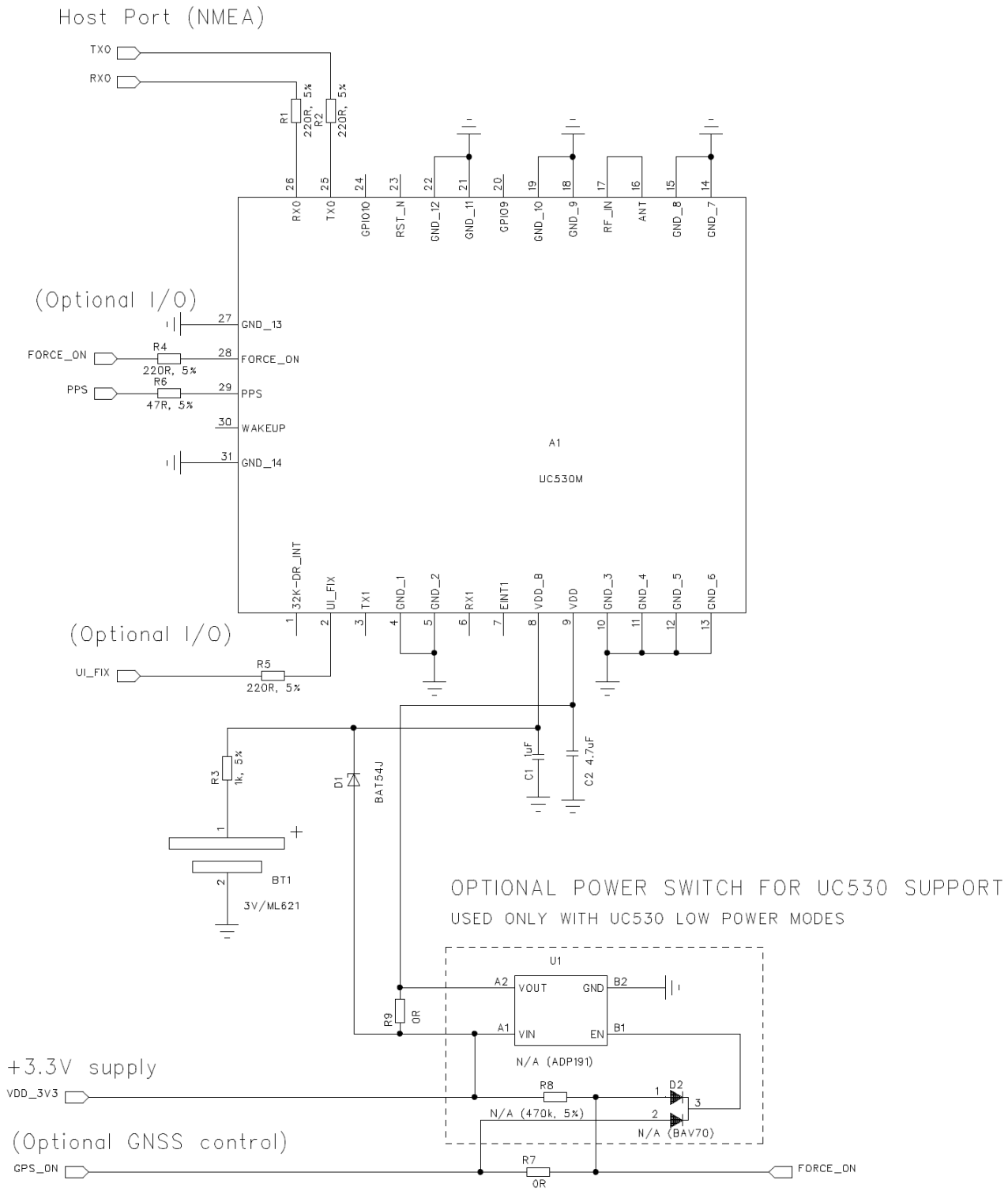

Figure 10: Reference circuit diagram, minimum connectivity

6.2 Reference circuit diagram, external antenna connectivity

The following reference circuit adds external GPS antenna connectivity by using a RF-connector (e.g. MCX) + Switch combo (e.g. Aliner 36-301AA), which detects the external antenna by the presence of the mating connector plugged and then switching RF signal path from external antenna at J1 to RF_IN.

The TVS diode D1 (e.g. Infineon ESD0P2RF) provides optional protection against static discharge (ESD) at J1. The transistor Q1 provides antenna bias switch function to switch bias voltage off during Standby and Backup modes and which is controlled by the WAKEUP signal. The Q1 provides also short circuit protection and limits bias current to 50… 60 mA typ.

WAKEUP signal can be used to drive external antenna bias ANT_BIAS (+3.3 V typ.) voltage switch (Q1) during Full Power/Standby/Backup Modes. L1 and C5 provide RF decoupling at VDD_ANT supply.

Keep RF signal traces to J1 short in order to minimize losses and keep transmission line impedance at 50 ohm, see next chapter.

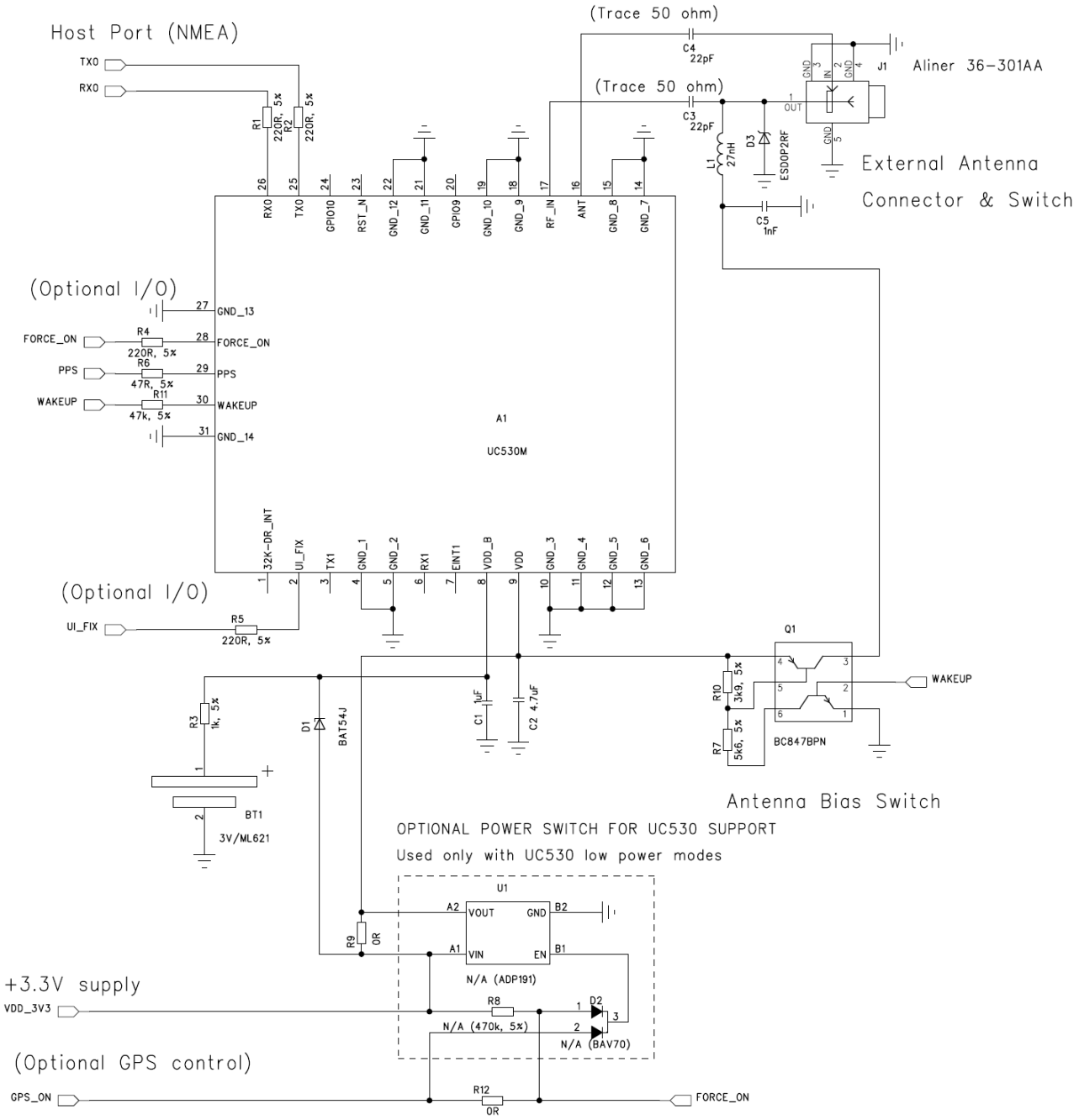

Figure 11: Reference circuit diagram, external antenna connectivity

6.3 PCB layout suggestion

The suggested 4-layer PCB build up is presented in the following table.

Layer	Description
1	Components + Ground plane (opening under UC530M antenna)
2	Signals and RF trace (opening under UC530M antenna)
3	Ground and power planes, signals (opening under UC530M antenna)
4	Ground plane, also short traces allowed (opening under UC530M antenna)

Table 8: Suggested PCB build up

The UC530M module is intended to be assembled at the top edge of the mother board. The embedded antenna operation relies on the ground plane on the mother board; optimum size is 80x40mm but larger or smaller ground plane can be used. Suggested minimum ground plane size is 45x20mm. Optimum placement is at the center of the top edge but offset placement is allowed by keeping at least 10mm distance to nearest ground plane edge.

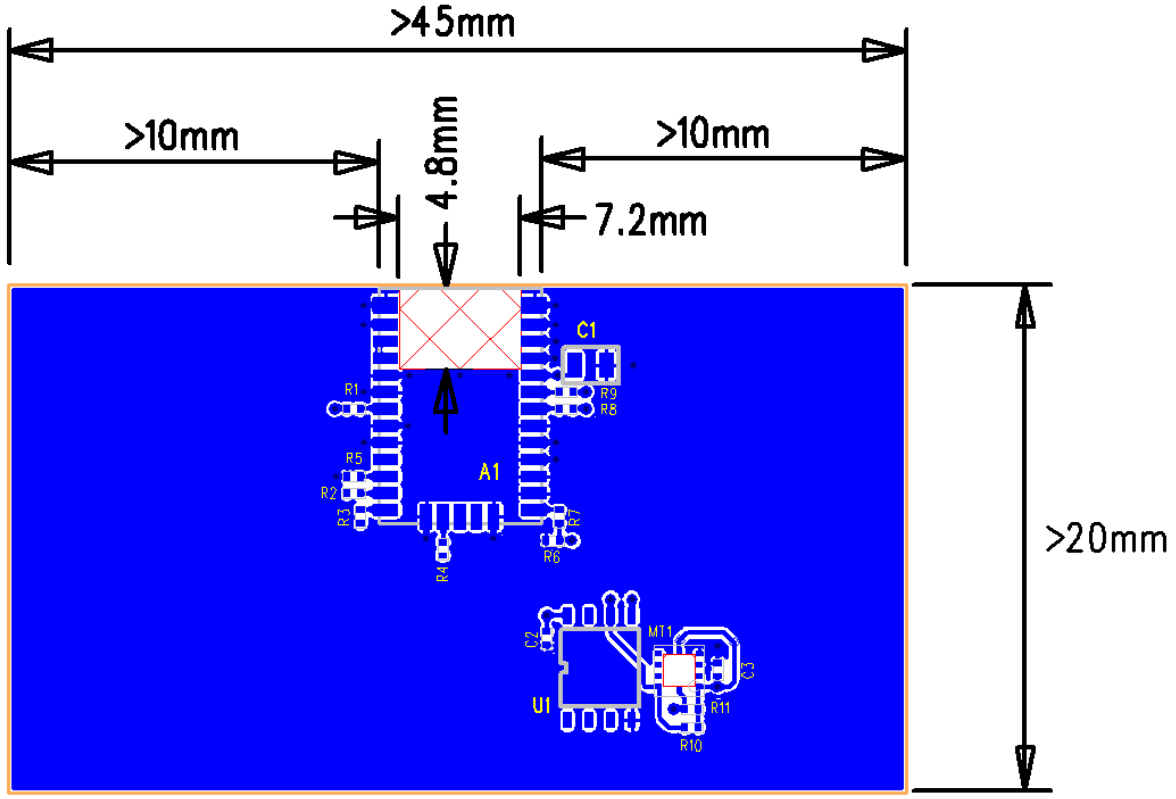

Figure 12: Mother board ground plane and UC530M placement

Note keepout 4.8x7.2mm under the embedded antenna. Follow also GND via hole suggestive locations.

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and assigned to ground plane (copper plane), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be minimized.

Note that the embedded GPS antenna requires a small ground plane clearance and void area (keep out 4.8x7.2mm) for copper plane & trace for all layers under the antenna. Placement of other components is not allowed under the keep out on opposite side.

For a multi-layer PCB the inner layers below the UC530M is suggested to be dedicated signal traces and copper plane for the rest of the area. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed as close to the UC530M module as possible. In this way the risk for the EMI leakage is minimized. For the same reason by-pass supply capacitors should be connected very close to the module with short traces to IO contacts and to the ground plane. Place a GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the UC530M to ground plane with short traces (thermals) to via holes, which are connected to the ground plane. Use preferably one via hole for each GND pad.

A RF signal is suggested to be routed clearly away from other signals between two ground planes as a Stripline Transmission Line; this minimizes the possibility of interference and coupling. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate, width of the signal trace and the height (separation) of the two ground planes. With FR-4 material the width of the trace shall be about 30% of the ground plane height. E.g. 0.4mm ground plane height results to 0.15mm trace width with FR-4 substrate.

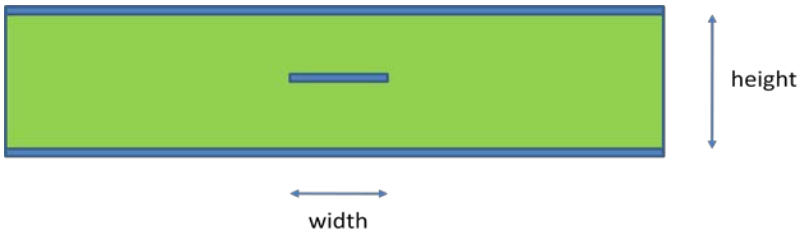

Figure 13: Stripline transmission line

Any board space free of signal traces should be covered with copper areas connected to ground net; in this way a solid RF ground plane is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend (wrap) during the PCB manufacturing or reflow soldering. Bending and wrapping may cause soldering failures and reduce end product reliability.

The AC530M Application Board layout described in next chapter can be also used as layout reference implementation.

Also a 2-layer PCB motherboard design is possible in order to reduce PCB cost but the layout design must be made carefully to fulfill ground plane minimum size requirements. The following pictures show suggested 2-layer GND plane and signal trace routing.

Notes on a 2-layer PCB motherboard design:

- Keep Bottom side ground plane as solid as possible; at least the minimum recommended 45x20mm
- Route signal traces away from the module on Top layer
- When necessary allow signal swap from Top to Bottom layer clearly away from module >20 mm
- Use copper pour ground planes on Top and Bottom layers; use multiple GND net via holes to tie separate ground plane areas tightly together

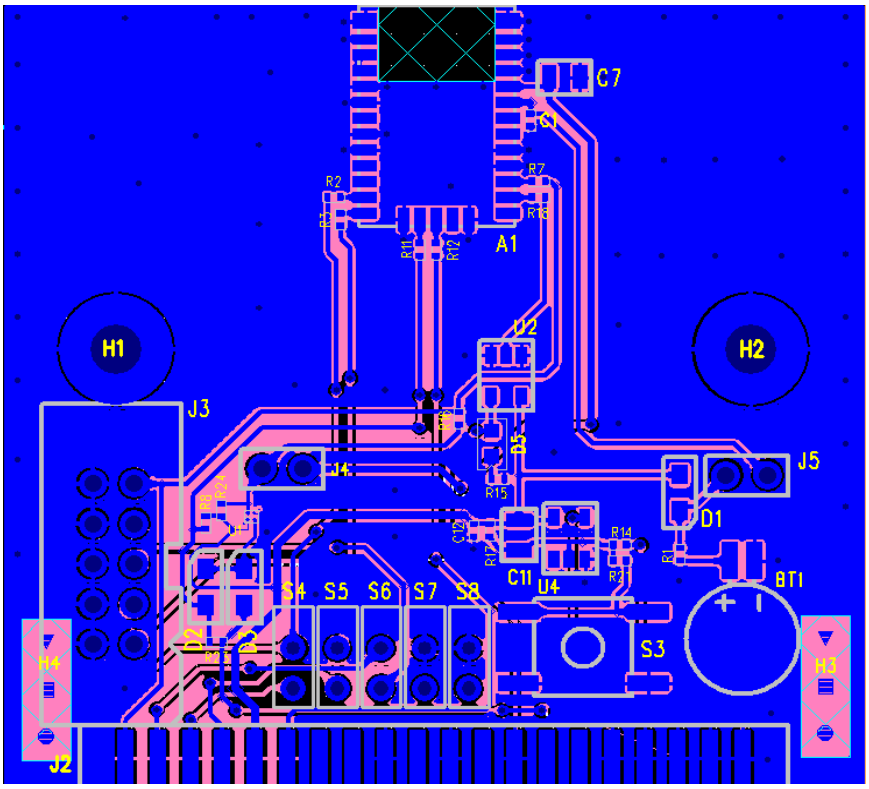

Figure 14: Example of 2-layer PCB, Top layer

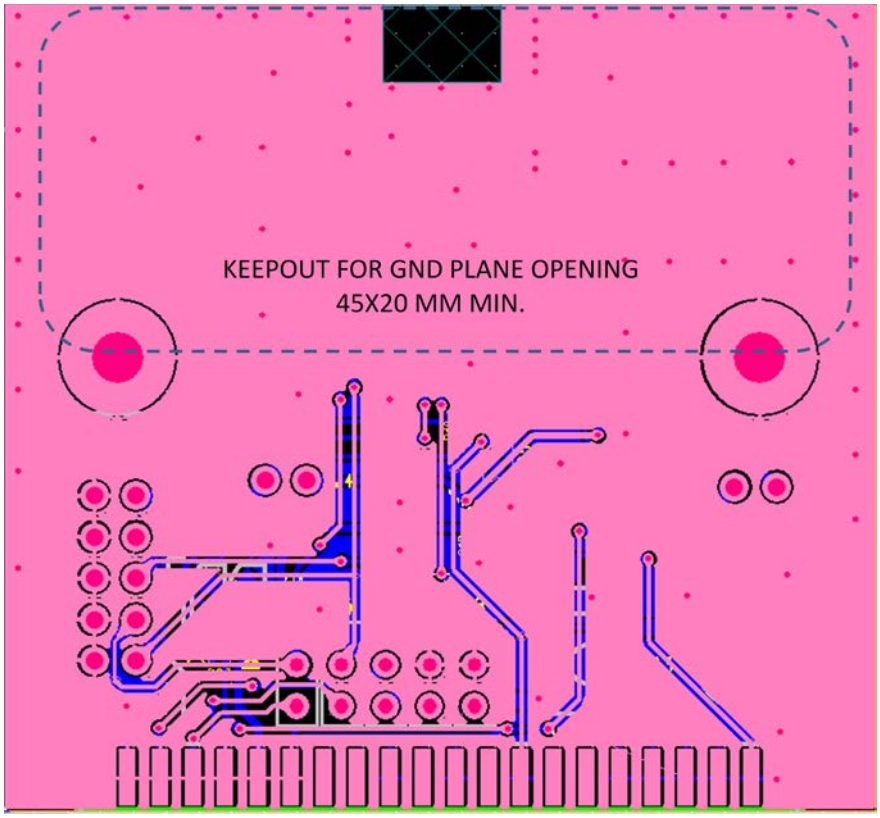

Figure 15: Example of 2-layer PCB, Bottom layer

6.3.1 Other electronics on mother board

Signal traces on top and bottom layers should have minimum length. Route signals mainly at inner layers below the top or bottom ground plane. In this way, a solid RF ground is achieved throughout the circuit board on top and bottom sides. Several via holes should be used to connect the ground areas between different layers.

Areas with dense component placing and dense routing requirements should be covered with a metal shield, which should be connected to ground plane with multiple GND via holes. Small ground plane openings for SMT components (length few mm, like LED or push buttons) in the ground plane are OK without a shield.

Dense areas having multiple via holes may open the ground plane for wide areas, thus blind and buried via holes are suggested to be used when changing layers for internal signals and power planes.

Use a power plane layer dedicated solely for power nets. Use wide trace width or even copper plane areas to achieve low impedance for power nets. Dedicate at least one layer as ground planes on adjacent layer above or below power plane layer in order to maximize capacitance to ground plane.

6.3.2 Avoiding EMI

Any GPS receiver is vulnerable to external spurious EMI signals since GPS signals are very weak below thermal noise floor. Any man made noise or spurious signals picked up by the nearby GPS antenna increases the noise floor and reduces GPS signal levels. Carrier Wave (CW) type spurious signals like clock harmonics on GPS band may also cause cross correlation products that may interfere with GPS signal tracking and cause position offsets.

The embedded GPS antenna may pick up local EMI signals and thus it is essential for good GPS performance that the following measures against EMI are properly implemented:

- High speed electronics like host CPU & memory bus are enclosed in a 'Faraday shield'. The electrical enclosure is formed by the ground planes on PCB + metal shield over components. Route signals at inner layers as discussed previously. Use preferably a power plane(s) layer for supply nets.
- Any signal that is routed outside the Faraday shield is protected against EMI noise on 1575MHz with a serial RF filter like
    - a serial resistor (> 330ohm, suitable for I/O with low current)
    - with a dedicated EMI filter (or ferrite bead) suitable for higher current
    - with suitable by-pass capacitor e.g. 18pF (low impedance due to series resonance at 1575MHz).

The following picture gives a suggestion for e.g. a 6-layer PCB build up, which forms a Faraday shield together with ground planes on PCB and with the shield over high speed electronics. Buried and blind via holes are used to keep EMI signal inside ground planes. I/O signals that are routed outside the Faraday enclosure are filtered with a suitable EMI filter. Power plane layer is used for supply nets with low impedance traces/planes.

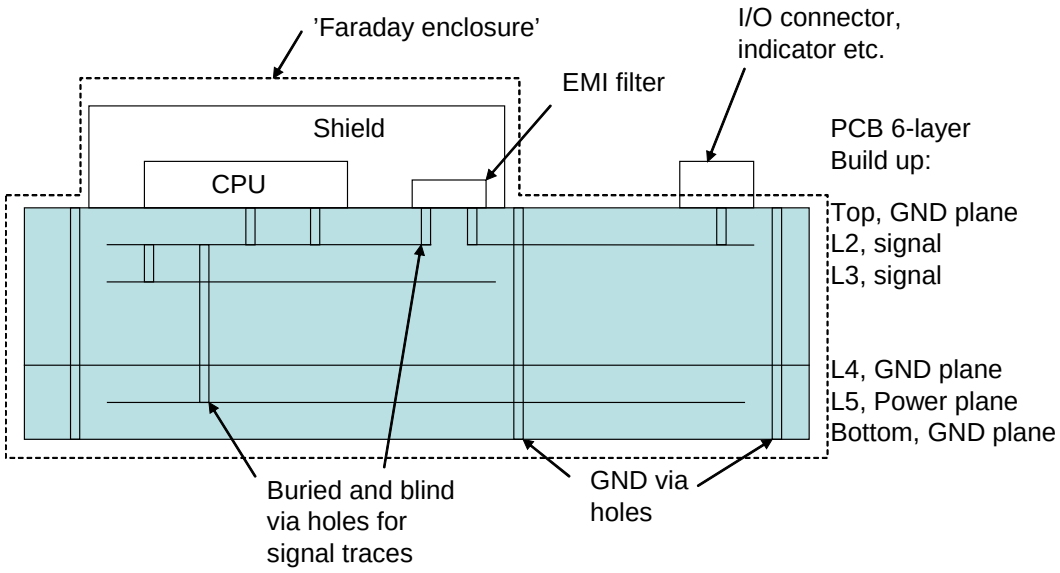

Figure 16: Avoiding EMI with Faraday enclosure

6.4 Embedded antenna operation

The embedded GPS antenna provides optimal radiation efficiency 80% typ. with 80x40mm ground plane. The antenna provides linear polarization with peak gain 1.1dBi and radiation pattern optimized for portable devices. The antenna is insensitive to surroundings and has high tolerance against frequency shifts. However on small ground plane widths the antenna gain and radiation efficiency reduces, e.g. the AC530M application board having 53mm width reduces signal levels by 2dB when compared to full 80x40mm ground plane dimensions. Radiation pattern of the embedded GPS antenna is shown in the picture below (on 80x40mm ground plane).

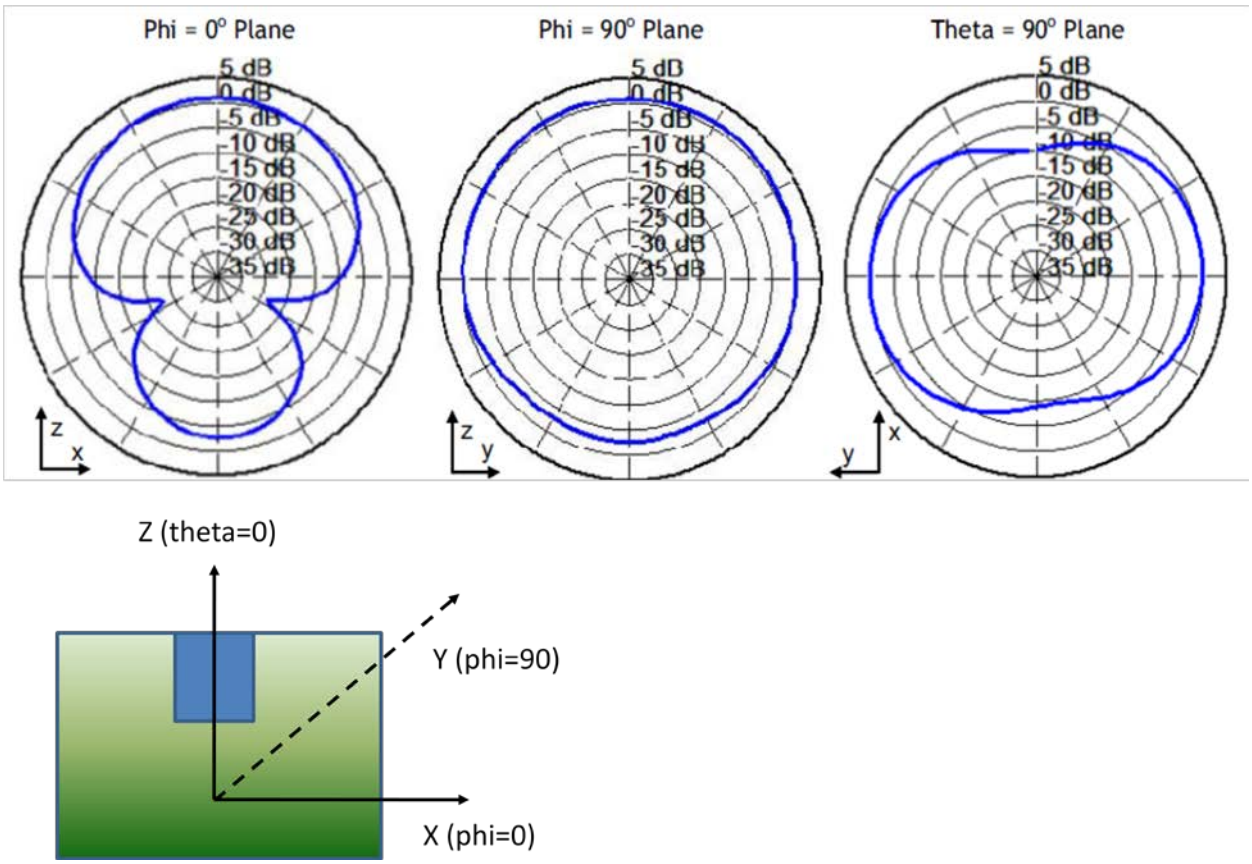

Figure 17: Radiation pattern of the embedded antenna, 80x40mm ground plane

Avoid placement of the module at a corner of the mother board. This will reduce radiation efficiency and cause frequency shifts. Optimal placement is at center of top edge; keep at least 10mm distance to nearest ground plane corner.

Placement of tall nearby components (h>3mm) should keep minimum d=6mm distance to the embedded antenna. Also any adjacent conductive metal plane should have d=6mm distance to the top edge of the module. Enclosure or plastic cover should have minimum d=1.5mm distance to the antenna.

Placement near human body (or any biological tissue) is accepted by keeping minimum d=10mm distance between mother board and the body. With smaller distances to the body, the radiation efficiency of the antenna will start to reduce due to signal losses in biological tissue. E.g. d=5mm to biological tissue will reduce GPS signal levels by about 6dB. Note also that the body will act also as a reflector and thus radiation pattern will point perpendicular to the body.

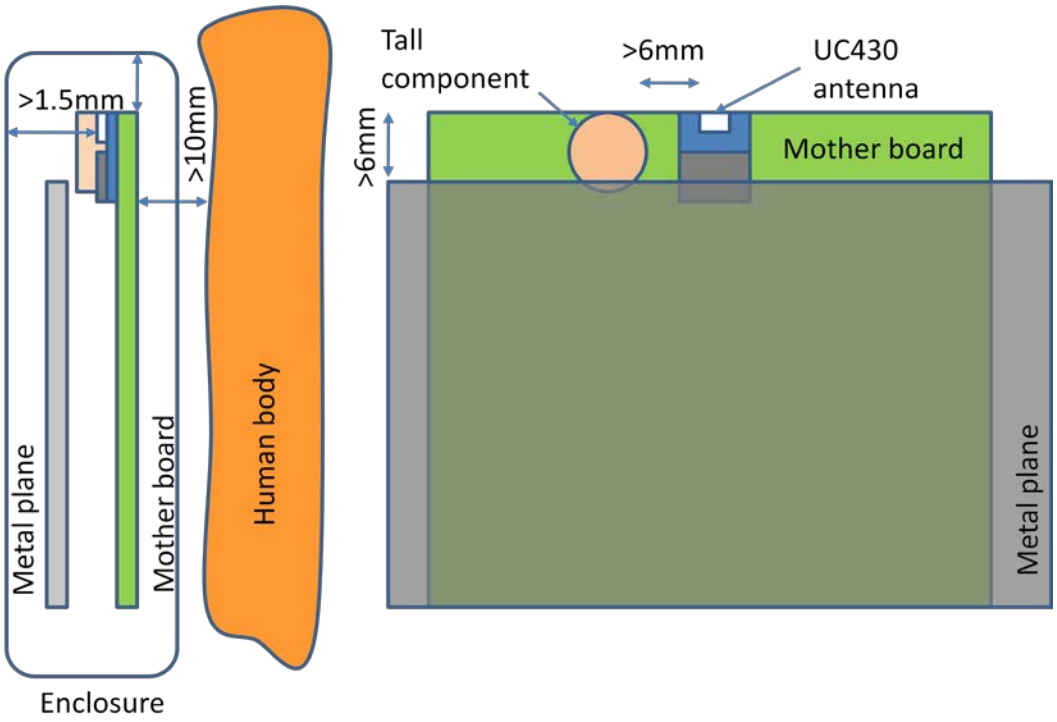

Figure 18: Placement of UC530M relative to surroundings

7 AC530M Application board for UC530M

The Fastrax Application Board AC530M provides the UC530M connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the UC530M module, MCX antenna connector, Antenna Bias +3.3 V switch, VDD Power Switch, switch for GPS_ON control and 2x20 pin Card Terminal connector.

Default host port configuration is set to UART by switch S4… S6 'ON' and S7 & S8 'OFF'.

7.1 Board Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. Note that UART Port 0 maps to serial Port 0 at the Fastrax Evaluation Kit. I/O signal levels are CMOS 3.3V compatible unless stated otherwise.

Pin	Signal	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
1	TX1	O	-	UART Port 1 async. output
2	GND	-	-	Ground
3	RX1	I	-	UART Port 1 async. input (RTCM)
4	GND	-	-	Ground
5	TX0	O	-	UART Port 0 async. output (NMEA)
6	GND	-	-	Ground
7	RX0	I	-	UART Port 0 async. input (NMEA)
8	GND	-	-	Ground
9	VDD_3V3	I	-	Power supply input +3.3V
10	GND	-	-	Ground
11	PPS	O	-	1PPS signal output
12	GND	-	-	Ground
13	RESET_N	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	-	I	-	Not connected
17	GND	-	-	Ground
18	-	-	-	Not connected
19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	-	-	-	Not connected
24	-	-	-	Not connected
25	GND	-	-	Ground
26	UI_FIX	O	-	UI indicator B output
27	-	-	-	UART CTS signal
28	-	-	-	Not connected
29	-	-	-	UART RTS signal
30	WAKEUP	O	-	UI indicator A output
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	I	-	Not connected
35	GND	-	-	Ground
36	EINT1	I	-	EINT1 (Standby) control input
37	GND	-	-	Ground

Pin	Signal	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
38	32K/DR_INT	I/O	-	Default: DR_INT wakeup control input
39	GND	-	-	Ground
40	GPS_ON_N	I	-	Inverted GPS_ON control input, pulled up to VDD_3V3

Table 9: Board terminal signals

7.2 Bill of materials

REF	TECHNICAL DESCRIPTION	VALUE
A1	UC530 MODULE	UC530M
BT1	PANASONIC ML621/F9D, 3V 5mAh	3V/ML621
C1	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
C2	Capacitor chip, 22pF 50V 5% NP0 0402	22pF
C3	Capacitor chip, 1nF 50V 10% X7R 0402	1nF
C4	Capacitor chip, 22pF 50V 5% NP0 0402	22pF
C7	4,7uF 6,3V X5R 0805 +20%	4u7F
C11	4,7uF 6,3V X5R 0805 +20%	4u7F
C12	Capacitor chip, 1uF 6.3V +20% X5R 0402	1uF
D1	Diode 40V 225mA, BAT54J	BAT54J
D2	Diode 40V 225mA, BAT54J	N/A
D3	Diode 40V 225mA, BAT54J	N/A
D4	LED Red	TLSU1008
D5	LED Red	TLSU1008
J1	Aliner Industries Inc, MCX connector with switch	Aliner 36-301AA
J2	EDGE MOUNT SOCKET STRIP 40 PINS	2x20 edge
J3	2x5 pin-header, straight, 2.54mm	2x5P2.54
J4	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J5	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
L1	Coil chip, 27nH 0402C +5%, 300mA, Q>60 @ 1.7GHz	27nH
PCB1	Application board for UC530 rev B	PCB/AC530B00
Q1	BC847B	BC847B
R1	Resistor chip, 1k 5% 0402 63mW	1k, 5%
R2	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R3	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R4	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R5	Resistor chip, 47R 0402 63mW 5%	47R, 5%
R6	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R7	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R8	Resistor chip, 1M 5% 0402 63mW	N/A
R9	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R10	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R11	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R12	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R13	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R14	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R15	Resistor chip, 470R 5% 0402 63mW	470R, 5%
R16	Resistor chip, 10k 5% 0402 63mW	N/A
R17	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R18	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R19	Resistor chip, 3.9k 5% 0402 63mW	3k9, 5%
R20	Resistor chip, 5k6 5% 0402 63mW	5k6, 5%
R21	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R22	Resistor chip, 47k 5% 0402 63mW	47k, 5%
R23	Resistor chip, 0R 0402	0R
R24	Resistor chip, 0R 0402	0R

R26	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R27	Resistor chip, 10k 5% 0402 63mW	10k, 5%
S1	Jumper, Pitch, 2.54mm, Red colour	J4/P1-P2
S2	Label 13x16mm iTrax03s	STICKER13x16
S3	Switch, SMD PUSH BUTTON	SW
S4	Switch, on-off	SW JMP 2P54
S5	Switch, on-off	SW JMP 2P54
S6	Switch, on-off	SW JMP 2P54
S7	Switch, on-off	SW JMP 2P54
S8	Switch, on-off	SW JMP 2P54
S9	Jumper, Pitch, 2.54mm, Red colour	J5/P1-P2
U1	POWER SWITCH 0.1 ohm	N/A
U2	Logic buffer	NC7SZ125
U4	Schmit-Trigger inverter	NC7SZ14M5X

Table 10: Bill of materials

7.3 AC530M Circuit diagram

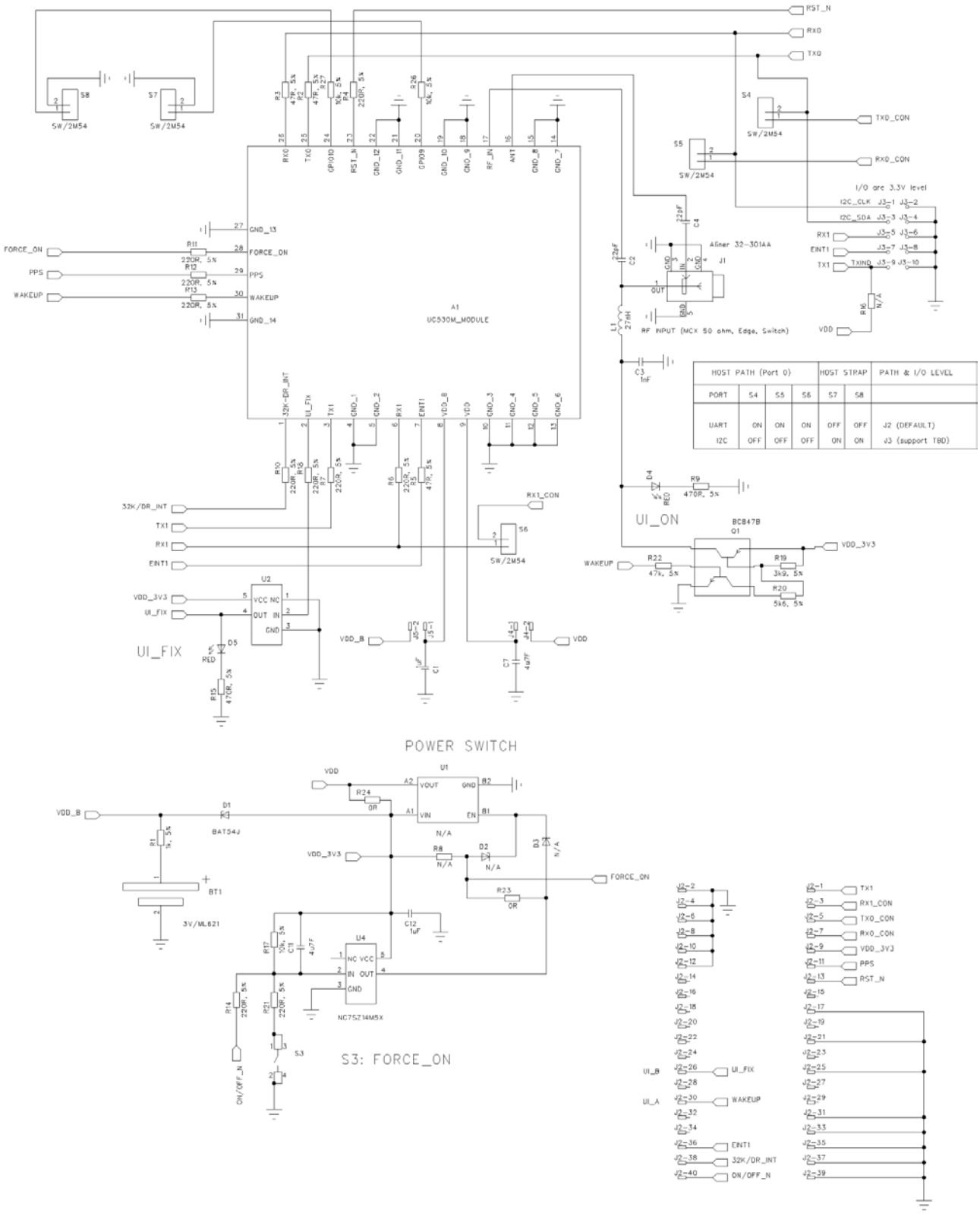

Figure 19: AC530M Circuit diagram

7.4 AC530M layout and assembly

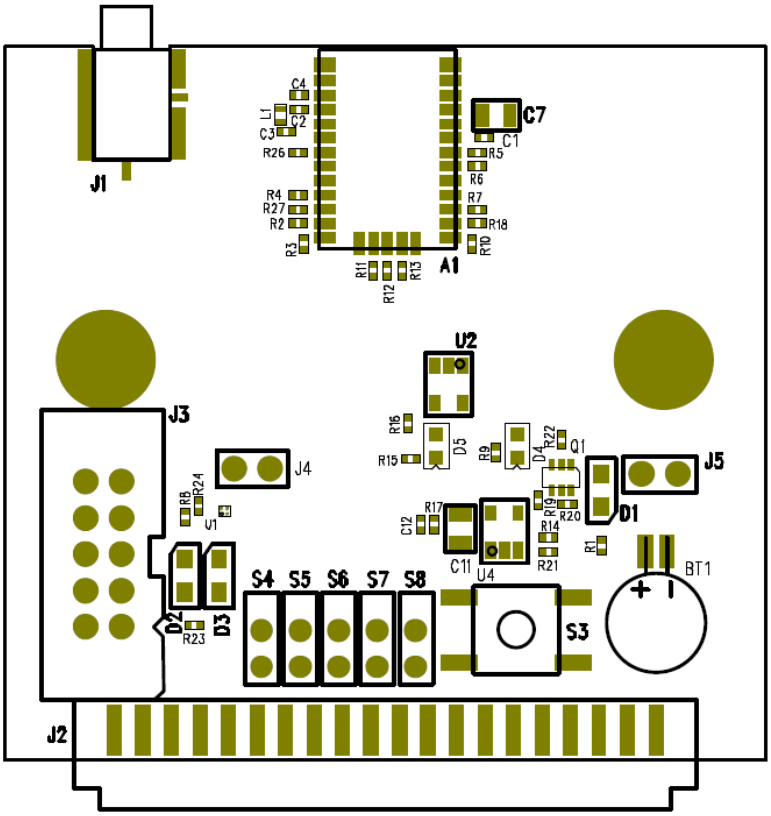

Figure 20: Assembly drawing, top side

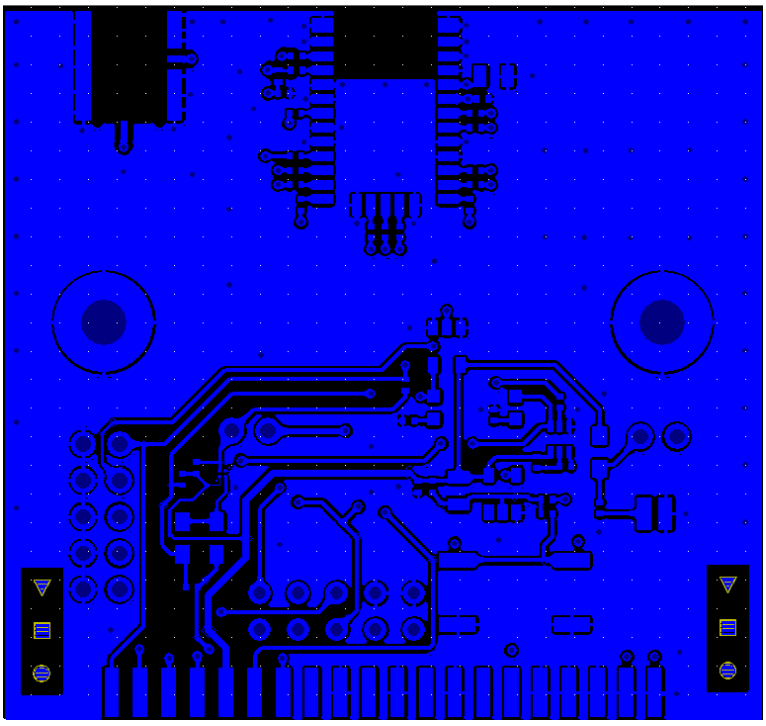

Figure 21: Layer 1, (top)

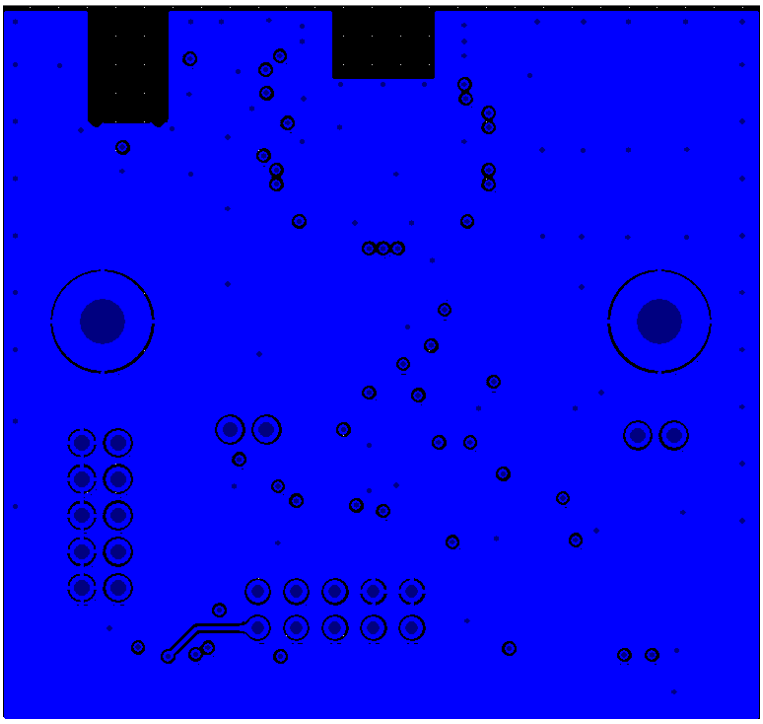

Figure 22: Layer 2

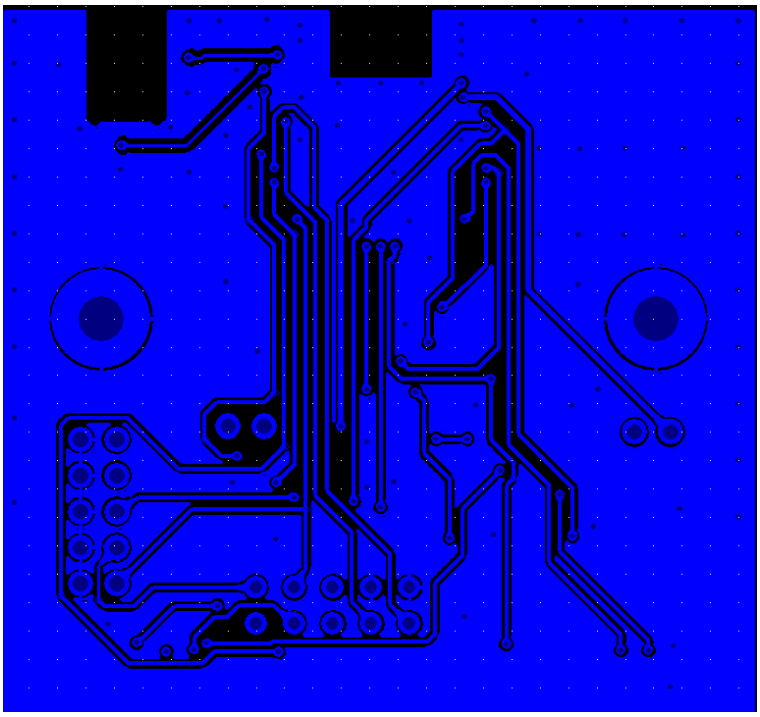

Figure 23: Layer 3

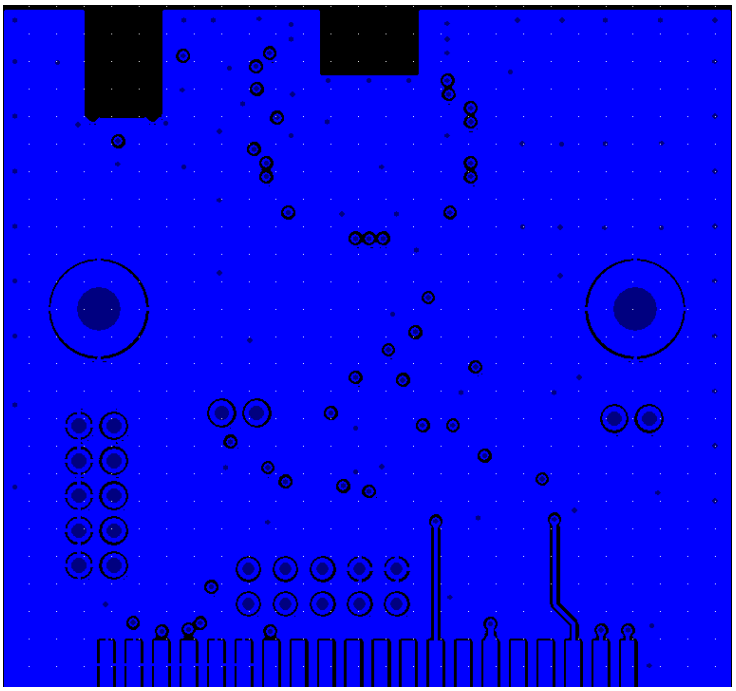

Figure 24: Layer 4 (bottom)

Related documents

[1] NMEA Manual for Fastrax IT500 Series GPS receivers, Docu. No. FTX-HW-13002
[2] Fastrax: Reflow Soldering Profile, Docu. No. FTX-HW-13004
[3] Fastrax: LOCUS manual for Fastrax IT500 Series, Docu. No. FTX-HW-13005

For complete contact information visit us at www.u-blox.com

Revision history

Revision	Date	Name	Status / Comments
1.0	11. Oct.2012	kkai	Initial documentation
1.1	23. Oct.2012	kkai	Corrected TIMER signal description to FORCE_ON signal
A	14. Jan.2013	kkai	Transfer to u-blox version

Contact

For complete contact information visit us at www.u-blox.com

u-blox Offices

North, Central and South America

u-blox America, Inc.
Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:
Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:
Phone: +1 703 483 3185
E-mail: support_us@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG
Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support @u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):
Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:
Phone: +91 959 1302 450
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan:
Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com