

Specifications

Model No : S220Z1 – M02

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval

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REVISION HISTORY

	Date	Section	Description
0.0	Mar, 12, 08'	-	S220Z1 Tentative Specifications was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

S220Z1-M02 is a 22" wide TFT Liquid Crystal Display module with 4 CCFL Backlight unit and a [30-pin TMDS interface](#). This module supports 1680 x 1050 WSXGA+ (16:10 wide screen) mode and displays up to 16.7 million colors. The inverter module for the Backlight Unit is not built in.

1.2 FEATURES

- Super Wide viewing angle.
- High contrast ratio
- Fast response time
- High color saturation
- WSXGA+ (1680 x 1050 pixels) resolution
- DE (Data Enable) only mode
- Reduce residue
- TMDS (Transition Minimized Differential Signaling) interface
- RoHS Compliance
- Real 120Hz frame rate at resolution 1680*1050
- Support Single link/Dual link

1.3 APPLICATION

- 2D TFT LCD Monitor
- 3D TFT LCD Monitor

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Diagonal Size	558.68	mm	
Active Area	473.76 (H) x 296.1 (V)	mm	(1)
Bezel Opening Area	477.7 (H) x 300.1 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1680 x R.G.B. x 1050	pixel	-
Pixel Pitch	0.282 (H) x 0.282 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Transmissive Mode	Normally White	-	-
Surface Treatment	Hard coating (3H), AG (Haz1 25%)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note	
Module Size	Horizontal(H)	(493.2)	(493.7)	(494.2)	mm	(1)
	Vertical(V)	(319.6)	(320.1)	(320.6)	mm	
	Depth(D)	(16)	(16.5)	(17)	mm	
Weight	-	-	(2550)	g	-	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

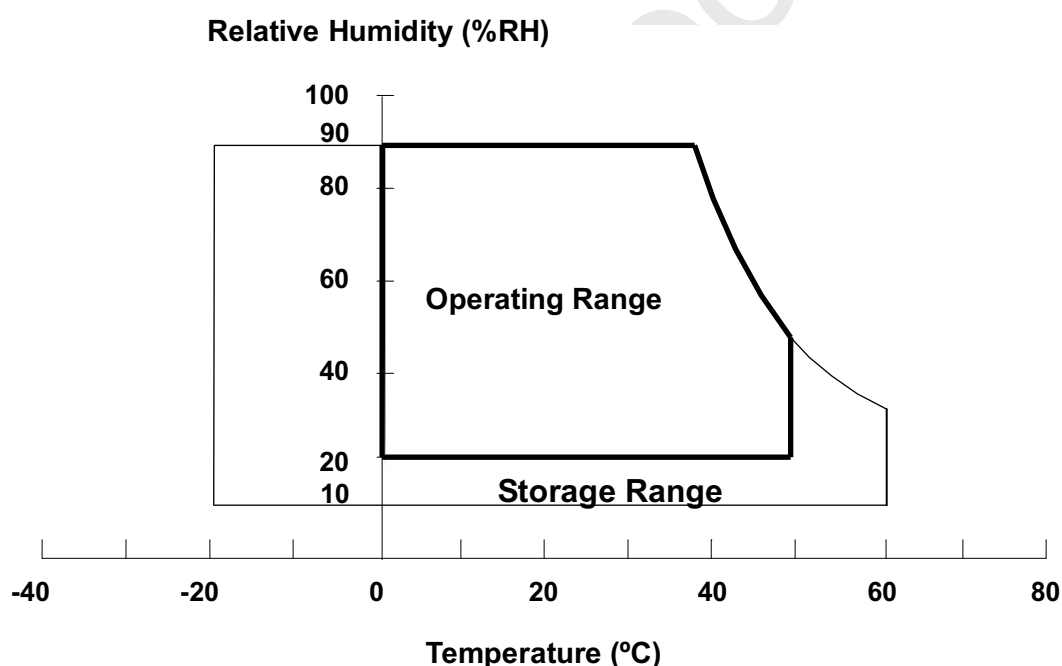
2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1	G	(4), (5)
LCD Cell Life Time	L _{CELL}	50,000	-	Hrs	MTBF based

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ($T_a \leq 40$ °C).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).
- (c) No condensation.



Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max.

Note (3) 11ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z.

Note (5) Upon the Vibration and Shock tests, the fixture used to hold the module must be firm and rigid enough to prevent the module from twisting or bending by the fixture.

2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage for LCD	V _{in}			V	(1)
Logic Input Voltage	V _{5A}			V	
Logic Input Voltage	V _{DD}			V	

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+5.5	V	(1)
Logic Input Voltage	V _{IN}	-0.3	+4.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _L	-	2.5K	V _{RMS}	(1), (2), I _L = 7.0mA
Lamp Current	I _L	3.0	8.0	mA _{RMS}	(1), (2)
Lamp Frequency	F _L	40	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

Parameter	SYMBOL	Value			UNIT	Note	
		MIN	TYP	MAX			
Power Supply Voltage for LCD	Vin	12.42	13.8	15.18	V		
Power Supply Current for LCD	Iin		300		mA		
Logic Input Voltage	V5A	4.75	5	5.25	V		
Logic Input Current	I5A		0.5		A		
Driver Logic Input Voltage	VDD	3.135	3.3	3.465	V		
Driver Logic Input Current	IDD		60		mA		
Differential Impedence	Zm		100		Ω		
Logic Input Voltage	High	VIH	0.8VDD	-	VDD	V	
	Low	VIL	0	-	VDD	V	
LCD Inrush Current	Irush		3		A	(2)	
Power Consumption	P		5		W		
PANEL On	High	PANEL_ON	2.5	3.3	0.6	V	MAX=3.6 is ok
	Low						
DCDC On	High	DCDC_ON	2.5	3.3	0.6	V	MAX=3.6 is ok
	Low						
VCOM PWM	High	VCOM_PWM	2.5		0.6	V	MAX=5.45 is ok
	Low						
VCOM PWM Frequency	VCOM_PWM		27			KHz	Adjustable Duty Cycle

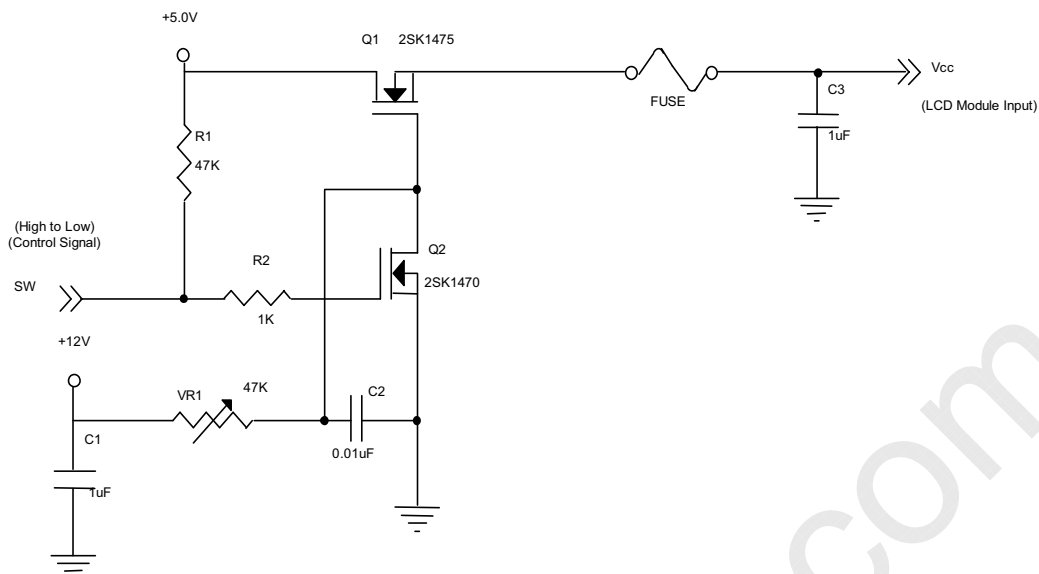
Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	Vcc	4.5	5.0	5.5	V	-	
Ripple Voltage	V _{RP}	-	--	250	mV	-	
Rush Current	I _{RUSH}	-	--	3	A	(2)	
Power Supply Current	White	I _{CC}	-	630	819	mA	(3)a
	Black		-	1170	1521	mA	(3)b
	f _V = 75Hz, V _{CC} =4.5V		-	1330	1729	mA	(4)
LVDS differential input voltage	V _{id}	200	-	600	mV		
LVDS common input voltage	V _{ic}	--	1.2	--	V		

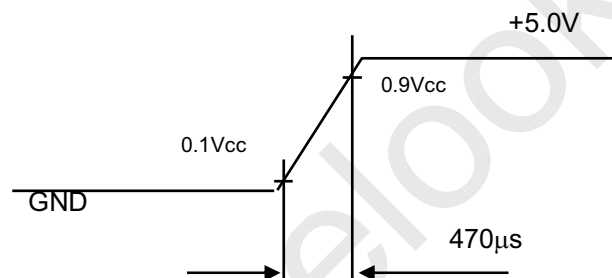
Above all conditions are VDD=5.0V, all black pattern at 75HZ.

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470 μ s



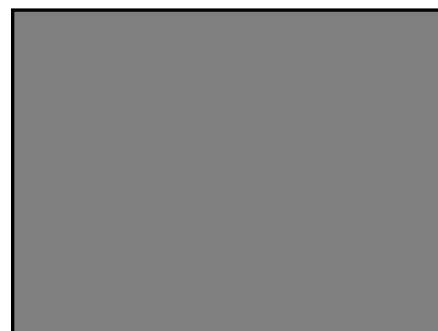
Note (3) The specified power supply current is under the conditions at $V_{cc} = 5.0 \text{ V}$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_v = 60 \text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

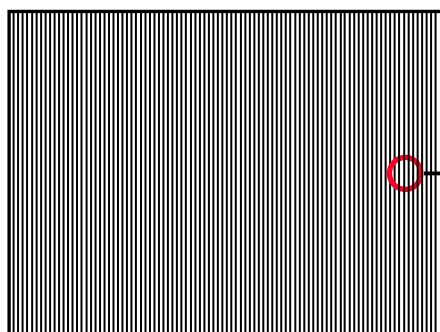
b. Black Pattern



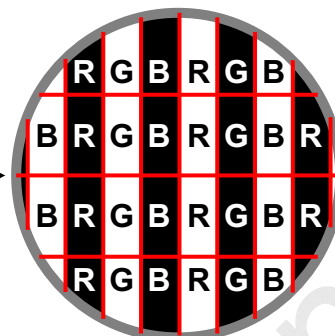
Active Area



c. Vertical Stripe Pattern

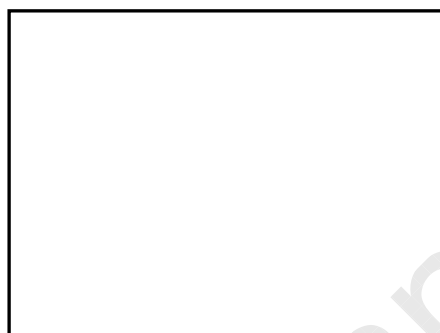


Active Area



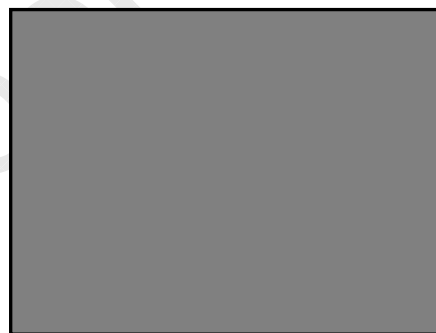
Note (3) The specified power supply current is under the conditions at $V_{cc} = 5.0 \text{ V}$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_v = 60 \text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern



Active Area

Note (4) The specified power supply current is under the conditions at $V_{cc} = 4.5 \text{ V}$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_v = 75 \text{ Hz}$, whereas a power dissipation check pattern (Black Pattern) below is displayed.

Black Pattern



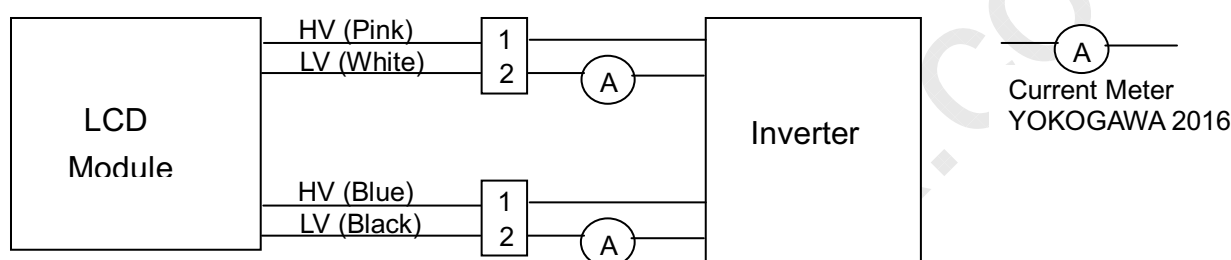
Active Area

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V _L	738	820	902	V _{RMS}	I _L = 7.0 mA
Lamp Current	I _L	3	7.0	8	mA _{RMS}	(1)
Lamp Turn On Voltage	V _S	-	-	1560(25°C)	V _{RMS}	(2)
		-	-	1800(0°C)	V _{RMS}	(2)
Operating Frequency	F _L	40	60	80	KHz	(3)
Lamp Life Time	L _{BL}	50000	-	-	Hrs	(5), I _L = 7.0 mA
Power Consumption	P _L	-	22.96	-	W	(4), I _L = 7.0 mA

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The voltage that must be larger than V_s should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times 4$ CCFLs

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition **Ta = 25 ± 2 °C and I_L = 7.0 mA rms** until one of the following events occurs:

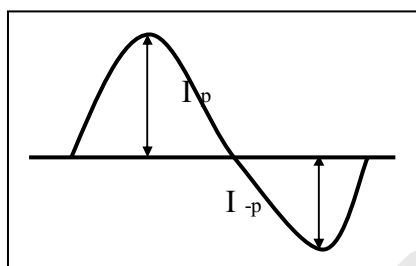
- When the brightness becomes or lower than 50% of its original value.
- When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interference with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below;
- The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
- The ideal sine wave form shall be symmetric in positive and negative polarities.



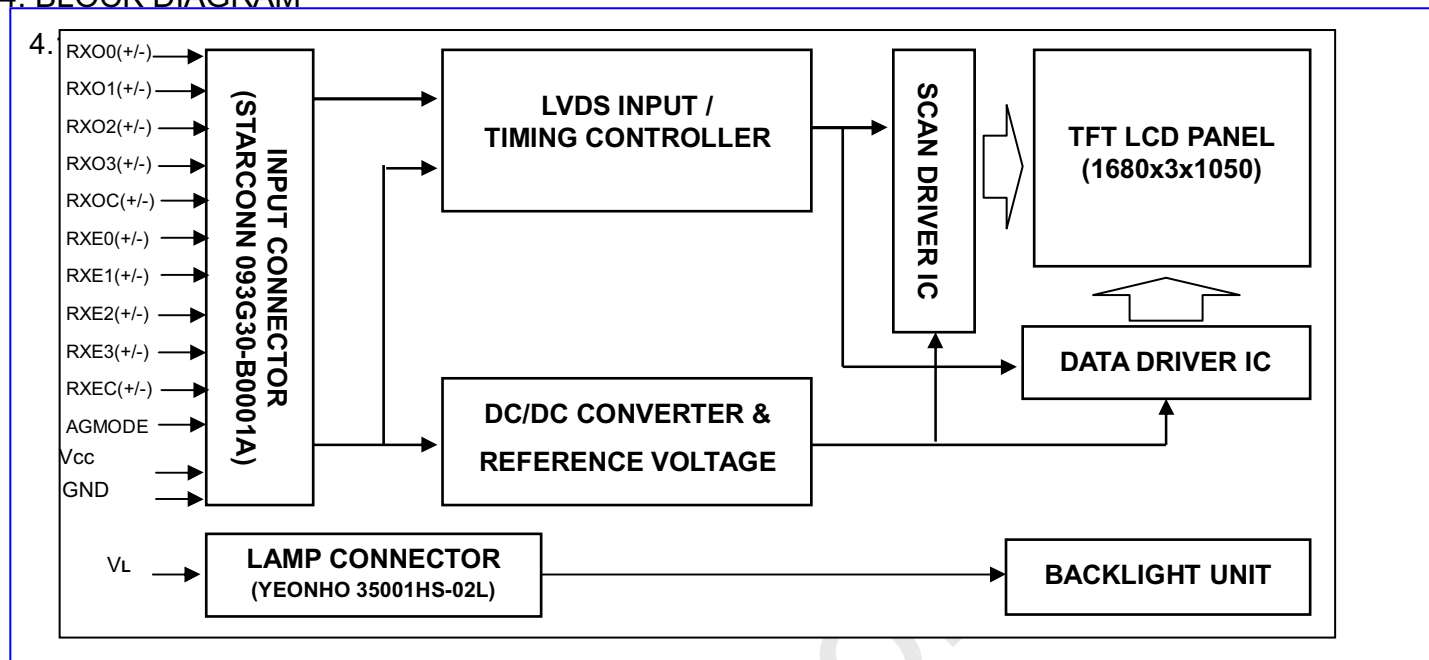
* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} * 100\%$$

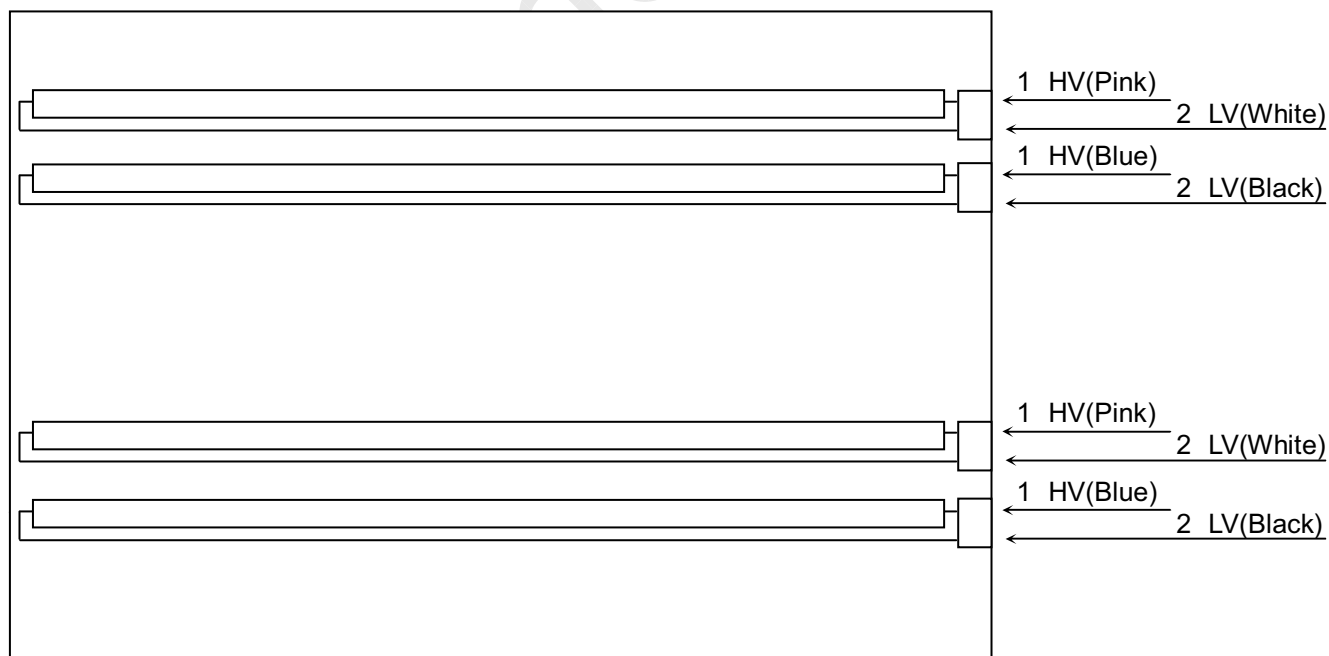
* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4. BLOCK DIAGRAM



4.2 BACKLIGHT UNIT



Note: On the same side, the same-polarity lamp voltage design for lamps is recommended

5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

(1)CN1 (Panel Interface)

Pin	Name	Description
1	Vin	Driver Power Input Voltage
2	Vin	Driver Power Input Voltage
3	V5A	Logic Input Voltage +5V
4	PANEL_ON	This pin is used to control the driver Logic Input Voltage VDD. When PANEL_ON input is "H", VDD will be to driver.
5	DCDC_ON	This pin is used to control the PWM IC. When DCDC_ON input is "H", it enable PWM IC.
6	VCM_PWM	This pin is used to generate common voltage for panel. Adjust pulse width could be changed common voltage.
7	GVOFF	Gate driver high voltage switch timing control.
8	NC	No connect
9	GND	Ground
10	BSTHI	Data driver start pulse input(Back)
11	GND	Ground
12	BR0N	Negative RSDS differential data input. Channel R0(Back)
13	BR0P	Positive RSDS differential data input. Channel R0(Back)
14	BR1N	Negative RSDS differential data input. Channel R1(Back)
15	BR1P	Positive RSDS differential data input. Channel R1(Back)
16	BR2N	Negative RSDS differential data input. Channel R2(Back)
17	BR2P	Positive RSDS differential data input. Channel R2(Back)
18	GND	Ground
19	BCKN	Negative RSDS differential clock input. (Back)
20	BCKP	Positive RSDS differential clock input. (Back)
21	GND	Ground
22	BG0N	Negative RSDS differential data input. Channel G0(Back)
23	BG0P	Positive RSDS differential data input. Channel G0(Back)
24	BG1N	Negative RSDS differential data input. Channel G1(Back)
25	BG1P	Positive RSDS differential data input. Channel G1(Back)
26	BG2N	Negative RSDS differential data input. Channel G2(Back)
27	BG2P	Positive RSDS differential data input. Channel G2(Back)
28	GND	Ground
29	BB0N	Negative RSDS differential data input. Channel B0(Back)
30	BB0P	Positive RSDS differential data input. Channel B0(Back)
31	BB1N	Negative RSDS differential data input. Channel B1(Back)
32	BB1P	Positive RSDS differential data input. Channel B1(Back)
33	BB2N	Negative RSDS differential data input. Channel B2(Back)
34	BB2P	Positive RSDS differential data input. Channel B2(Back)
35	GND	Ground
36	GND	Ground

(2)CN1 (Panel Interface)

Pin	Name	Description
1	VDD	Driver Logic Input Voltage
2	VDD	Driver Logic Input Voltage
3	XAO	When /XAO input pin is low, all the Gate driver output pins are forced to VGH level. Note that this pin has higher priority than OE.
4	STV	Gate driver start pulse is read at the rising edge of CKV and a scan signal is output from the gate driver output pin.
5	CKV	Gate driver shift clock
6	OE	This pin is used to control the Gate driver output. When OE input is "H", gate driver output is fixed to VGL level regardless CKV.
7	GND	Ground
8	FR0N	Negative RSDS differential data input. Channel R0(Front)
9	FR0P	Positive RSDS differential data input. Channel R0(Front)
10	FR1N	Negative RSDS differential data input. Channel R1(Front)
11	FR1P	Positive RSDS differential data input. Channel R1(Front)
12	FR2N	Negative RSDS differential data input. Channel R2(Front)
13	FR2P	Positive RSDS differential data input. Channel R2(Front)
14	GND	Ground
15	POL	Data driver polarity inverting input
16	STB	The contents of the data driver register are transferred to the latch circuit at the rising edge of STB. Then the gray scale voltage is output from the device at the falling edge of STB.
17	GND	Ground
18	FCKN	Negative RSDS differential clock input. (Front)
19	FCKP	Positive RSDS differential clock input. (Front)
20	GND	Ground
21	FG0N	Negative RSDS differential data input. Channel G0(Front)
22	FG0P	Positive RSDS differential data input. Channel G0(Front)
23	FG1N	Negative RSDS differential data input. Channel G1(Front)
24	FG1P	Positive RSDS differential data input. Channel G1(Front)
25	FG2N	Negative RSDS differential data input. Channel G2(Front)
26	FG2P	Positive RSDS differential data input. Channel G2(Front)
27	GND	Ground
28	FB0N	Negative RSDS differential data input. Channel B0(Front)
29	FB0P	Positive RSDS differential data input. Channel B0(Front)
30	FB1N	Negative RSDS differential data input. Channel B1(Front)
31	FB1P	Positive RSDS differential data input. Channel B1(Front)
32	FB2N	Negative RSDS differential data input. Channel B2(Front)
33	FB2P	Positive RSDS differential data input. Channel B2(Front)
34	FSTHI	Data driver start pulse input(Front)
35	GND	Ground
36	GND	Ground

Note (1) Connector Part No.: IL-FHR-F36S-HF.

Pin	Name	Description
1	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
2	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
3	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
4	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
5	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
6	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)
24	GND	Ground
25	NC	Not connection, this pin should be open.
26	VCOM	VCOM Control, should be open.
27	AGMODE	AGMODE should be tied to ground or open.
28	VCC	+5.0V power supply
29	VCC	+5.0V power supply
30	VCC	+5.0V power supply

Note (1) Connector Part No.: 093G30-B0001A(STARCONN) or FI-X30SSL-HF(JAE) or EQUIVALENT.

Note (2) Mating Connector Part No.:FI-X30H ; FI-X30C* ; FI-X30M* ; FI-X30HL(-T),FI-X30C*L(-T) [JAE]

Note (3) The first pixel is odd.

Note (4) Input signal of even and odd clock should be the same timing.

5.2 LVDS DATA MAPPING TABLE

LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6
LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6

5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Remark
1	HV	High Voltage	Pink
2	LV	Low Voltage	White
1	HV	High Voltage	Blue
2	LV	Low Voltage	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB (JST) or equivalent

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

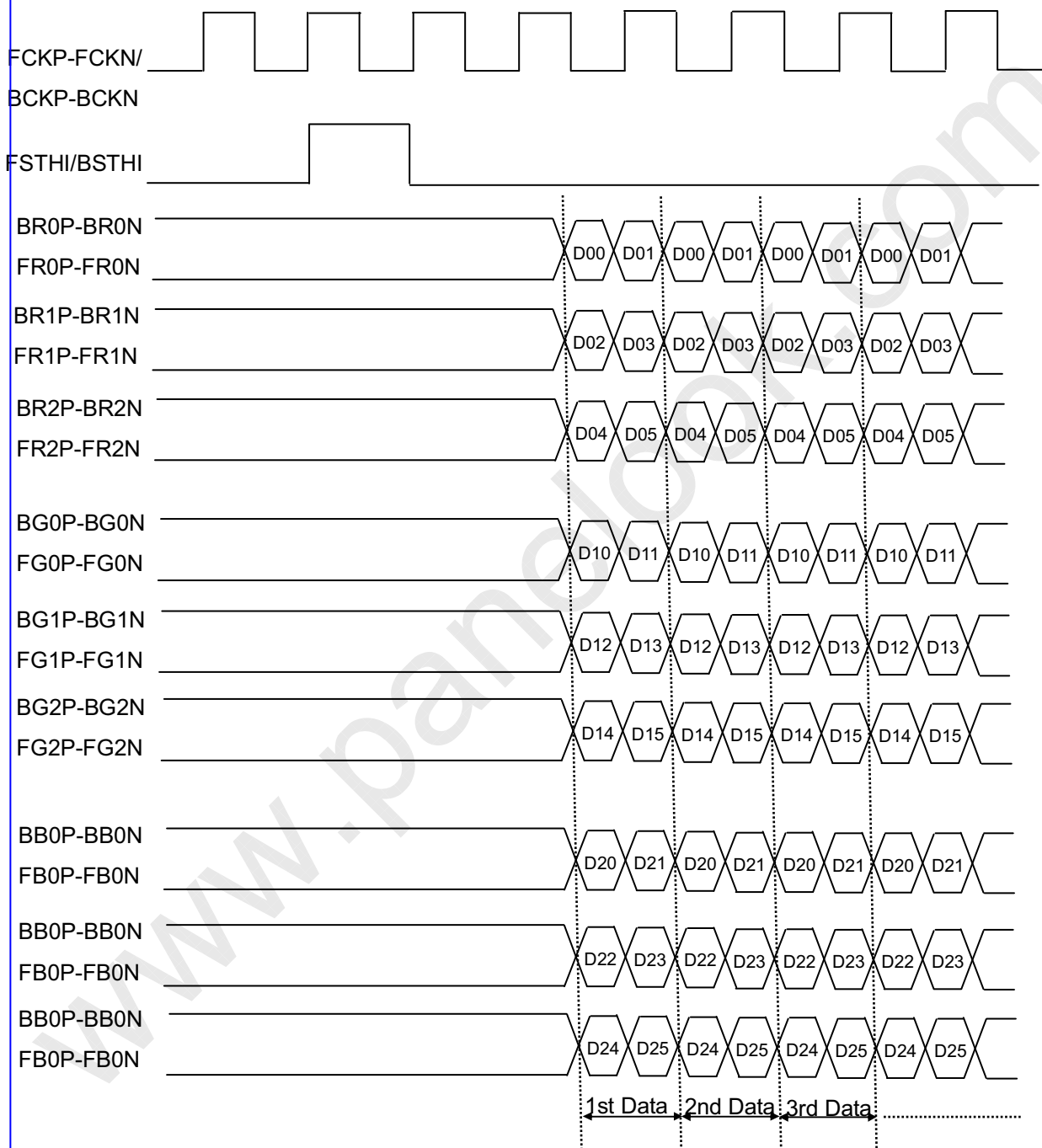
Color	Data Signal																							
	Red								Green								Blue							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1



Tentative

6. INTERFACE TIMING

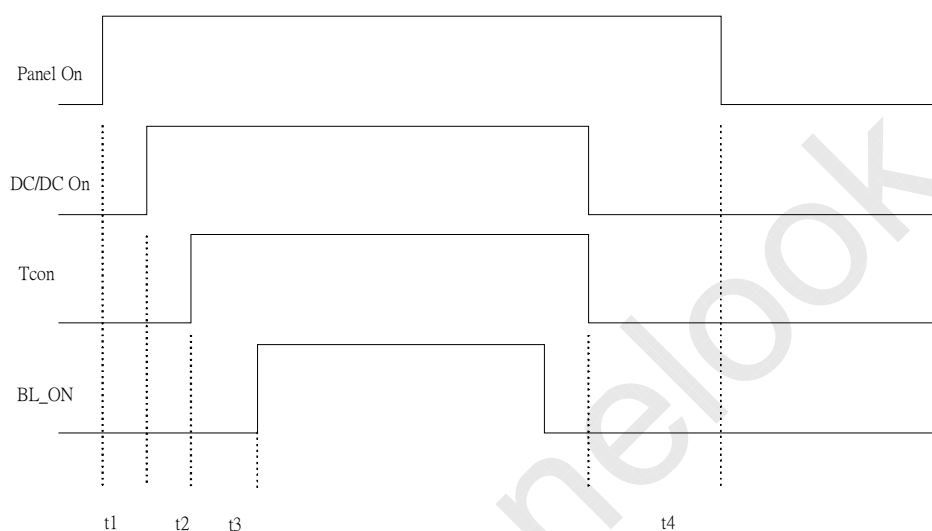
6.1 INPUT SIGNAL TIMING SPECIFICATIONS



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

Parameter	Symbol	Condition	Spec			Unit
			Min.	Typ.	Max.	
Panel On to DC/DC On	t_1	-	10	-	-	mS
DC/DC On to RSDS Data	t_2	-	40	50	60	
RSDS Data to BL_On	t_3	-	100	200	-	
RSDS Data Off to Panel Off	t_4	-	80	100	120	

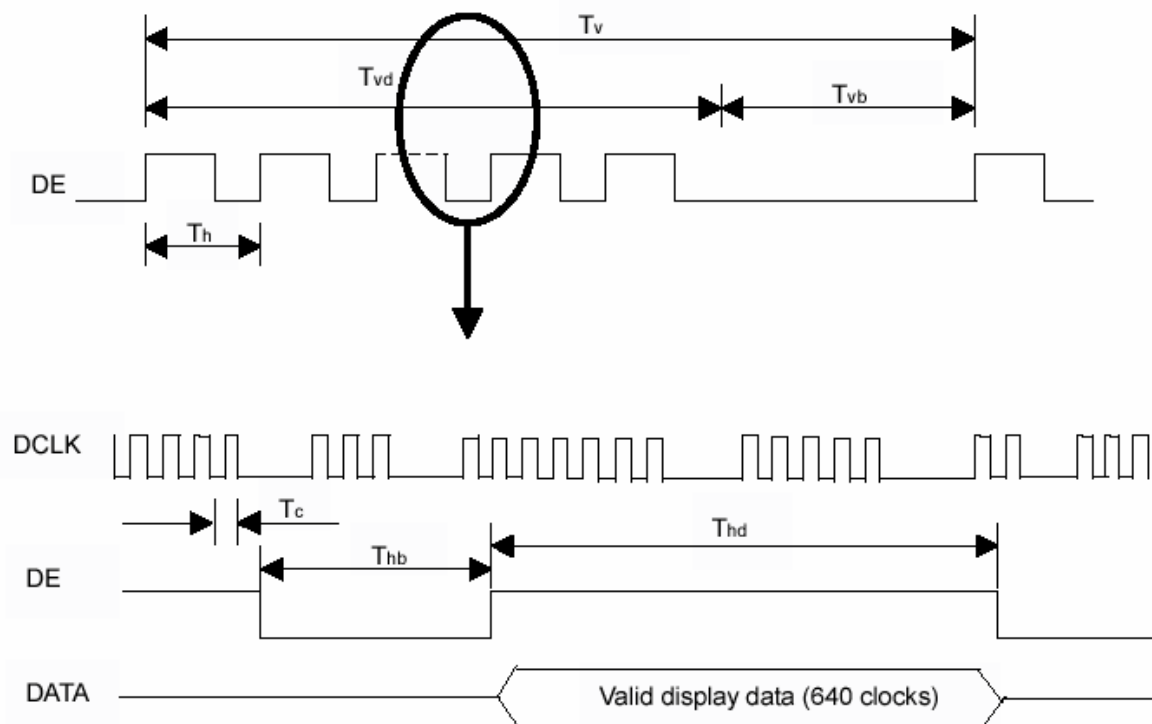


6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

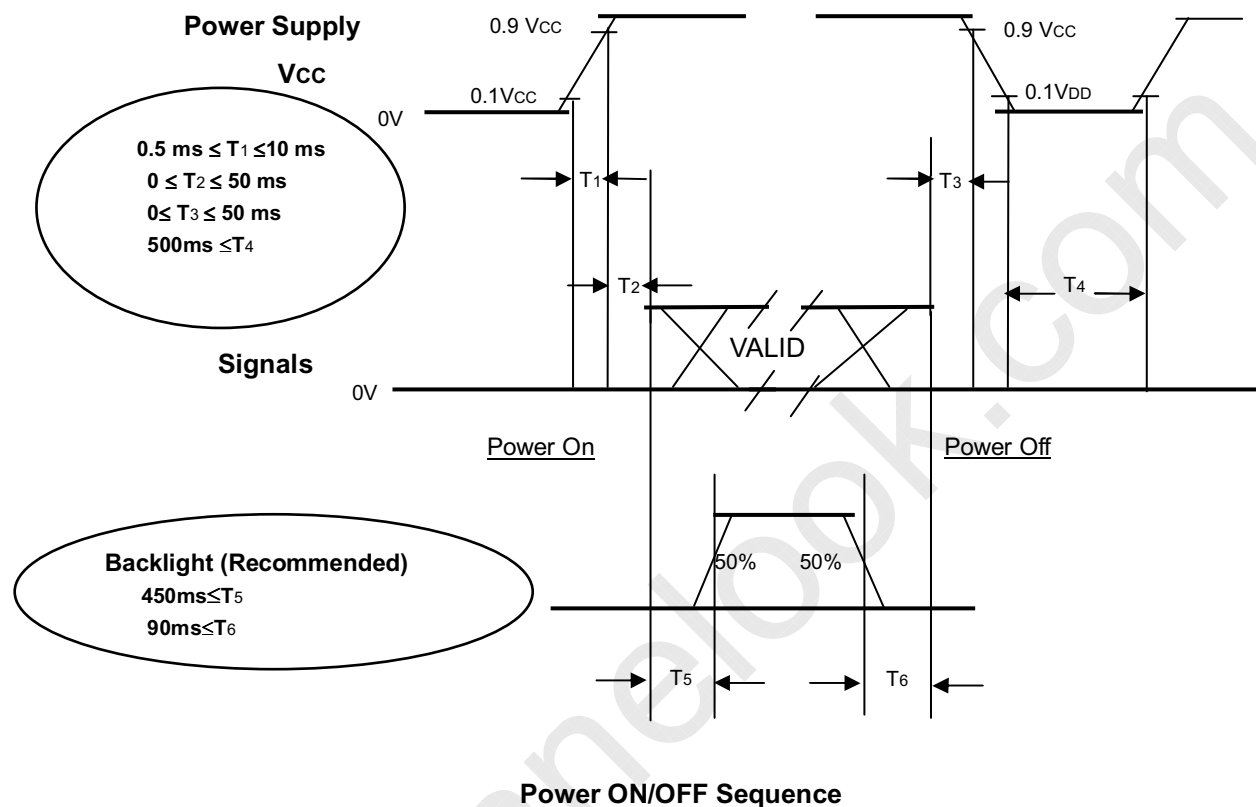
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	Fc	50	59.5	82	MHz	-
	Period	Tc	13.4	16.8	-	ns	-
	High Time	Tch	-	4/7	-	Tc	-
	Low Time	Tcl	-	3/7	-	Tc	-
LVDS Data	Setup Time	Tlvs	600	-	-	ps	-
	Hold Time	Tlvh	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr	50	60	76	Hz	Tv=Tvd+Tvb
	Total	Tv	1060	1080	1195	Th	-
	Display	Tvd	1050	1050	1050	Th	-
	Blank	Tvb	Tv-Tvd	30	Tv-Tvd	Th	-
Horizontal Active Display Term	Total	Th	890	920	1000	Tc	Th=Thd+Thb
	Display	Thd	840	840	840	Tc	-
	Blank	Thb	Th-Thd	80	Th-Thd	Tc	-

Note : (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the conditions shown in the following diagram.



Note.

- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) Please apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off, the display may, instantly, function abnormally.
- (3) In case of vcc = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power on/off periods.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. Driver DC Characteristics

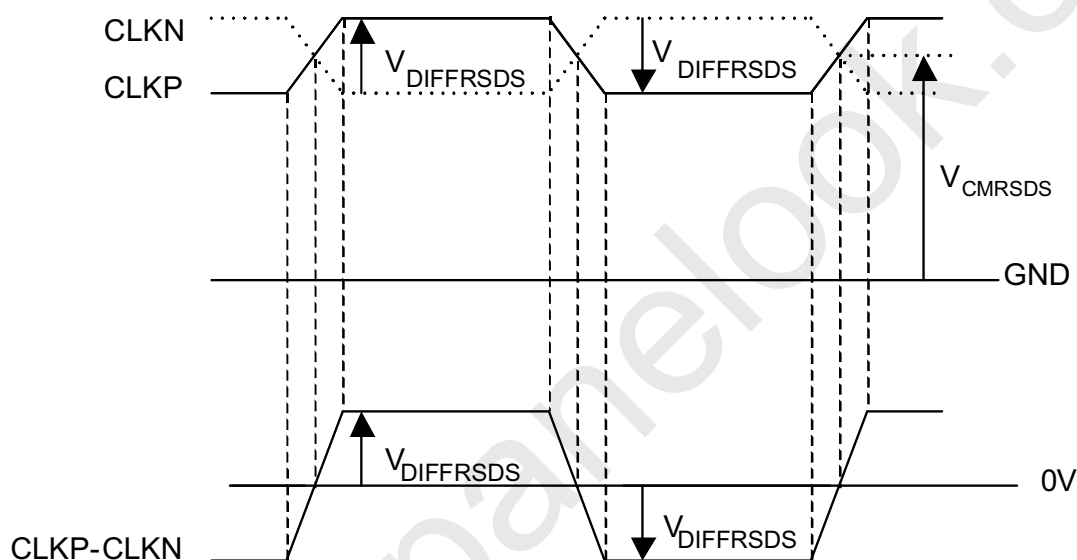
7.1 RSDS CHARACTERISTICS

(Ta = - 10 to +85 °C, VDD = 2.3 to 3.6 V, VDDA = 8.0 to 13.5 V, VSSD = VSSA = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RSDS high input voltage	$V_{DIFFRSDS}$	$V_{CMRSDS} = + 1.2 V^{(1)}$	100	200	-	mV
RSDS low input voltage	$V_{DIFFRSDS}$	$V_{CMRSDS} = + 1.2 V^{(1)}$	-	-200	- 100	mV
RSDS common mode input voltage range	V_{CMRSDS}	$V_{DIFFRSDS} = + 200 mV^{(2)}$	$V_{SSD} + 0.1$	-	$V_{DDD} - 1.2$	V
RSDS input leakage current	IDL	DxxP, DxxN, CLKP, CLKN	-10	-	10	μA

Note: (1) $V_{CMRSDS} = (V_{CLKP} + V_{CLKN}) / 2$ or $V_{CMRSDS} = (V_{DxxP} + V_{DxxN}) / 2$

(2) $V_{DIFFRSDS} = V_{CLKP} - V_{CLKN}$ or $V_{DIFFRSDS} = V_{DxxP} - V_{DxxN}$



7.2 Electrical Characteristics (VSSD=VSSA=0V)

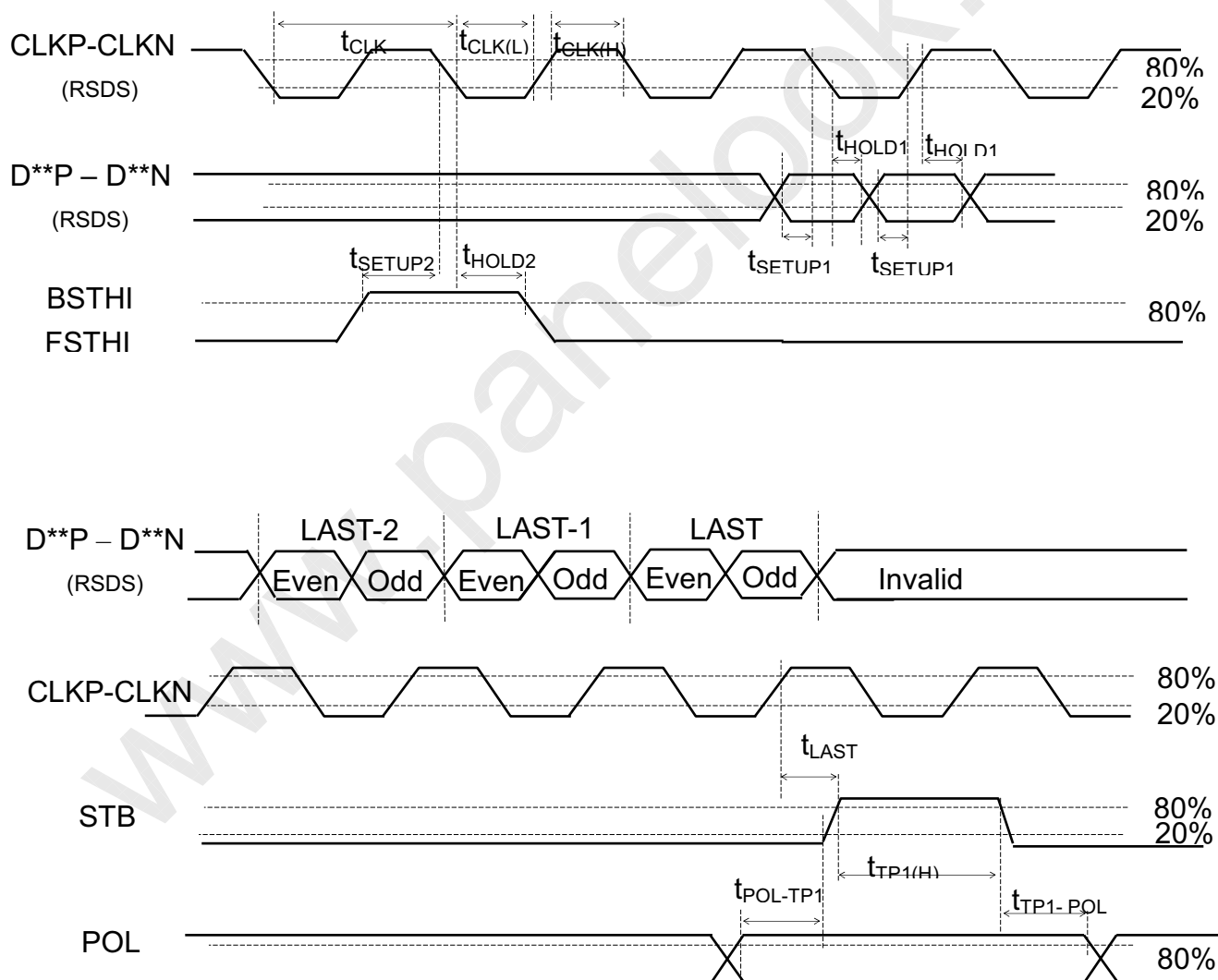
Parameter	Symbol	Condition	Spec			Unit
			Min.	Typ.	Max.	
RSDS input "Low" Voltage	$V_{DIFFRSDS}$	DX[2:0]P,DX[2:0]N, CLKP,CLKN	-	-200	-	mV
RSDS input "High" Voltage	$V_{DIFFRSDS}$		-	200	-	mV
RSDS reference voltage	V_{CMRSDS}		VSSD+0.1	1.2	VDDD-1.2	V
Input "Low" voltage	V_{IL}	EIO1,EIO2,DIR,TP1, POL	GND	-	0.2VDDD	μ A
Input "High" voltage	V_{IH}		0.8VDDD	-	VDDD	μ A
Input leak current	IL		-	-	10	μ A
Supply current (In operation mode)	I_{CCD1}	VDDD=3.6V	-	TBD	TBD ⁽¹⁾	mA
Supply current (In stand-by mode)	I_{CCD2}	VDDD=3.6V	-	TBD	TBD	mA
Supply current (In operation mode)	I_{CCA1}	VDDA=13.5V	-	TBD	TBD ⁽¹⁾⁽²⁾	mA
Supply current (In stand-by mode)	I_{CCA2}	VDDA=13.5V	-	TBD	TBD	mA
Output current	I_{VOH}	$V_{out}=V_{\gamma} 1-1V$	-	-	-100	μ A
	I_{VOL}	$V_{out}=V_{\gamma} 10+1V$	-	-	100	μ A
Output Voltage range	V_{out}	OUT1~OUT432	VSSA+0.1	-	VDDA-0.1	V
Output Voltage deviation	Vcho-dev	VDDA=13.5V Dxx=0 to 63 Gray	-	± 5	± 10	mV
Gamma impedance	Rr	$V_{\gamma} 1 \sim V_{\gamma} 5, V_{\gamma} 6 \sim V_{\gamma} 10$	0.5Typ	16820	1.5Typ	Ω

Note: (1) Test condition: TP1= 20 μ s, CLK =54MHz, data pattern =1010....checkerboard pattern, Ta=25°C

(2) No load condition

8.Driver AC Characteristics

Parameter	Symbol	Condition	Spec			Unit
			Min.	Typ.	Max.	
Clock pulse width	t_{CLK}	-	11	-	-	ns
Clock pulse low period	$t_{CLK(L)}$	-	5	-	-	ns
Clock pulse high period	$t_{CLK(H)}$	-	5	-	-	ns
Data setup time	t_{SETUP1}	-	2	-	-	ns
Data hold time	t_{HOLD1}	-	0	-	-	ns
Start pulse setup time	t_{SETUP2}	-	1	-	-	ns
Start pulse hold time	t_{HOLD2}	-	2	-	-	ns
TP1 high period	$t_{TP1(H)}$	-	1	-	-	CLKP
Last data CLK to TP1 high	t_{LAST}	-	0	-	-	CLKP
TP1 high to EIO n high	t_{NEXT}	-	6	-	-	CLKP
POL to TP1 setup time	$t_{POL-TP1}$	POL toggle to TP1 rising	3	-	-	ns
TP1 to POL hold time	$t_{TP1-POL}$	TP1 falling to POL toggle	2	-	-	ns



9.Vertical Timing

Parameter	Symbol	Condition	Spec			Unit	Remark
			Min.	Typ.	Max.		
CKV period	t_{CKV}	-	5	-	-	μs	
CKV pulse width	t_{CKVH}, t_{CKVL}	50% duty cycle	2.5	-	-	μs	
OE pulse width	t_{OE}	-	1	-	3.5	μs	Note2
/XAO pulse width	t_{WXAO}	-	6	-	-	μs	
Data setup time	t_{SU}	-	700	-	-	ns	
Data hold time	t_{HD}	-	700	-	-	ns	
OE to CKV time	t_{OE-CKV}			0.5		μs	
STB to CKV	$t_{STB-CKV}$		0	0	0	μs	
STB Pulse Width	t_{STB}			0.5		μs	
CKV to GVOFF	$t_{CKV-GVOFF}$			-0.5		μs	
GVOFF Pulse width	t_{GVOFF}			12.8		μs	Note1

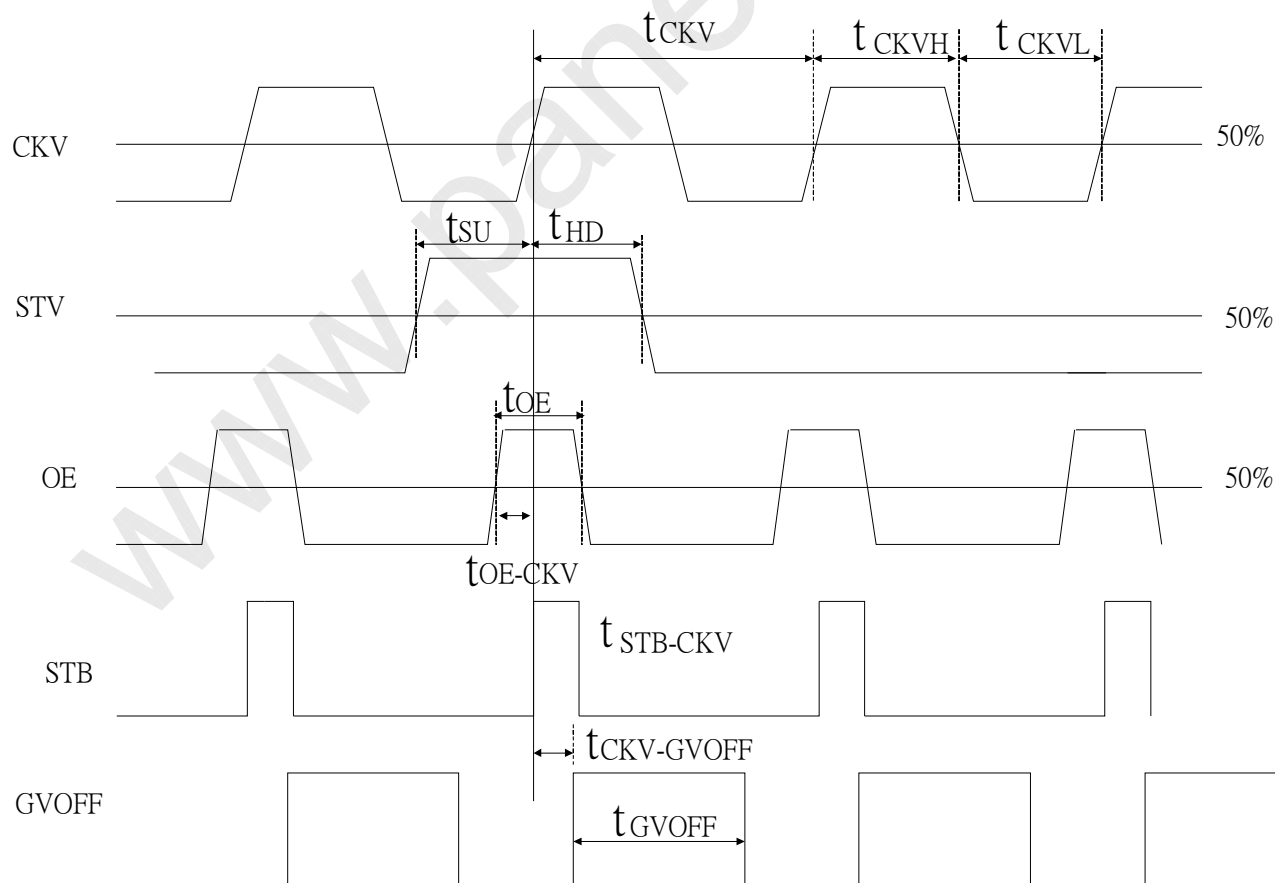
Note 1:GVOFF,OE,STB frequency same as CKV

Note 2:Width of OE pulse should be according to vertical frequency.

Ex:2.4 μs with 75Hz V-Sync ; 3.0 μs with 60Hz V-Sync.

Note 3 : GVOFF is used to make 3-step wave form to avoid V-Through on panel.

Note 4 : OE is used to control VGH_P output to panel. When OE is "H" , VGH_P output to panel is fixed to "L" regardless CKV.



10. OPTICAL CHARACTERISTICS

10.1 TEST CONDITIONS

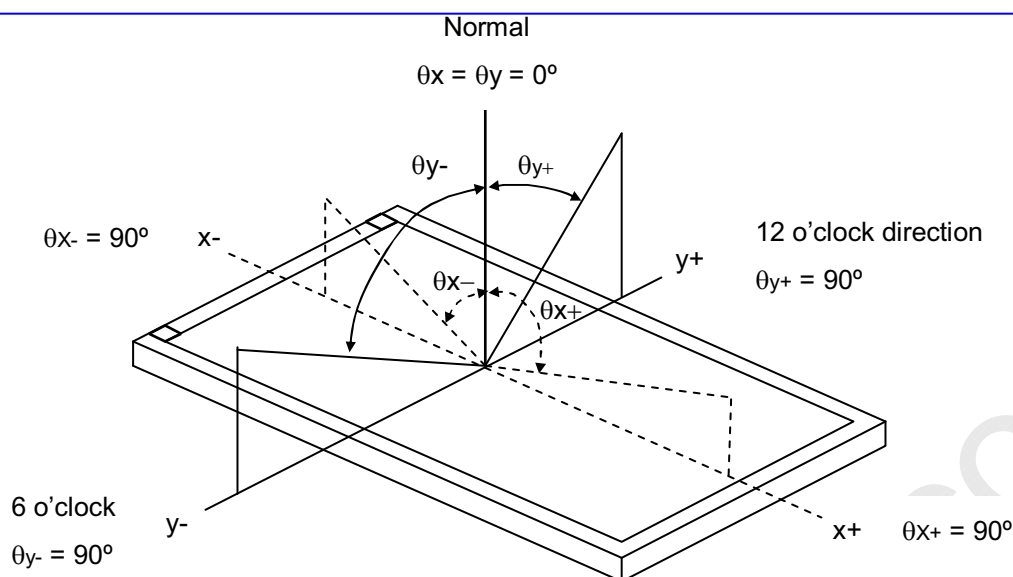
Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	7.0	mA
Inverter Driving Frequency	F _L	61	KHz
Inverter	Darfon VK.13165.101		

10.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_y=0^\circ$ CS-1000T R=G=B=255 Grayscale	Typ - 0.03	0.649	Typ + 0.03	(1), (5)	
		R _y			0.335			
	Green	G _x			0.283			
		G _y			0.605			
	Blue	B _x			0.151			
		B _y			0.073			
	White	W _x			0.313			
		W _y			0.329			
Center Luminance of White	L _c		250	300	---	cd/m ²	(4), (5)	
Contrast Ratio	CR		700	1000	---	-	(2), (6)	
Response Time	T _R	$\theta_x=0^\circ, \theta_y=0^\circ$	---	1.3	2.2	ms	(3)	
	T _F		---	3.7	5.8	ms		
White Variation	δW	$\theta_x=0^\circ, \theta_y=0^\circ$	---	1.3	1.42	-	(5), (6)	
Viewing Angle	Horizontal	θ _{x+}	CR>10	75	85	---	Deg.	(1), (5)
		θ _{x-}		75	85	---		
	Vertical	θ _{y+}		70	80	---		
		θ _{y-}		70	80	---		

Note (1) Definition of Viewing Angle (θ_x, θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

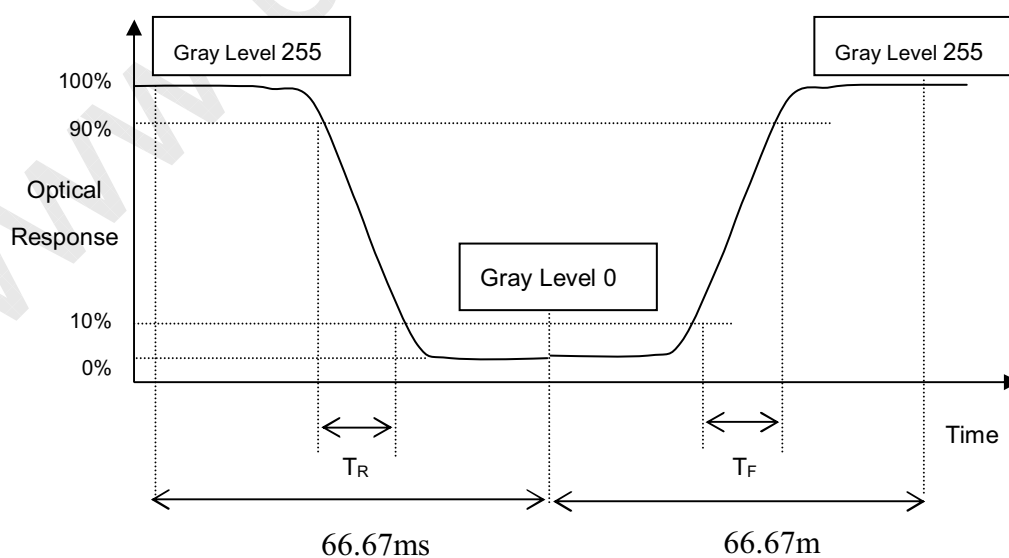
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Luminance of White (L_C):

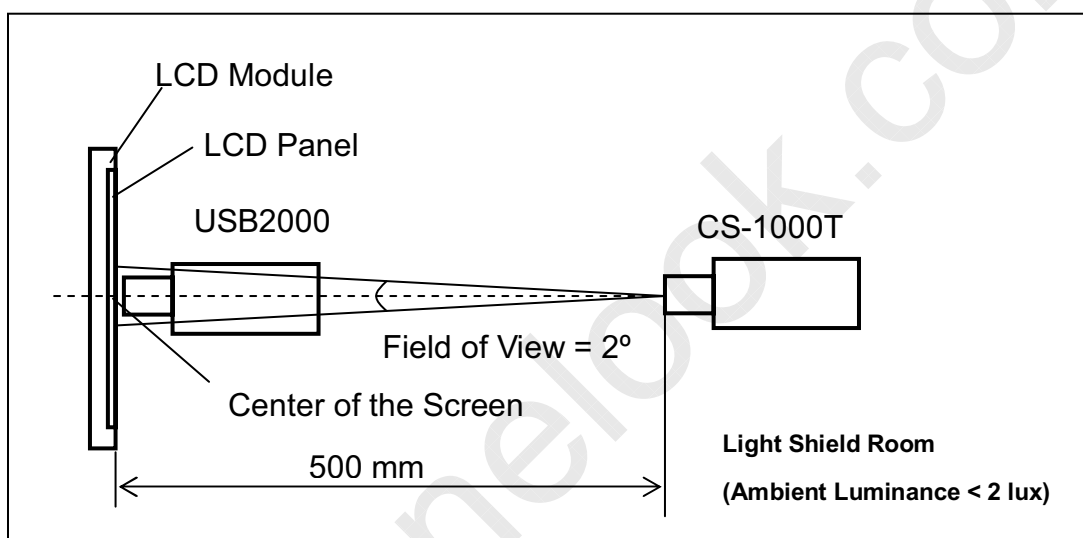
Measure the luminance of gray level 255 at center point

$$L_C = L(5)$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

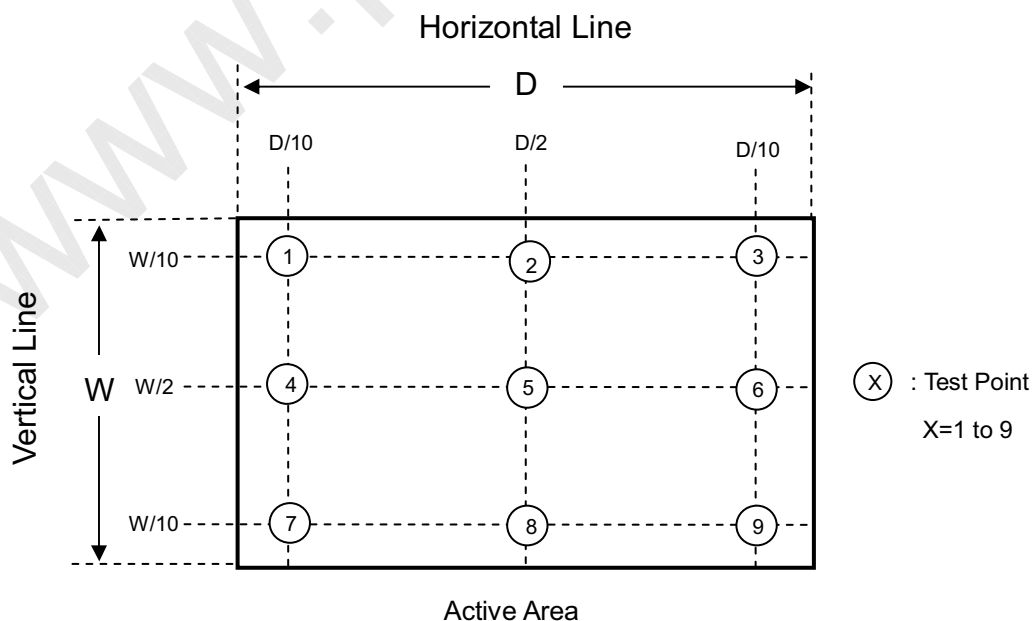
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 9 points

$$\delta W = \text{Maximum } [L(1) \sim L(9)] / \text{Minimum } [L(1) \sim L(9)]$$



11. PACKAGING

11.1 PACKING SPECIFICATIONS

- (1) 6 LCD modules / 1 Box
- (2) Box dimensions: 595(L) X 330 (W) X 440 (H) mm
- (3) Weight: 17.3 Kg (6 modules per box)

11.2 PACKING METHOD

- (1) Carton Packing should have no failure in the following reliability test items.

Test Item	Test Conditions	Note
Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Dropping Test	1 Angle, 3 Edge, 6 Face, 60cm	Non Operation

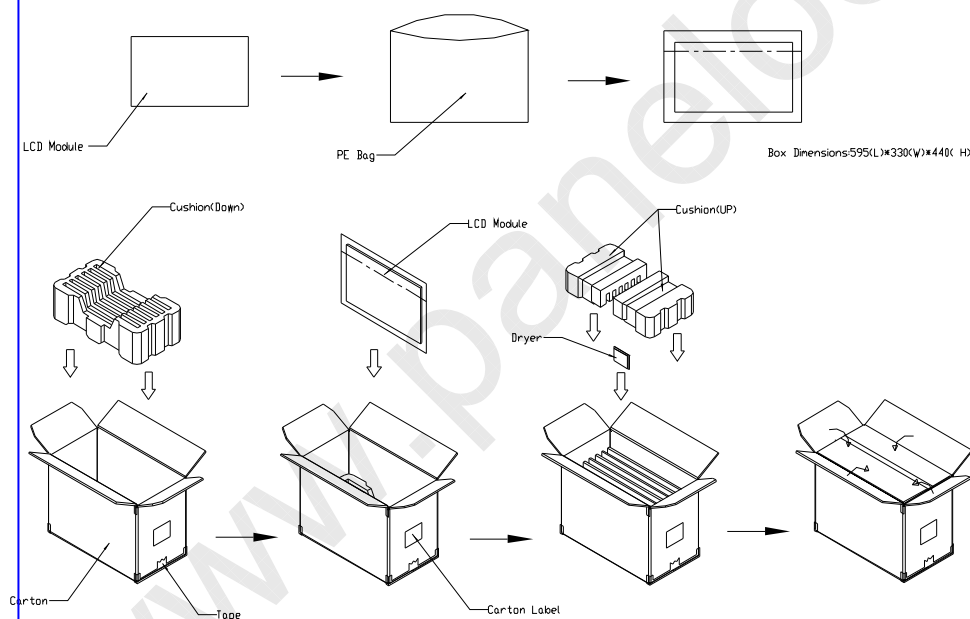


Figure. 8-1 Packing method

For ocean shipping

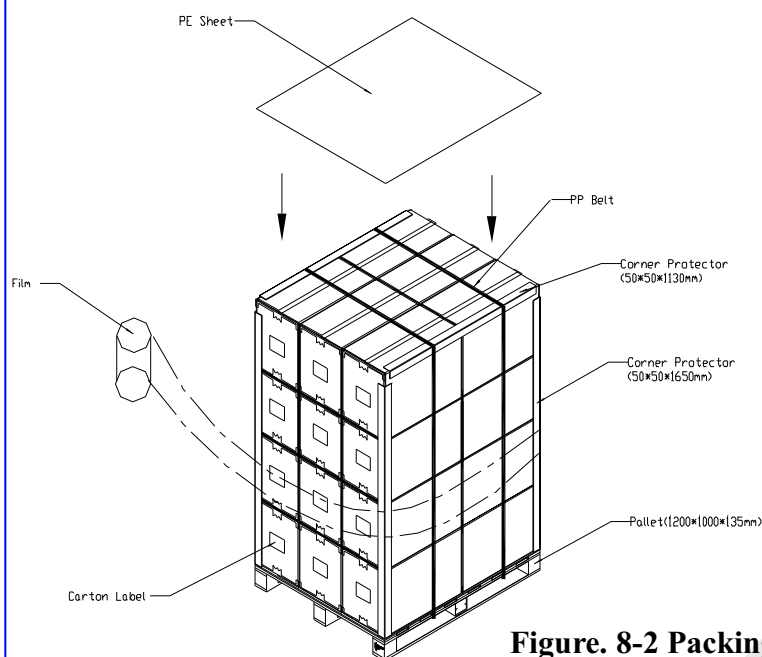


Figure. 8-2 Packing method

For air transport

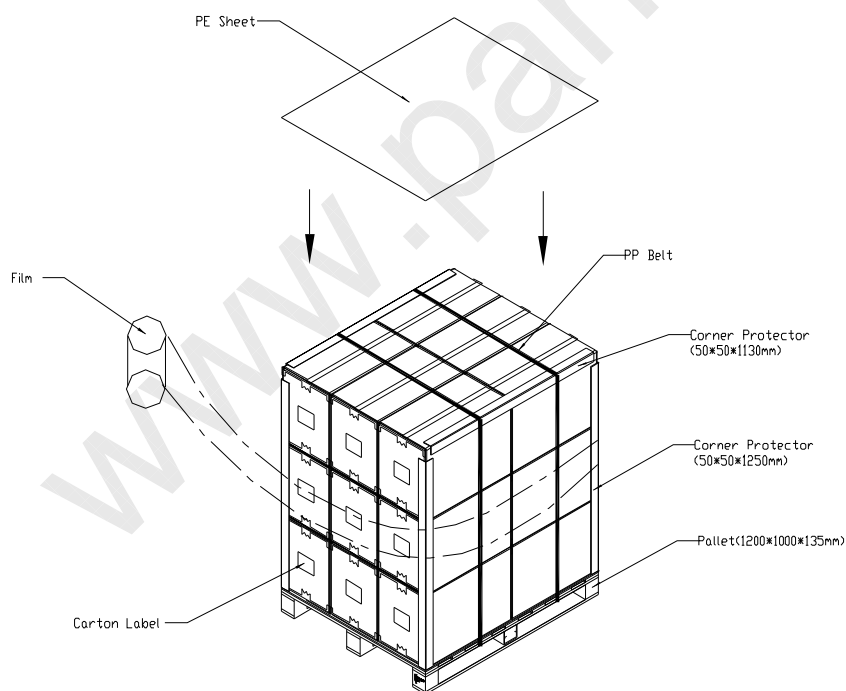


Figure. 8-3 Packing method

12. DEFINITION OF LABELS

12.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: M220Z1-L03
 (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
 (c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X	CMO internal use	-
XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

- (d) Customer's barcode definition:

Serial ID: CM-22Z13-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
22Z13	Model number	M220Z1-L03=22Z13
X	Revision code	ZBD, C1=A, C2=B, Non ZBD, C1=1, C2=2,
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renesas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	1~12=0~C
XX	Module location	Tainan, Taiwan=TN; Ningbo China=NP
L	Module line #	1~12=0~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, T, U, V
NNNN	Serial number	By LCD supplier

13. PRECAUTIONS

13.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

13.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.