

DESCRIPTION

The following specifications are applied to the following TFT open cell.

Product Name: VVF37F115G00

General Specifications

Effective Display Area	: (H) 819.36 × (V) 460.89	(mm)
Number of Pixels	: (H)1,920×(V)1,080	(pixels)
Pixel Pitch	: (H) 0.42675 × (V) 0.42675	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti-Reflection Clear (Haze ≤ 1%)	
Number of Colors	: 1,073,741,824	(colors)
Viewing angle range	: Wide version	
External Dimensions	: (H)854 x (V)516.3 x (t)6 typ	(mm)
Weight	: Typ 1,700	(g)

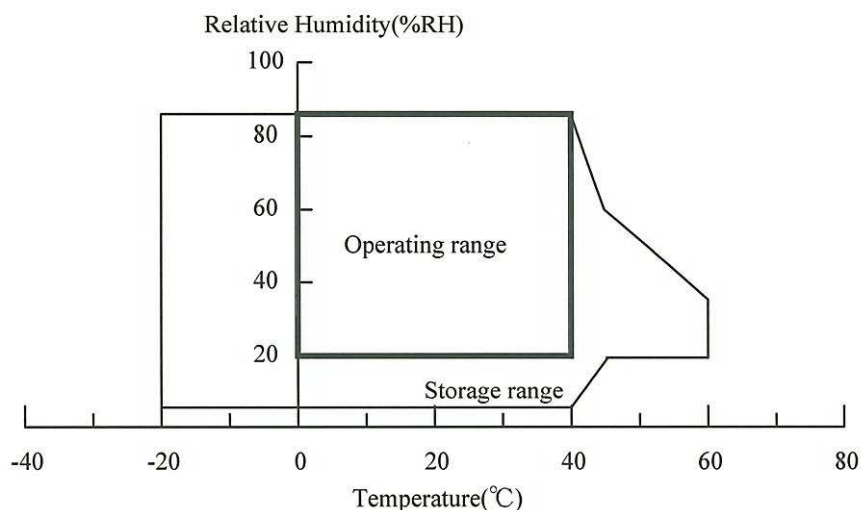
1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1),5),6),7)
Humidity	2)		2)		%RH	1),7)
Vibration	-	4.9(0.5G)	-	9.8(1.0G)	m/s ²	3),7)
Shock	-	29.4(3G)	-	196(20G)	m/s ²	4),7)
Corrosive Gas	Not Acceptable		Not Acceptable		-	7)

Note 1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.

- 2) $T_a \leq 40\text{ }^\circ\text{C}$ ······Relative humidity should be less than 85 %RH max. Dew is prohibited.
 $T_a > 40\text{ }^\circ\text{C}$ ······Relative humidity should be lower than the moisture of the 85 %RH at 40 °C.



- 3) Frequency of the vibration is between 15 Hz and 100 Hz.
 4) Pulse width of the shock is 10 ms.
 5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.
 However, it does not affect the characteristics and reliability of the product.
 6) The temperature of LCD front surface would be 65 °C in operating, it may affect the optical characteristics however it does not damage the function of the module.
 7) Environmental Absolute Maximum Ratings is Based on IPS Alpha Technology TFT standard module.
 Leave TFT open cell alone, this environmental ratings can't be guaranteed. The users have a responsibility in considering ability of other parts of TFT module and TFT module process.

1.2 Electrical Absolute Maximum Ratings

Based on IPS Alpha Technology, Ltd. Standard Module

V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	0	13.2	V	
Input Voltage for logic	V1	-0.3	4.0	V	1)
Electrostatic Durability	VESD0	±100		V	2),3)
	VESD1	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.

2)Discharge Coefficient : 200pF-250 Ω , Environmental : 25°C-70%RH

3)It is applied to I/F connector pins.

4)It is applied to the surface of a metallic bezel and a LCD panel.

1.3 Environmental Absolute Ratings of TFT open cell

Storage Condition : With shipping package

Storage temperatue range : 25 ± 5 °C

Storage humidity range : 50 ± 10%RH

Shelf life : 1 month from the delivery date

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

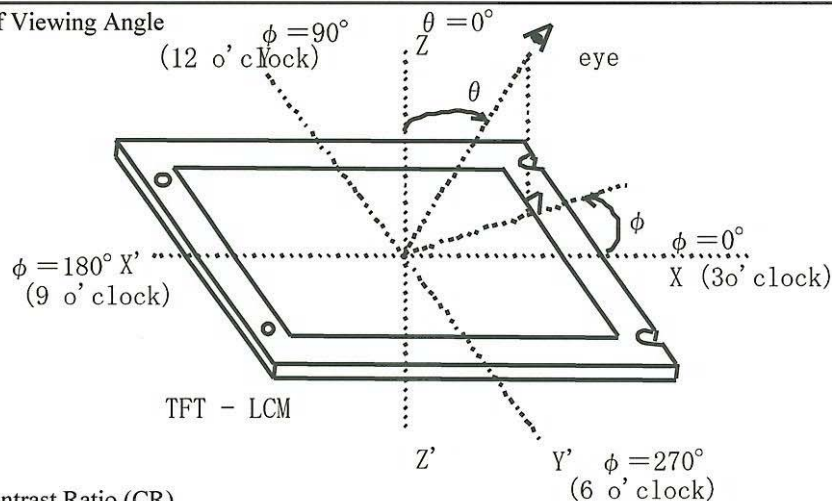
Measuring equipment : CS-1000A, or equivalent

Ambient Temperature =25°C、VDD=12.0V、f V=120Hz、

Light source is backlight of AX094G077H module.

ITEM	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE	
Contrast Ratio	C R		800	1400	-	-	2)	
Response Time	Rise	ton	-	8	20	ms	3)	
	Fall	toff	-	6	20	ms	3)	
Brightness of white	Bwh		370	470	-	cd/m ²		
Brightness uniformity	Buni		-	-	30	%	4)	
Color Chromaticity (CIE)	Red	x	0.618	0.648	0.678	-	【Gray scale =1023】	
		y	0.300	0.330	0.360			
	Green	x	0.271	0.301	0.331			
		y	0.589	0.619	0.649			
	Blue	x	0.123	0.153	0.183			
		y	0.035	0.065	0.095			
	White	x	0.243	0.273	0.303			
		y	0.245	0.275	0.305			
Variation of Color Position (CIE)	Red	Δx	-	-	0.04	-	5) 【Gray scale =1023】	
		Δy	-	-	0.04			
	Green	Δx	$\theta = 50^\circ$	-	-			0.04
		Δy	$\varphi = 0^\circ,$	-	-			0.04
	Blue	Δx	$90^\circ,$	-	-			0.04
		Δy	$180^\circ,$	-	-			0.04
	White	Δx	270°	-	-			0.04
		Δy	1)	-	-			0.04
Contrast Ratio at 89°	CR89	6)	10	(100)	-	-	Estimated value	

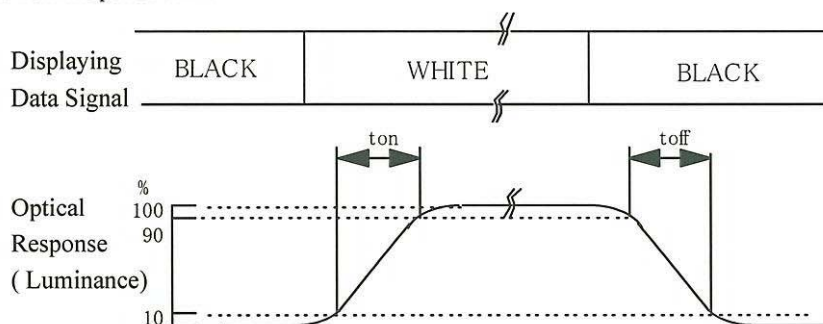
Note 1) Definition of Viewing Angle



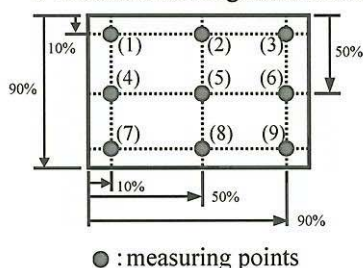
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity Display pattern is white (255 level). The brightness



uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$B_{uni} = \frac{|B_{max} \text{ or } B_{min} - B_{ave}|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness

B_{min} = Minimum brightness

$$B_{ave} = \text{Average brightness} = \frac{\sum_{k=1}^9 (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at $\theta = 0^\circ$ and at $\theta = 50^\circ$ & $\phi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$.

6) Contrast ratio at 89°

Evaluation conditions are on horizontal & vertical axis

3. ELECTRICAL CHARACTERISTICS

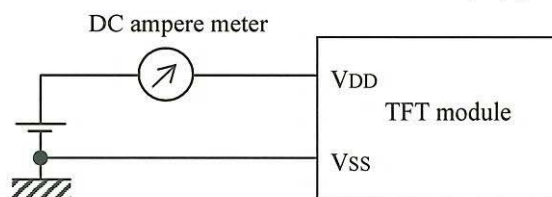
Based on IPS Alpha Technology, Ltd. Standard Module

3.1 TFT-LCD module

Ta = 25 °C, VSS = 0 V

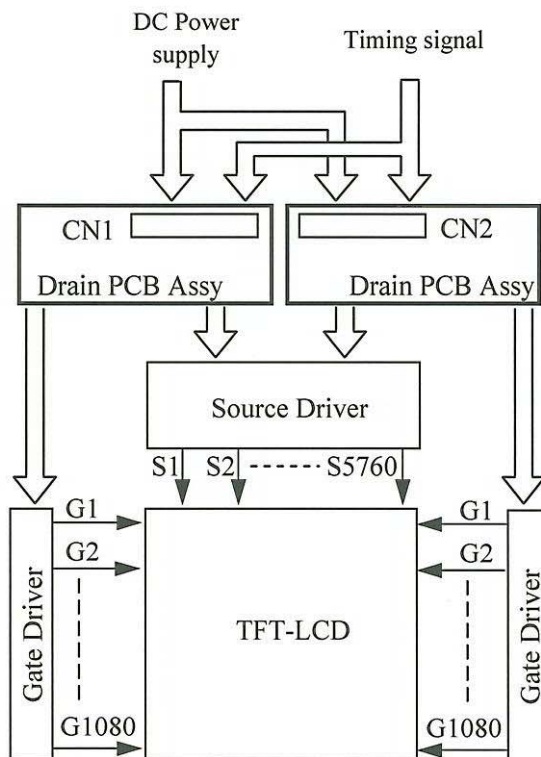
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE	
Power supply voltage	VDD	11.4	12.0	12.6	V		
Power supply current	IDD	-	0.8	1.2	A	1),2)	
Ripple voltage of power supply	VDDR	-	-	150	mV		
FRC on/off	High	FRC	3.0	3.3	3.6	V	
	Low		0	0	0.6	V	
LVDS select	High	LVDSSEL	3.0	3.3	3.6	V	
	Low		0	0	0.6	V	

Note 1) fv=120.0Hz, fCLK=130MHz, VDD=12.0V, and display pattern is horizontal stripe.



- 2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of electrical circuit of module.

4. BLOCK DIAGRAM



5. INTERFACE PIN ASSIGNMENT

5.1 TFT open cell.

CN1:IRISO IMSA-9637S-60Y922

(Matching FFC : SUMITOMO SML2CD-60X41.0-BDX6(BL)-P0.5-S4.0+4.0-M-N(35)-AUP UL20861)

PIN No.	Symbol	Description	Note
1	VCOMS	Common Voltage	
2	CPV	Control Signal	
3	DATA1	Control Signal	
4	DATA2	Control Signal	
5	VON	Reference Voltage	
6	VOFF2		
7	NC	No Connection	
8	VSS	GND(0V)	
9	VRF1	Reference Voltage	
10	VRF2		
11	VRF3		
12	VRF4		
13	VRF5		
14	VRF6		
15	LP	Control Signal	
16	POL	Control Signal	
17	VDD	Logic Voltage	
18	CSMODE	Control Signal	
19	VSS	GND(0V)	
20	D13-	Pixel Data	
21	D13+		
22	D12-	Pixel Data	
23	D12+		
24	VSS	GND(0V)	
25	D11-	Pixel Data	
26	D11+		
27	D10-	Pixel Data	
28	D10+		
29	VSS	GND(0V)	
30	CLK-	Pixel Clock	

PIN No.	Symbol	Description	Note	
31	CLK+	Pixel Clock		
32	VSS	GND(0V)		
33	D03-	Pixel Data		
34	D03+			
35	D02-	Pixel Data		
36	D02+			
37	VSS	GND(0V)		
38	D01-	Pixel Data		
39	D01+			
40	D00-	Pixel Data		
41	D00+			
42	VSS	GND(0V)		
43	VDD	Logic Voltage		
44	VDD			
45	VRF8	Reference Voltage		
46	VRF9			
47	VRF10			
48	VRF11			
49	VRF12	Analog Voltage		
50	VSS			GND(0V)
51	AVDD			
52	AVDD			
53	AVDDMH			
54	AVDDMH			
55	AVDDML			
56	AVDDML			
57	VSS	GND(0V)		
58	VSS			
59	VCOM	Common Voltage		
60	VCOM			

5. INTERFACE PIN ASSIGNMENT

CN2:IRISO IMSA-9637S-60Y922

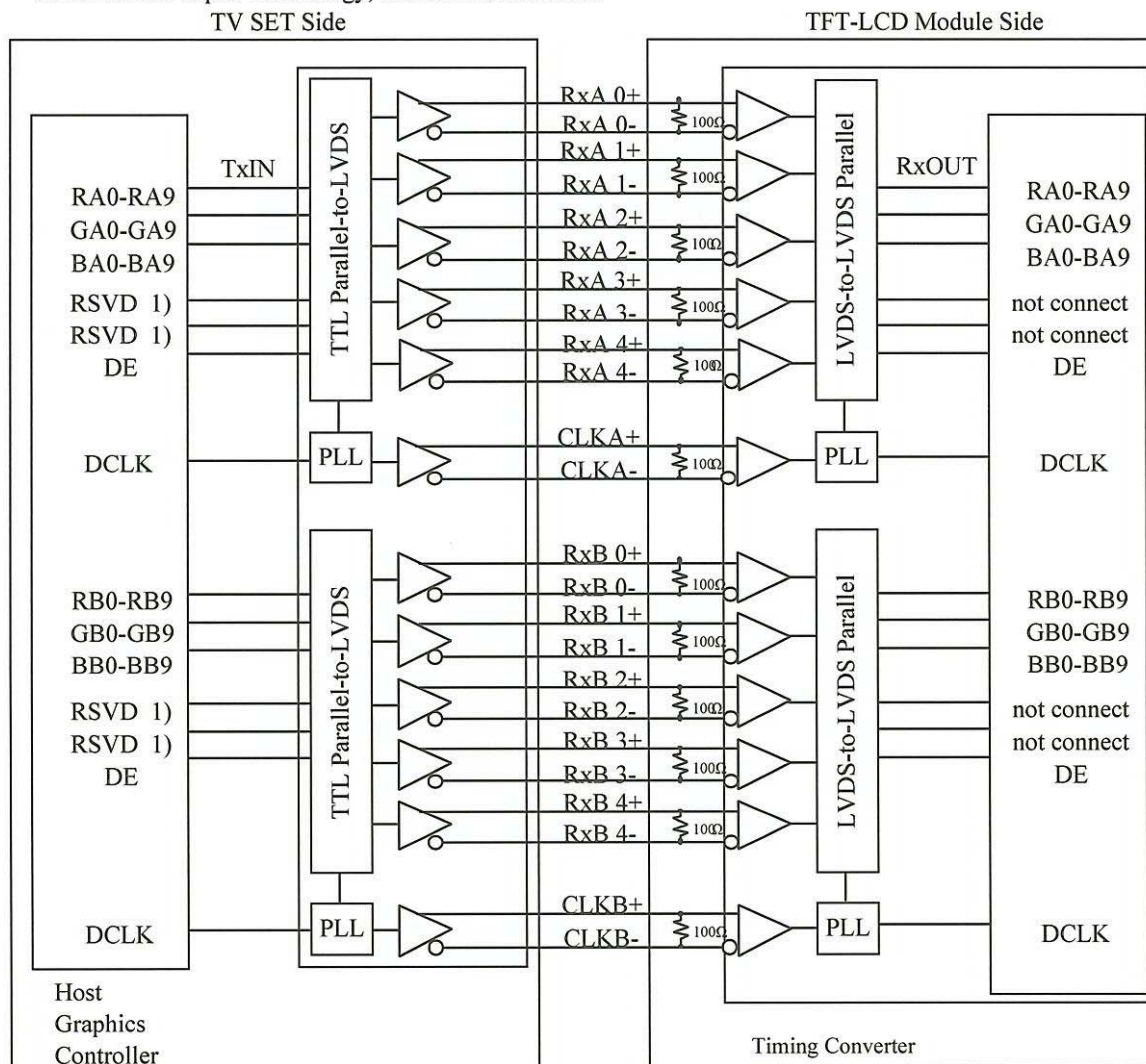
(Matching FFC : SUMITOMO SML2CD-60X41.0-BDX6(BL)-P0.5-S4.0+4.0-M-N(35)-AUP UL20861)

PIN No.	Symbol	Description	Note
1	VSS	GND(0V)	
2	CPV	Control Signal	
3	DATA1	Control Signal	
4	DATA2	Control Signal	
5	VON	Reference Voltage	
6	VOFF2		
7	NC	No Connection	
8	VSS	GND(0V)	
9	VRF1	Reference Voltage	
10	VRF2		
11	VRF3		
12	VRF4		
13	VRF5		
14	VRF6		
15	LP	Control Signal	
16	POL	Control Signal	
17	VDD	Logic Voltage	
18	CSMODE	Control Signal	
19	VSS	GND(0V)	
20	D13-	Pixel Data	
21	D13+		
22	D12-	Pixel Data	
23	D12+		
24	VSS	GND(0V)	
25	D11-	Pixel Data	
26	D11+		
27	D10-	Pixel Data	
28	D10+		
29	VSS	GND(0V)	
30	CLK-	Pixel Clock	

PIN No.	Symbol	Description	Note
31	CLK+	Pixel Clock	
32	VSS	GND(0V)	
33	D03-	Pixel Data	
34	D03+		
35	D02-	Pixel Data	
36	D02+		
37	VSS	GND(0V)	
38	D01-	Pixel Data	
39	D01+		
40	D00-	Pixel Data	
41	D00+		
42	VSS	GND(0V)	
43	VDD	Logic Voltage	
44	VDD		
45	VRF8	Reference Voltage	
46	VRF9		
47	VRF10		
48	VRF11		
49	VRF12		
50	VSS	GND(0V)	
51	AVDD	Analog Voltage	
52	AVDD		
53	AVDDMH		
54	AVDDMH		
55	AVDDML		
56	AVDDML		
57	VSS	GND(0V)	
58	VSS		
59	VCOM	Common Voltage	
60	VCOM		

5.2 Block diagram of interface

Based on IPS Alpha Technology, Ltd. Standard Module



RA0~RA9, RB0~RB9 : Pixel R Data (9; MSB, 0; LSB)
 GA0~GA9, GB0~GB9 : Pixel G Data (9; MSB, 0; LSB)
 BA0~BA9, BB0~BB9 : Pixel B Data (9; MSB, 0; LSB)
 DE : Data Enable

- Note 1) The system must have the transmitter to drive the module.
 2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5. 3 LVDS interface

Based on IPS Alpha Technology, Ltd. Standard Module

The LVDSSEL signal of CN1 pin No.7 specification is "L" or open.【LVDSSEL = L or open】

	SIGNAL	TRANSMITTER		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL		
		THC63LVD1023B		TV Set	TFT-LCD	PIN	OUTPUT	INPUT		
		PIN	INPUT							
30bit	RA0/RB0	76/120	TA10/TA20	TA1+/TA2+	RA1+/RA2+	67/18	RA10/RA20	RA0/RB0		
	RA1/RB1	77/121	TA11/TA21			68/19	RA11/RA21	RA1/RB1		
	RA2/RB2	78/122	TA12/TA22			69/20	RA12/RA22	RA2/RB2		
	RA3/RB3	79/123	TA13/TA23			72/23	RA13/RA23	RA3/RB3		
	RA4/RB4	80/124	TA14/TA24			73/24	RA14/RA24	RA4/RB4		
	RA5/RB5	81/127	TA15/TA25			74/25	RA15/RA25	RA5/RB5		
	GA0/GB0	84/128	TA16/TA26	TA1-/TA2-	RA1-/RA2-	79/33	RA16/RA26	GA0/GB0		
	GA1/GB1	85/129	TB10/TB20			82/34	RB10/RB20	GA1/GB1		
	GA2/GB2	86/130	TB11/TB21			83/35	RB11/RB21	GA2/GB2		
	GA3/GB3	87/131	TB12/TB22			84/36	RB12/RB22	GA3/GB3		
	GA4/GB4	88/132	TB13/TB23			85/37	RB13/RB23	GA4/GB4		
	GA5/GB5	89/133	TB14/TB24			86/40	RB14/RB24	GA5/GB5		
	BA0/BB0	90/134	TB15/TB25	TB1+/TB2+	RB1+/RB2+	93/45	RB15/RB25	BA0/BB0		
	BA1/BB1	91/135	TB16/TB26			94/48	RB16/RB26	BA1/BB1		
	BA2/BB2	92/136	TC10/TC20			95/49	RC10/RC20	BA2/BB2		
	BA3/BB3	95/139	TC11/TC21			96/50	RC11/RC21	BA3/BB3		
	BA4/BB4	96/140	TC12/TC22			99/51	RC12/RC22	BA4/BB4		
	BA5/BB5	97/141	TC13/TC23			100/52	RC13/RC23	BA5/BB5		
	RSVD1)	98/142	TC14/TC24	TC1+/TC2+	RC1+/RC2+	101/-	RC14/RC24	RSVD1)		
	RSVD1)	99/143	TC15/TC25			102/-	RC15/RC25	RSVD1)		
	DE/DE	100/144	TC16/TC26			103/-	RC16/RC26	DE/DE		
	RA6/RB6	101/1	TD10/TD20			TC1-/TC2-	RC1-/RC2-	65/16	RD10/RD20	RA6/RB6
	RA7/RB7	102/2	TD11/TD21					66/17	RD11/RD21	RA7/RB7
	GA6/GB6	103/5	TD12/TD22					77/31	RD12/RD22	GA6/GB6
	GA7/GB7	106/6	TD13/TD23	78/32	RD13/RD23			GA7/GB7		
	BA6/BB6	107/7	TD14/TD24	91/43	RD14/RD24			BA6/BB6		
	BA7/BB7	108/8	TD15/TD25	92/44	RD15/RD25			BA7/BB7		
	RSVD 1)	110/9	TD16/TD26	TD1+/TD2+	RD1+/RD2+	104/55	RD16/RD26	RSVD 1)		
	RA8/RB8	111/10	TE10/TE20			63/14	RE10/RE20	RA8/RB8		
	RA9/RB9	112/11	TE11/TE21			64/15	RE11/RE21	RA9/RB9		
GA8/GB8	115/12	TE12/TE22	75/26			RE12/RE22	GA8/GB8			
GA9/GB9	116/17	TE13/TE23	76/27			RE13/RE23	GA9/GB9			
BA8/BB8	117/18	TE14/TE24	87/41			RE14/RE24	BA8/BB8			
BA9/BB9	118/19	TE15/TE25	TD1-/TD2-	RD1-/RD2-	90/42	RE15/RE25	BA9/BB9			
RSVD 1)	119/20	TE16/TE26			105/56	RE16/RE26	RSVD 1)			
	DCLK	15,16	CLKIN1 CLKIN2	TCLK1+/TCLK2+ TCLK1-/TCLK2-	RCLK1+/RCLK2+ RCLK1-/RCLK2-	60	CLKOUT	DCLK		

RA0~RA9, RB0~RB9 : Pixel R Data (9; MSB, 0; LSB)
 GA0~GA9, GB0~GB9 : Pixel G Data (9; MSB, 0; LSB)
 BA0~BA9, BB0~BB9 : Pixel B Data (9; MSB, 0; LSB)
 DE : Data Enable

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

The LVDSSEL signal of CN1 pin No.7 specification is "H".【LVDSSEL = H】

	SIGNAL	TRANSMITTER		INTERFACE CONNECTOR		RECEIVER		TFT CONTROL
		THC63LVD1023B		TV Set	TFT-LCD	PIN	OUTPUT	INPUT
		PIN	INPUT					
30bit	RA4/RB4	76/120	TA10/TA20	TA1+/TA2+	RA1+/RA2+	67/18	RA10/RA20	RA4/RB4
	RA5/RB5	77/121	TA11/TA21			68/19	RA11/RA21	RA5/RB5
	RA6/RB6	78/122	TA12/TA22			69/20	RA12/RA22	RA6/RB6
	RA7/RB7	79/123	TA13/TA23			72/23	RA13/RA23	RA7/RB7
	RA8/RB8	80/124	TA14/TA24	TA1-/TA2-	RA1-/RA2-	73/24	RA14/RA24	RA8/RB8
	RA9/RB9	81/127	TA15/TA25			74/25	RA15/RA25	RA9/RB9
	GA4/GB4	84/128	TA16/TA26			79/33	RA16/RA26	GA4/GB4
	GA5/GB5	85/129	TB10/TB20			82/34	RB10/RB20	GA5/GB5
	GA6/GB6	86/130	TB11/TB21	TB1+/TB2+	RB1+/RB2+	83/35	RB11/RB21	GA6/GB6
	GA7/GB7	87/131	TB12/TB22			84/36	RB12/RB22	GA7/GB7
	GA8/GB8	88/132	TB13/TB23			85/37	RB13/RB23	GA8/GB8
	GA9/GB9	89/133	TB14/TB24			86/40	RB14/RB24	GA9/GB9
	BA4/BB4	90/134	TB15/TB25	TB1-/TB2-	RB1-/RB2-	93/45	RB15/RB25	BA4/BB4
	BA5/BB5	91/135	TB16/TB26	TC1+/TC2+	RC1+/RC2+	94/48	RB16/RB26	BA5/BB5
	BA6/BB6	92/136	TC10/TC20			95/49	RC10/RC20	BA6/BB6
	BA7/BB7	95/139	TC11/TC21			96/50	RC11/RC21	BA7/BB7
	BA8/BB8	96/140	TC12/TC22			99/51	RC12/RC22	BA8/BB8
	BA9/BB9	97/141	TC13/TC23	TC1-/TC2-	RC1-/RC2-	100/52	RC13/RC23	BA9/BB9
	RSVD1)	98/142	TC14/TC24			101/-	RC14/RC24	RSVD1)
	RSVD1)	99/143	TC15/TC25			102/-	RC15/RC25	RSVD1)
	DE/DE	100/144	TC16/TC26			103/-	RC16/RC26	DE/DE
	RA2/RB2	101/1	TD10/TD20	TD1+/TD2+	RD1+/RD2+	65/16	RD10/RD20	RA2/RB2
	RA3/RB3	102/2	TD11/TD21			66/17	RD11/RD21	RA3/RB3
	GA2/GB2	103/5	TD12/TD22			77/31	RD12/RD22	GA2/GB2
	GA3/GB3	106/6	TD13/TD23			78/32	RD13/RD23	GA3/GB3
	BA2/BB2	107/7	TD14/TD24	TD1-/TD2-	RD1-/RD2-	91/43	RD14/RD24	BA2/BB2
	BA3/BB3	108/8	TD15/TD25			92/44	RD15/RD25	BA3/BB3
	RSVD 1)	110/9	TD16/TD26			104/55	RD16/RD26	RSVD 1)
	RA0/RB0	111/10	TE10/TE20			TE1+/TE2+	RE1+/RE2+	63/14
	RA1/RB1	112/11	TE11/TE21	64/15	RE11/RE21			RA1/RB1
	GA0/GB0	115/12	TE12/TE22	75/26	RE12/RE22			GA0/GB0
	GA1/GB1	116/17	TE13/TE23	76/27	RE13/RE23			GA1/GB1
BA0/BB0	117/18	TE14/TE24	TE1-/TE2-	RE1-/RE2-	87/41	RE14/RE24	BA0/BB0	
BA1/BB1	118/19	TE15/TE25			90/42	RE15/RE25	BA1/BB1	
RSVD 1)	119/20	TE16/TE26			105/56	RE16/RE26	RSVD 1)	
DCLK	15,16	CLKIN1 CLKIN2			TCLK1+/TCLK2+ TCLK1-/TCLK2-	RCLK1+/RCLK2+ RCLK1-/RCLK2-	60	CLKOUT

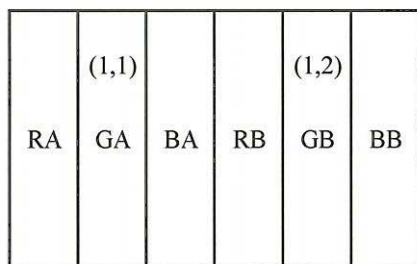
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 GA0~GA9, GB0~GB9 : Pixel G Data (9; MSB, 0; LSB)
 BA0~BA9, BB0~BB9 : Pixel B Data (9; MSB, 0; LSB)
 DE : Data Enable

Note 1) RSVD(reserved) pins on the transmitter shall be tied to"H"or"L".

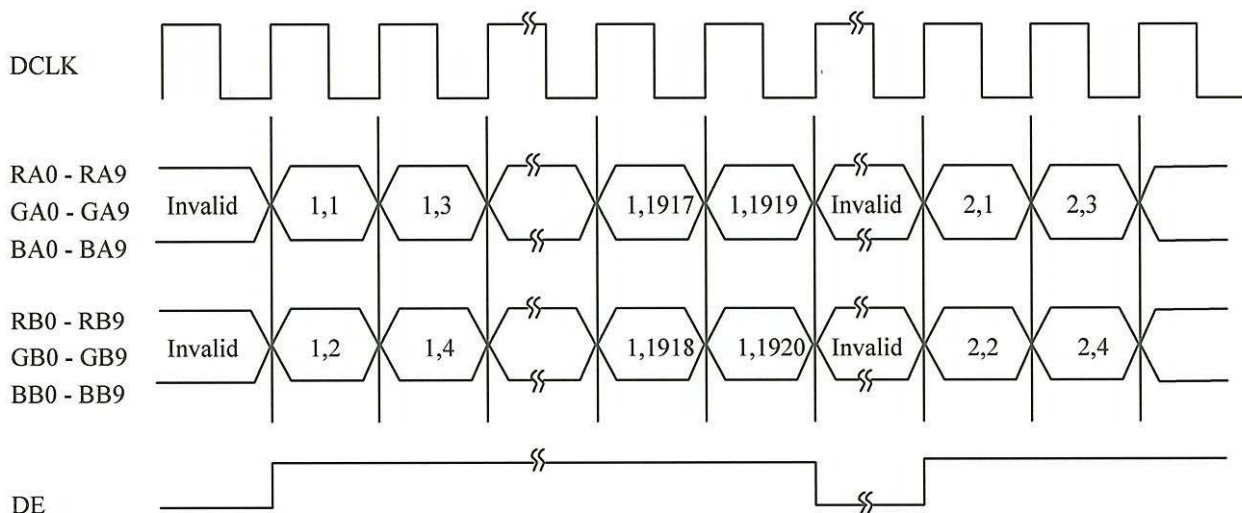
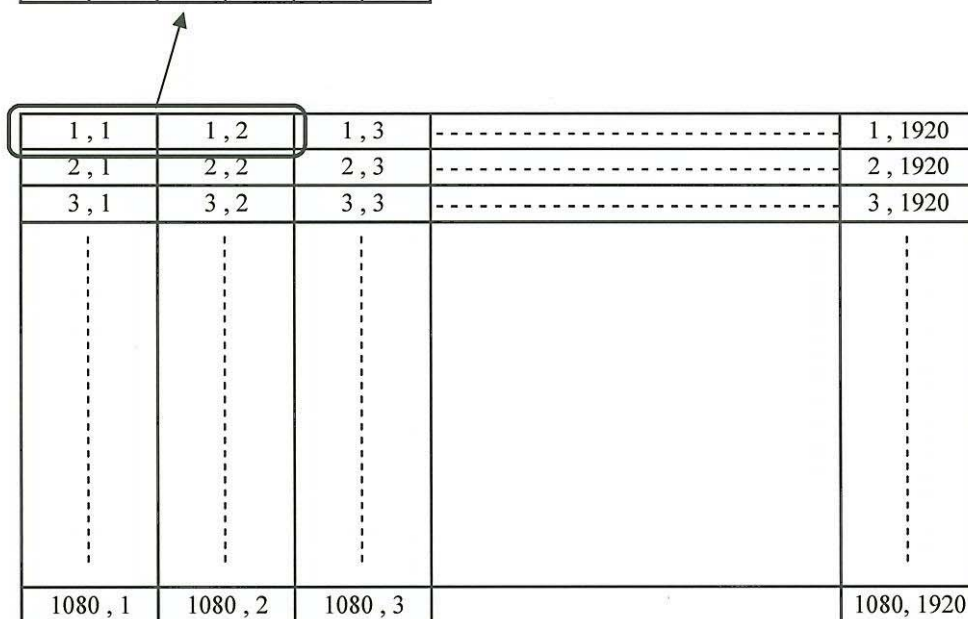
5. 4 Correspondence between input data and display image

Based on IPS Alpha Technology, Ltd. Standard Module

Display data of adjacent one pixel is latched during one cycle of DCLK.



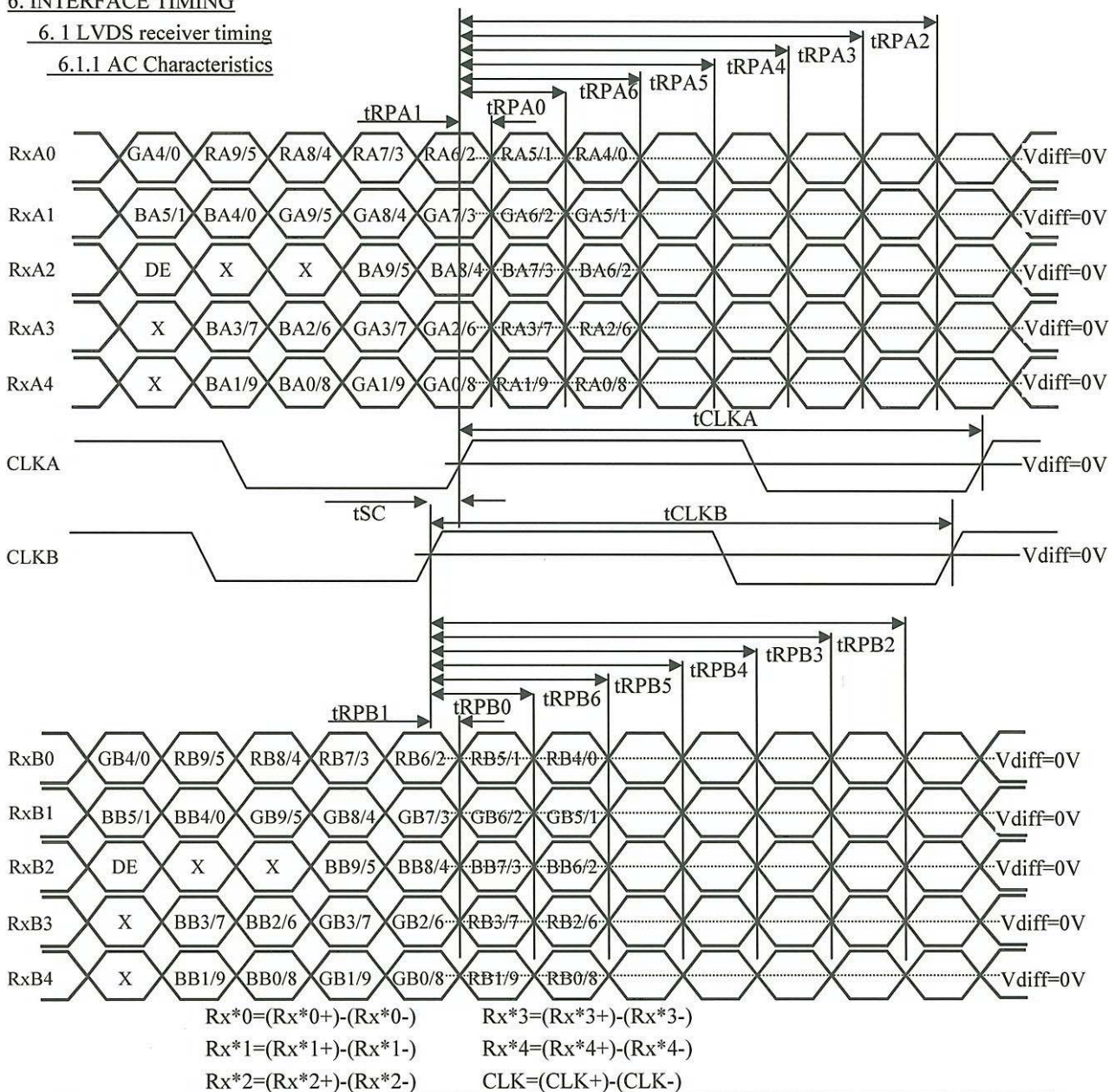
ODD pixel : RA0 - RA9 : R data
 GA0 - GA9 : G data
 BA0 - BA9 : B data
 EVEN pixel RB0 - RB9 : R data
 GB0 - GB9 : G data
 BB0 - BB9 : B data



6. INTERFACE TIMING

6.1 LVDS receiver timing

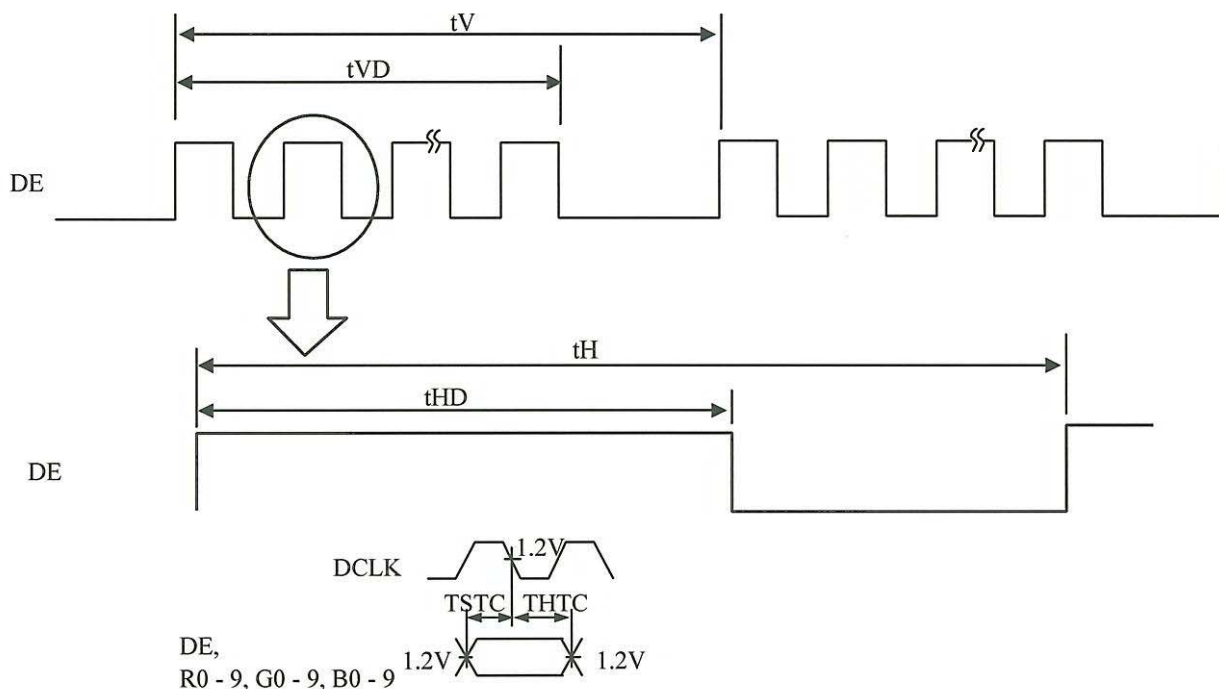
6.1.1 AC Characteristics



Item	Symbol	Min	Typ	Max	Unit	Note	
CLK	Frequency	DCLK	128	132	135	MHz	=1/tCLK
	CLK Skew	tSC	-2.0	0	2.0	ns	
Rx*0	0 data position	tRP0	1/7tCLK - 0.25	1/7tCLK	1/7tCLK + 0.25	ns	
	1st data position	tRP1	-0.25	0	0.25		
	2nd data position	tRP2	6/7tCLK - 0.25	6/7tCLK	6/7tCLK + 0.25		
	3rd data position	tRP3	5/7tCLK - 0.25	5/7tCLK	5/7tCLK + 0.25		
	4th data position	tRP4	4/7tCLK - 0.25	4/7tCLK	4/7tCLK + 0.25		
	5th data position	tRP5	3/7tCLK - 0.25	3/7tCLK	3/7tCLK + 0.25		
6th data position	tRP6	2/7tCLK - 0.25	2/7tCLK	2/7tCLK + 0.25			

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6.2 Synchronization signal timing



Note 1) Reference level for each timing signal is 1.2 V unless it is stated on the chart, high level voltage(VIH) and low level voltage(VIL) are defined as follows:

$$VIH \geq 2.0 V \quad VIL \leq 0.8 V$$

2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.

I)120Hz

2pxl/clock

Item	Symbol	Min	Typ	Max	Unit	Note
DE	Vertical Frequency	fV	115	120	125	Hz
	Vertical Period	tV	1090	1100	1150	tH
	Vertical Valid	tVD	1080			tH
	Horizontal Frequency	fH	127	132	134	kHz
	Horizontal Period	tH	972	1000	1035	tCLK
	Horizontal Valid	tHD	960			tCLK

II)100Hz

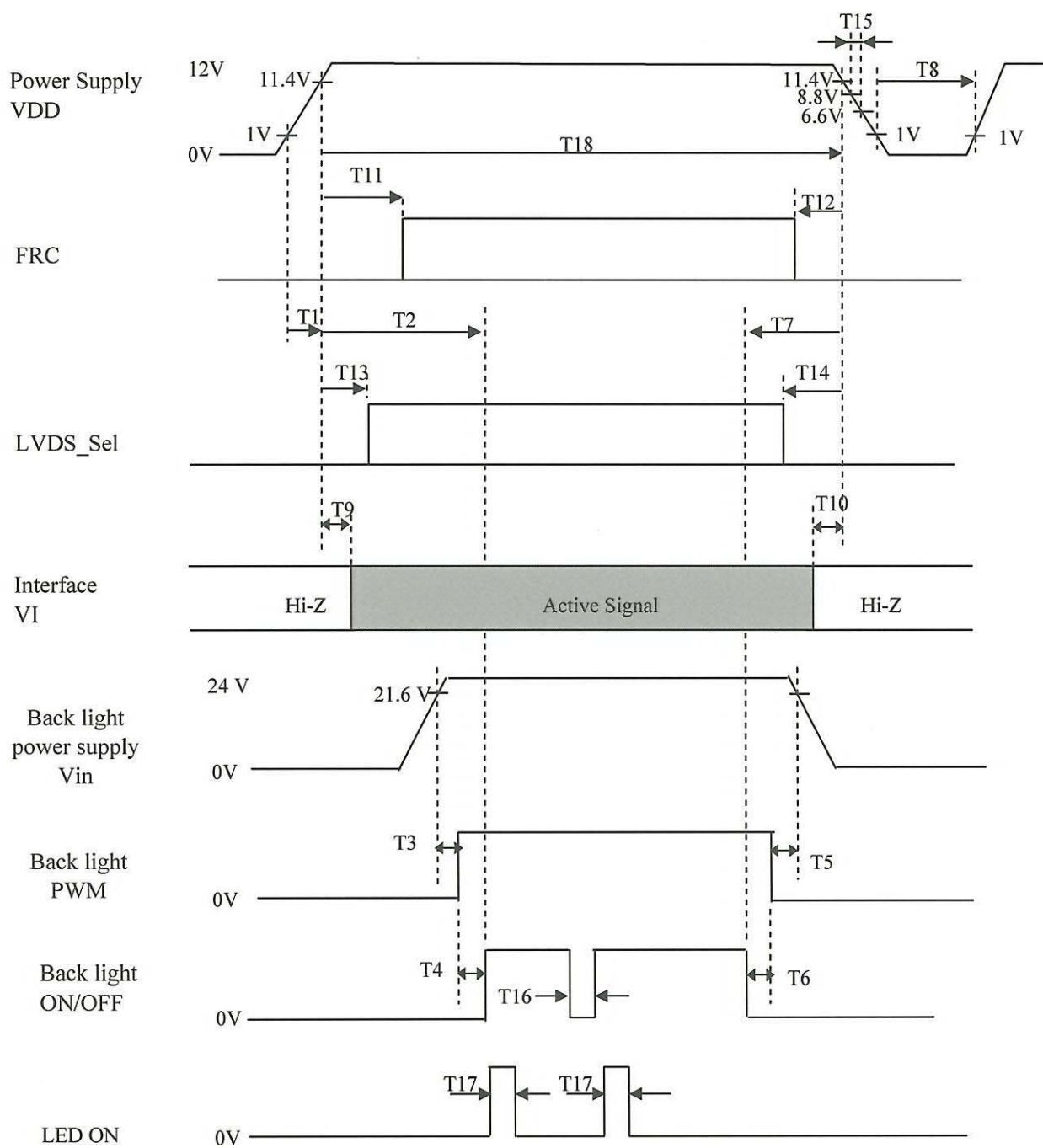
2pxl/clock

Item	Symbol	Min	Typ	Max	Unit	Note
DE	Vertical Frequency	fV	93	100	105	Hz
	Vertical Period	tV	1310	1320	1370	tH
	Vertical Valid	tVD	1080			tH
	Horizontal Frequency	fH	127	132	134	kHz
	Horizontal Period	tH	972	1000	1035	tCLK
	Horizontal Valid	tHD	960			tCLK

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6.3 Timing between interface signals power supply

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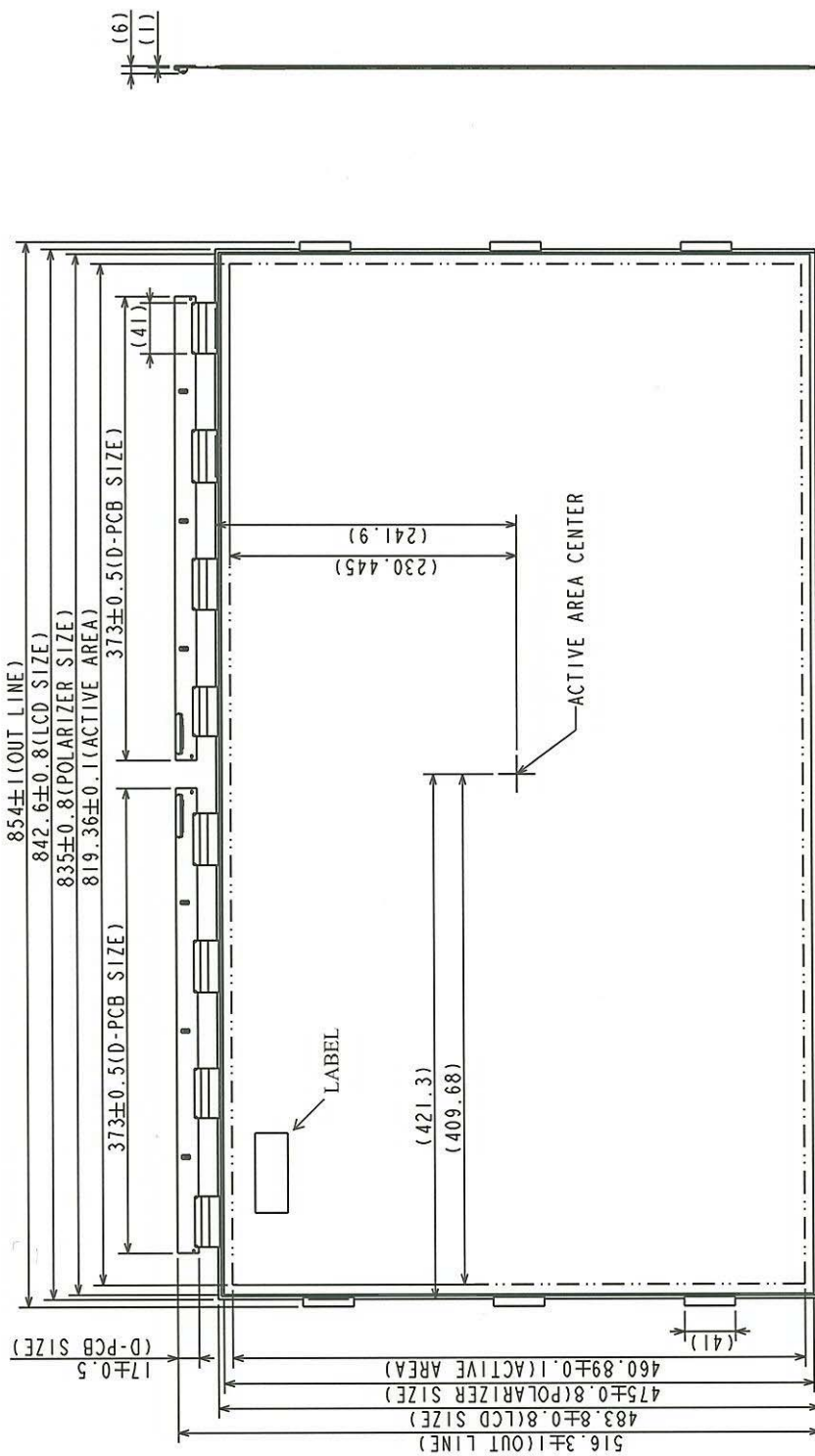
$0 \leq T1 \leq 10$	$0 \leq T7$	$0 \leq T10$	$T13 \leq T2 - 150$	$T16 > 500$ (wait to the restart)
$500 \leq T2$	$1000 \leq T8$	$T11 \leq T2 - 150$	$T14$ don't care	$T17 = (4.2s \text{ typ } (Ta = 25^\circ C))$
$0 < T3, T4, T5, T6$	$30 \leq T9$	$T12$ don't care	$20 < T15$	$T18 > 500$

Unit : ms

- Note 1) T16 : Wait to the restart
 2) T17 : LED lighting period

7. DIMENSIONAL OUTLINE

(1) FRONT VIEW I



Note 1) The dimension in a parenthesis is a reference value
 2) Unspecified tolerance to be ± 0.8

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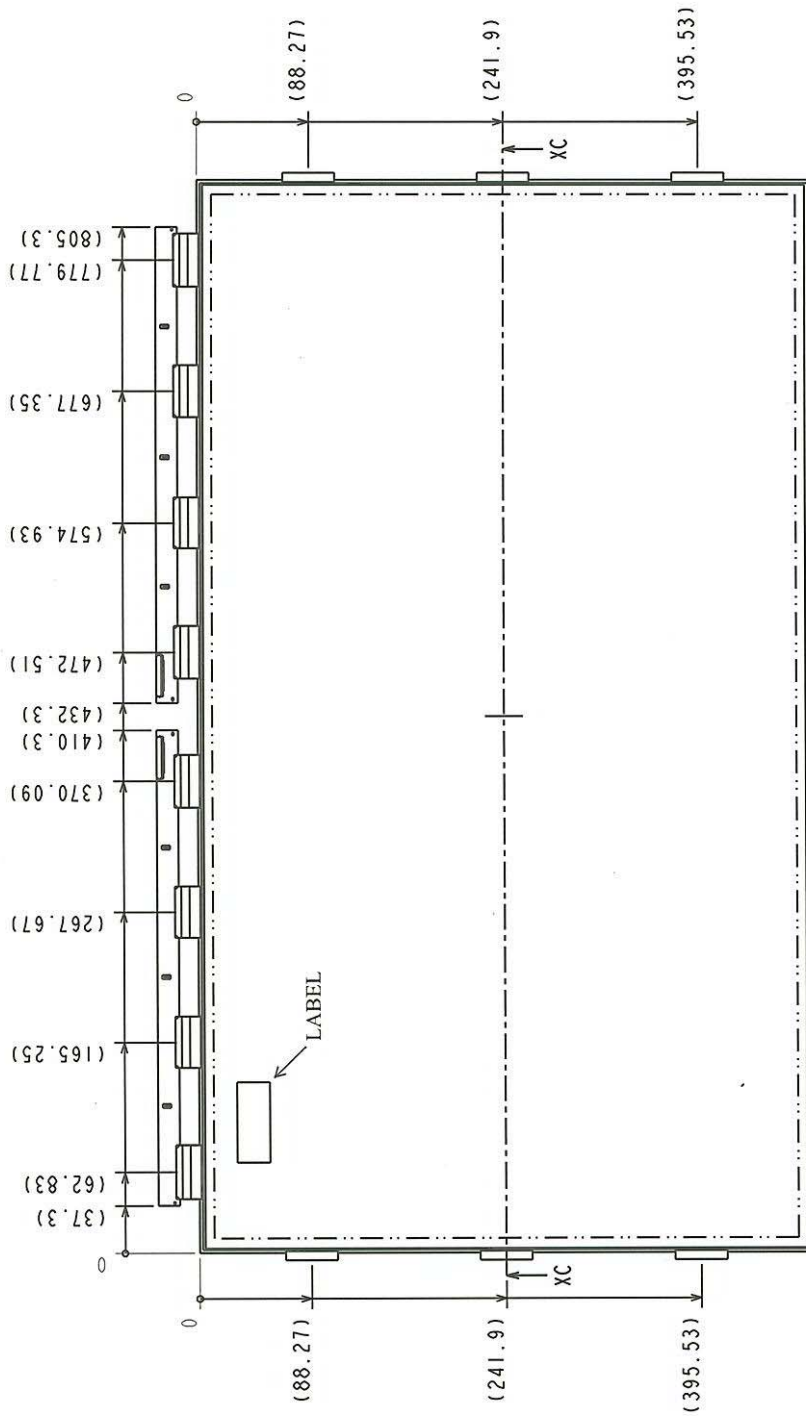
Date Jul. 22, 2010

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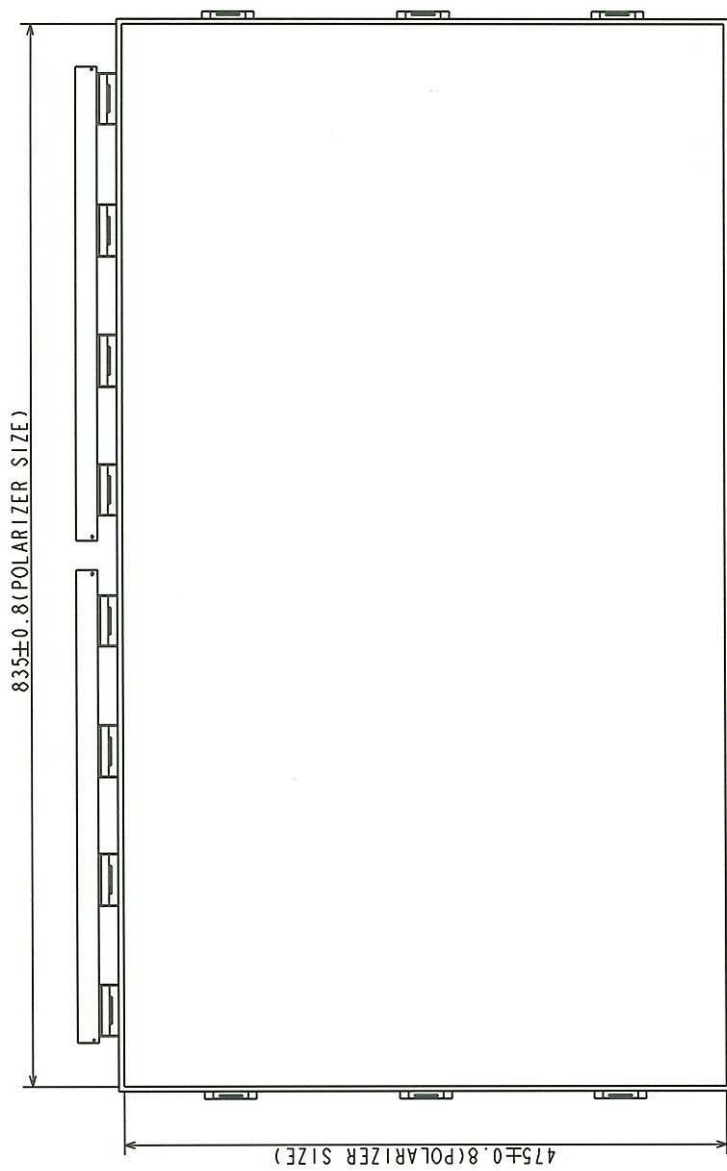
(1) FRONT VIEW 2



Section XC-XC
(2:1)

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(2)BACK VIEW



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