Product Specification of PDP Module

CUSTOMER APPROVAL SPECIFICATION

(●) Preliminary Specification
( ) Final Specification

Title	PDP50T4 (50” HD PDP MODULE)

Customer	-
Model Name	PDP50T4T010.ASBBB
Part No.	EAJ61908544
Customer	
Model Name	
Part No.	
Customer	
Model Name	
Part No.	
Customer	
Model Name	
Part No.	

Supplier	PDP Division
Model Name	PDP50T4T010.ASBBB
Part No.	EAJ61908544
Supplier	
Model Name	
Part No.	
Supplier	
Model Name	
Part No.	
Supplier	
Model Name	
Part No.	

Signature / Date	
Approved by	
Please return 1 copy for our confirmation With your signature	

Signature / Date	
Approved by	
PDP Division LG Electronics Inc.	

Confidential

Record of Revisions

Revision No.	Effective Date	Comments
0.0	2013.03.30	- Established

CONTENTS

0. Warnings and Cautions

✓ WARNING indicates hazards that may lead to death or injury if ignored.
✓ CAUTION indicates hazards that may lead to injury or damage to property if ignored.

1) This product uses a high voltage (450 V max.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage is dropped to a sufficiently low level.

2) Do not supply a voltage higher than that specified to this product. This may damage the product and may cause a fire.

3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where flammable materials surround it. Do not install or use the product in a location that does no satisfy the specified environmental conditions. This may damage the product and may cause a fire.

4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the products it may cause fire or electric shock.

5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If noting is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.

6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunction.

7) Do not pull out or insert the power cable from/to an outlet with wet hands. It may cause electric shock.

8) Do not damage or modify the power cable. It may cause fire or electric shock.

9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.

10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

CAUTION

❑ General

1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.

2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries of electric shock.

3) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.

4) Before disconnecting cable from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.

5) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.

6) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.

7) The temperature of the glass surface of the display may rise to 80°C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

8) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.

9) If you glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.

10) Do not place an object on the glass surface of the display. The glass may break or be scratched.

❑ Design

1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.

2) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult LGE in advance.

3) This product emits near infrared rays (800 to 1000nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

❑ Design (continued)

4) This product uses high-voltage switching and a high –speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

5) **The materials which contain sulfur are forbidden to use, because they may damage PDP module**.

6) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

7) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

8) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

9) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

10) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit board. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

11) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

12) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

13) If this product is used as a display board to display a static image, “image sticking” occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by reducing signal level difference between bright area and less bright area through signal processing.

14) In case of AC PDP driving mechanism, Because the brightness of output is not always proportional to input signals. Therefore the non-linearity of gray can occasionally be observed in certain gray levels as well as Contour and Error Diffusion Noise can be appeared when a dark picture is on the screen especially. These are phenomena that can be observed on the PDP driving mechanism. With simple adjustment to picture brightness control, these can be reduced considerably.

15) Because of the need to control the power consumption on the PDP driving mechanism, the APL (Average Picture Level) mode was equipped. Thus, as the picture on the screen changes, there can be slightly switched in brightness. This also is a phenomenon that can be observed on the PDP driving mechanism.

16) This product is designed to LGE’s “Standard” quality grade. If you wish to use the product for applications outside the scope of the “Standard” quality grade, be sure to consult LGE in advance to assess the technological feasibility before starting to design your system.

❑ USE

1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.

2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.

3) PDP ’s brightness and contrast ratio is lower than that of the CRT. The picture is dimmer with surrounding light and better for viewing in dark condition.

4) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.

5) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.

6) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2hours (aging).

7) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.

8) Do not tilt or turn upside down while the module package is carried, the product may be damaged.

9) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

❑ Others

1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.

2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult LGE in advance.

1. GENERAL DESCRIPTION

❑ DESCRIPTION

The PDP50T4#### is a 50-inch 16:9 color plasma display module with resolution of 1024(H) × 768(V) pixels.

❑ APPLICATIONS

- ✓ Public information display
- ✓ Video conference systems
- ✓ Education and training systems

(Image)

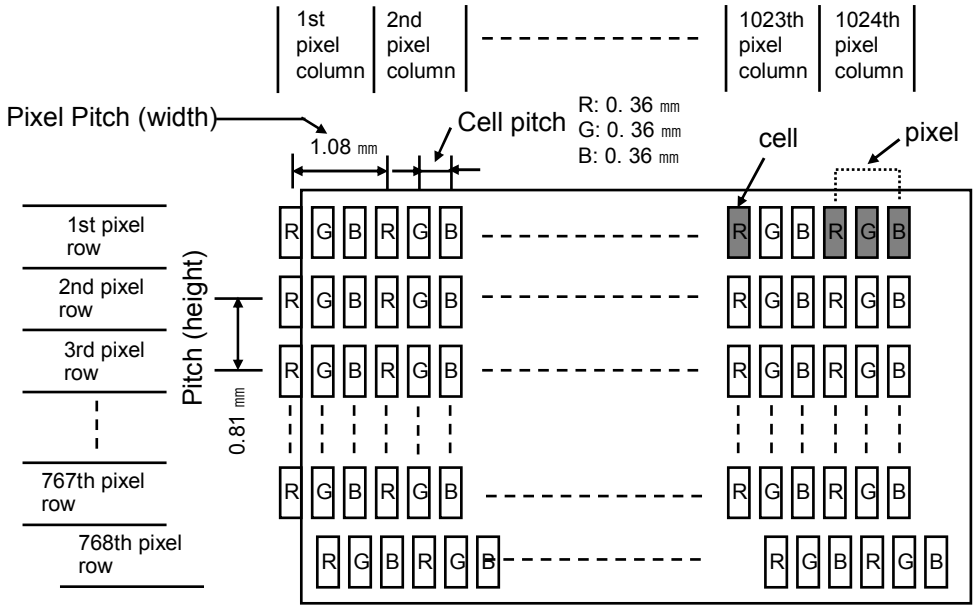
❑ ELECTRICAL INTERFACE OF PLASMA DISPLAY

The PDP50T4#### requires only 8/12bits of digital video signals for each RGB color.
In addition to the video signals, five different DC voltages are required to operate the display.

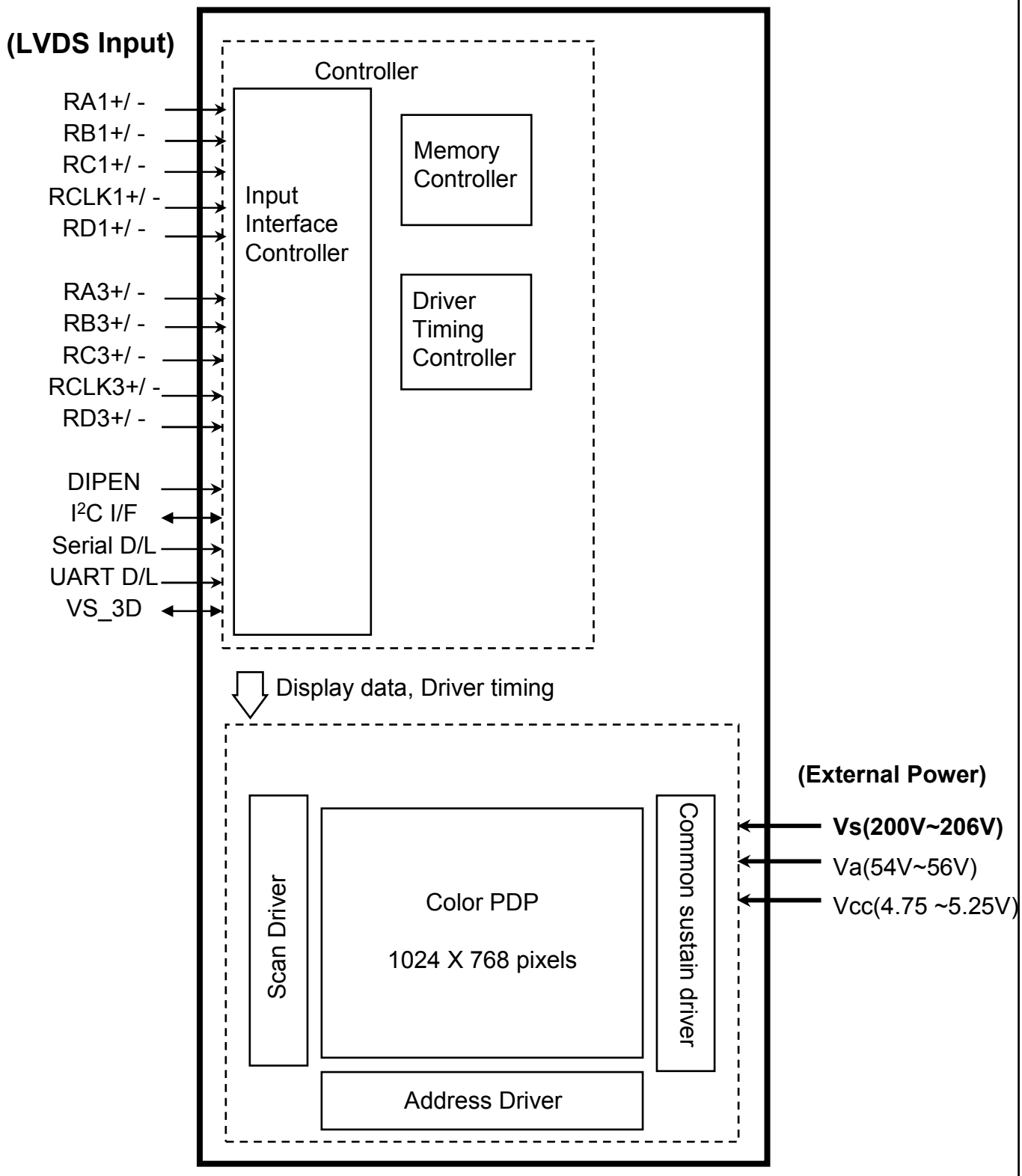
❑ GENERAL SPECFICATIONS

✓ Model Name	PDP50T4#### (50T4 Model)
✓ Number of Pixels	1024(H) X 768(V) (1pixel=3 RGB cells)
✓ Pixel Pitch	1080 ㎛ (H) X 810 ㎛ (V)
✓ Cell Pitch	360 ㎛ (H) X 810 ㎛ (V)
✓ Display Area	1105.92(H) X 622.08(V) ±0.5 (mm)
✓ Outline Dimension	1156 ±1.5 (H) X 677.6 ±1 (V) X 37.9(D) ±1.5 (mm)
✓ Pixel Type	RGB Closed (Well) type
✓ Number of Gradations	10bit : (R)1024 X (G)1024 X (B)1024 (1.07billion Color) 8bit : (R)256 X (G)256 X (B)256 (16.78 Million Color)
✓ Weight	Glass filter 14.65±0.5 (Kg) : Net Glass filter 250.2±5 (Kg) : Gross
✓ Aspect Ratio	16:9
✓ Power Consumption	Max. 300 W (Full-White)

✓ Display Dot Diagram



❑ BLOCK DIAGRAM



Applied Voltage is set by input voltage of several board

☞ Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel.

2. ELECTRICAL SPECIFICATIONS

❑ Absolute Power Specifications

Item	Symbol	Condition	Min.	Max.	Unit	Remarks
Logic Voltage	Vcc	25°C	-	6	V	
Address Voltage	Va	25°C	-	57	V	
Sustain Voltage	Vs	25°C	-	215	V	

❑ Input Power Specifications

➢ Logic Power Supply (Vcc)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	-	4.75	5	5.25	V
Voltage Stability	-	-	-	± 3.0	%
Average Current	-	0.1	-	2.5	Amean
Ripple	-	-	-	30	mVp-p
Noise	-	-	-	300	mVp-p

➢ Address Power Supply (Va)

Item	Condition & Remarks	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	54	55	56	V
Voltage Stability	-	-	-	± 1.5	%
Average Current	Variable with the image	0.01	-	2.0	A_{mean}
Ripple & Noise	-	-	-	300	mV_{p-p}

☞ Max current of Va is measured when 2-dot on/off pattern is displayed.

➢ Sustain Power Supply(Vs)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	200	-	206	V
Voltage Stability	-	-	-	± 1.0	%
Peak Current	-	-	-	21	A
Average Current	Dependent on the characteristics of each PDP	0.1	-	1.4	A_{mean}
Voltage Regulation	At the peak current	-	-	3	V
Ripple & Noise	-	-	-	500	mVp-p

☞ Voltage should be set to a specified value which is indicated on the label attached to the module.

❑ Input Power Specifications (Continued)

➢ Writing Scan Bias Power Supply (-Vy)

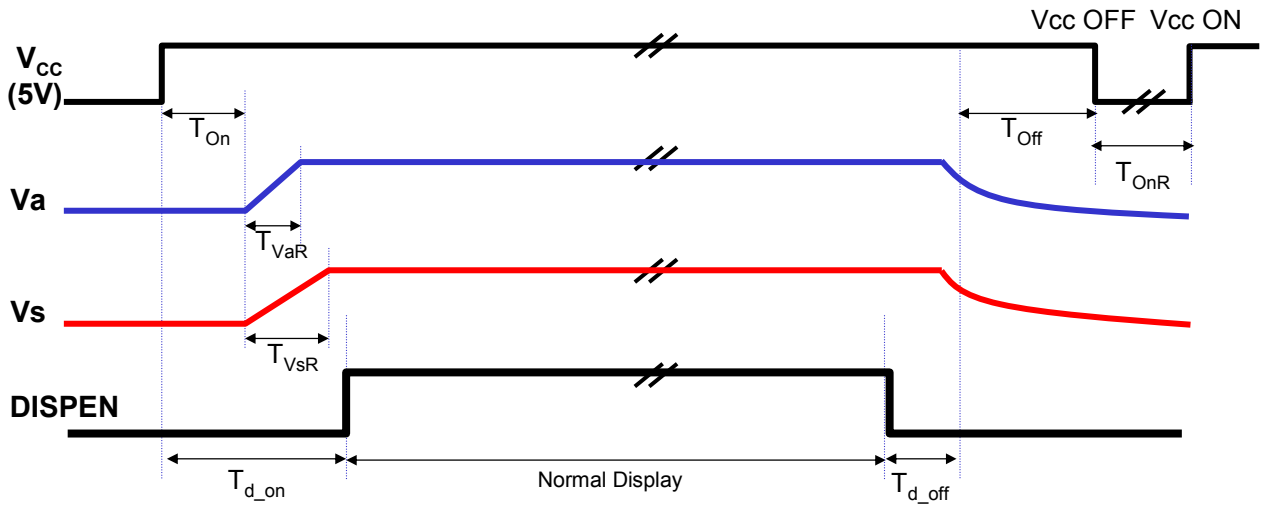
Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	-198	- 190	-188	V
Voltage Stability	-	-	-	±3.0	%
Average Current	-	-	-	100	mA
Voltage Regulation	At the peak current	-	-	2	V
Ripple & Noise	-	-198	- 190	-188	V

➢ Z-bias Power Supply (Vzb)

Item	Condition	Min.	Typ.	Max.	Unit
Adjustable Range	Dependent on the characteristics of each PDP	115	120	135	V
Voltage Stability	-	-	-	±3.0	%
Average Current	-	-	-	250	mA
Voltage Regulation	At the peak current	-	-	5	V

☞ Voltage should be set to a specified value which is indicated on the label attached to the module.

❑ Power Supply Sequence (In Case of Discharge resistance remove)



Symbol	Description	Min.	Typ	Max.	unit
T_{On}	Time interval between 90% of Vcc and 10% of Vs when Power On	200	250	300	msec
T_{Off}	Time interval between 90% of Vs and 10% of Vcc when Power Off	2000	2500		msec
T_{OnR}	Time interval between 20% of Vcc OFF (falling) to 20% of Vcc On (rising) when Power On	2000			msec
T_{VaR}	Rising Time of Va (10% to 90%)	50		200	msec
T_{VsR}	Rising Time of Vs (10% to 90%)	50		200	msec
T_{d_on}	Time interval between 90% of Vcc and DISPEN rising edge when Power On	2000			msec
T_{d_off}	Time interval between DISPEN falling edge and 90% of Vs when Power Off	800	1000	6000	msec
$T_{d\_off\_I2C}$	Time between DISPEN OFF to I2C ON (off sequence)			700	msec

☞ Vcc should be lower than 0.1V when turn on just after turn off.

☞ If power sequence does not meet to above sequence diagram, PDP drivers may be damaged permanently.

☞ If Vs is off on purpose (or not), for example recording mode, Vcc should be off before turn on again.
Again, When you are turn on, 5V on. And then, Va, Vs on.

☞ AC off Condition is treated as the exception. But It can make optical noise in a short time, for example uncontrollable dot and image sticking, etc.

☞ DISPEN signal shall be certainly applied after Vs On..

☞ T_{off} Min time is except for turn Off using AC Power supply.

❑ LVDS Signal and LVDS Receiver

➢ Definitions and Functions of LVDS Signal

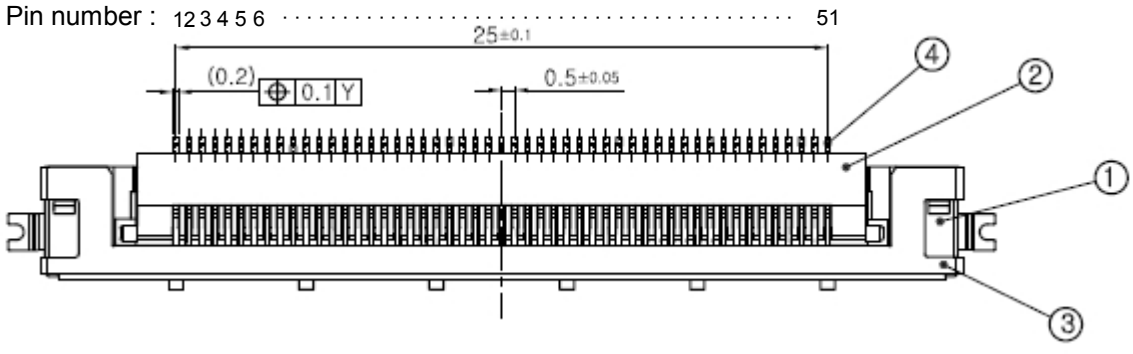
Symbol	Function and Description
RA1+	Channel A Pos. Receiver Input for 2D video signal
RA1-	Channel A Neg. Receiver Input for 2D video signal
RB1+	Channel B Pos. Receiver Input for 2D video signal
RB1-	Channel B Neg. Receiver Input for 2D video signal
RC1+	Channel C Pos. Receiver Input for 2D video signal
RC1-	Channel C Neg. Receiver Input for 2D video signal
RD1+	Channel D Pos. Receiver Input for 2D video signal
RD1-	Channel D Neg. Receiver Input for 2D video signal
RE1+	Channel E Pos. Receiver Input for 2D video signal
RE1-	Channel E Neg. Receiver Input for 2D video signal
RCLK1+	Clock Pos. Receiver Input for 2D video signal
RCLK1-	Clock Neg. Receiver Input for 2D video signal

➢ 2D Video Input Connector (P106) Connector Type : C-NET, 3018-56151 51P

For 2D video signal

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	GND	18	GND	35	RCLK3-
2	Serial Download CLK	19	RCLK1-	36	RCLK3+
3	Serial Download Data	20	RCLK+	37	GND
4	I^2C_SCLK	21	GND	38	RD3-
5	DISPEN	22	RD-	39	RD3+
6	I^2C_SDATA	23	RD+	40	GND
7	NC	24	GND	41	GND
8	NC	25	GND	42	GND
9	NC	26	GND	43	GND
10	NC	27	GND	44	GND
11	GND	28	RA3-	45	GND
12	RA1-	29	RA3+	46	NC
13	RA1+	30	RB3-	47	NC
14	RB1-	31	RB3+	48	UART Rx
15	RB1+	32	RC3-	49	UART Tx
16	RC1-	33	RC3+	50	VS_3D
17	RC1+	34	GND	51	GND

3018-56151 51P Pin number (Top view)



① Housing, ② Actuator, ③ Shell, ④ Pin

1) When using the 2D video signal ➔ Differential Signal (RA3, RB3, RC3, RD3, RCLK3) is not used.

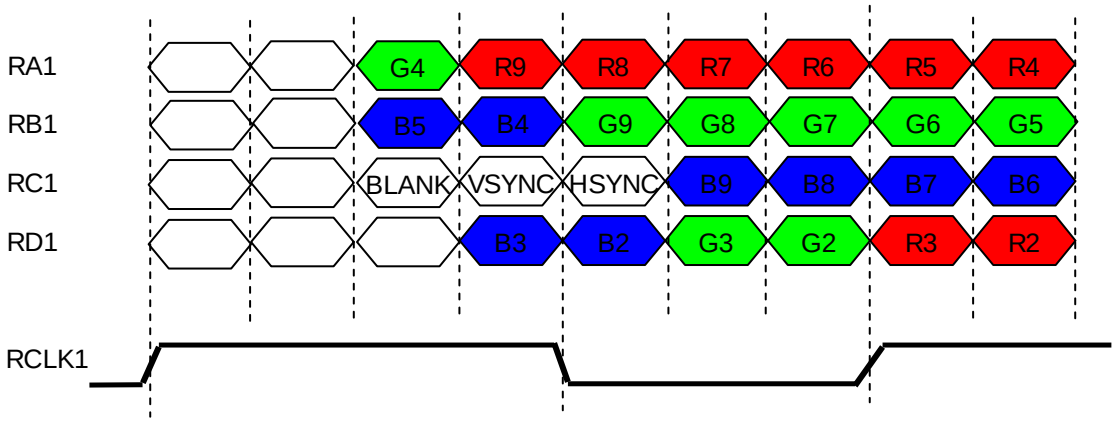
❑ **LVDS Signal and LVDS Receiver** (continued)

For 2D video signal

Symbol	Function and Description
R9~R2	8 bit Red video signal (R9 : MSB, R2 : LSB)
G9~G2	8 bit Green video signal (G9 : MSB, G2 : LSB)
B9~B2	8 bit Blue video signal (B9 : MSB, B2 : LSB)
PIX_CLK	Clock Signal which synchronous to video signal
$\overline{\text{Vsync}}$	Vertical synchronous signal
$\overline{\text{Hsync}}$	Horizontal synchronous signal
$\overline{\text{BLANK}}$	'HIGH' level : data is valid, 'LOW' level : data is invalid
Dispen	The panel will not malfunction, if DISPEN is high at start up

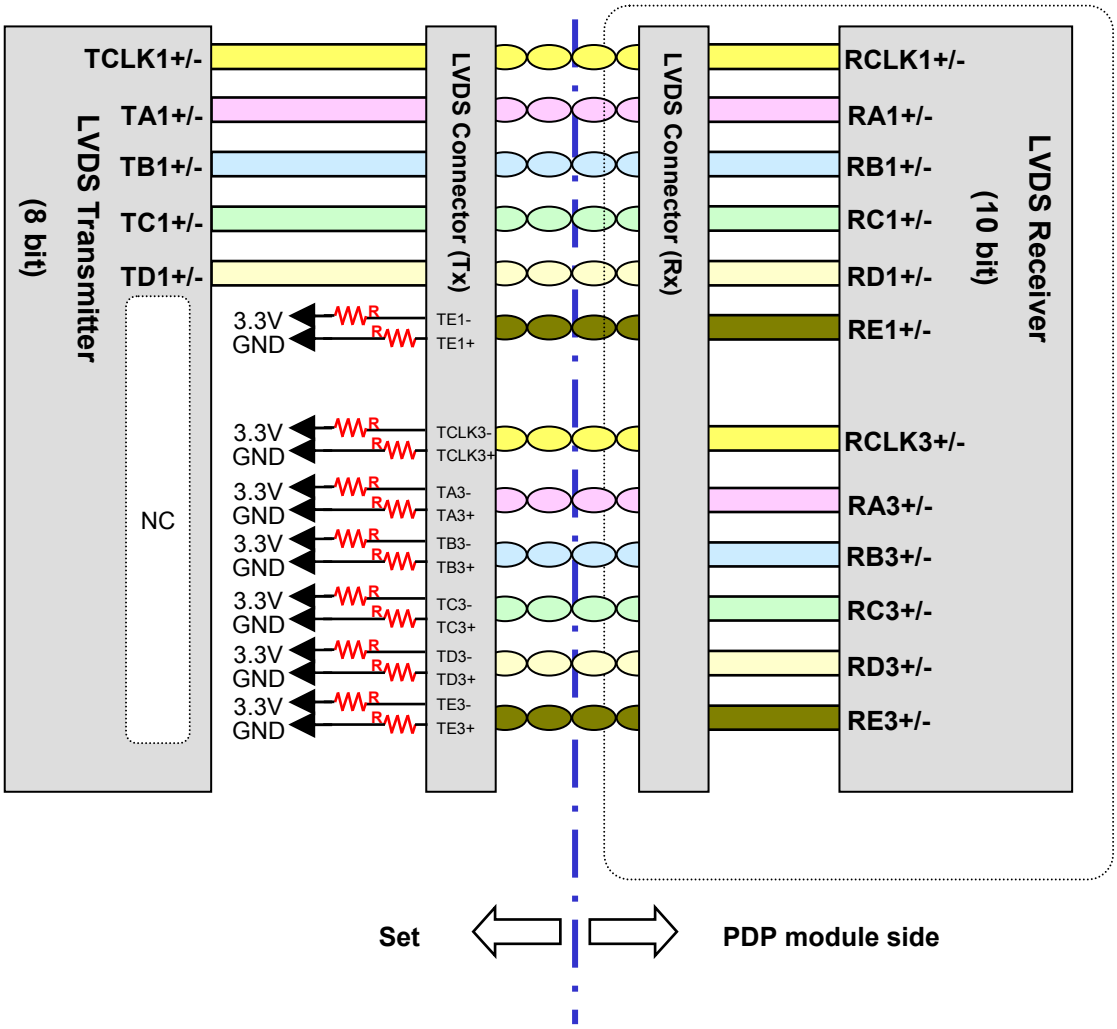
☞ Each of the RGB signals can be changed with the Gamma Mode.
☞ You should not adjust any inverse gamma compensation. Because the inverse gamma compensation is adjusted in the PDP side already.
☞ In preparing the LDVS signal cable, The twisted pair cable should be used for the differential signal.
☞ Dispen signal is HIGH (3.3V) in normal state. However Dispen can be inversed to LOW(GND) from time to time.

LVDS-Rx IP Signal mapping for 8 bit video signal



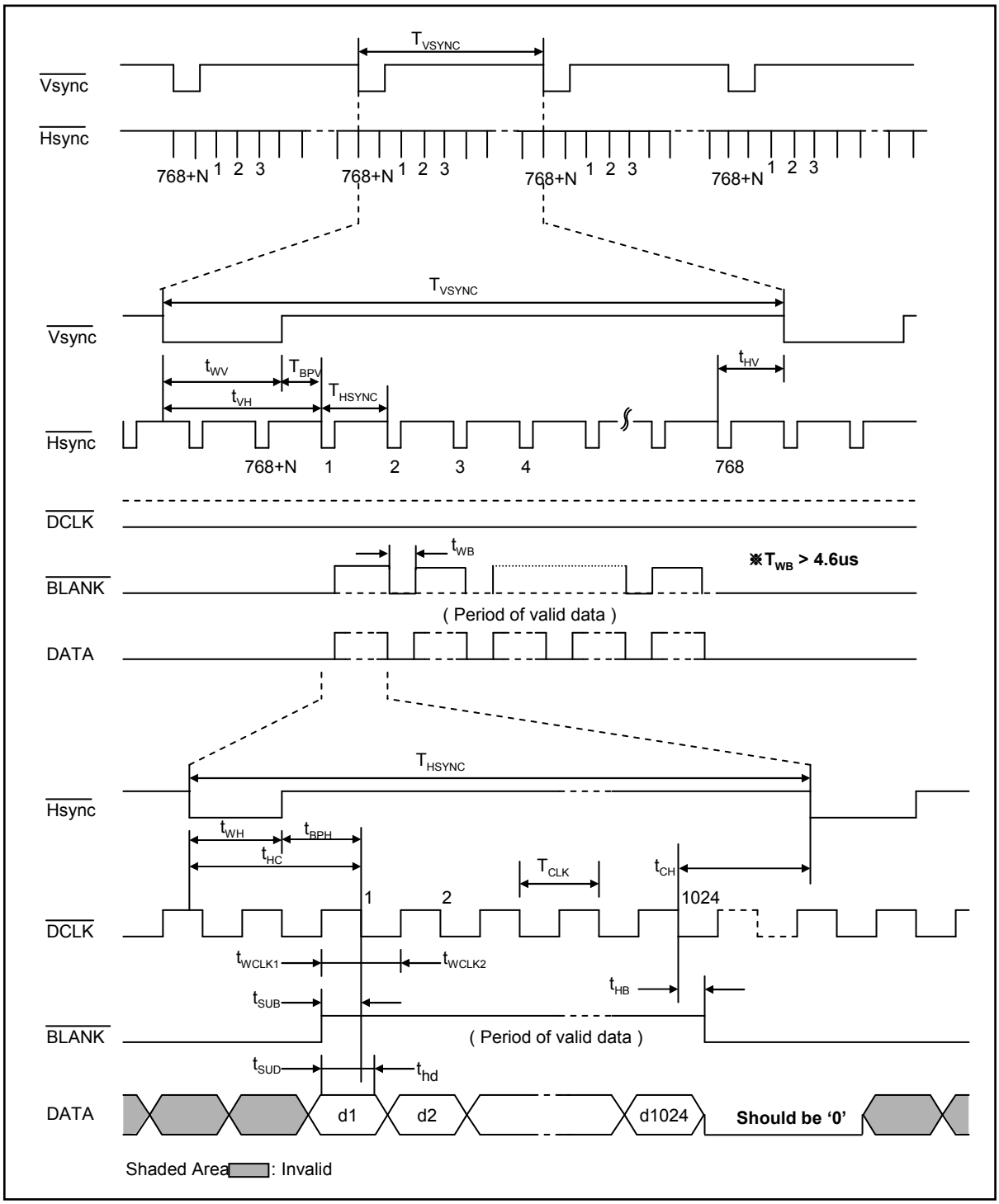
1) RE1 is not used for 8bit video signal.

For 2D 8bit application



1) To use 2D video signal, “TCLK3+, TA3+, TB3+, TC3+, TD3+, TE3+” are to be tied to ground signal and “TCLK3-, TA3-, TB3-, TC3-, TD3-, TE3-” are to be tied to 3.3V signal.
2) Pull up / down R value is recommended 10kΩ

❑ Input Signal Timing Diagram (Non-interlaced Signal)



☞ T_{WB} must be longer than 4.6μs

❑ Input Signal Timing Specification

➢ 60Hz Mode

No.	Symbol	Min.	Typ.	Max.	Unit	Remark
1	T_{vsync}	16.531 (799H)	16.676 (806H)	16.820 (813H)	ms (H)	1 frame = 59.47Hz ~ 60.52Hz
2	t_{wv}	82 (4H)	124 (6H)	165 (8H)	μs (H)	
3	t_{vh}	393 (19H)	455 (22H)	517 (25H)	μs (H)	$t_{vh} \geq 19H$
4	t_{hv}	103(5H)	331(16H)		μs (H)	
5	T_{hsync}	20.63 (1340D)	20.69 (1344D)	20.75 (1348D)	μs (D)	
6	t_{wh}	2.03(132D)	2.09(136D)	2.15(140D)	μs (D)	
7	t_{hc}	4.49 (292D)	4.55(296D)	4.62(300D)	μs (D)	
8	t_{ch}		0.36(24D)		μs (D)	
9	t_{clk}	15.2 (65.8MHz)	15.4 (65MHz)	15.6 (64MHz)	ns	$t_{clk} = t_{wclk1} + t_{wclk2}$
10	t_{wclk1}		7.7		ns	
11	t_{wclk2}		7.7		ns	
12	t_{sub}		7.7		ns	$t_{sub} \leq t_{hc}$
13	t_{hb}		7.7		ns	$t_{hb} \leq t_{ch}$
14	t_{sud}		7.7		ns	
15	t_{hd}		7.7		ns	

☞ Min. & Max. of each signal is measured value when other signal is Typ.

☞ When Timing is changed, Recommend even value of VSYNC and HSYNC(D, H)

☞ Thv (Vertical Front Porch) ≥ 5H

☞ Tvh (Vertical sync width + Vertical Back Porch) ≥ 19H

❑ Input Signal Timing Specification (Continued)

➢ 48Hz Mode

No.	Symbol	Min.	Typ.	Max.	Unit	Remark
1	T_{vsync}	20.627 (997H)	20.834 (1007H)	21.062 (1018H)	ms (H)	1 frame = 47.50Hz ~ 48.50Hz
2	t_{wv}	82 (4H)	124 (6H)	165 (8H)	μs (H)	
3	t_{vh}	393 (19H)	455 (22H)	517 (25H)	μs (H)	$t_{vh} \geq 19H$
4	t_{hv}	103 (5H)	4487 (217H)		μs (H)	
5	T_{hsync}	20.63 (1340D)	20.69 (1344D)	20.75 (1348D)	μs (D)	
6	t_{wh}	2.03(132D)	2.09(136D)	2.15(140D)	μs (D)	
7	t_{hc}	4.49 (292D)	4.55(296D)	4.62(300D)	μs (D)	
8	t_{ch}		0.36(24D)		μs (D)	
9	t_{clk}	15.2 (65.8MHz)	15.4 (65MHz)	15.6 (64MHz)	ns	$t_{clk} = t_{wclk1} + t_{wclk2}$
10	t_{wclk1}		7.7		ns	
11	t_{wclk2}		7.7		ns	
12	t_{sub}		7.7		ns	$t_{sub} \leq t_{hc}$
13	t_{hb}		7.7		ns	$t_{hb} \leq t_{ch}$
14	t_{sud}		7.7		ns	
15	t_{hd}		7.7		ns	

☞ Min. & Max. of each signal is measured value when other signal is Typ.

☞ When Timing is changed, Recommend even value of VSYNC and HSYNC(D, H)

☞ Thv (Vertical Front Porch) ≥ 5H

☞ Tvh (Vertical sync width + Vertical Back Porch) ≥ 19H

❑ Input Signal Timing Specification (Continued)

➢ 50Hz Mode

No.	Symbol	Min.	Typ.	Max.	Unit	Remark
1	T_{vsync}	19.800 (957H)	20.007 (967H)	20.214 (977H)	ms (H)	1 frame = 49.49Hz ~ 50.52Hz
2	t_{wv}	82 (4H)	124 (6H)	165 (8H)	μs (H)	
3	t_{vh}	393 (19H)	455 (22H)	517 (25H)	μs (H)	$t_{vh} \geq 19H$
4	t_{hv}	103 (5H)	3660 (177H)		μs (H)	
5	T_{hsync}	20.63 (1340D)	20.69 (1344D)	20.75 (1348D)	μs (D)	
6	t_{wh}	2.03(132D)	2.09(136D)	2.15(140D)	μs (D)	
7	t_{hc}	4.49 (292D)	4.55(296D)	4.62(300D)	μs (D)	
8	t_{ch}		0.36(24D)		μs (D)	
9	t_{clk}	15.2 (65.8MHz)	15.4 (65MHz)	15.6 (64MHz)	ns	$t_{clk} = t_{wclk1} + t_{wclk2}$
10	t_{wclk1}		7.7		ns	
11	t_{wclk2}		7.7		ns	
12	t_{sub}		7.7		ns	$t_{sub} \leq t_{hc}$
13	t_{hb}		7.7		ns	$t_{hb} \leq t_{ch}$
14	t_{sud}		7.7		ns	
15	t_{hd}		7.7		ns	

☞ Min. & Max. of each signal is measured value when other signal is Typ.

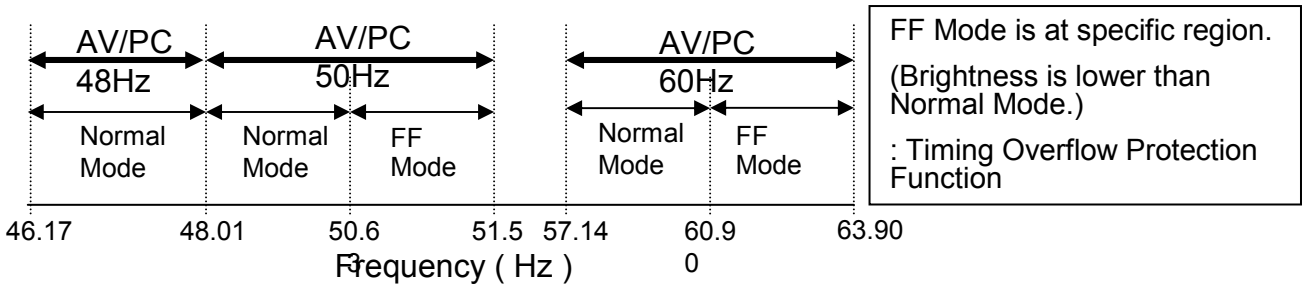
☞ When Timing is changed, Recommend even value of VSYNC and HSYNC(D, H)

☞ Thv (Vertical Front Porch) ≥ 5H

☞ Tvh (Vertical sync width + Vertical Back Porch) ≥ 19H

➢ Brightness Variation Function by Frequency

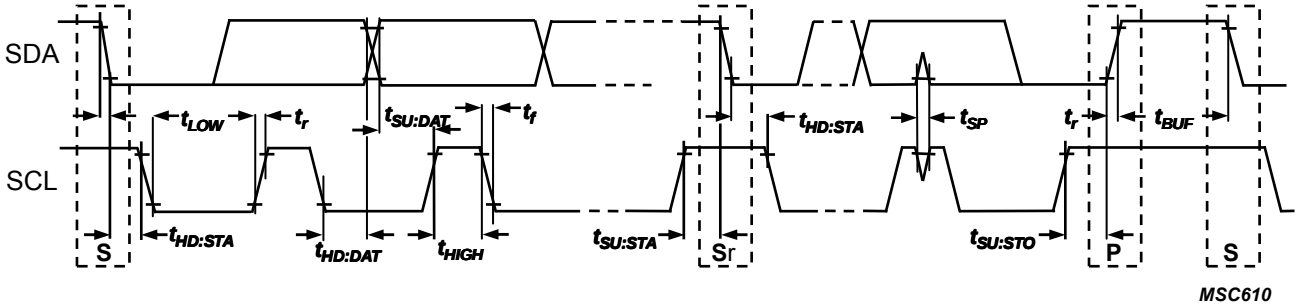
▶ If input Vsync period is longer than normal range, brightness reduction mode operates for protecting waveform overflow.
▶ This function is for special range of input Vsync frequency.



➢ **Min. Max. value of Vsync is the value when timing spec is typical of timing spec(4.51~2)**
➢ **When input Vsync is out of the above frequency range, making mode operates.**
(Making Mode: Vsync, 22msec[45.45Hz] displayed black)

❑ I²C Timing Specification

➢ I²C Timing Diagram



➢ I²C Timing Specification (Characteristics of the SDA and SCL bus lines)

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	kHz
Hold time (repeated) START condition After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	µs
Set-up time for a repeated START condition	f_{SCL}			µs
Data hold time: for CBUS compatible masters for I²C bus devices	$t_{HD;DAT}$	 5.0 0(2)	 - 3.45(3)	 µs µs
DATA Set-up time	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	ns
Fall time of both SDA and SCL signals	t_f			ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	µs
Capacitive load for each bus line	C_b	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	-	V
Noise margin at the High level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	-	V

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table 6 are allowed.

※n/a = not applicable

❑ I²C Timing Specification

➢ I²C Timing Specification (Characteristics of the SDA and SCL I/O stages)

PARAMETER	SYMBOL	STANDARD-MODE		UNIT
		MIN.	MAX.	
LOW level input voltage: fixed input levels VDD-related input levels	VIL	 -0.5 -0.5	 1.5 0.3VDD	 V V
HIGH level input voltage: fixed input levels VDD-related input levels	VIH	 3.0 0.7VDD	 (2) (2)	 V V
Hysteresis of Schmit trigger inputs: VDD > 2V VDD < 2V	Vhys	 n/a n/a	 n/a n/a	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2V VDD < 2V	 VOL1 VOL3	 0 n/a	 0.4 n/a	 V V
Out fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	Tof	-	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	ns
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9VDDmax	Ii	-10	10	MA
Capacitance for each I/O pin	Ci	-	10	pF

Notes

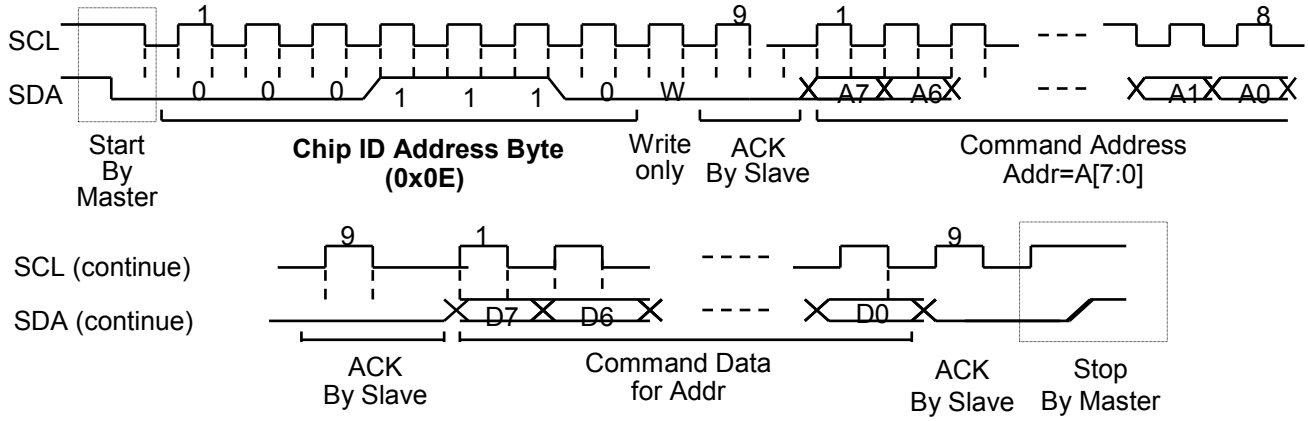
1. Devices that use non-standard supply voltages which do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DD} voltage to which the pull-up resistors R_p are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5$ V.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table 5 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.36 without exceeding the maximum specified t_f.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

※ n/a = not applicable

❑ ASIC I²C Timing & Register Description

➢ Individual data Write mode of I2C control

※ Master: Image Board, Slave: PDP Module



✓ For "Write" function, first 1byte data should be **000 1110 (0)** ← last 1bit is 0(write mode).
✓ Start /Stop condition is generated by Master (=Image B'D).
✓ Before start condition and/or after stop condition, SDA should not be recognized as a valid data.
✓ Start condition : SCL high & SDA transition from H to L
✓ Stop condition : SCL high & SDA transition from L to H

➢ I²C Register Brief

R : Reserved(don't care)

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x07	Bright Mode Registers							
	R	R	R	R	50_2D(2)	60_2D(2)	0	0
0x08	Bright Mode Registers							
	br_mode_50_2D(1:0)		br_mode_60_2D(1:0)		0		0	
0x09	Power Save Mode Registers							
	R	R	ps_mode_50_2D(2:0)			ps_mode_60_2D(2:0)		
0x0A	Power Save Mode Registers							
	R	R	000			000		
0x18	ISM Mode Registers							
	R	R	R	R	R	ism_mode	1	1
0x20	Pattern Generation Registers							
	R	R	0	auto_ pat_gen	R	R	R	R
0x49	Power-Off Sequence							
	R	R	R	R	R	R	R	Power_off

❑ ASIC I²C Timing & Register Description (continued)

➢ Bright Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x07	Bright Mode Registers							
	R	R	R	R	50_2D(2)	60_2D(2)	0	0
0x08	Bright Mode Registers							
	br_mode_50_2D(1:0)		br_mode_60_2D(1:0)		0		0	
Default	0	0	0	0	0	0	0	0

• br_mode_50_2D(2:0) : Bright mode for 2D 50Hz mode
• br_mode_60_2D(2:0) : Bright mode for 2D 60Hz mode

➢ Power Save Mode Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x09	Power Save Mode Registers							
	R	R	ps_mode_50_2D(2:0)			ps_mode_60_2D(2:0)		
0x0A	R	R	000			000		
Default	R	R	0	0	0	0	0	0

• ps_mode_50_2D(2:0) : Power save mode for 2D 50Hz mode
• ps_mode_60_2D(2:0) : Power save mode for 2D 60Hz mode

➢ Power-Off Sequence

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x49	Power-Off Sequence							
	R	R	R	R	R	R	R	power_off

• power_off : power off sequence start , '1' → on , '0' → off

• 0x49 address is a password region , the password must be transferred before use that.
Password : address 0x38, transfer data : 0x19

❑ ASIC I²C Timing & Register Description (continued)

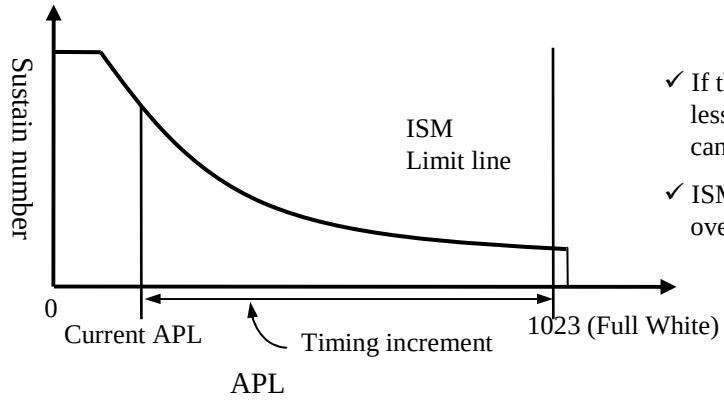
➢ ISM Mode Registers

▷ Image Sticking Minimization Method

ISM_CTRL, BWINV and SCROLL are all Image Sticking Minimization methods.
Two/three of them can be activated at a time, because they operate independently.

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x18	ISM Mode Registers							
	R	R	R	R	R	ism_mode	1	1
Default	R	R	R	R	R	1	1	1

• ims_mode : ISM mode switch (1: ON, 0:OFF)



✓ If there is no movement (APL data variation is less tan ± 5) for 5min. approximately, the brightness can be fallen near to Full White level.

✓ ISM mode doesn't activated when APL is over the ISM limit line.

➢ Pattern Generation Registers

I²C Addr.	I²C Data							
	7	6	5	4	3	2	1	0
0x20	Pattern Generation Registers							
	R	R	0	auto_ pat_gen	R	R	R	R
Default	R	R	0	0	R	R	R	R

• pat_auto_gen : Automatically pattern generation mode switch, 0:OFF, 1:ON
• automatically generated pattern sequence

1) 1 pixel with fore-ground color at the start coordinate
2) full window with foreground
3) Peak window with X-Y coordinates
4) Life Pattern
5) 9 point box
6) 5 point box for testing the load effect
7) color bar
8) cross bar
9) gray level with 32*32 rectangular
10) vertical gray bar, 256 level
11) horizontal gray bar, 256 level
12) box window
13) horizontally scrolling the vertical gray bar
14) vertically scrolling the horizontal gray bar
15) horizontally moving the vertical bar
16) vertically moving the horizontal bar
17) Random Pattern

3. ELECTRO OPTICAL SPECIFICATIONS

❑ Electro Optical characteristic Specifications (60/50Hz)

Item			Symbol	Condition	Min	Typical	Max	Unit
Peak White Brightness			B_{WP}	1% White Window	700	-	-	cd/㎡
Average White Brightness			B_W	Full White	90	100	-	cd/㎡
Brightness Uniformity			B_V	Full White	-25	0	+25	%
Color Coordinate	Red	X	X_R	Full Pattern	0.635	0.655	-	-
		Y	Y_R		0.315	0.335	0.355	
	Green	X	X_G		0.295	0.315	0.325	
		Y	Y_G		0.600	0.620	-	
	Blue	X	X_B		-	0.150	0.170	
		Y	Y_B		-	0.060	0.080	
	White	X	X_W		0.275	0.295	0.315	
		Y	Y_W		0.280	0.300	0.320	
Color Coordinate Uniformity			C_V	Full White	-0.020	Center	0.020	-
Power Consumption			Pw	Full / 25% White Window	-	276	300	W

- Respective value is measured at stable panel's characteristics (over 20 min.)
- Basis on CA-210
- Vs margin set -4V at 2 period (room temperature)

4. MECHANICAL & ENVIRONMENTAL SPECIFICATIONS

❑ Mechanical Characteristic Specifications

Item		Specification	Unit	Remark
Outline Dimensions		1156.0 ± 1.5 (H) X 677.6 ± 1 (V) X 37.9(D) ± 1.5	mm	Glass Filter (GLOBAL)
Display Area		1105.92(H) X 622.08(V) ± 0.5	mm	Common
Module Weight	Net	14.2± 0.5(1EA)	kg	Glass Filter (GLOBAL)
	Gross	250.2± 5 (15EA / 1BOX)	kg	

❑ Vibration and Drop Specifications

Item	Condition	Spec	Remark
Vibration	1.04Grms, 2~200Hz random, total 30 min	Meet Characteristics and other Spec.	boxing state (Y dir.)
Drop	20 cm		

❑ Recommended Environmental Conditions

Item		Condition	Spec.	Remark
Ambient temperature	Operation	0℃ ~ 60℃	Meet Characteristics and other Spec.	Module Condition
	Storage	- 20℃ ~ 60℃		
Panel Temperature	Surface	Under 120℃		
	Change ratio	< 20℃/cm		
Humidity	Operation	20% ~ 80%		
	Storage	10% ~ 90%		
Air pressure	Operation	800 ~ 1100 hPa		
	Storage	700 ~ 1100 hPa		

5. IMAGE STICKING CHARACTERISTICS

❑ Image Sticking

The fluorescent substance used in the plasma module loses its brightness with the lapse of lighting time. This deterioration in brightness appears to be a difference in brightness in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in brightness is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.

When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in brightness in the pattern shown shortly before changeover. If this conditions is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

❑ Secular change in brightness

The life of brightness, defined as the reduction to half the initial level, is more than 25 thousand hours on average.

Conditions: All white (100% white) input at an ambient temperature of 25°C.

However, this lifetime is not a guarantee value for life and brightness. It should be recognized simply as the data for reference.

❑ Cause of deterioration in brightness

A major possible cause of deterioration in brightness is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

❑ Practical value for Image sticking

The relationship between integrated lighting time and brightness in this plasma module is described in the attached material. In particular, the deterioration in brightness tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking. The practical value for image sticking is difficult in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

❑ Proposed measures taken to relieve image sticking

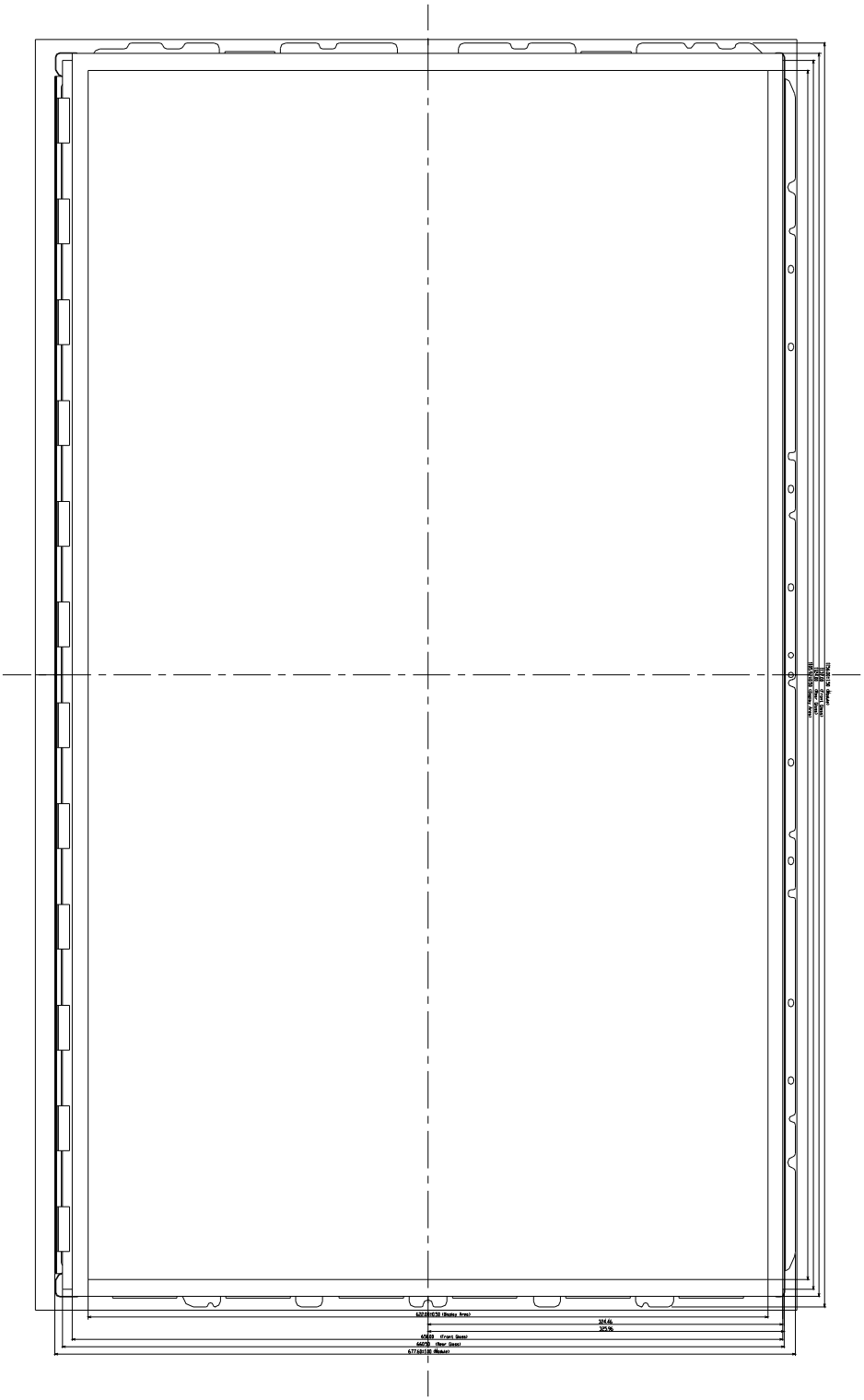
So long as there is the reduction of brightness in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in brightness reduction among the displayed dots.
The images from TV broadcasting involve a high rate of motion picture displays. Therefore, there is less chance of being a cause of difference in brightness reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes. Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in brightness as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in brightness achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.
The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

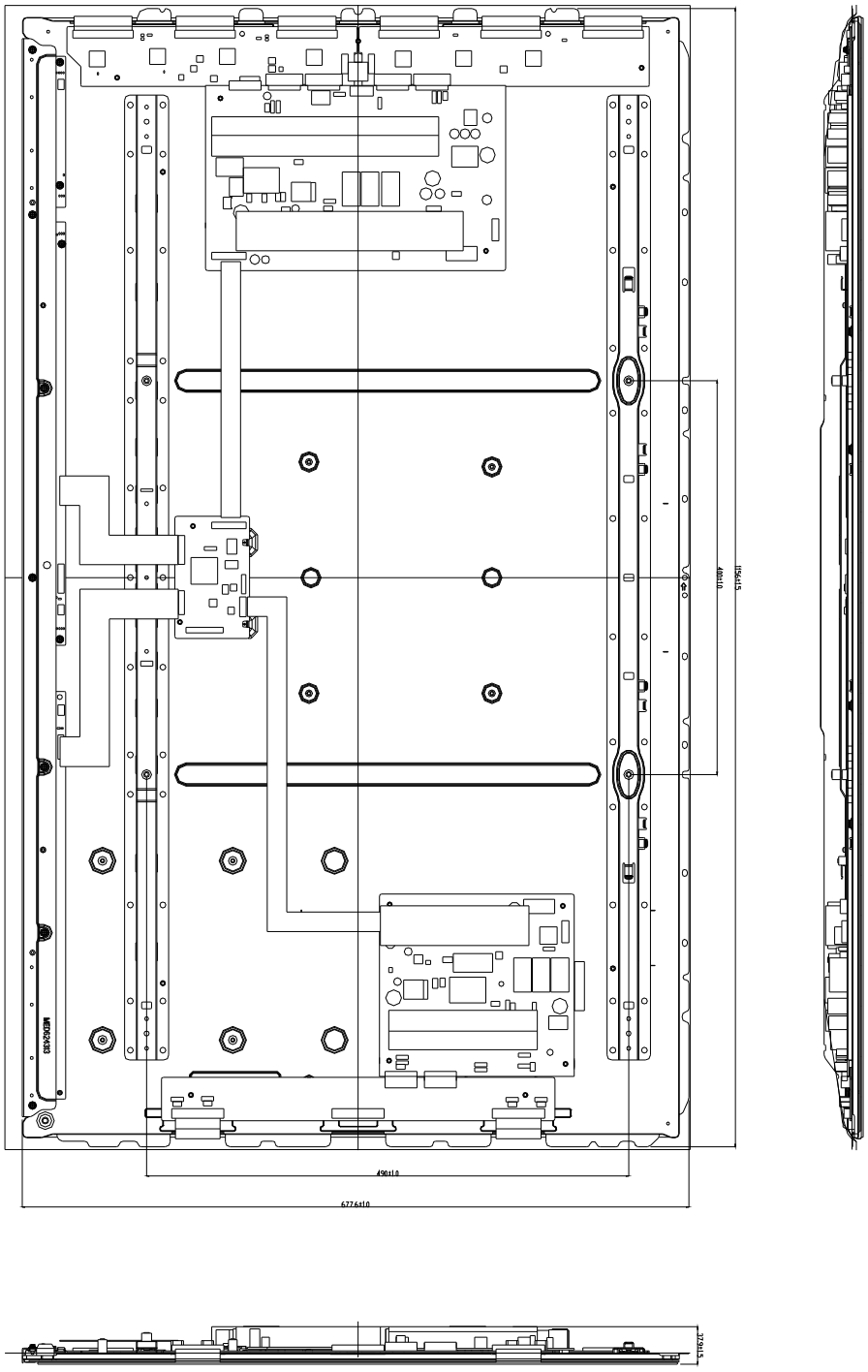
Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.
Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize display period of the fixed pattern.
Example of Proposal 4: During operation, the brightness of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

6. OUTLINE DRAWING

❑ Front View



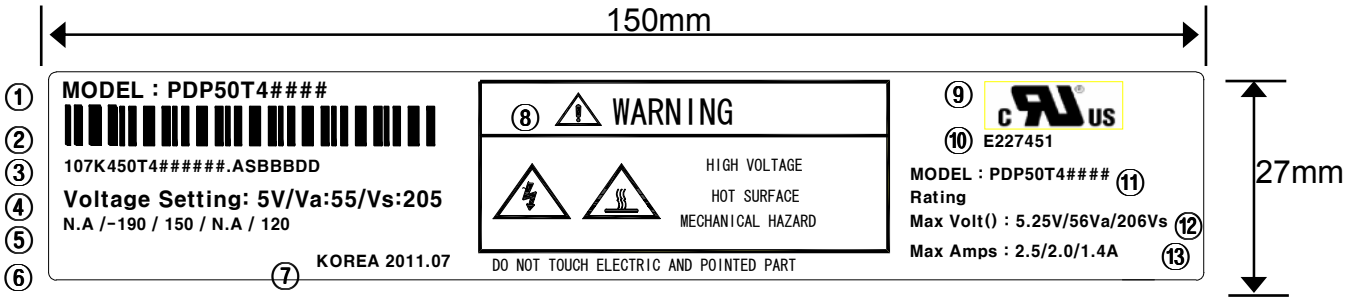
❑ Rear View



8. LABEL

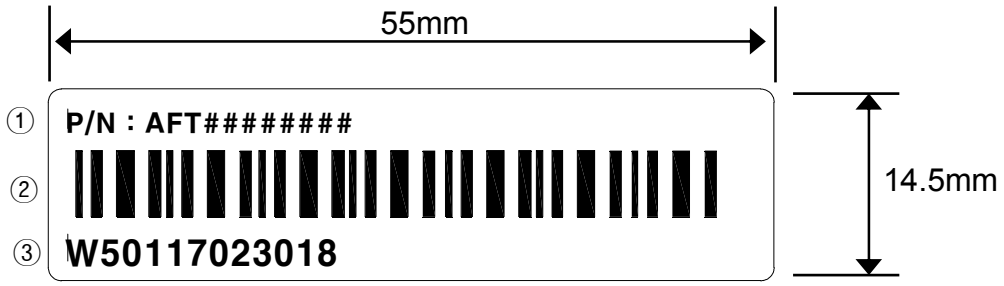
❑ LABEL Sticking Position

➢ LABEL ① : Unification Label



①	Model Name	PDP50T4####
②	Bar Code (Code 128, Contains the manufacture No.)	
③	Manufacture No.	
④	Adjusting Voltage (DC Va, Vs)	5V / Va:55 / Vs:205
⑤	Adjusting Voltage (Set up/ -Vy/ Vsc/ Ve/ Vzb)	N.A / -190 / 150 / N.A / 120
⑥	-	
⑦	Manufactured date (Year & Month)	
⑧	Warning	
⑨	UL Approval Mark	
⑩	UL Approval No.	E227451
⑪	Model Name	PDP50T4####
⑫	Max. Volts	5.25V/56Va/206Vs
⑬	Max. Amps	2.5A/2.0A/1.4A

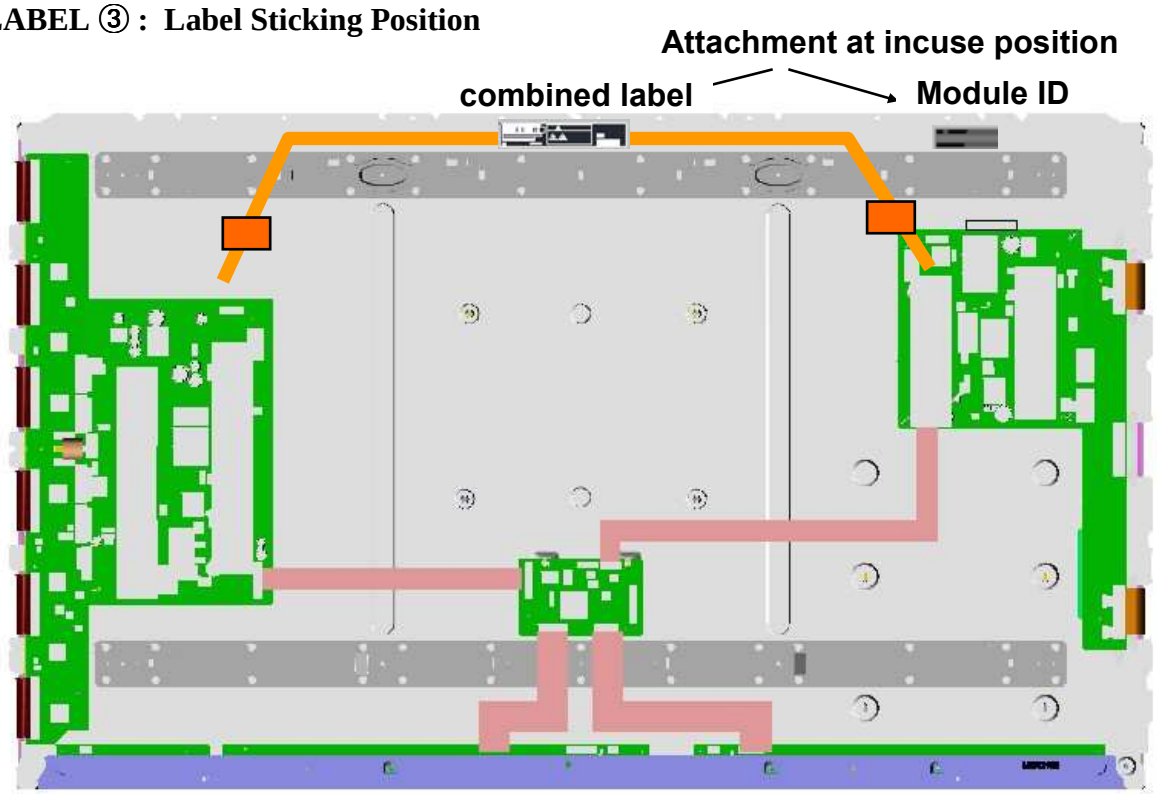
➢ LABEL ② : Unification Label



① Module frame ass'y part number
② Bar Code Containing the manufacture No.
③ Manufacture No.

❑ LABEL Sticking Position

➢ LABEL ③ : Label Sticking Position

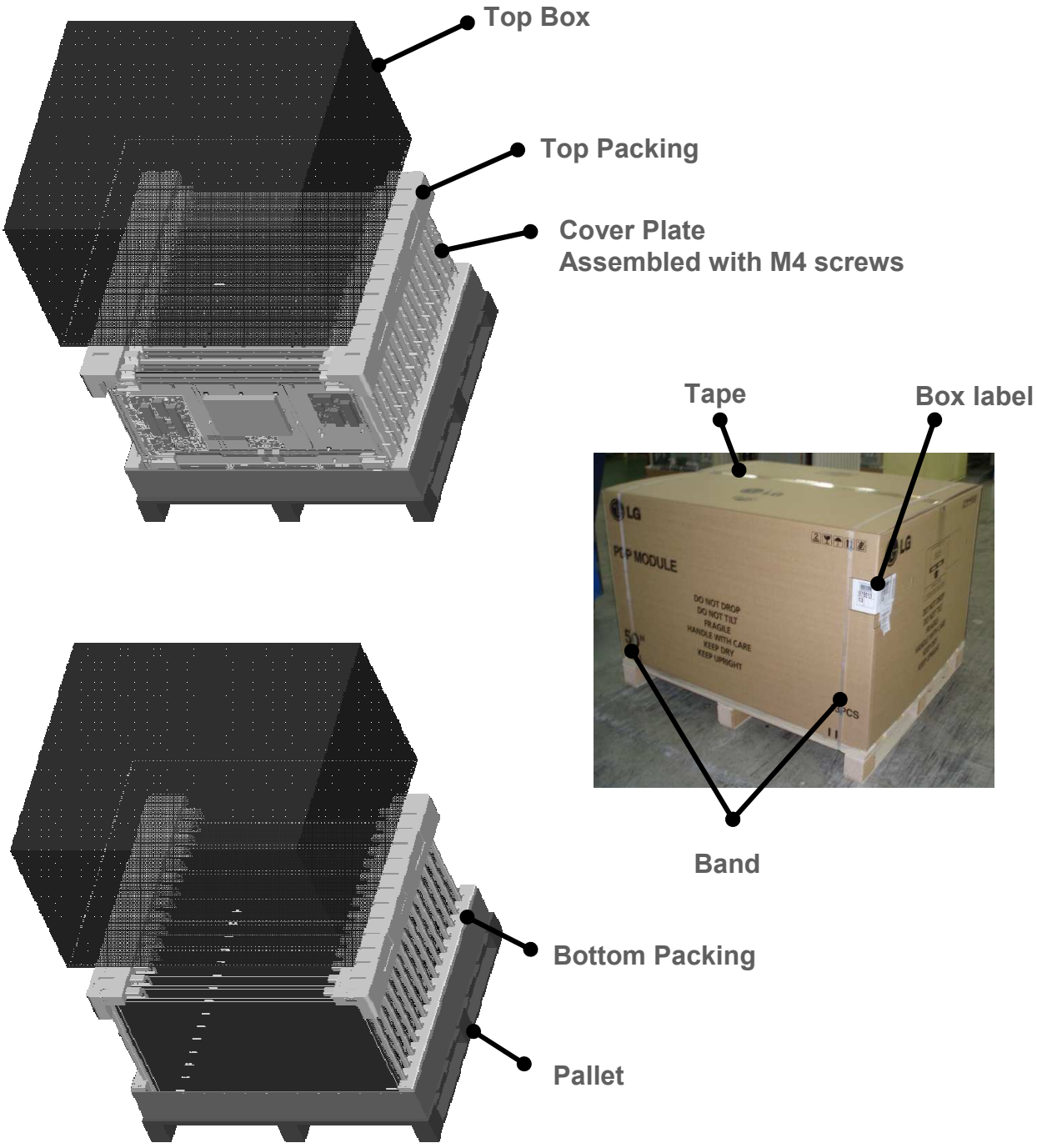


9. PACKING

❑ Box packing (15 modules per each Box)

➢ **Packing composition** : cover plate, M4 screw, pallet, bottom / top packing box, bottom / top box, tape, band, box label

➢ **Module quantity in box** : 15 EA



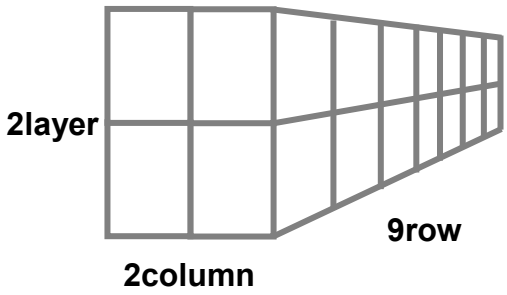
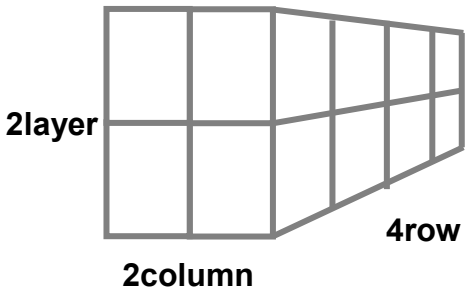
➢ Packing movement, loading and Keeping

- Left & right Direction of Module should be matched with direction of forklift.
- When forklift is moving into direction of module's front and rear, Don't rapidly accelerate and decelerate.
- Two layer loading and Keeping.
- Humidity and temperature is maintained in sharehouse.

➢ Forklift loading

- When module box is loaded in car, length direction of product should be matched with Direction of forklift.
- Spare packing (under 14ea) should be loaded at last top in car and Quantity should be written at box.

Direction of forklift.

40 feet Container	20 feet Container
36 boxes (540 Modules) loading	16 boxes (240 Modules) loading
	

10. PSU SPECIFICATION

II. SPECIFICATION

1. Input Requirement

Nominal Input Voltage	AC100V to AC240V
Input Voltage Variation	AC90V to AC264V
Input Current	Max 3.7A at 100Vac Max 1.7A at 240Vac, Norminal Load, 50/60Hz
Nominal Frequency	50 / 60 Hz
Frequency Variation Range	47Hz to 63Hz
Phase	Single
Inrush Current	50A zero-pk max at cold start and any specified line, load, and temperature conditions.
Efficiency	More than 85% at the 230Vac Rated load
Leakage Current	0.5mA max. (AC264 / 60Hz) at Nominal Load
Impulse Noise Surge	±2kV / 50ns to 1000ns / 0° to 360°
Dip Test	100% 1cycle 60% 5cycle (AC100 ~ 240V, Normal load Ta=25℃) <Judgment > 100% : No St-by Mode, No Memory Reset / No Hardware Fail 60% : No Hardware Fail Related Regulation : IEC 61000-4-11, EN61000-4-11
Surge Immunity	4kV (Common Mode) : 2 time each polarity 4kV (Normal Mode) : 2 time each polarity
Electrostatic Discharge	8kV

2. Output Characteristics CTQ

Output		Voltage variable range [V]	Rated	Rated Current (Min, Max) [Amean] *note 1	Voltage Regulation [V]	Ripple Voltage [mVp-p]
PDP Module	Vs (205V)	200V ~ 206V	1.0A	0.1 ~ 1.4A	±1%	500
	Va (55V)	-	1.0A	0.01 ~ 2.0A	±1.5%	300
	M5V (5.2V)	-	1.5A	0.5 ~ 2.5A	±5%	100
VSC Board (Signal Interface)	17V	-	1.5A	0 ~ 3.0A	±5%	500
	5.2V	-	1.5A	0.1 ~ 3.0A	±5%	200
	STBY	3.5V (Before RL_ON)	0.1A	0 ~ 0.2A	±4%	100
				STBY: 9mA (Below 0.3W Condition)		
		5.2V (After RL_ON)	1.0A	0 ~ 2.0A	±5%	200

※ Module Max Spec : 300W
※ Aging, RQA test condition : Rated Current
※ Voltage Regulation Condition
- When regulation test for 17V, total current of 5.2V+M5V+STBY set upper 2A.
- When regulation test for each voltage, current of other output set below rated value.
- When regulation test for M5V, it's reinforced GND

※ The following instruments shall be used for measuring ripple voltage.
1. Probe having impedance ratio of 1:1.
2. Oscilloscope having frequency characteristic of 100MHz or more.
3. Vs ripple voltage is 2000mVp-p, Va ripple voltage is 600mVp-p, STBY(5.2V),5.2V and M5V ripple voltage is 200mVp-p, STBY(3.5V) ripple voltage is 200mVp-p at the electric-load and room temperature with metal ground plane.

※ All regulations must satisfy spec. which are recorded in approval.

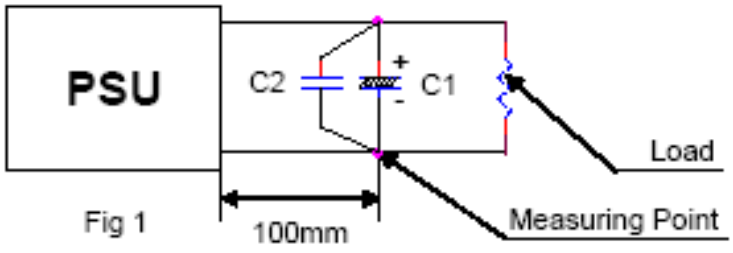


Fig 1

As shown in fig.1 C1(47uF) electrolytic capacitor and C2 (0.1uF) film capacitor shall be connected between measuring points when measuring ripple noise.

3. Environment Requirement

Operating Temperature Range	0 to 70 deg.
Operating Humidity Range	20 to 80 %
Storage Temperature Range	-20 to 70 deg.
Storage Humidity Range	10 to 90 %
MTBF Mean Time Between Failure	440,000hour(Tool_Telcordia Issue 1)
Cooling Condition	Natural Air
Shock	98㎧ Shock test consists of pivoting the power supply, from one edge of it's bottom side, on a flat surface (such as wood having thickness of 10mm or more) and allowing the opposite edge to fall from a height of 50mm to this surface. The test is performed three times on each edge of the bottom side of the power supply

		Under Development	Mass Product
Vibration	Frequency (Hz)	2~200	2~200
	Acceleration (Grms)	1.04	0.84
	Time (min)	20 min. / ㎐	
	Direction	X, Y, Z	

4. Dielectric Strength Voltage

Safety

Dielectric Strength Voltage	① Live & Neutral to all Secondary(+ line) : 3.0KVac or 4242Vdc for 1 Minute ② Live & Neutral to all Secondary GND : 1.5KVac or 2121Vdc for 1 Minute. ※ 1.8KVac for 1 seconds (Mass Production)

※ Above tests are performed at room temperature in non-condensing atmospheric conditions

※ Frame grounds are connected to secondary circuits.

※ Cut OFF condition : 10mA

5. Insulation Resistance

Safety

Insulation Resistance	Insulation resistance shall be 8MΩ ~ ∞ Ω at 500Vdc after 60sec. between primary Live, Neutral line and secondary.

6. Interface

Signal	Description	Signal Direction	Active	Level
RL_ON	5.2V, 17V ON/OFF	Input	HIGH : 5.2V, 17V ON LOW : 5.2V, 17V OFF	High : more than 2V Low : Less than 0.7V
M_ON (Module_ON)	M5V / Vs Va ON / OFF	Input	HIGH : M5V / Vs,Va ON LOW : M5V / Vs,Va OFF	High : more than 3V Low : Less than 0.7V
AC_DET	Monitor for AC input voltage	Output	HIGH : Active LOW : Inactive	High : more than 4V Low : Less than 0.7V

•Auto Power turn on System
- If VSC B/D is not connected PSU through 18pin connector, auto power on mode is operated from PDP Set Signal.

7. Product Safety

Safety Standards to be applied	Design to meet the requirements as follows UL60065 and IEC/EN60065
EMI / RFI Standards to be applied	Design to meet the requirements as follows FCC and EN55020 Class B with 4dB minimum margin.

8. Construction

Weight	Less than 670g / PSU
Unit Size	196(W) x 245(D) x 27(H)(with PCB)
Lead Length	1.6mm ~ 3.0 mm under IC102,IC103,IC352,IC902,IC903 are 4.8mm under D351,Q356 are 5.5mm under
Height	27mm (with PCB) TH101,C907,C351 and C502 are Max. 27mm height (without PCB) RL103 are Max. 27mm+5mm height (without PCB) T901 are Max. 29mm height (without PCB)

9. Function of protection CTQ

Protection	Output Circuit	Trip point	Notes
Over Current	STBY	2.5A ~ 20A	Hiccup or Shut down
	5.2V	6A ~ 20A	
	M5V	4.1A ~ 20A	
	17V	3.1A ~ 8A	
	Va	2.1A ~ 12A	Shut down
	Vs	1.5A ~ 6A	
Under Voltage	5.2V	3.5V ~ 4.5V	Shut down
	M5V	3.5V ~ 4.5V	
	17V	8V ~ 14V	
	Va	40V ~ 50V	
	Vs	165V ~ 180V	
Over Voltage	5.2V	5.5V ~ 9.0V	Shut down
	M5V	5.5V ~ 7.0V	
	17V	19.5V ~ 28V	
	Va	60V ~ 70V	
	Vs	215V ~ 240V	

※ The OCP test of STBY, 5.2V, M5V and 17V should setup current rise slew rate greater than 3.6A/S.
※ This Power Supply has above-mentioned protections.
※ The time for short shall be less than 10sec.
※ PSU should be shutdown by under voltage protection when short circuit test
※ PSU should be wake up normally when AC off-on / Relay off-on / protection removal
※ Short circuit protection between different output terminals is not considered.
※ Trip point for over voltage indicates the operating point when the output voltage slowly increases.
※ The conditions of Over Current measurement

구분	측정포인트	부하조건					
		5.2Vst	5.2Vsc	M5V	17V	Va	Vs
OCP (100Vac)	5.2Vst	–	Nom	Nom	1A	0.3A	0.3A
	5.2Vsc	Nom	–	Nom	1A		
	M5V	Nom	Nom	–	1A		
	17V	Nom	Min	Min	–		
	Va	MIN				–	0.1A
	Vs	MIN				0.01A	–
OVP (100Vac)	전출력	MIN				MIN	MIN
UVP (100Vac)	전출력	MIN				MIN	MIN
출력전압 조정 (110Vac)	Va	NOMINAL(42"/50FHD/60FHD:55V)					
	Vs	NOMINAL(42HD/50FHD/60FHD :205V)					

10. AC Over-voltage Test
1) Over voltage shall test 315Vac~340Vac.
2) No fire, shock hazard or explosion shall occur.

11. Input / output Pin Assignment

AC Input

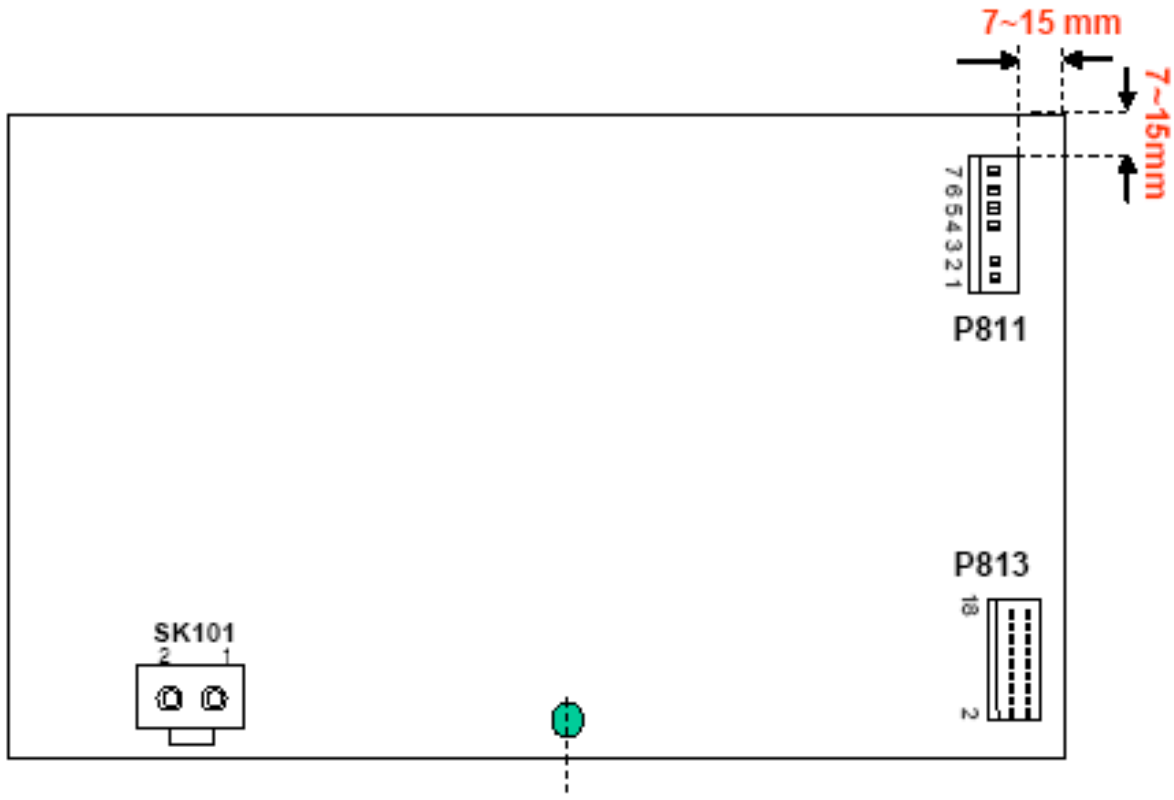
	SK101
1	AC
2	AC
Wafer	YAW396-02M1

PSU ↔ VSC Board

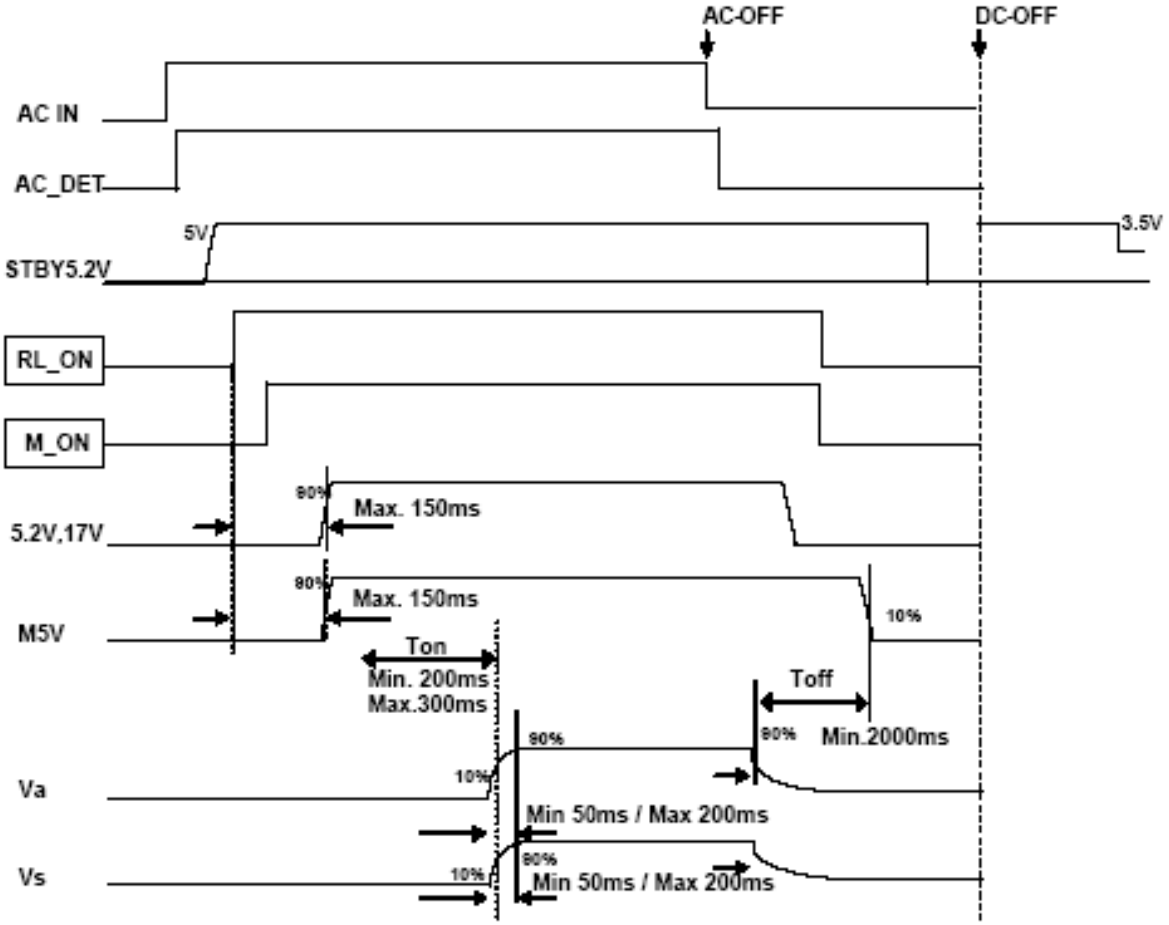
P813			
1	17V	2	17V
3	GND	4	GND
5	5V	6	5V
7	5V	8	Error_DET
9	GND	10	GND
11	GND	12	GND
13	STBY	14	STBY
15	RL_ON	16	AC DET
17	M_ON	18	AUTO_GND
Wafer	SMAW200-H18S2		

PSU ↔ PDP Module

Pin	P811
1	Vs
2	Vs
3	NC
4	GND
5	GND
6	Va
7	M5V
Wafer	YAW396-H73FD

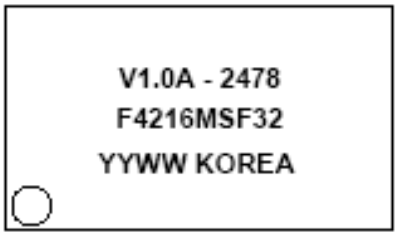


12. Power Sequence



※ * RL_ON, M_ON signal is come from VSC B'd, So, Sequence spec related RL_ON, M_ON is just guide spec for PDP Buyer. Measured data can't be judged OK or NG.
Va, Vs 전압이 10% 이하 일 경우에만 상기의 Ton , TVaR , TVsR 에 meet 할 수 있다.
Toff 시간은 AC 전원으로 (플러그 해제) off 한 경우는 제외된다.
※ M_ON은 RL_ON 이후 Max50ms이전에 입력 되었을 경우로 한다

13. Micom Definitions



※ Version : V1.0A
Checksum : 2478