Elektronische Bauelemente

STT3962NE

2.3A , 60V , $R_{DS(ON)}$ 0.153 Ω
N-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

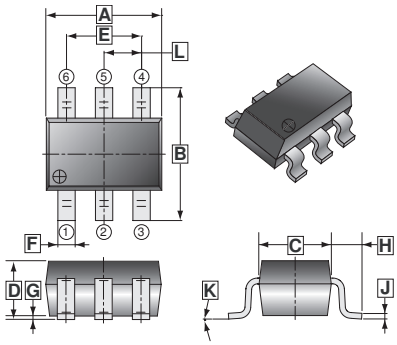
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

TSOP-6

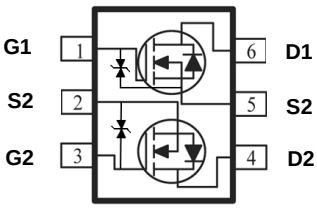


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60 REF.	
C	1.40	1.80	J	0.12 REF.	
D	1.10 MAX.		K	0°	10°
E	1.90 REF.		L	0.95 REF.	
F	0.30	0.50			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7 inch

ESD
Protection Diode
2KV



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_A=25℃	I_D	2.3	A
	T_A=70℃		1.9	
Pulsed Drain Current [2]		I_{DM}	8	A
Continuous Source Current (Diode Conduction) [1]		I_S	1.05	A
Power Dissipation [1]	T_A=25℃	P_D	1.15	W
	T_A=70℃		0.7	
Operating Junction and Storage Temperature Range		Tj, Tstg	-55~150	℃
Thermal Resistance Rating				
Maximum Junction to Ambient [1]	t ≦ 10 sec	$R_{\theta JA}$	100	℃ / W
	Steady State		166	

Notes:
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Body Leakage Current	I_{GSS}	-	-	100	uA	V_{DS}=0, V_{GS}=20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	uA	V_{DS}=48V, V_{GS}=0
		-	-	10		V_{DS}=48V, V_{GS}=0, T_J=55°C
On-State Drain Current [1]	$I_{D(on)}$	5	-	-	A	V_{DS} =5V, V_{GS}=10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	0.153	Ω	V_{GS}=10V, I_D=2.3A
		-	-	0.185		V_{GS}=4.5V, I_D=2.1A
Forward Transconductance [1]	g_{fs}	-	10	-	S	V_{DS}=5V, I_D=2.3A
Diode Forward Voltage [1]	V_{SD}	-	0.8	-	V	I_S=1.05A, V_{GS}=0
Dynamic [2]						
Total Gate Charge	Q_g	-	3	-	nC	V_{DS}=15V, V_{GS}=4.5V, I_D=2.3A
Gate-Source Charge	Q_{gs}	-	0.6	-		
Gate-Drain Charge	Q_{gd}	-	1	-		
Turn-on Delay Time	$T_{d(on)}$	-	5	-	nS	V_{DD}=15V, V_{GS}=4.5V, R_{GEN}=15Ω, I_D=1A
Rise Time	T_r	-	12	-		
Turn-off Delay Time	$T_{d(off)}$	-	13	-		
Fall Time	T_f	-	7	-		

Notes:
1. Pulse test: PW ≦ 300us duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.