SSD2805

Advance Information

MIPI Master Bridge

1 GENERAL DESCRIPTION

The SSD2805 IC is a MIPI master bridge chip that connects a host processor with traditional parallel LCD interface and an LCD driver with MIPI slave interface. The SSD2805 supports parallel RGB and MCU interface and serial SPI interface.

2 FEATURES

- Support up to 700Mbps over 2 data lanes (350Mbps per lane)
- Reduce number of signals to 8 lines over the serial link (DATAP0, DATAN0, DATAP1, DATAN1, CLKP, CLKN, MIPI_RES# and SYS_CLK)
- Reduce power consumption and decrease EMI by using low amplitude signal over differential pair for serial data.
- Support parallel MCU interface up to 16 bits (6800, 8080)
- Support parallel RGB interface up to 24 bits
- Support serial SPI interface up to 24 bits (8 Bit 4 Wire, 8 Bit 3 Wire, 24 Bit 3 Wire)
- Support 16, 18 and 24 bit per pixel for both MCU and RGB interfaces
- Support dual display panel (MCU + MCU panels or MCU + RGB panels)
- Support both command mode and video mode in MIPI DSI standard
- Support bi-directional data transfer (forward link in High Speed and Low Power mode and reverse link in Low Power mode)
- Ultra Low Power mode in idle state
- On-chip PLL with programmable output frequency
- Power supply: (V_{DDD} and V_{DDA}) 1.8V +/-10%
- IO Power supply: (V_{DDIO}) 3.3V +/-10%, 1.8V +/-10%
- Support of MIPI standard DSI v1.01r9, D-PHY v0.89
- 8KV (HBM) ESD protection on MIPI lanes

3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form	Remark
SSD2805CG39	64 TFBGA (RoHS Package in Tray form)	
SSD2805CG39R	64 TFBGA (RoHS Package in Tape & Reel form)	
SSD2805DG39	64 TFBGA (RoHS + Halogen free Package in Tray form)	
SSD2805DG39R	64 TFBGA (RoHS + Halogen free Package in Tape & Reel form)	
SSD2805G39	64 TFBGA (RoHS Package in Tray form)	EOL
SSD2805AG39	64 TFBGA (RoHS Package in Tray form)	EOL
SSD2805BG39	64 TFBGA (RoHS Package in Tray form)	EOL

4 BLOCK DIAGRAM

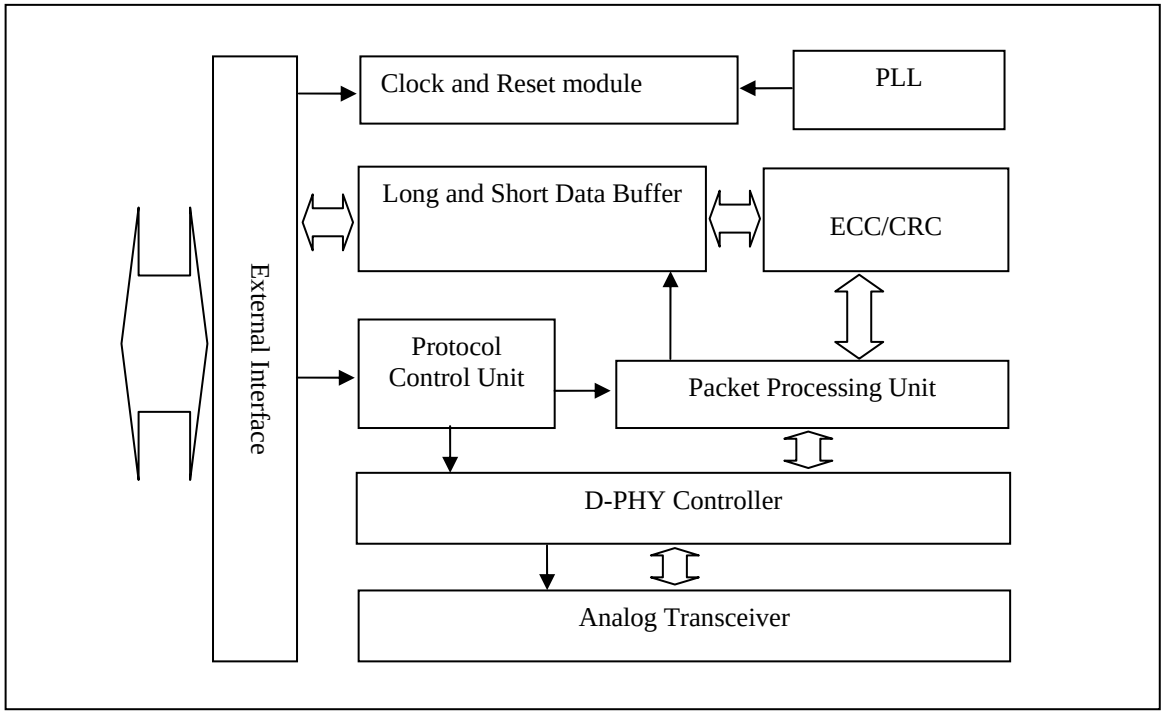


Figure 4-1: SSD2805 Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 Functional Blocks

5.1.1 Clock and Reset Module

The Clock and Reset Module controls the generation of the operation clock for the whole system.

5.1.2 External Interface Module

The External Interface Module controls the communication with the host processor. Three types of interface are supported:

- Parallel RGB Interface for dumb display controller. 16 bit, 18 bit and 24 bit data bus width are supported
- Parallel MCU Interface for smart display controller. User can select one of the following 4 MCU interface mode by setting PS3 and PS2:
  - 8 bit 8080 MCU interface
  - 16 bit 8080 MCU interface
  - 8 bit 6800 MCU interface
  - 16 bit 6800 MCU interface
- Serial SPI interface supports three modes by setting PS1 and PS0:
  - 8 Bit 3 Wire (SCSX, SCK, DIN, DOUT)
  - 8 Bit 4 Wire (SCSX, SCK, SD/C#, DIN, DOUT)
  - 24 Bit 3 Wire (SCSX, SCK, DIN, DOUT)

User can use RGB + SPI interface or MCU interface by setting the IF_SEL pin.

5.1.3 Protocol Control Unit (PCU)

The PCU handles outgoing and incoming data stream including:

- Decide the packet type to be sent when an event comes in
- how to react to the received packet.

5.1.4 Packet Processing Unit (PPU)

The PPU is in charge of packet assembly and disassembly. During transmission, the PPU constructs the packet according to the instruction from the PCU. During reception, the PPU extracts information from the incoming packet and pass the information to the PCU.

5.1.5 Error Correction Code / Cyclic Redundancy Check (ECC/CRC)

During transmission, the ECC/CRC module generates ECC or CRC for outgoing bit stream.

During reception, the ECC/CRC module checks the correctness of the ECC and CRC field of the incoming stream.

- If 1 bit error is detected in the data and ECC field, the ECC module will correct the error.
- If more than 1 bit of error is detected in the data and ECC field, the ECC module will report the error.
- If error is detected in the data and CRC field, the CRC module will report the error.

5.1.6 Internal Long and Short Buffer

The internal buffers serve as temporary storage for incoming data from the host processor. After a complete packet is written into the buffer, the SSD2805 will send out the packet.

5.1.7 D-PHY Controller

The D-PHY Controller is in charge of the communication with the Analog Transceiver. During transmission, it receives data from PPU and informs the analog transmitter how to transmit. During reception, it receives data from analog receiver and passes the data to the PPU for further processing. At the same time, it is also performing the handshaking process, such as, bus turn around and switching between different modes.

5.1.8 Analog Transceiver

The Analog Transceiver is front-end for signal communication with MIPI slave. High speed parallel data from D-PHY controller is serialized and transmitted by the high speed transmitter. For control operation, low power transmitter and receiver are used while contention detection is implemented for checking the state conflict.

5.1.9 PLL

The PLL uses either the TX_CLK or the PCLK as reference clock source to generate operating clock for the whole system.

When powering up SSD2805, the PLL is in sleep mode. The system will operate at TX_CLK until PLL is locked.

In HS mode, the PLL output clock is used to generate the clock and data on the MIPI lane. User shall program the PLL such that its output frequency is the same as the data rate required on each data lane.

Refer to SSD2805 Application Note for details in programming the PLL.

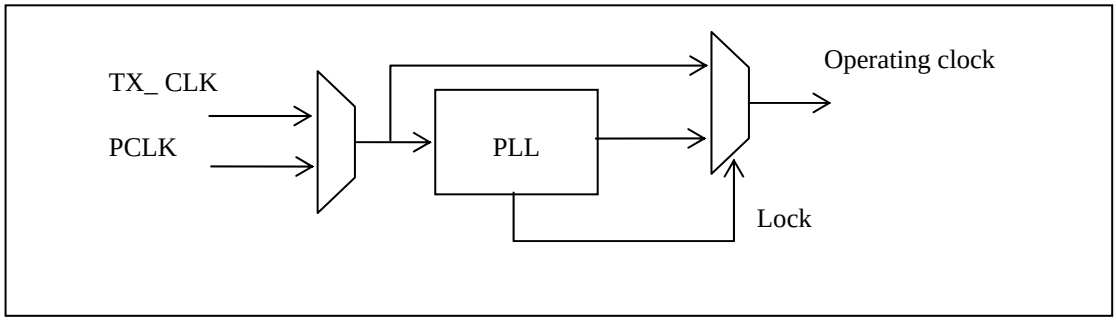


Figure 5-1: SSD2805 Clocking Scheme

5.2 Interface Configuration

The SSD2805 supports two interface configurations:

- MCU interface
- RGB + SPI interface.

Multiple displays can be supported in both configurations.

5.2.1 RGB + SPI Interface

To select this configuration, the user shall:

- set the IF_SEL pin to low
- select the desired SPI interface by setting PS[1:0]

The host processor can use this configuration to drive

- a dumb display panel
- a smart display panel
- a dumb display panel + a smart display panel

Under this configuration, the RGB interface and SPI interface are operating independently. The RGB interface is used to provide display data. The SPI interface is used to:

- program the local registers of SSD2805
- program the registers of the dumb display panel if connected
- configure the smart display panel and send data to the smart display panel

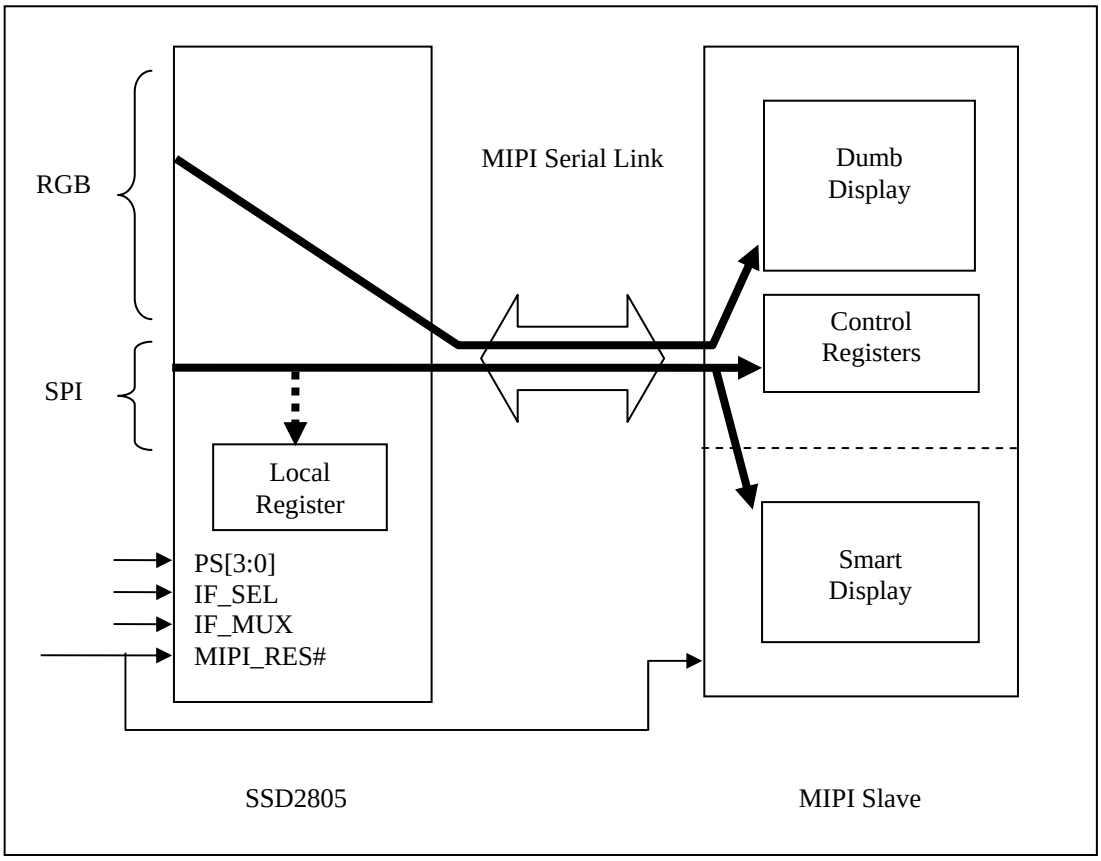


Figure 5-2: SSD2805 with RGB + SPI Interface

5.2.2 MCU Interface

The host processor can use this configuration to drive multiple smart display panels. The MCU interface control signals are multiplexed with the RGB interface control signals. Two multiplexing schemes are provided. For the details please refer to Multiplexing Scheme for RGB and MCU interface in Table 6-1. The user needs to set the IF_SEL pin to high, set IF_MUX pin to select the desired interface multiplexing scheme and set PS[3:2] to select the desired MCU interface. When the MCU interface is not used, the CSX pin needs to be kept high.

The MCU interface is used to program the local registers of SSD2805, configure and send display data to the smart panels in command mode. SSD2805 can drive multiple smart panels. Below are some illustrations for the use case.

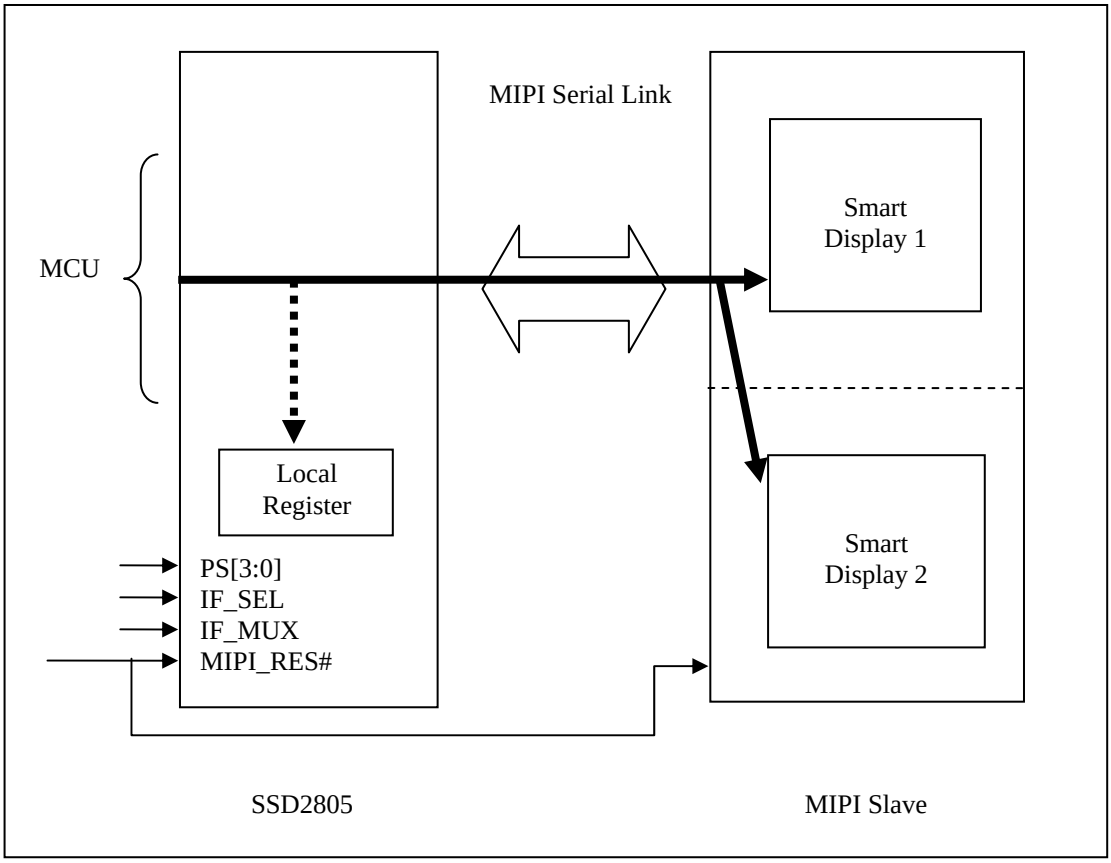


Figure 5-3: SSD2805 with MCU Interface

5.3 Operating Modes

5.3.1 Video Mode

In video mode, the host processor send pixel data to SSD2805 through the RGB interface in real time and send configuration data to SSD2805 through the SPI interface.

To enable the video mode transmission, user shall set IF_SEL to 0 to select RGB + SPI interface.

The SSD2805 supports three data transmission formats:

- Non-Burst Mode with Sync Pulses
- Non Burst Mode with Sync Events
- Burst Mode

Following pixel formats are supported in all transmission format:

- 16 bpp (5,6,5 RGB) using DATA[15:0]
- 18 bpp (6,6,6 RGB) packed using DATA[17:0]
- 18 bpp (6,6,6 RGB) loosely packed using DATA[17:0]
- 24 bpp (8,8,8 RGB) using DATA[23:0]

5.3.2 Command mode

In command mode, TX_CLK shall be selected as the PLL reference clock. The PCLK pin is used as part of the MCU interface. MCU interface supports both 8 bit and 16 bit data bus. To support different bus width, the following data pins are used.

- DATA[7:0] for 8 bit interface.
- DATA[15:0] for 16 bit interface.

5.4 Interrupt

An output active low interrupt signal INT# is provided for the SSD2805 to trigger the host processor. User can select events to activate interrupt setting register bits in the SSD2805. Refer to SSD2805 Application Note for details.

6 PIN ARRANGEMENT

6.1 64 pin TFBGA

Figure 6-1: Pinout Diagram – 64 TFBGA (Bottom view)

	1	2	3	4	5	6	7	8
H	INT#	DATAP0	DATAN0	CLKP	CLKN	DATAP1	DATAN1	TAPAD
G	SCK	MIPI_RES#	SD/C#	VSSD	VDDA	VSSA	TEST0	TEST1
F	SCSX	DIN	DOUT	DATA1	HSYNC	PS1	TEST_GPIO0	TEST2
E	SYS_CLK	DATA21	DATA20	VDDIO	VDDD	PS2	TEST_GPIO1	TEST_GPIO2
D	DATA23	DATA22	DATA14	DATA12	DATA8	CM	PS0	TX_CLK
C	DATA18	DATA19	DATA9	DATA7	DATA2	SHUT	PS3	PCLK
B	DATA17	DATA16	DATA11	DATA5	DATA3	DEN	IF_SEL	LANE_SEL
A	DATA15	DATA13	DATA10	DATA6	DATA4	DATA0	VSYNC	IF_MUX

6.2 PIN DESCRIPTIONS

Key: I = Input
O =Output
I/O = Bi-directional (input/output)
PU = Pull Up with 75k ohm
PD = Pull Down with 75k ohm
P = Power/Ground Pin
Hi-Z = High impedance

6.2.1 MIPI Interface Pins

Pin Name	Type	Pin #	Description
CLKP	O	H4	Positive polarity of low voltage differential clock signal
CLKN	O	H5	Negative polarity of low voltage differential clock signal
DATA0P	I/O	H2	Positive polarity of low voltage differential data signal 0
DATA0N	I/O	H3	Negative polarity of low voltage differential data signal 0
DATA1P	I/O	H6	Positive polarity of low voltage differential data signal 1
DATA1N	I/O	H7	Negative polarity of low voltage differential data signal 1

6.2.2 RGB / MCU Interface Pins

Pin Name	Type	Pin #	Description
PCLK	I, PD	C8	Multiplexed pins for RGB and MCU interface. Refer to Table 6-1, Table 6-2 and Table 6-3 for multiplexing scheme and pin usage in RGB mode and MCU mode.
VSYNC	I, PD	A7	
HSYNC	I, PD	F5	
DEN	I, PD	B6	
DATA[23:0]	I/O, PD	A1-A6, B1-B5, C1-C5, D1-D5, E2-E3, F4	
CM	I, PD	D6	Color mode control signal for RGB interface 1: 8-color display 0: 16M/262k/64k color display
SHUT	I, PD	C6	Shutdown signal for RGB interface (to put the driver into sleep mode) 1: The panel is shut down 0: The panel is operating

Table 6-1: Host Interface Pins Multiplexing Scheme

Pin Name	RGB Mode	MCU Mode			
		Scheme 1 (IF_MUX =0)		Scheme 2 (IF_MUX =1)	
		6800	8080	6800	8080
PCLK	PCLK	RWX	RDX	E	WRX
VSYNC	VSYNC	E	WRX	DCX	DCX
HSYNC	HSYNC	CSX	CSX	RWX	RDX
DEN	DEN	DCX	DCX	CSX	CSX
DATA[15:0]	DATA[15:0]	DATA[15:0]			
DATA[16]	DATA[16]	TE			
DATA[23:17]	DATA[23:17]	Not Used			

Table 6-2: MCU Mode Interface Signals

Name	Type	Description
CSX	I	Chip select for MCU interface
DCX	I	Data or command signal for MCU interface
WRX	I	Write enable signal for MCU interface. Enabled when low. *Note: for 8080 interface only.*
RDX	I	Read enable signal for MCU interface. Enabled when low. *Note: for 8080 interface only.*
E	I	E clock. *Note: for 6800 interface only.*
RWX	I	Read/Write selection signal. Read cycle when high, write cycle when low. *Note: for 6800 interface only.*
DATA[15:0]	I/O	Data bus for MCU interface
TE	O	Tearing effect output signal

Table 6-3: RGB Mode Interface Signals

Name	Type	Description
DATA[23:0]	I	Data bus for RGB interface
VSYNC	I	Frame synchronization signal for RGB interface
PCLK	I	Dot-clock signal for RGB interface
HSYNC	I	Line synchronization signal for RGB interface
DEN	I	Display enable for RGB interface

6.2.3 SPI Interface Pins

Pin Name	Type	Pin #	Description
SD/C#	I, PD	G3	Data or command (for 8 Bit 4 Wire only)
SCSX	I, PD	F1	Chip select
SCK	I, PD	G1	Serial clock
DIN	I, PU	F2	Serial data input
DOUT	O	F3	Serial data output

Note: The SPI interface is not operational when MCU interface is selected.

6.2.4 Control Pins

Pin Name	Type	Pin #	Description
PS[1:0]	I, PD	F6, D7	SPI interface mode select 00: 24 Bit 3 Wire SPI interface 01: 8 Bit 3 Wire SPI interface 10: 8 Bit 4 Wire SPI interface 11: No SPI interface
PS[3:2]	I, PD	E6, C7	MCU interface mode select when IF_SEL is set to 1 00: 8 bit 8080 MCU interface 01: 16 bit 8080 MCU interface 10: 8 bit 6800 MCU interface 11: 16 bit 6800 MCU interface
IF_SEL	I, PD	B7	Interface configuration 0: RGB + SPI interface is selected 1: MCU interface is selected
IF_MUX	I, PD	A8	Interface multiplex scheme selection 0: Multiplex scheme 1 1: Multiplex scheme 2
LANE_SEL	I, PD	B8	Number of data lane selection 0: 1 data lane 1: 2 data lanes
TX_CLK	I, PD	D8	Input system clock, input frequency range from 5MHz to 50MHz
SYS_CLK	O	E1	Optional output system clock for MIPI slave
INT#	O	H1	Output interrupt
MIPI_RES#	I, PU	G2	Active low reset signal to the chip
TEST [2:0]	I, PD	F8, G8, G7	Test mode selection, set to 000 for normal operation
TEST_GPIO[2:0]	I/O	E8, E7, F7	GPIO pins for testing purpose. There pins are in floating state in normal operation.
TAPAD	O	H8	Connect a 0.1μF ceramic capacitor between this pin and ground.

6.2.5 Power Pins

Pin Name	Type	Pin #	Description
VDDA	P	G5	Power supply for internal analog blocks and PLL.
VDDD	P	E5	Power supply for the internal digital core.
VDDIO	P	E4	Power supply for interface IO pads.
VSSA	P	G6	Ground for internal analog blocks.
VSSD	P	G4	Ground for internal digital logic circuit and digital I/O.

Note: 0.1μF ceramic capacitors shall be connected between the power supply pins (VDDA, VDDD & VDDIO) and ground for decoupling.

7 MAXIMUM RATINGS

Table 7-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DDD}	Digital Core Power Supply	-0.3 to 2.16	V
V_{DDA}	Analog Core Power Supply	-0.3 to 2.16	V
V_{DDIO}	I/O Power Supply	-0.3 to 4.0	V
VIN	Input Voltage	-0.3 to 4.0	V
T_{SOL}	Solder Temperature / Time	225 for 40 sec max at solder ball	^{o}C
T_{STG}	Storage Temperature	-40 to 100	^{o}C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits specified in the electrical characteristics tables and Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} be constrained to the range $V_{SS} \le V_{IN} \le V_{DDIO}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 RECOMMENDED OPERATING CONDITIONS

Table 8-1: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDD}	Digital Core Power Supply	1.62	1.8	1.98	V
V_{DDA}	Analog Core Power Supply	1.62	1.8	1.98	V
V_{DDIO}	I/O Power Supply	2.97	3.3	3.63	V
		1.62	1.8	1.98	V
T_A	Operating Temperature	-30	25	85	°C

8.1 Power-up sequence

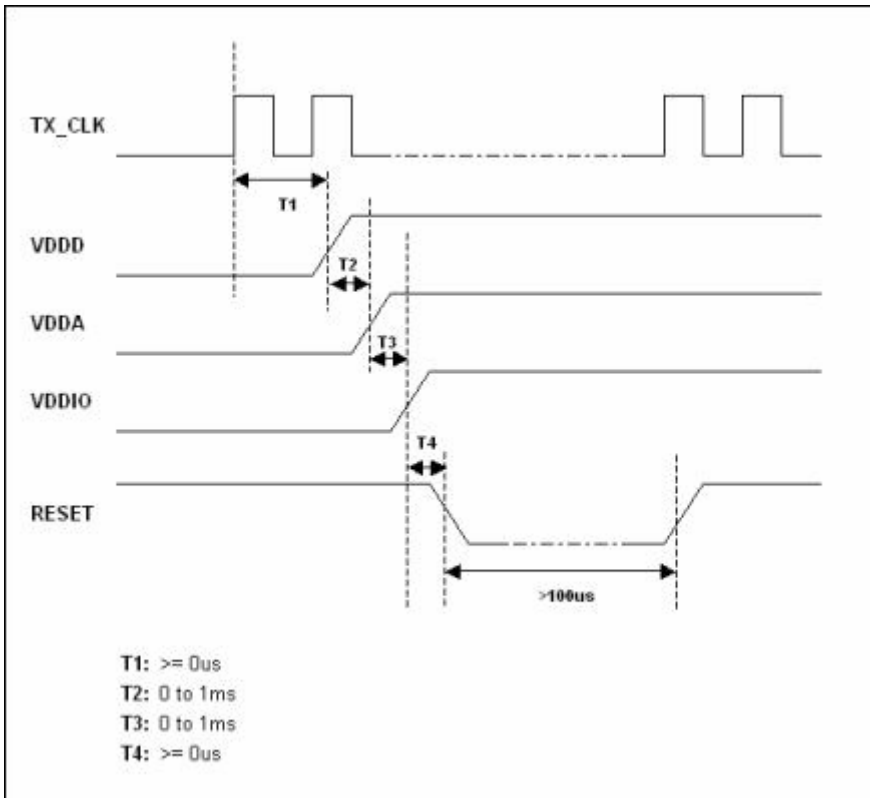


Figure 8-1: Power Up Sequence

9 DC CHARACTERISTICS

Conditions: Voltage referenced to V_{SS}
V_{DDD}, V_{DDA} = 1.8V, V_{DDIO} = 3.3V, T_A = 25°C

Table 9-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{DDD_HS}	High Speed Mode Current	240Mbps	-	7	8	mA
I_{DDA_HS}			-	8	12	mA
I_{DDIO_HS}			-	1	2	mA
I_{DDD_LP}	Low Power Mode Current	80Mbps	-	2	3	mA
I_{DDA_LP}			-	4	5	mA
I_{DDIO_LP}			-	0.5	1.5	mA
I_{DDD_ULPS}	Ultra Low Power State Current	PLL off, no change in all input signals	-	20	100	μA
I_{DDA_ULPS}			-	10	50	μA
I_{DDIO_ULPS}			-	20	50	μA
$V_{OH\ (CMOS)}$	Output High Voltage (CMOS)	I_{OH} = -2 ~ -16 mA	V_{DDIO} x 0.8	-	-	V
$V_{OL\ (CMOS)}$	Output Low Voltage (CMOS)	I_{OL}= 2 ~ 16 mA	-	-	V_{DDIO} x 0.15	V
$V_{IH\ (CMOS)}$	Input High Voltage (CMOS)		V_{DDIO} x 0.7	-	-	V
$V_{IL\ (CMOS)}$	Input Low Voltage (CMOS)		-	-	V_{DDIO} x 0.2	V
I_{OZ}	Tri-state Output Leakage Current		-	+/-1	-	μA
I_{IN}	Input Leakage Current	V_{IN} = V_{DDIO} or V_{SS}	-	+/-1	-	μA
C_{IN}	Input Capacitance		-	2.2	-	pF

Table 9-2: HS Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}	HS Transmit Static Common-mode Voltage	130	-	250	mV
$\|V_{OD}\|$	HS Transmit Differential Voltage	140	-	270	mV
$\|\Delta V_{OD}\|$	HS Differential Mismatch	-	-	10	mV
V_{OHHS}	HS Output High Voltage	-	-	360	mV

Table 9-3: LP Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	LP Thevenin Output High Level	1.1	1.22	1.3	V
V_{OL}	LP Thevenin Output Low Level	-50	-	50	mV
Z_{OLP}	LP Transmitter Output Impedance	110	-	-	Ohm

Table 9-4: LP Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	LP Logic 1 Input Voltage	880	-	-	mV
V_{IL}	LP Logic 0 Input Voltage	-	-	550	mV

10 AC CHARACTERISTICS

10.1 MIPI Lane Timing

Table 10-1: HS Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_R	HS 20%~80% Rise Time (transfer rate at 350Mbps)	-	-	0.3	UI
		150	-		ps
t_F	HS 80%~20% Fall Time (transfer rate at 350Mbps)	-	-	0.3	UI
		150	-		ps
T_{SKEW}	HS Data to Clock Phase Shift	0.35	-	0.65	UI
T_{DUTY}	Duty Cycle for CLK and DATA Lane	47.5	-	52.5	%

Note: UI = 1/(Lane Frequency X 2)

Table 10-2: LP Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}	LP 15%~85% Rise Time (Cload = 70pF)	-	-	85	ns
T_{FLP}	LP 85%~15% Fall Time (Cload = 70pF)	-	-	85	ns
$\delta V/\delta t_{SR}$	LP Slew rate @ Cload = 0pF	30	-	800	mV/ns
	LP Slew rate @ Cload = 5pF	30	-	500	mV/ns
	LP Slew rate @ Cload = 20pF	30	-	300	mV/ns
	LP Slew rate @ Cload = 70pF	30	-	150	mV/ns
T_{WAKEUP}	Recovery Time from Ultra Low Power State (ULPS)	1	-	-	ms

Table 10-3: LP Receiver AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{MIN-RX}	LPRX Minimum Pulse Width Response	20	-	-	ns

10.2 6800 MCU Interface Timing

Table 10-4: 6800 MCU Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	6T	-	-	ns
PW_{CSH}	Control Pulse Low Width	3T	-	-	ns
PW_{CSL}	Control Pulse High Width	3T	-	-	ns
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{ACC}	Data Access Time	-	-	5+4T	ns
t_{DHR}	Read Data Hold Time	1+2T	-	5+4T	ns
t_R	Rise Time	-	-	2	ns
t_F	Fall Time	-	-	2	ns

Note: T is PLL output clock period

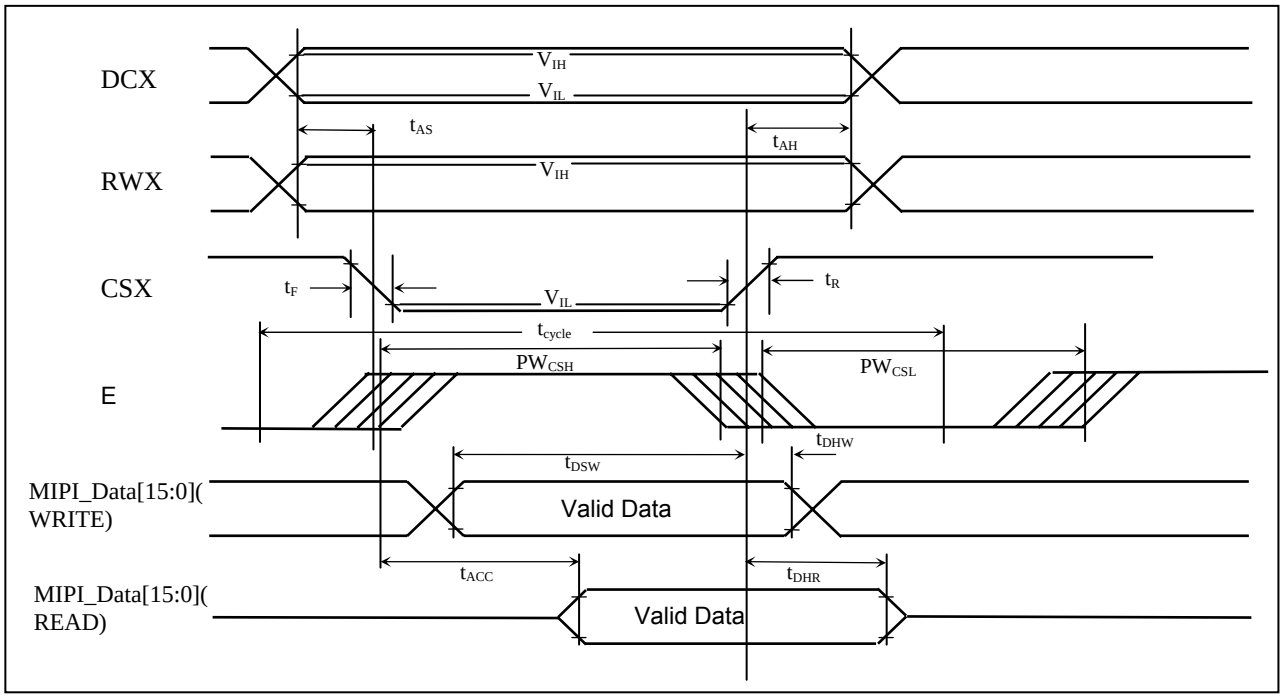


Figure 10-1: 6800 MCU Interface Timing Diagram

10.3 8080 MCU Interface Timing

Table 10-5: 8080 MCU Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	6T	-	-	ns
PW_{CSH}	Control Pulse Low Width	3T	-	-	ns
PW_{CSL}	Control Pulse High Width	3T	-	-	ns
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{ACC}	Data Access Time	-	-	5+4T	ns
t_{DHR}	Read Data Hold time	1+2T	-	5+4T	ns
t_R	Rise Time	-	-	2	ns
t_F	Fall Time	-	-	2	ns

Note: T is PLL output clock period

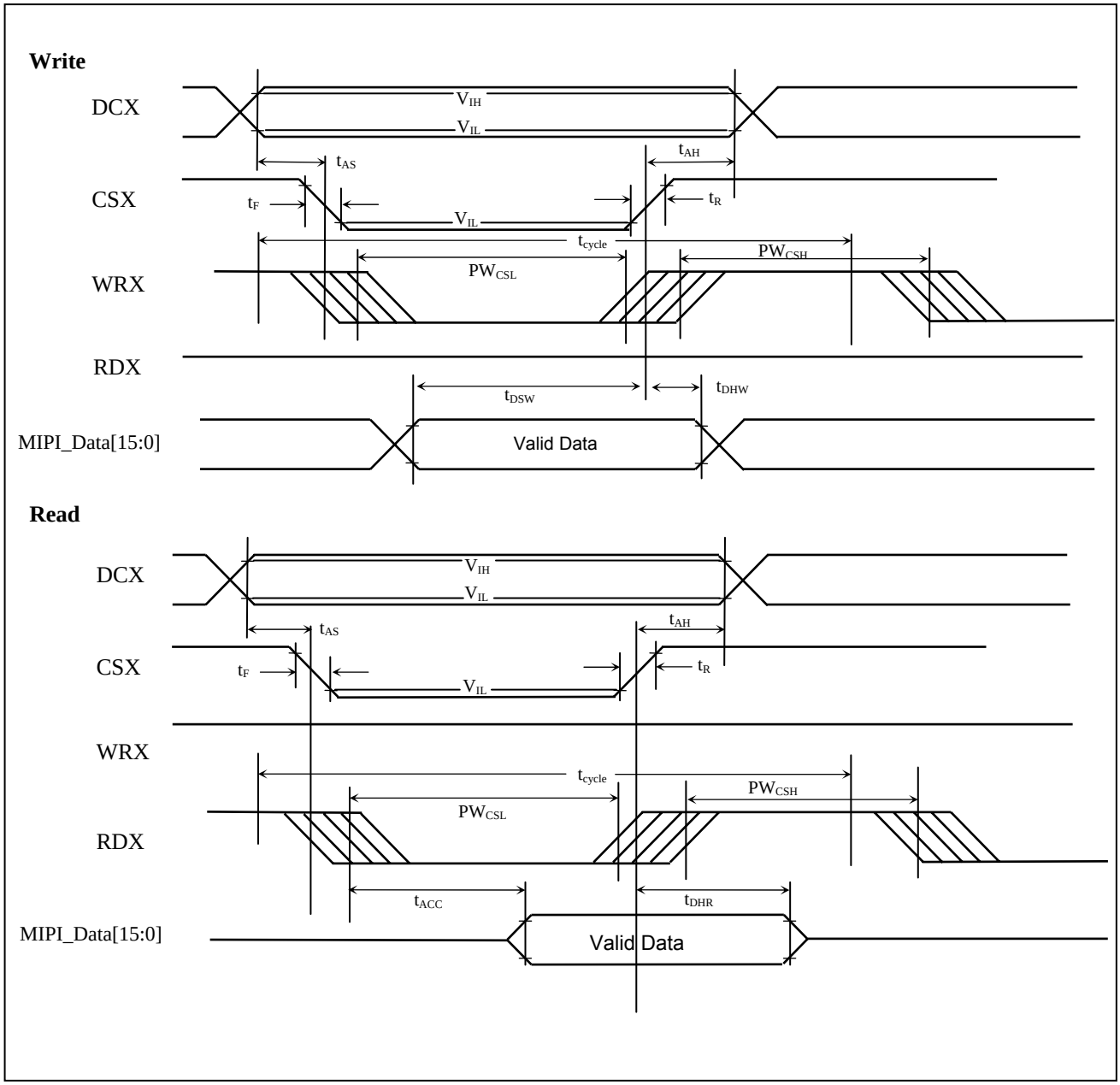


Figure 10-2: 8080 MCU Interface Timing Diagram

10.4 SPI Interface Timing

Table 10-6: SPI Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	8T		-	ns
f_{CLK}	Serial Clock Frequency	-		1/8T	MHz
t_{AS} (2)	Register Select Setup Time	4		-	ns
t_{AH} (2)	Register Select Hold Time	0		-	ns
t_{CSS}	Chip Select Setup Time	4		-	ns
t_{CSH}	Chip Select Hold Time	0		-	ns
t_{DSW}	Write Data Setup Time	4		-	ns
t_{DHW}	Write Data Hold Time	0		-	ns
t_{ACC}	Read Data Access Time	-		4+6T	ns
t_{DHR}	Read Data Hold Time	2+4T		4+6T	ns
t_{CLKL}	Clock Low Time	4T		-	ns
t_{CLKH}	Clock High Time	4T		-	ns
t_{CSWD}	Chip Select Write Delay Time	8T		-	ns
t_{CSRD}	Chip Select Read Delay Time	16T		-	ns
t_R	Rise Time	-		2	ns
t_F	Fall Time	-		2	ns

Note: (1) T is PLL output clock period
(2) for 8 Bit 4 Wire SPI interface only

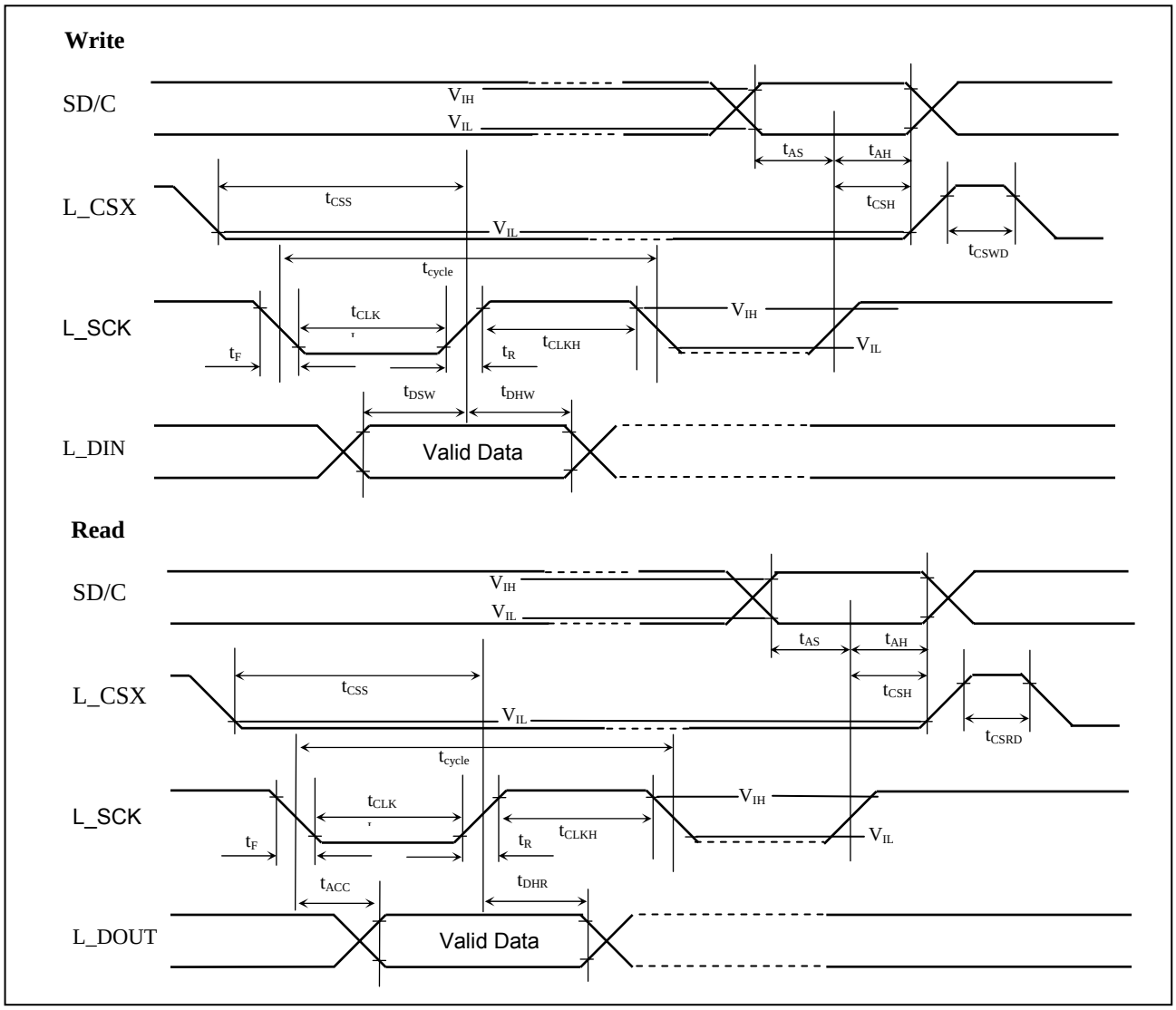


Figure 10-3: 8 Bit 4 Wire SPI Interface Timing Diagram

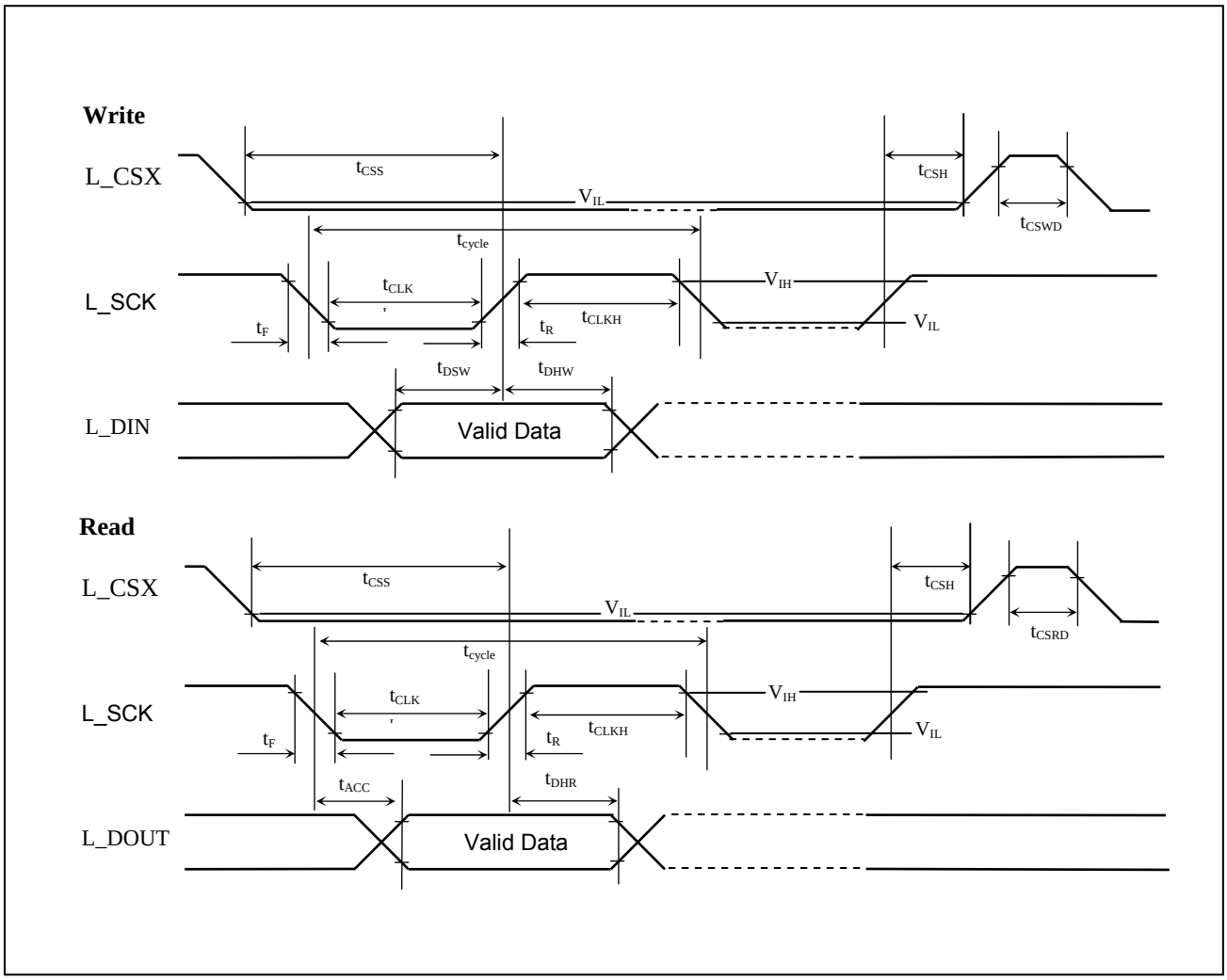


Figure 10-4: 8 Bit 3 Wire & 24 Bit 3 Wire SPI Interface Timing Diagram

10.5 RGB Interface Timing

Table 10-7: RGB Interface Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
t_{DOTCLK}	PCLK Period	16/18/24T	16/18/24T	-	ns
t_{vsys}	Vertical Sync Setup Time	5	-	-	ns
t_{vsyh}	Vertical Sync Hold Time	5	-	-	ns
t_{hsys}	Horizontal Sync Setup Time	5	-	-	ns
t_{hsyh}	Horizontal Sync Hold Time	5	-	-	ns
t_{hv}	Phase difference of Sync Signal Falling Edge	0	-	W	ns
t_{CKL}	PCLK Low Period	8/9/12T	8/9/12T	-	ns
t_{CKH}	PCLK High Period	8/9/12T	8/9/12T	-	ns
t_{ds}	Data Setup Time	5	-	-	ns
t_{dh}	Data Hold Time	5	-	-	ns

Note:

- *T is PLL output clock period*
- *W is the number of pixel in a horizontal line*
- *The PCLK period depends on the bit per pixel (bpp) setting and whether the video mode is burst or non-burst mode. In burst mode, the values in the Min column should be followed. In non-burst mode, the values inthe Typ column should be followed.*

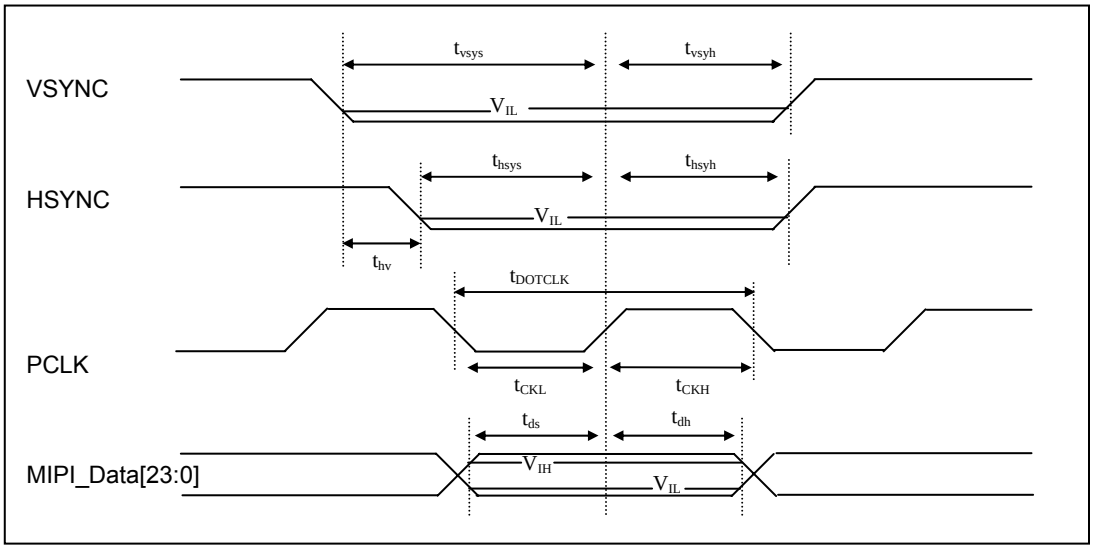


Figure 10-5: RGB Interface Timing Diagram

10.6 RESET Timing

Table 10-8: RESET Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{RESET}	RESET "Low" Pulse Width	100	-	-	μs

10.7 TX_CLK Timing

Table 10-9: TX_CLK Timing Characteristics

Symbol	Parameters	Min	Typ	Max	Units
f_{TXCLK}	TX_CLK Frequency	5	-	50	MHz
t_R	Rise Time	-		5	ns
t_F	Fall Time	-		5	ns

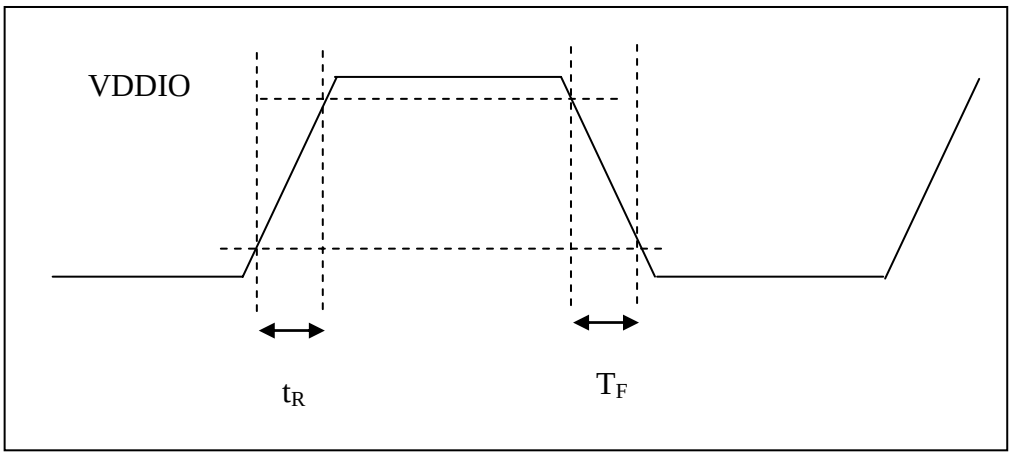
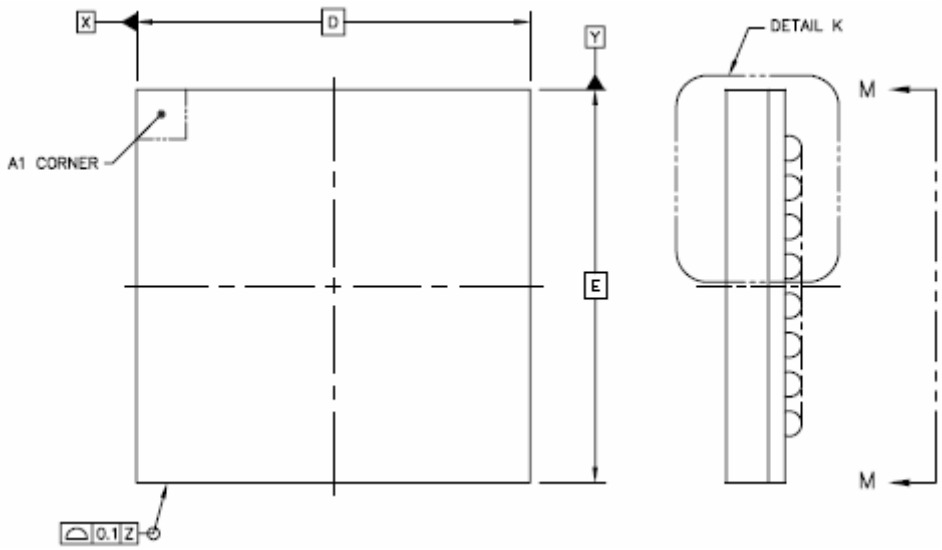
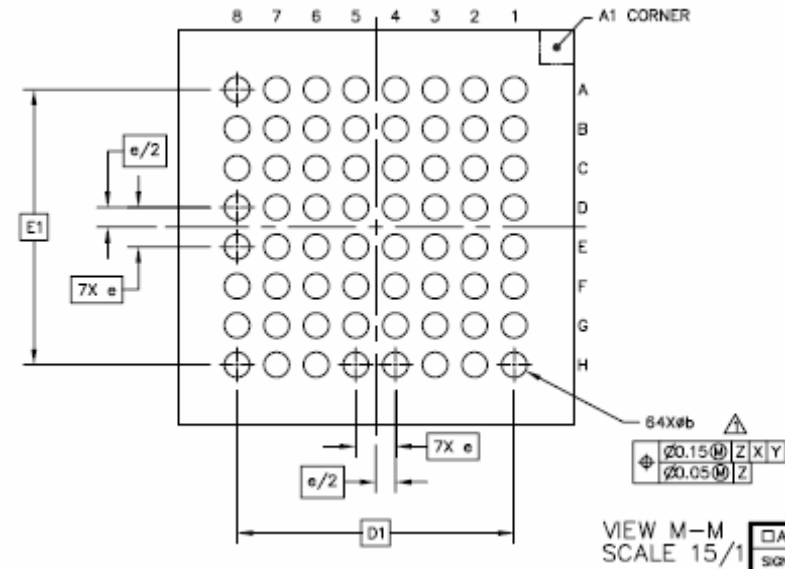


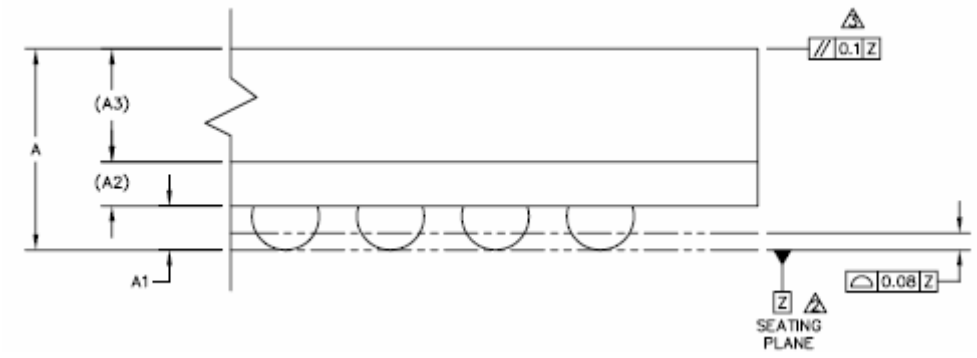
Figure 10-6: TX_CLK Timing Diagram

11 PACKAGE INFORMATION

11.1 64 TFBGA Drawing







Dimension in mm			
Symbol	**Min**	**Typical**	**Max**
A	--	--	1.1
A1	0.16	---	0.26
A2	---	0.21	0.71
A3	---	0.54	0.25
b	0.27	---	0.37
D	---	5.00 BSC	---
E	---	5.00 BSC	---
e	---	0.5 BSC	---
D1	---	3.50 BCS	---
E1	---	3.50	---

11.2 SSD2805 Tape & Reel Drawing

Reel diameter : 330mm

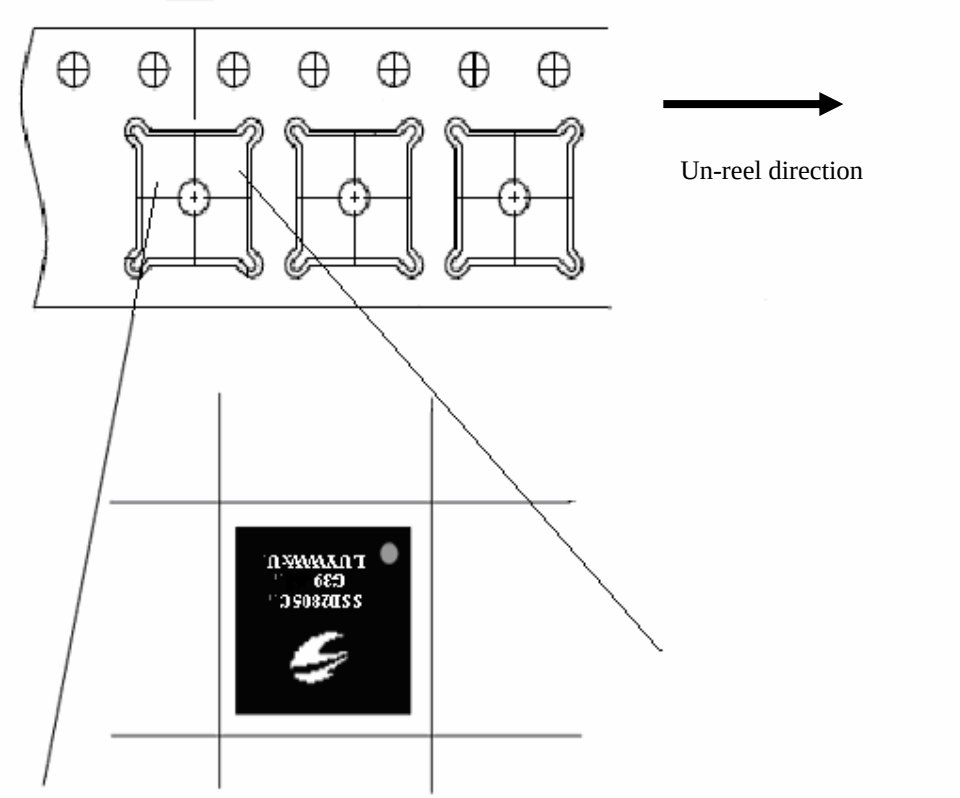
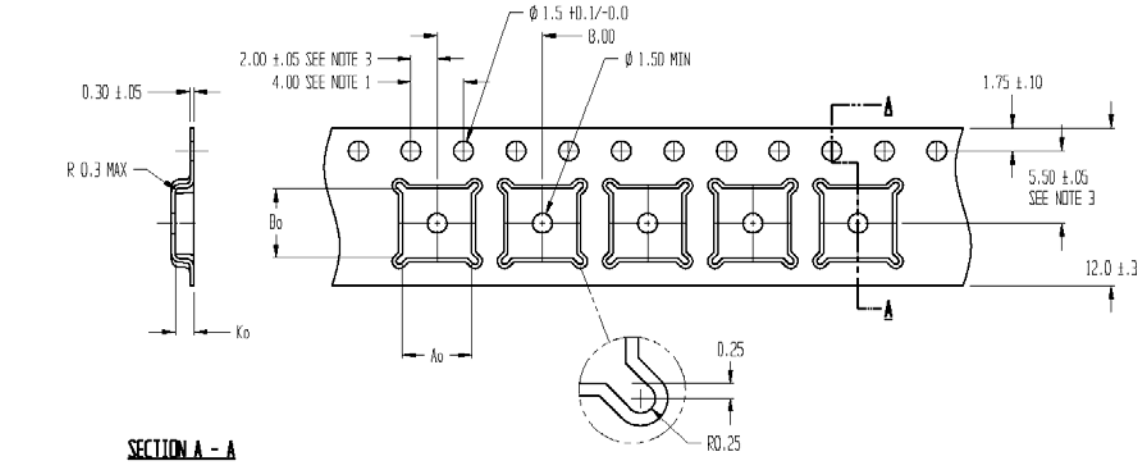


Figure 11-1 Tape & Reel direction



Ao = 5.25
Bo = 5.25
Ko = 1.40

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Figure 11-2 Mechanical drawing of Tape & Reel

12 APPLICATION EXAMPLE

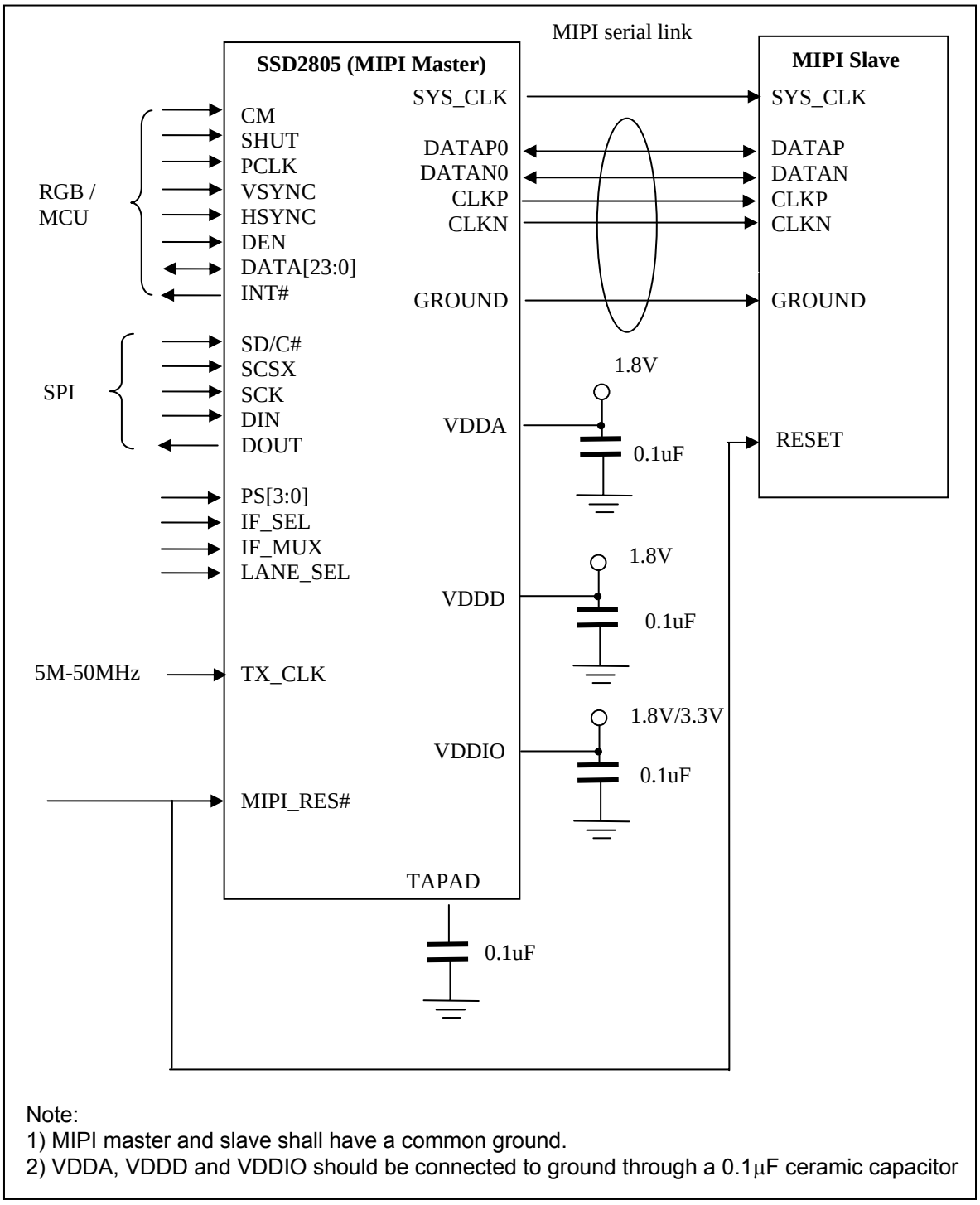


Figure 12-1: SSD2805 Application Block Diagram

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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