



CCD 181

Variable-Element High-Speed Linear Image Sensor

FEATURES

- 2592 x 1 photosite array
- 10 μm x 10 μm photosites on 10 μm pitch
- Anti-blooming and integration control
- Voltage-selectable array lengths:

2592 Elements	2048 elements
1728 elements	1024 elements
- Enhanced spectral response (particularly in the blue region)
- Excellent low-light-level performance
- Low dark signal
- High responsivity
- High speed operation
- Dynamic range typical: 7500:1
- Over 1 V peak-to-peak outputs
- Dark references contained in sampled-and-held outputs
- Special selection available - consult factory



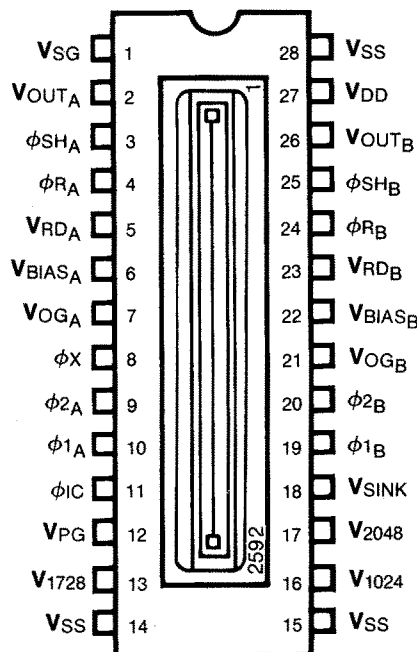
PIN NAME

VSG
 VOUTA
 ϕSHA
 ϕRA
 VRDA
 VBIASA
 VOGA
 ϕX
 ϕ2A , ϕ2B
 ϕ1A , ϕ1B
 ϕIC
 VPG
 V1728
 VSS
 V1024
 V2048
 VSINK
 VOGB
 VBIASB
 VRDB
 ϕRB
 ϕSHB
 VOUTB
 VDD

DESCRIPTION

Amplifier Signal Ground
 Output Amplifier A Source
 Sample and Hold Gate A
 Reset Gate A
 Reset Drain A
 Output Amplifier A Bias
 Output Gate A
 Transfer Clock
 Transport Clocks
 Transport Clocks
 Integration Control Clock
 Photogate
 1728 Active Pixels Switch
 Substrate Ground
 1024 Active Pixels Switch
 2048 Active Pixels Switch
 Anti-Blooming Sink
 Output Gate B
 Amplifier B Bias
 Output Amplifier B Bias
 Reset Gate B
 Sample and Hold Gate B
 Output Amplifier B Source
 Output Amplifier Drain

PIN CONNECTION DIAGRAM (TOP VIEW)



GENERAL DESCRIPTION

The CCD181 is a 2592-element line image sensor designed for industrial measurement, telecine, and document scanning applications which require high resolution, high sensitivity and high data rate. Incorporation of on-chip anti-blooming and integration controls allow the CCD181 to be extremely useful in an industrial measurement and control environment or in environments where lighting conditions are difficult to control.

The CCD181 is equipped with special gates which allow the user to select 4 effective array lengths:

2592 elements: 300-lines/inch across 8.5 inch wide document
 2048 elements: 240-lines/inch across 8.5 inch wide document
 1728 elements: 200-lines/inch across 8.5 inch wide document
 1024 elements: 120-lines/inch across 8.5 inch wide document

The CCD181 is a third generation device having an overall improved performance compared with first and second generation devices, including enhanced blue response and excellent low light level performance, and high-speed operation up to 20 MHz.

The photoelement size is $10\mu\text{m}$ (0.39 mils) $\times$ $10\mu\text{m}$ (0.39 mils) on $10\mu\text{m}$ (0.39 mils) centers. The device is manufactured using Fairchild Imaging's advanced charge-coupled device n-channel isoplanar buried-channel technology.

FUNCTIONAL DESCRIPTION

The CCD181 consists of the following functional elements illustrated in the Block Diagram and Circuit Diagram (see Fig. 1A).

Photosites — A row of 2592 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination

intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gate — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the photosites are transferred in parallel via the transfer gates (ϕ_X) to the transport shift registers whenever the transfer gate voltages go high. Alternate charge packets are transferred to the A and B transport registers.

Two Analog Shift Registers — The transport shift registers are used to move the light generated charge packets delivered by the transfer gates. (ϕ_{1A} , ϕ_{1B} , ϕ_{2A} , ϕ_{2B}) serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets at the output amplifiers.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharge capacitor whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the input gate of the two-stage NMOS amplifiers producing a signal at the output "VOUT" pin. Before each charge packet is sensed, a reset clock (ϕ_{RA} , ϕ_{RB}) recharges the input node capacitor to a fixed voltage (V_{RDA} , V_{RDB}).

Integration and Anti-Blooming Controls — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output. (see Fig. 2)

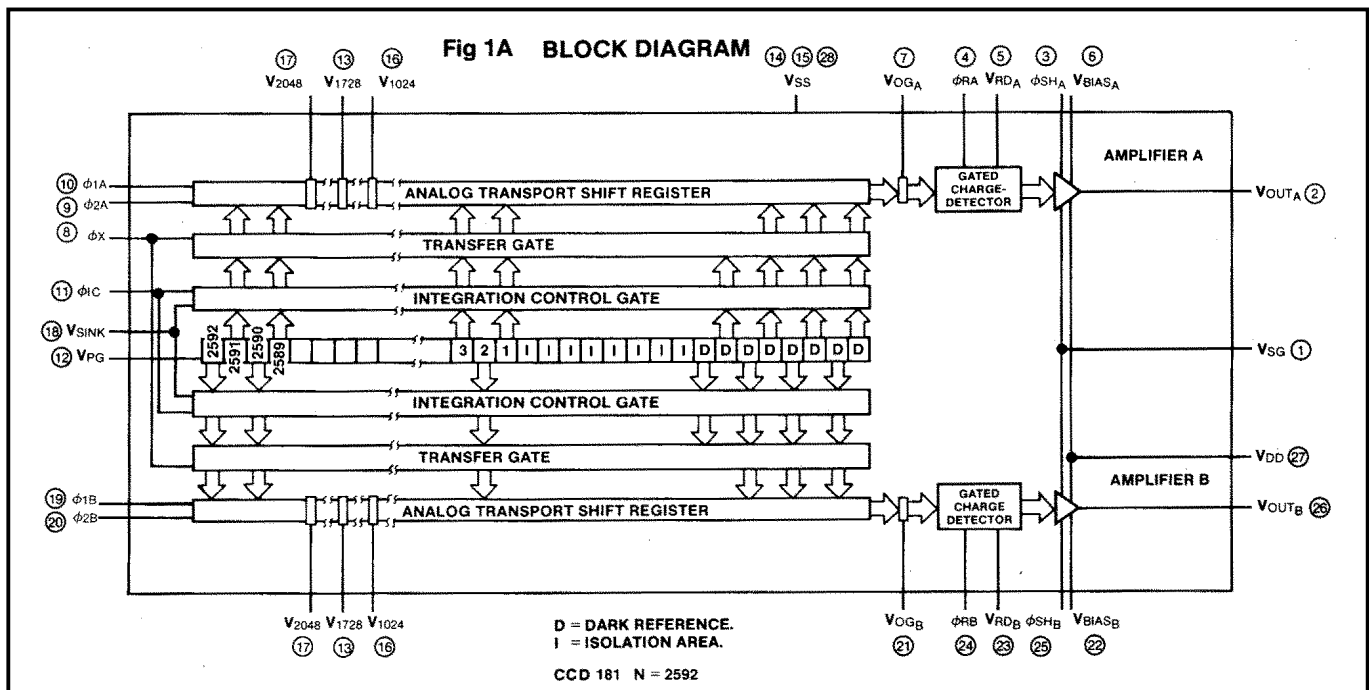


Fig. 1B CIRCUIT DIAGRAM NEAR PIXEL #1024

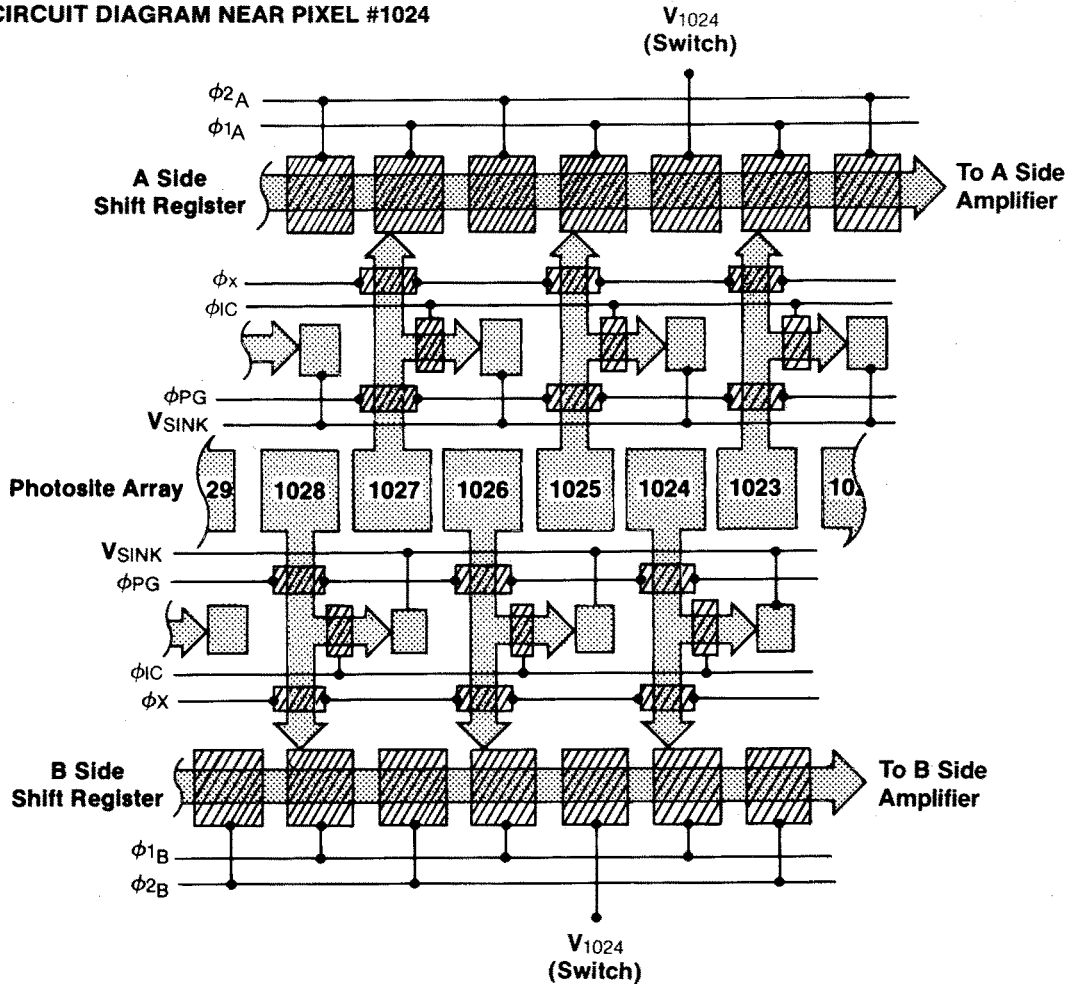


Fig. 2 MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} Voltage

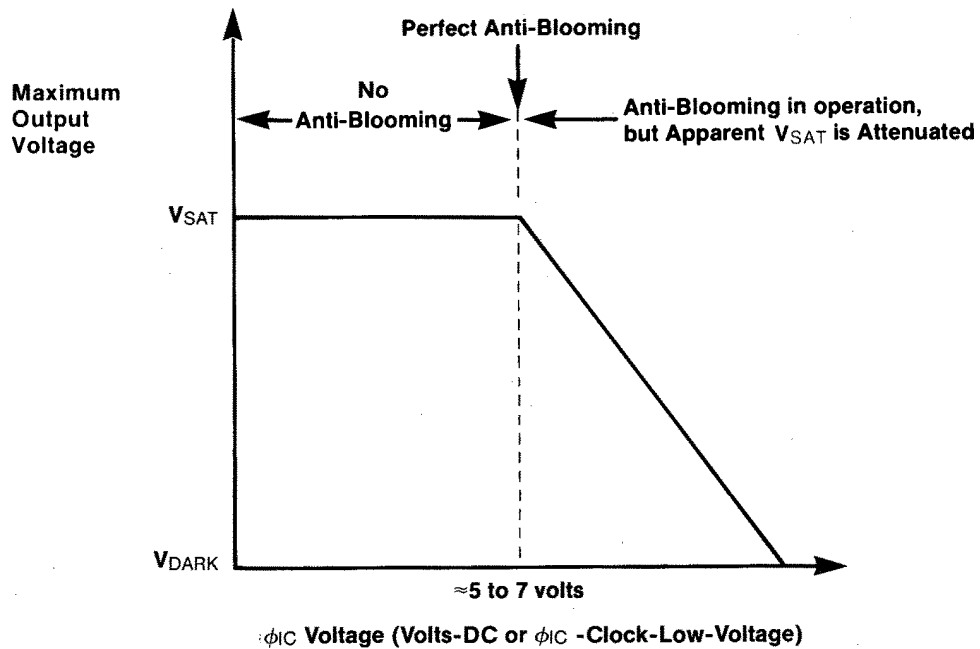
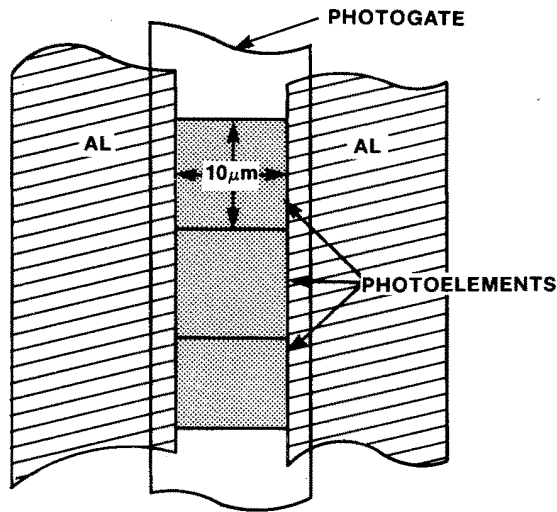
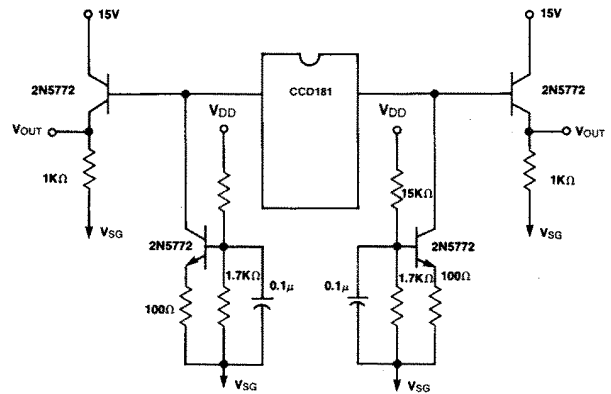




Fig. 4: PHOTOELEMENT DIMENSIONS



TEST LOAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-25° C to +125° C
Operating Temperature	-25° C to +70° C
CCD 181: Pins 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27	-0.3V to +18V
Pin 1	0V
Pins 14, 15, 28	-3.0V to 0V
Pins 2, 26	See Caution Note

CAUTION NOTE:

These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $V_{OUT(A+B)}$ to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: $T_P = 25^\circ\text{C}$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	Note 2
$V_{RD(A+B)}$	Output Reset Drain Supply Voltages	13.5	14.0	14.5	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	
$V_{OG(A+B)}$	Output Gate Bias Voltages	5.5	6.0	6.5	V	
$V_{BIAS(A+B)}$	Amplifier Bias Voltages	2.5	3.0	3.5	V	
V_{SG}	Amplifier Signal Ground	0.0	0.3	0.5	V	
V_{SS}	Substrate Ground	-3.0	-2.0	-1.0	V	
I_{DD}	Output Amplifier Drain Supply Current	6.0	10.0	15.0	mA	

CLOCK CHARACTERISTICS: $T_P = 25^\circ\text{C}$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi X}$ HIGH	Transfer Clock HIGH	11.0	11.5	12.0	V	Note 3
$V_{\phi 1}$ HIGH (A+B) $V_{\phi 2}$ HIGH (A+B)	Transport Clock HIGH	9.5	10.0	10.5	V	Note 3
$V_{\phi R}$ HIGH (A+B)	Reset Clock HIGH	11.0	11.5	12.0	V	Note 3
$V_{\phi SH}$ HIGH (A+B)	Sample/Hold Clock HIGH	11.0	11.5	12.0	V	Note 3
$V_{\phi 1024}$ HIGH	Select 1024 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V_{\phi 1728}$ HIGH	Select 1728 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V_{\phi 2048}$ HIGH	Select 2048 Elements Clock HIGH	9.5	10.0	10.5	V	Note 3
$V_{\phi IC}$ HIGH	Integration Control Clock HIGH		10.0		V	Note 3
$V_{\phi IC}$ LOW	Integration Control Clock LOW		6.0		V	Note 2, 3
$V_{\phi X}$ LOW	Transfer Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V_{\phi 1}$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V_{\phi 2}$ LOW (A+B)	Transport Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V_{\phi R}$ LOW (A+B)	Reset Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V_{\phi SH}$ LOW (A+B)	Sample/Hold Clock LOW	0.0	0.3	0.7	V	Note 2, 3
$V_{\phi 1024}$ LOW	Select 1024 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V_{\phi 1728}$ LOW	Select 1728 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$V_{\phi 2048}$ LOW	Select 2048 Elements Clock LOW	0.0	0.3	0.7	V	Note 2, 3, 5
$f_{data\ max}$	Maximum Output Data Rate	10.0	20.0		MHz	Note 6

AC CHARACTERISTICS: $T_P = 25^\circ\text{C}$, (Note 1, 7), $f_{data} = 3.0\text{MHz}$, $t_{int} = 1.0\text{ms}$, Light Source = $2854^\circ\text{K} + 2.0\text{mm}$ thick Schott BG-38 and OCLI WBHM Filters (Note 4).

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)		1500:1 7500:1			
NEE	RMS Noise Equivalent Exposure		50×10^{-6}		$\mu\text{J}/\text{cm}^2$	
SE	Saturation Exposure		0.3		$\mu\text{J}/\text{cm}^2$	
CTE	Charge Transfer Efficiency	.99996	.99999			Note 8
V_O	Output DC Level	4.0	9.5	11	V	
Z	Output Impedance		1		K Ω	
P	On-Chip Power Dissipation: Amplifiers		159	200	mW	
N	Peak-to-Peak Temporal Noise		0.7		mV	

PERFORMANCE CHARACTERISTICS: $T_P = 25^\circ\text{C}$ (Note 1, 7), $f_{\text{data}} = 3.0\text{MHz}$, $t_{\text{int}} = 1.0\text{ms}$, Light Source = $2854^\circ\text{K} + 2.0\text{mm}$ thick Schott BG-38 and OCLI WBHM filters (Note 4).

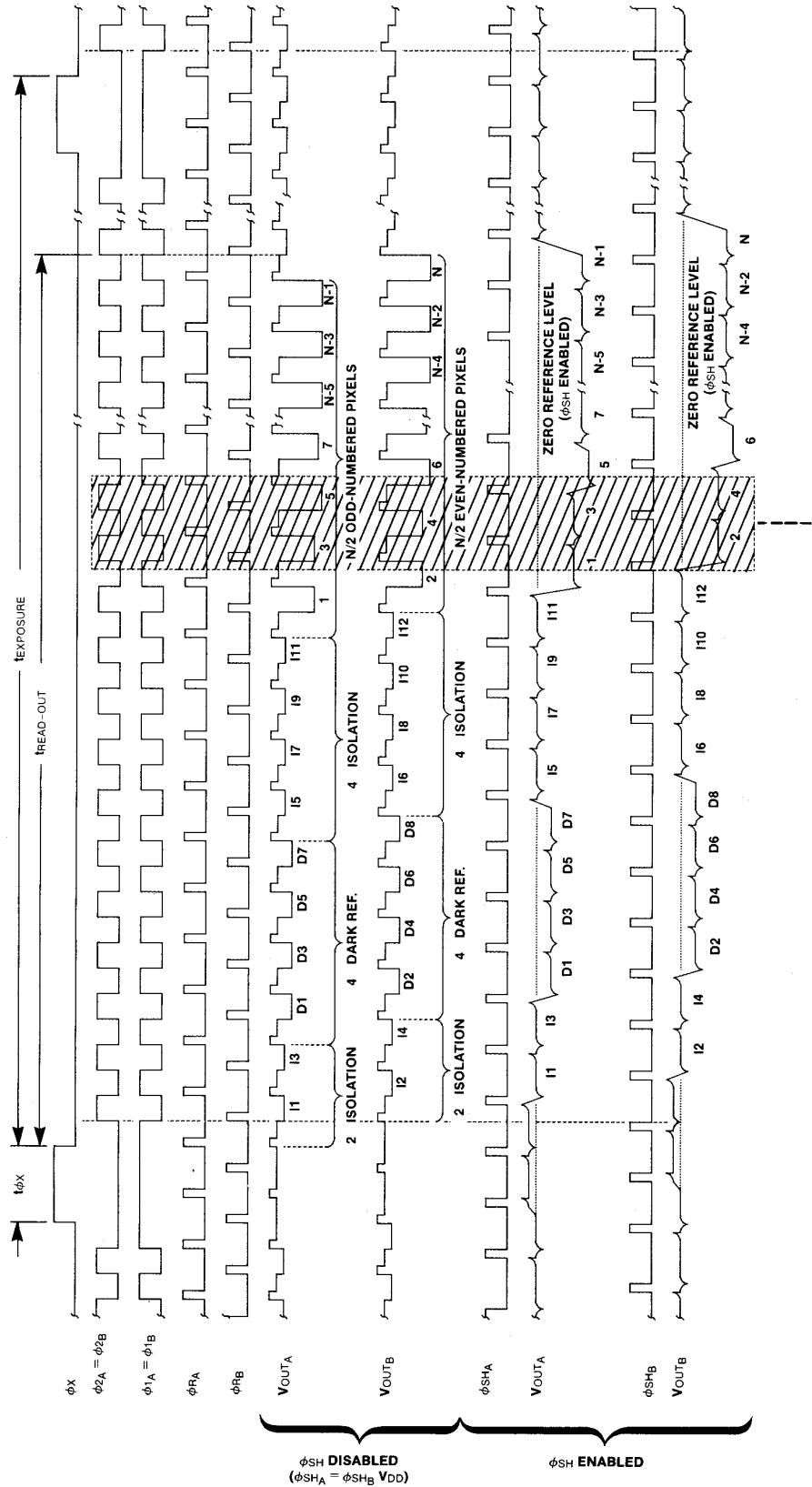
SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITION
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-uniformity					
	Peak-to-Peak		60	160	mV	
	Peak-to-Peak without single pixel and Positive and Negative Pulses		40		mV	
	Single-pixel Positive Pulses		35		mV	
	Single-pixel Negative Pulses		35		mV	
M Video	Video Mismatch		50	150	mV	Note 9
M DC	DC Mismatch		0.5	2.0	V	Note 10
DS	Dark Signal:					Notes 11, 12
	DC Component		1	2	mV	
	Low Frequency Component		1	2	mV	
SPDSNU	Single Pixel DS Non-Uniformity		1	2	mV	Note 12
R	Responsivity		4.0		V/ $\mu\text{J}/\text{cm}^2$	
VSAT	Saturation Output Voltage	0.7	1.0	1.8	V	

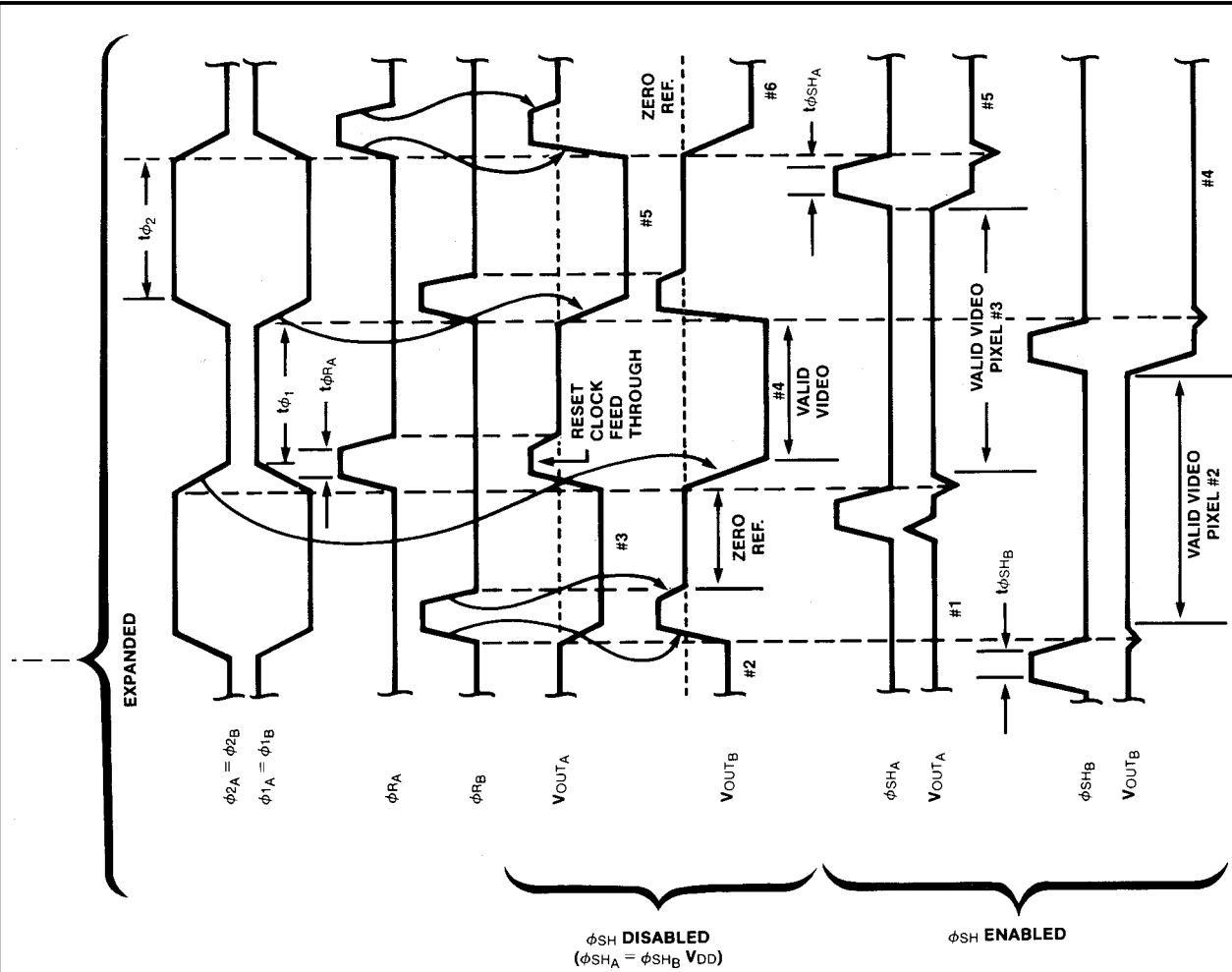
- * All PRNU measurements are taken at an 800 mV output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

NOTES:

1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the package.
2. Negative transients on any clock pin going below 0.0 volts may cause charge injection, which results in an increase in apparent DS. Adjusting V_{SS} to a more negative voltage than the clock low voltages will reduce charge injection, if present.
3. $C_{\phi X} = 150\text{pF}$, $C_{\phi EC} = 250\text{pF}$, $C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} = 300\text{pF}$
 $C_{\phi RA} = C_{\phi RB} = C_{\phi SHA} = C_{\phi SHB} = 5\text{pF}$, $V_{1024} = V_{1728} = V_{2048} = 50\text{pF}$
4. OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.
5. Pixel Length Selection
 - (a) To use the device with 2592 active pixel elements:
Connect V_{1024} , V_{1728} , and V_{2048} to the ϕ_2 (A or B) clock.
 - (b) To use the device with 2048 active pixel elements:
Connect V_{1024} , V_{1728} to the ϕ_2 (A or B) clock.
Connect V_{2048} to V_{SS}
 - (c) To use the device with 1728 active pixel elements:
Connect V_{1024} and V_{2048} to the ϕ_2 (A or B) clock.
Connect V_{1728} to V_{SS}
 - (d) To use the device with 1024 active pixel elements:
Connect V_{1728} and V_{2048} to the ϕ_2 (A or B) clock.
Connect V_{1024} to V_{SS}
6. The minimum clock frequency is limited by increases in dark signal.
7. Measurements made with sample and hold enabled.
8. CTE is the measurement for a one-stage transfer.
9. Video mismatch is the difference in AC amplitudes between $V_{OUT A}$ and $V_{OUT B}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
10. DC mismatch is the difference in DC output level V_O between V_{OUT} and $V_{OUT B}$.
11. Dark signal component approximately doubles for every 5 to 15°C in T_P .
12. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5 to 15°C increase in T_P .

CCD181 TIMING DIAGRAM





- NOTES:
- Timing requirements for ϕ_1 and ϕ_2 :
 - $50 \pm 10\%$ duty cycle, $\sim 180^\circ$ out of phase (See 1b).
 - ϕ_1 and ϕ_2 clocks must cross at $\geq 4V$.
 - (Both ϕ_1 and ϕ_2 must not be $< 4V$ simultaneously.)
 - $(0.1 \cdot t_{\phi_2}) \leq (t_{rise} = t_{fall}) < (0.4 \cdot t_{\phi_2})$
 - Timing requirements for ϕ_{RA} and ϕ_{RB} :
 - $20ns \leq (t_{rise} = t_{fall}) < (0.3 \cdot t_{\phi_1})$
 - $30ns \leq (t_{\phi_{RA}} = t_{\phi_{RB}}) < t_{\phi_2}$
 - tail time of ϕ_{RA} must not overlap t_{rise} of ϕ_{RA}
 - tail time of ϕ_{RB} must not overlap t_{rise} of ϕ_{RB}
 - Timing requirements for ϕ_{SHA} and ϕ_{SHB} :
 - $20ns \leq (t_{rise} = t_{fall}) < (0.3 \cdot t_{\phi_2})$
 - $(t_{\phi_{SHA}} = t_{\phi_{SHB}}) \geq 80ns$
 - tail time of ϕ_{SHA} must not overlap t_{fall} time of ϕ_2
 - tail time of ϕ_{SHB} must not overlap t_{fall} time of ϕ_1
 - Timing requirements for ϕ_X :
 - $t_{\phi_X} \geq 0.1 \mu s$
 - t_{rise} and t_{fall} times of ϕ_X must not overlap t_{rise} or t_{fall} times of ϕ_1 or ϕ_2 .
 - Effective number of pixels "N" is selected by "V_{switch} (#1)" pins as follows:

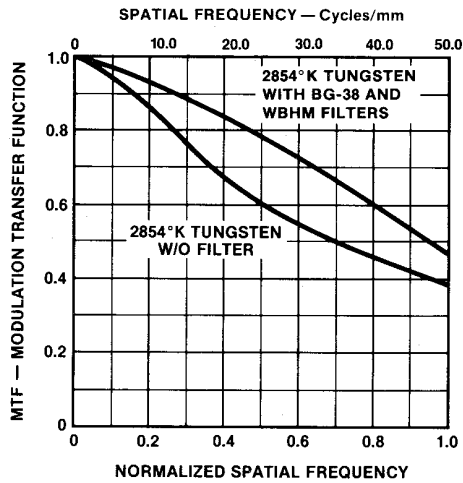
INPUTS TO V _{SWITCH} PINS:			
N	V _{SWITCH} (1024)	V _{SWITCH} (1728)	V _{SWITCH} (2048)
1024	V _{SS}	ϕ_2	ϕ_2
1728	ϕ_2	V _{SS}	ϕ_2
2048	ϕ_2	ϕ_2	V _{SS}
2592	ϕ_2	ϕ_2	ϕ_2

Resistance between the clocked V_{switch} pins and the ϕ_{2A} and ϕ_{2B} pins should be negligible ($< 10\Omega$).

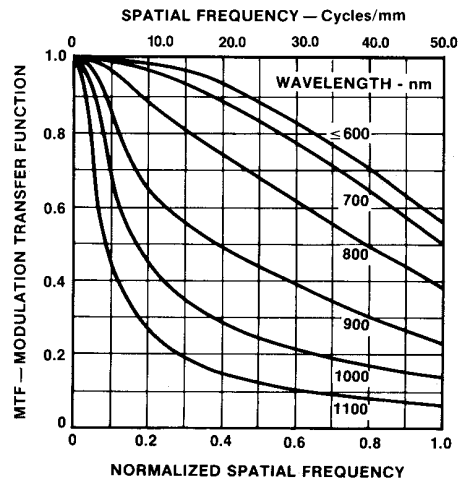
- Integration Control Clock (ϕ_{IC}) has been omitted from these timing diagrams for clarity. See "Integration Control Clock Timing" diagram for details (Fig. 3).

TYPICAL PERFORMANCE CURVES

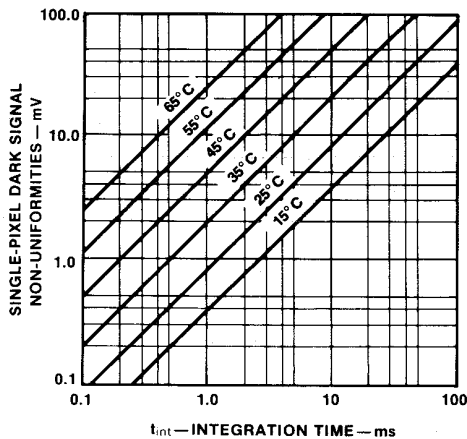
MODULATION TRANSFER
FUNCTIONS FOR TWO BROADBAND
ILLUMINATION SOURCES



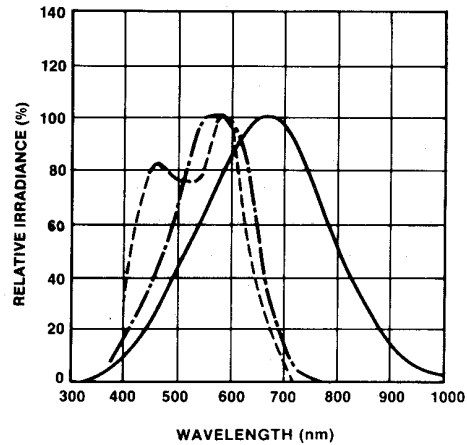
MODULATION TRANSFER
FUNCTIONS FOR NARROW BAND
ILLUMINATION SOURCES



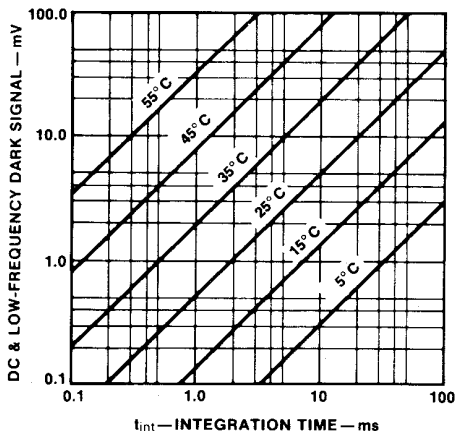
SINGLE-PIXEL DARK
SIGNAL NON-UNIFORMITIES
VERSUS INTEGRATION TIME



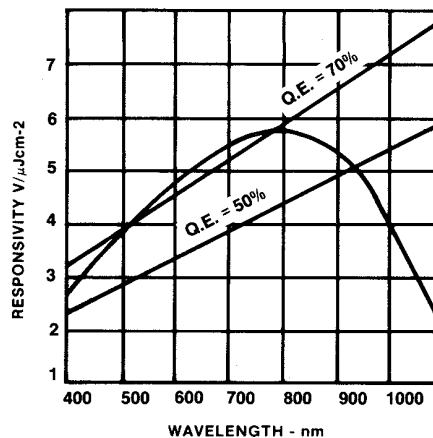
*RELATIVE RADIANT FLUX
VS WAVELENGTH



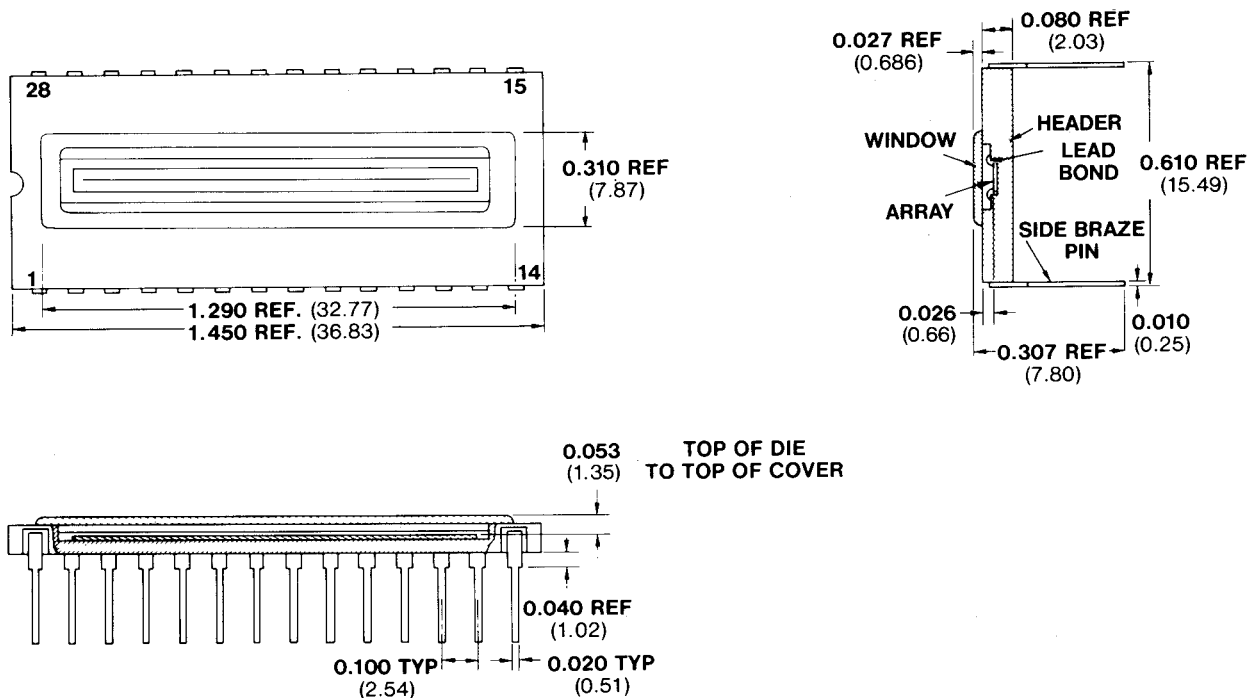
DC AND LOW-FREQUENCY
DARK SIGNAL VS INTEGRATION TIME



TYPICAL SPECTRAL RESPONSE



PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 12°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD181DC where "D" stands for a ceramic package and "C" for commercial temperature range.

