1. GENERAL DESCRIPTION

The W538A8xx, a member of the ***ViewTalk***™ family, is an 8-bit microprocessor (uP) with a speech and melody synthesizer and 64SEG x 16COM LCD driver unit, which includes an internal regulator, pump circuit and two pages of dedicated LCD RAM. The W538A8xx can synthesize 8 channels of melody or speech (up to 2 of these channels can be speech; the rest are melody) and drive an LCD display simultaneously. The W538A8xx accepts midi scores in MIDI format 0, and it has multiple power modes to minimize power dissipation, based on different speech, melody, and LCD needs.

The Serial-memory Interface Manager (**SIM**) is designated for cartridge applications. Using the SIM, the W538A8xx can access Winbond-proprietary, serial-memory chips W55Fxx and W551Cxxx.

It is also ideal for games, remote controllers, watches, clocks and other applications that incorporate both LCD display and speech or midi.

Item	W538A8xx	
CPU	8 bits µC	
ROM	W538A801	121 KB
	W538A802	249 KB
	W538A804	505 KB
	W538A806	761 KB
	W538A808	1017 KB
Working RAM	1K Bytes	
LCD RAM	2* **128** Bytes	
Dedicated I/O (1)	W538A802/1	20*
	W538A808/6/4	24

* (1). P0, BP1, BP2.4 ~ BP2.7

Voice duration calculation (Unit: Kbyte)

Item	ROM	Timbre and F/W Library	LCD Picture (1)	User program	Midi song (2)	Voice Duration (sec) (3)
W538A802	249	64	62.5	40	20	16 sec
W538A804	505	64	62.5	40	20	84 sec
W538A806	761	64	62.5	40	20	153 sec
W538A808	1017	64	62.5	40	20	221 sec

(1). LCD picture = 62.5KB for 500 picture (based on 1 K dots [bits])

(2). 5 midi songs and 4 KB / song.

(3). Voice duration using 5-bit MDPCM, 6-KHz sample rate.

2. FEATURES

- [1]High performance 8-bit uP able to synthesize speech, melody and to draw pictures:
  - 4MHz @ 2.4V
  - 5MHz @ 2.7V
  - 6MHz @ 2.9V
  - 8MHz @ 3.2V
  - 10MHz @ 3.6V
- Two System clocks, main-clock and sub-clock, both configurable
  - The Main-clock can be X'tal or ring type (based on **pin option**)
  - The Sub-clock (32768Hz) can be X'tal or RC type (based on **mask option**)
- Sophisticated power management methodology: SLOW, HOLD and STOP modes
- Single ROM architecture to store program, user data/table, speech, timbre, score and picture
- 1 KB of Working RAM (**W-RAM**) for complicated application
- Dual-page, 2 x 128 bytes LCD RAM (**L-RAM**) for smooth animation
- LCD driver unit
  - 64 SEG X 16 COM
  - 1/4 or 1/5 bias and 1/8 or 1/16 duty cycle
  - Built-in LCD regulator for stable display quality while speech or melody is playing
  - Built-in drawing operators, such as PUT, INV, AND, OR, XOR, etc., to simplify programming
- Maximum 24 I/O pins (BP0 ~ 2) and 8 of them can sinking 8mA
  - 8 I/O pins can sink 8mA
  - Some LCD SEGMENT pins can be used as additional input or output pins
- 8 channels of simultaneous speech and melody synthesis
  - Unlimited kinds of instruments with pre-stored waveforms
  - Speech synthesis at programmable playback rates
  - 1-channel speech + 7-channel WinMelody
  - 1-channel voice-melody + 7-channel WinMelody
  - 1-channel speech + 1-channel percussion + 6-channel WinMelody
- Speaker driver
  - DAC current type: maximum output 3mA / 5mA (register option), 10 bit resolution

[1] The minimum operating voltage deviation is 0.2V.

- ❑ PWM direct drive: 10-bit resolution, maximum 128 KHz sampling rate @ 8MHz system clock
- Automatic IR-carrier generation for interactive applications
- Low battery detector (**LVD**) for battery-life management application
- Low Voltage Reset (**LVR**)
- Serial-Memory Interface Manager (**SIM**) to interface with cartridge applications
- Built-in Watch-Dog Timer (**WDT**) that is activated by mask option only

3. PIN DESCRIPTION

Name	I/O	Description
BP0.0 – BP0.7	I/O	Bi-direction port 0. As an input pin, it can be pulled-high or float. As an output port, it can be an inverter or open drain type output. The configuration is controlled by the associated bits in BP0D and BP0M registers. BP0.7 share with the IR carrier output. Each BP0 port can detect SEG strobe queuing signal in BP0V register.
BP1.0 – BP1.7	I/O	Bi-direction port 1. As an input port, it can be pulled-high or float. As an output port, it can be an inverter or open drain type output. The configuration is controlled by the associated bits in the BP1D and BP1M registers. If the SIM is enabled, the BP1.0 pin shares with the DATA pin, BP1.1 shares with the ADDR pin, and BP1.2 shares with the CLK pin to access data from the external serial flash (W55FXX) or mask ROM (W551Cxx).
BP2.0 – BP2.7[2]	I/O	Bi-direction port 2. As an input port, it can be pulled-high or float. As an output port, it can be an inverter or open drain type output. The configuration is controlled by the associated bits in the BP2D and BP2M registers.
DAC/PWM+	O	DAC output / PWM driver positive output
PWM-	O	PWM driver negative output
TEST	I	Test pin, internally pulled low. It is pulled high in TEST mode.
XIN	I	Input pin for the main-oscillator. When XSEL is high, connect a resister between RXIN and VSS to generate the main clock. When XSEL is low, connect 4MHz to 10MHz crystal between XIN and XOUT.
XOUT	O	Output pin for the main-oscillator. Connect a 4MHz to 10MHz crystal between XIN and XOUT.
XSEL	I	Main clock select pin. When XSEL is high, the ring oscillator is used; when XSEL is low, the crystal oscillator is used. This is a floating input.
X32I	I	Input pin for the sub-oscillator. When mask option set RC type, connect RS to X32O to generate the sub clock. When mask option set crystal, connect a 32KHz crystal between X32I and X32O.
X32O	O	Output pin for the sub-oscillator. Connect a 32KHz crystal between X32I and X32O.
DH1-DH2	I	Connection terminals the voltage doubling capacitor used in the LCD driver.

Notes:

[2] @ W538A802 and W538A801: BP2.4 ~ BP2.7

Name	I/O	Description
V2[3]	I/O	Voltage regulator output pin. It requires an external capacitor (0.1uf). If the internal pump is enabled (LCDMC1.5 = 0/default), the V2 output level is controlled by LCDMC0[6:3] If the external reference voltage is selected (LCDMC1.5 = 1), the V2 input voltage should not be over 1.5 Volts to prevent chip damage. The LCD operating voltage (VLCD) is 4 * V2 or 5 * V2, depending on 1/4 bias or 1/5 bias. VLCD should be higher than (VDD - 0.5 V) to prevent chip leakage currents.
V3-V6	O	LCD COM / SEG output driving voltage. Each pin requires an external capacitor.
SEG59-SEG56, SEG51-SEG48	O/I	LCD segment output pads. These can be shared to provide additional input pins using register LCDIMC.0 and 1 bit 1. The default function is LCD segment output pad.
SEG63-SEG60, SEG55-SEG52	O/O	LCD segment output pads. These can be shared to provide additional output pins using register LCDOMC.0 and 1 bit 1. The default function is LCD segment output pad.
SEG47-SEG16	O	LCD segment output pins.
SEG15-SEG0	O	LCD segment output pins. These can be shared to provide output pins for key-matrix scanning.
COM15-COM0	O	LCD common output pins.
VDD1_SPK	-	Positive power PWM/DAC driver.
VSS1_SPK	-	Negative power PWM/DAC driver.
VSS2_SPK	-	Negative power PWM/DAC driver.
VDD * 2	-	Positive power supply. Used by oscillator, uP, logic cells and I/O buffers.
VSS * 2	-	Negative power supply. Used by oscillator, uP, logic cells and I/O buffers.

[3] 0.1uF is default value, but the capacitor value should be larger than 0.1uF if the LCD dot size is over 0.5mm * 0.5mm

4. When working at NMOS open drain mode, external pull high voltage can't higher than VDD to avoid leakage current

4. ELECTRICAL CHARACTERISTICS

. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

A. D.C. Characteristics

(VDD–VSS = 4.5V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD panel on with dot size 0.5mm*0.5mm; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V_{DD}	-	2.4	-	5.5	V
Operating Current	I_{OP1}	Dual clock, VDD=3V	-	5	7.5	mA
	I_{OP1}	Sub clock only, VDD=3V	-	40	50	uA
Hold Mode Current (Sub-clock active only)	I_{OP2}	LCD OFF, VDD=3V,		8	10	uA
		LCD ON, VDD=3V,	-	-	70	uA
Standby Current (STOP)	I_{OP3}	LCD OFF, VDD=3V	-	-	1	uA
LCD supply current (No load)	I_{LCD}	LCD ON, All SEG ON, VDD=3V	-	30	40	uA
Input Low Voltage	V_{IL}	All Input Pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All Input Pins	0.7V_{DD}	-	V_{DD}	V
Input Current BP0, BP1, BP2	I_{IN}	VIN = 0V	-5	-	-15	μA
Input Current RESETB	I_{IN1}	VIN = 0V	-15	-	-45	μA
Output Current BP0	I_{OL1}	VDD = 3V, VOUT = 0.4V	8	-	-	mA
	I_{OH1}	VDD = 3V, VOUT = 2.6V	-4	-	-	mA
Output Current BP1, BP2	I_{OL2}	VDD = 3V, VOUT = 0.4V	4	-	-	mA
	I_{OH2}	VDD = 3V, VOUT = 2.6V	-4	-	-	mA
Output Current LCDOP0	I_{OL3}	VDD = 3V, VOUT = 0.4V	-300	-	-	μA

DC Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Current SPK0+ / SPK0-[4]	I_{OL1}	RLOAD=8 Ohm, Connection: [SPK+]----[R]----[SPK-]	+200	-	-	mA
	I_{OH1}		-200	-	-	mA
DAC full scale current	I_{DAC}	RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
COM/SEG on resister	Ron	IOH=+/- 50uA	-	5	10	KΩ
V2 Pad Output Voltage	V_{RR}	Depended on LCDM4	0.7	-	1.45	V
V2 Pad Output Deviation [5]	V_{D1}	No Load	-	-	± 5	%
V2 Pad Voltage Step	V_{R2}	V2 increased 1 level	-	50	-	mV
V2 input voltage	V_{EXT}	LCDMC1.5 = 1	0.7	-	1.45	V
V6 Pad Output Voltage [4] (LCD's VLCD depends on LCDMC0 register)	V_{LCD}	1/4 Bias & no load	3.9 *V2	-	4 *V2	V
	V_{LCD}	1/5 Bias & no load	4.75 *V2	-	4.95 *V2	V
LVD operating current	I_{LVD}		-	10	20	uA
LVD tolerance of threshold voltage	V_{D2}			5	7.5	%
LVR operating current	I_{LVR}		-	5	10	uA

[4] PWM current deviation will be ±20%.

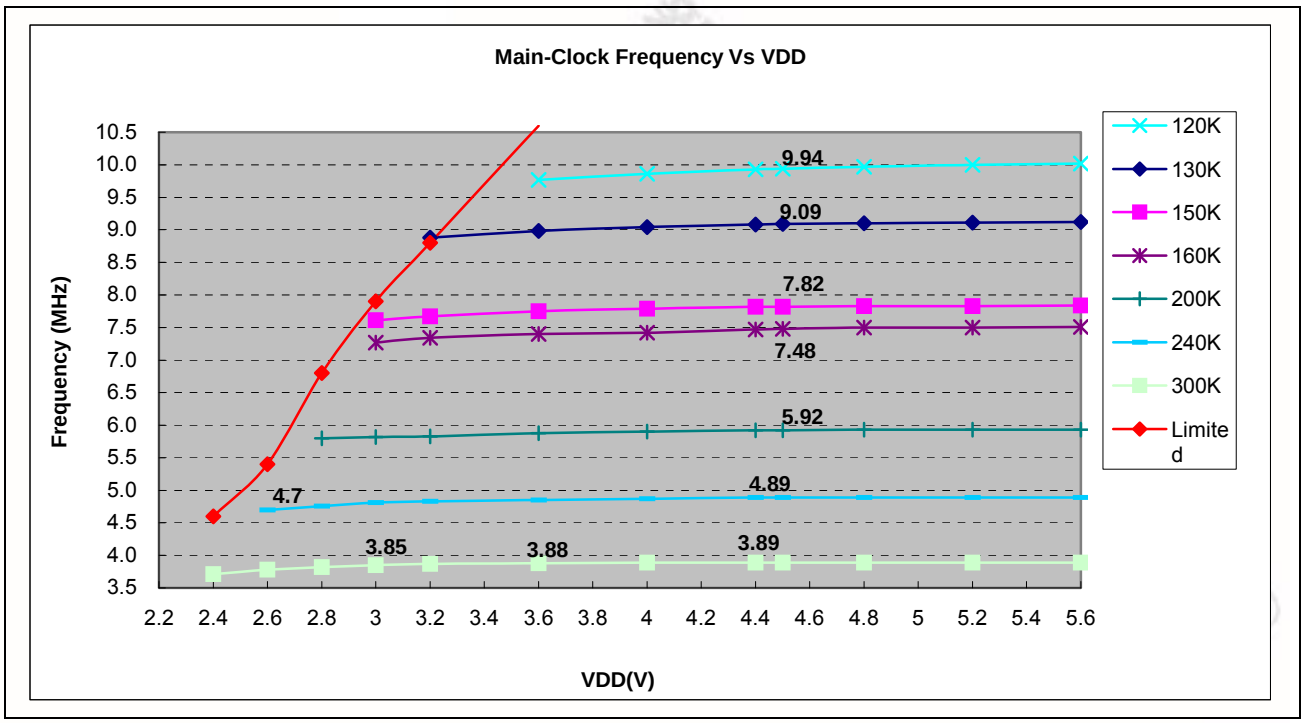
[5] Deviation is governed by LCD dot size. Larger LCD dots get larger deviations

AC CHARATERISTICS

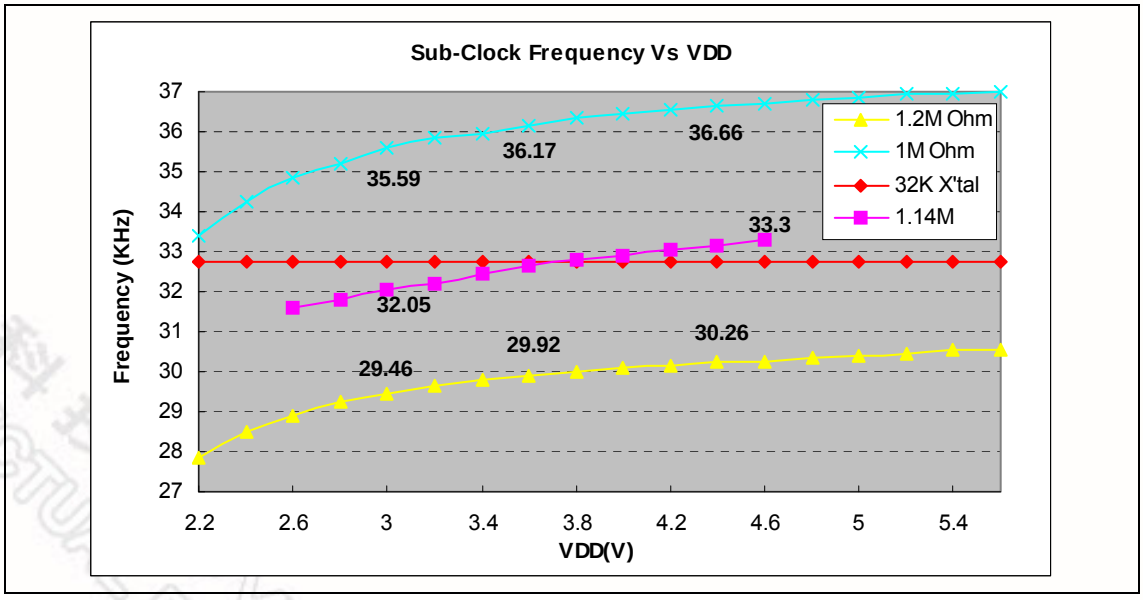
(VDD–VSS = 3.0V, No load, FM = 4 MHz with Ring mode, Fs = 32.768 KHz, with Xtal mode, T_A = 25° C, STN LCD on with dot size 0.5mm*0.5mm; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-clock Frequency	F_{SUB}	Crystal type and X32I and X32O.	-	32768	-	Hz
Main-clock Frequency	F_M	Ring type/Crystal type	-	-	10M	Hz
Chip Operation Frequency	F_{OSC}	CLCK.0=0,F_{SYS}=F_{SUB}	-	32768		Hz
		CLCK.0=1,F_{SYS}= F_{MAIN}	-	-	10M	
Cycle Time	T_{CYC}	F_{SYS} = 4 MHz	250	-	DC	nS
Reset Active Width	T_{RAW}	F_{OSC} = 32.768 KHz	1	-	-	μS
Interrupt Active Width	T_{IAW}	F_{OSC} = 32.768 KHz	1	-	-	μS
Main clock Ring frequency	F_{ROSC}	Rosc =300KΩ	-	4M	-	Hz
		Rosc =200KΩ	-	6M	-	
		Rosc =160KΩ	-	8M	-	
		Rosc =120KΩ		10M		
Sub-Clock RC Oscillator	F_{RSUB}	R_{SUB}=1.1MΩ		32		KHz
Sub-Clock Oscillation Stable Time @ Cold Start	F_{STOP}	R_{SUB}=1.1MΩ	0.8	-	1	S
Frequency Deviation of main-clock F_m = 4 MHz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	3	5	%
Frequency Deviation of main-clock F_m = 6 MHz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	5	10	%
Frequency Deviation of main-clock F_m =4 ~10MHz	$\frac{\Delta f}{f}$	$\frac{F(5.5V)-F(3.6V)}{F(3.6V)}$	-	3	5	%
Frequency Deviation of F_{RSUB} = 32768Hz	$\frac{\Delta f}{f}$	$\frac{F(3.6V)-F(2.4V)}{F(3.6V)}$	-	5	10	%
Frequency Deviation of F_{RSUB} = 32768Hz	$\frac{\Delta f}{f}$	$\frac{F(5.5V)-F(3.6V)}{F(3.6V)}$	-	3	5	%
Frame frequency	F_{LCD}	LCDMC1=03H (default)	-	64		Hz

B. Main-Clock oscillation Freq Vs. Resistor

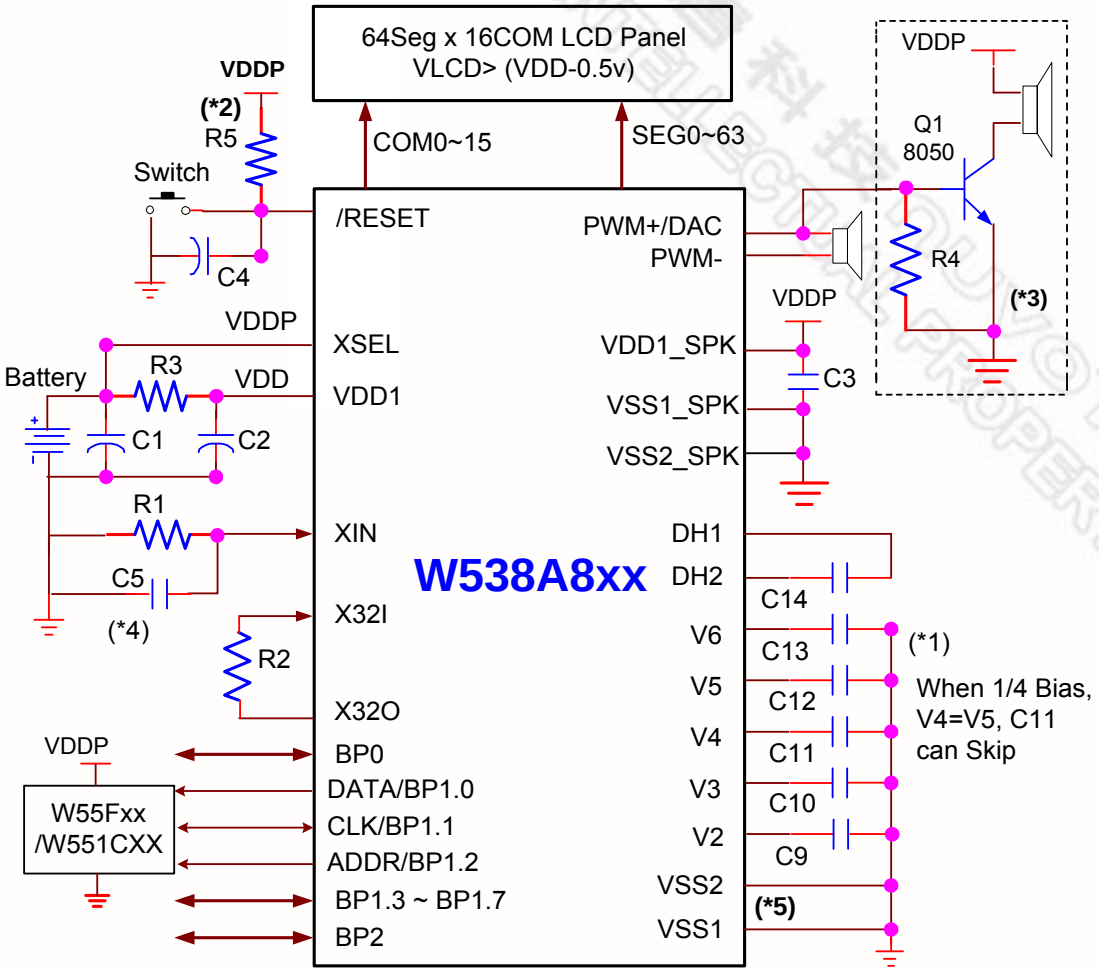


C. Sub-Clock oscillation Freq Vs. Resistor



5. TYPICAL APPLICATION CIRCUIT

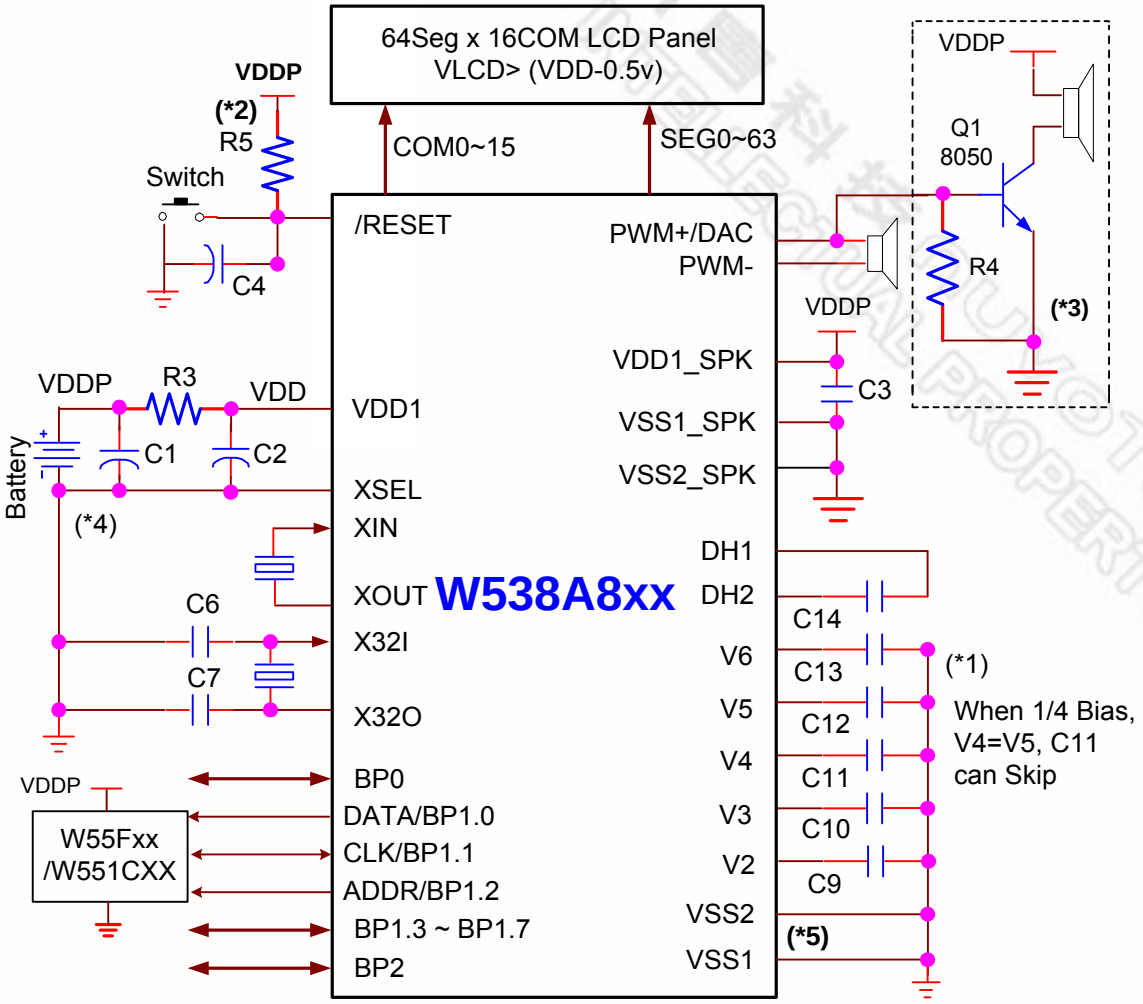
Main clock: Ring type



COMPONENT	C1	C2~C4	C5	C9~C14	R1	R2	R3	R4
Value	4.7uF	0.1uF	100pF	0.1~1uF	300KΩ/4MHz 200KΩ/6MHz 150KΩ/8MHz 120KΩ/10MHz	1.1MΩ	1 ~ 10 Ω	470 ~560Ω

Note:
1. C9~C14 depends on LCD panel dot size.
2. Optional R5 equals 100Ω if high noise immunity is needed.
3. For optional DAC application.
4. Depending on the mask ROM version (e.g., demo, mass production, …), C_5 can be skipped. **If use W538A802 body, C5 is needed.**
5. To be sure chip operation properly, please bond VDD_PWM and VDD together, bond VSS_PWM1, VSS_PWM2 and VSS together; and connect VSS as closely as possible to battery ground.
6. Main clock with Ring type, the frequency deviation depends on VDD and the resistor value

Main clock: Crystal type



COMPONENT	C1	C2 ~ C4	C6, C7	C9~C14	R3	R4
Value	4.7uF	0.1uF	15~ 30pF	0.1~1uF	1 ~ 10 Ω	470 ~560Ω

Note:
1. C9~C14 depends on LCD panel dot size.
2. Optional R5 equals 100Ω if high noise immunity is needed.
3. For optional DAC application.
4 To be sure chip operation properly, please bond VDD1_SPK and VDD together, bond VSS1_SPK, VSS2_SPK and VSS together; and connect VSS as closely as possible to battery ground.

6. REVISION HISTORY

Version	Date	Reasons for Change
A1	Nov 2004	Preliminary release.
A1.1	Dec 2004	Spec correction
A1.2	Apr 2005	LCD COM output from COM0 ~ COM15 Notes description
A2.0	Jul 2005	Spec correction
A2.1	Sep 2005	Modify the features
A2.2	Oct 2005	Remove SCI function
A2.3	Nov 2005	Revise LCD RAM
A3.0	Dec 2005	
A3.1	Mar 2006	Revise LCD COM from COM15 ~ COM0
A3.2	May 2006	Add application circuit Ring type note 4
A4.0	Dec 2007	Modify the new winbond logo.
A5	Jul 2008	Change logo

Important Notice

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