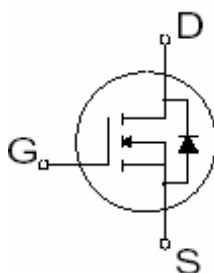


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



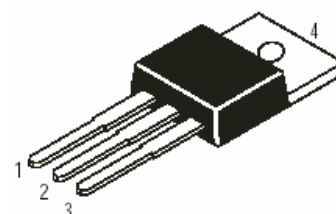
$$V_{DS} = 100V$$

$$I_{D25} = 5.6A$$

$$R_{DS(ON)} = 0.4 \Omega$$

Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate

Pin2-Drain

Pin3-Source

Application

- Switching application

Absolute Maximum Ratings

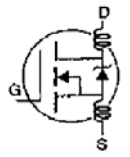
	Parameter	Max.	Units
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS}@10V$	5.6	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS}@10V$	4.0	
I_{DM}	Pulsed Drain Current ①	20	
$P_D@T_C=25^{\circ}C$	Power Dissipation	33	W
	Linear Derating Factor	0.22	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	63	mJ
I_{AR}	Avalanche Current ①	5.6	A
E_{AR}	Repetitive Avalanche Energy ①	3.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	$^{\circ}C$
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	4.51	$^{\circ}C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62.5	

Electrical Characteristics @T_J=25 °C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _(BR) DSS	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _(BR) DSS/ΔT _J	Breakdown Voltage Temp.Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D =250μA
R _{DS(on)}	Static Drain-to-Source On-resistance	—	—	0.4	Ω	V _{GS} =10V, I _D =2.8A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =5V, I _D =250μA
g _{fs}	Forward Transconductance	—	3.49	—	S	V _{DS} =40V, I _D =2.8A
I _{DSS}	Drain-to-Source Leakage current	—	—	10	μA	V _{DS} =100V, V _{GS} =0V
		—	—	100		V _{DS} =80V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	8.5	12	nC	I _D =5.6A
Q _{gs}	Gate-to-Source charge	—	1.6	—		V _{DS} =80V
Q _{gd}	Gate-to-Drain("Miller") charge	—	4.1	—		V _{GS} =10V See Fig.6 and 12④⑤
t _{d(on)}	Turn-on Delay Time	—	10	30	nS	V _{DD} =50V
t _r	Rise Time	—	14	40		I _D =5.6A
t _{d(off)}	Turn-Off Delay Time	—	28	70		R _G =24Ω
t _f	Fall Time	—	18	50		See Figure13④⑤
L _D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm(0.25in.)
L _S	Internal Source Inductance	—	13	—		from package and center of die contact
C _{iss}	Input Capacitance	—	190	240	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	55	65		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	21	25		f=1.0MHz See Figure 5


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.6	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	20		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J =25°C, I _S =5.6A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	85	—	nS	T _J =25°C, I _F =5.6A
Q _{rr}	Reverse Recovery Charge	—	0.23	—	nC	di/dt=100A/μs ④
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Notes:

① Repetitive rating;pulse width limited by max.junction temperature(see figure 11)

② L =3mH, I_{AS} = 5.6 A, V_{DD} = 25V, R_G = 27Ω, Starting T_J = 25°C

③ I_{SD}≤5.6A, di/dt≤250A/μ S, V_{DD}≤V_(BR)DSS, T_J≤25°C

④ Pulse width=250 μ S; duty cycle≤2%