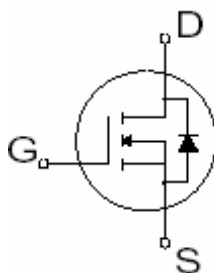


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



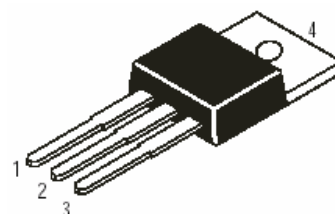
$$V_{DSS} = 650V$$

$$I_{D25} = 7A$$

$$R_{DS(ON)} = 1.3 \Omega$$

Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate
Pin2-Drain
Pin1-Source

Application

- Switching application

Absolute Maximum Ratings

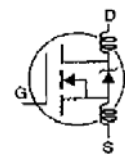
	Parameter	Max.	Units
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS}@10V$	7	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS}@10V$	4.8	
I_{DM}	Pulsed Drain Current ①	30	
$P_D@T_C=25^{\circ}C$	Power Dissipation	175	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	230	mJ
I_{AR}	Avalanche Current ①	7	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	0.9	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @T_J=25 °C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	650	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp.Coefficient	—	0.06	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-resistance	—	1.18	1.3	Ω	V _{GS} =10V, I _D =3.5A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	7.5	8.8	—	S	V _{DS} =40V, I _D =3.5A
I _{DSS}	Drain-to-Source Leakage current	—	—	25	μA	V _{DS} =650V, V _{GS} =0V
		—	—	250		V _{DS} =520V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	—	36	nC	I _D =7A
Q _{gs}	Gate-to-Source charge	—	—	5.5		V _{DS} =520V
Q _{gd}	Gate-to-Drain("Miller") charge	—	—	20		V _{GS} =10V See Fig.6 and 13④
t _{d(on)}	Turn-on Delay Time	—	45	—	nS	V _{DD} =325V
t _r	Rise Time	—	130	—		I _D =3.5A
t _{d(off)}	Turn-Off Delay Time	—	170	—		R _G =25Ω
t _f	Fall Time	—	71	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1250	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	138	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	30		
V _{SD}	Diode Forward Voltage	—	—	1.4	V	T _J =25°C, I _S =7A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	—	250	nS	T _J =25°C, I _F =7A
Q _{rr}	Reverse Recovery Charge	—	3.5	—	nC	di/dt=100A/μs ④
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Notes:

① Repetitive rating;pulse width limited by
max.junction temperature(see figure 11)

② L = 7.3mH, I_{AS} = 7 A, V_{DD} = 50V,
R_G = 25 Ω, Starting T_J = 25°C

③ I_{SD} ≤ 7A, di/dt ≤ 200A/μS, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 25°C

④ Pulse width ≤ 300 μS; duty cycle ≤ 2%