Low Voltage / Low Power CMOS 16-bit Micro-controller

TMP93PS42AF

1. OUTLINE AND DEVICE CHARACTERISTICS

The TMP93PS42A is OTP type MCU which includes 64K byte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP93CS42A by general EPROM programmer.

The TMP93PS42A has the same pin-assignment as the TMP93CS42A (Mask ROM type).

Writing the program to Built-in PROM, the TMP93PS42A operates as the same way as the TMP93CS42A.

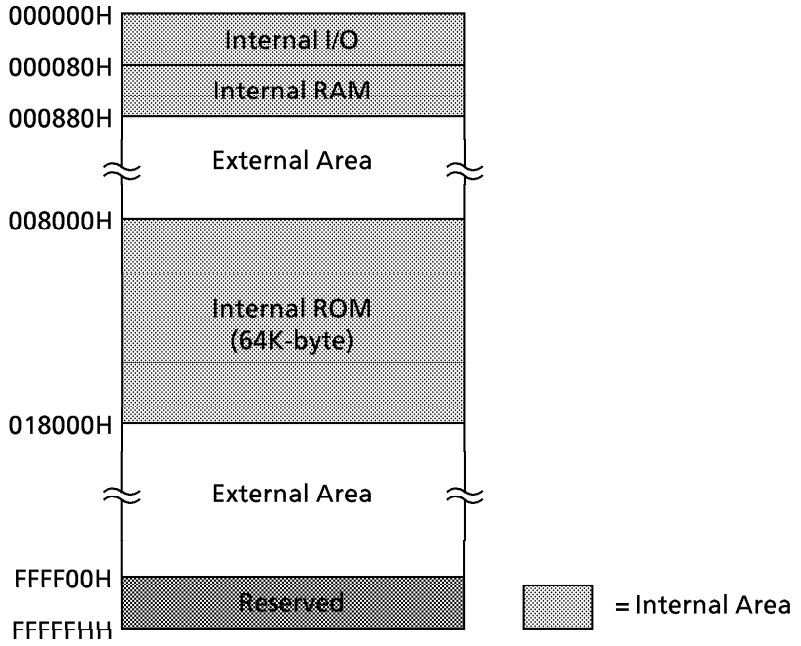


Figure 1.1 Memory map of TMP93PS42A/TMP93CS42A

MCU	ROM	RAM	Package	Adapter Socket
TMP93PS42AF	OTP 64K-byte	2K-byte	QFP100-P-1414-0.50	BM11109

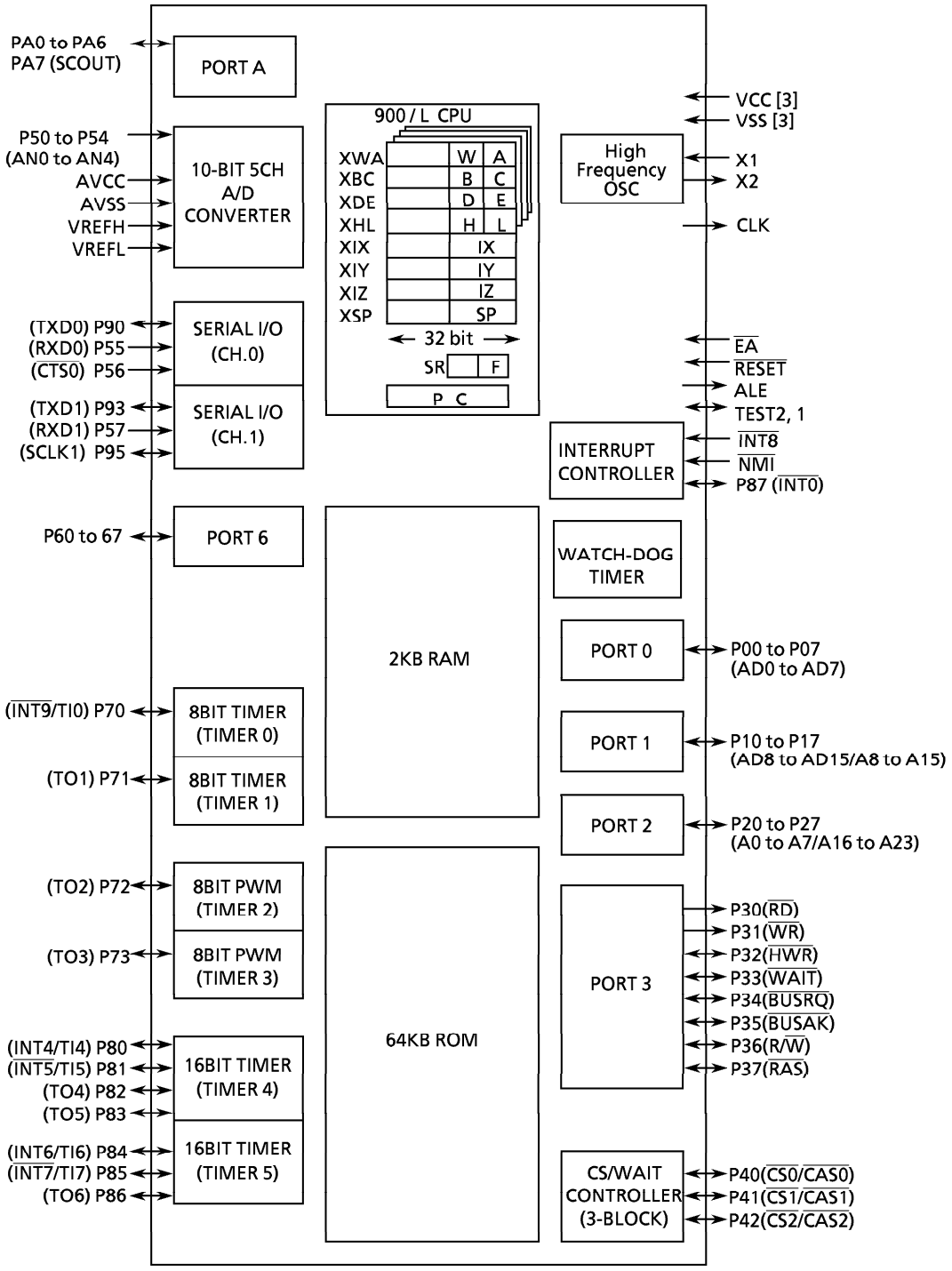


Figure 1.2 TMP93PS42A block diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for the TMP93PS42A their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP93PS42AF.

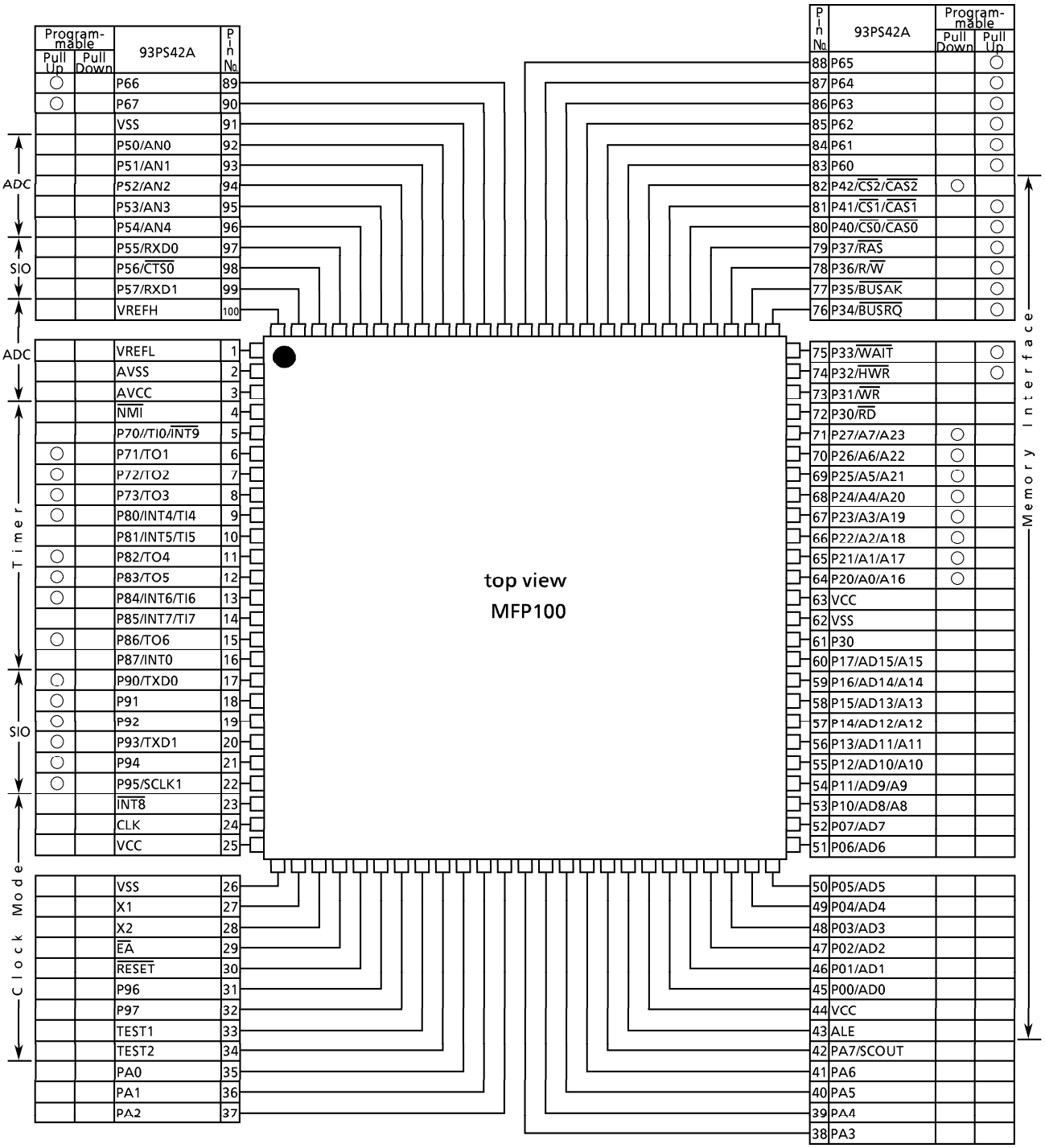


Figure 2.1 Pin Assignment (100-pin MFP)

2.2 Pin Names and Functions

The TMP93PS42A has MCU mode and PROM mode.

(1) Pin function of TMP93PS42A in MCU mode.

Table 2.2 (1) Name and function of in MCU mode

Pin name	Number of pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows selection of I/O on a bit basis Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	2 1	Output Output	Port 30: Output port. 72 pin is also used as $\overline{RD}$, 61 pin is used only for P30. Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Pin used to request bus release
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Pin used to request bus release acknowledge
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note : This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Pin name	Number of pins	I/O	Function
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN4 RXD0 $\overline{CTS0}$ RXD1	8	Input Input Input Input Input	Port 5: Input port Analog input: Analog signal input for A/D converter Serial receive data 0 Serial data send enable 0 (Clear To Send) Serial receive data 1
VREFH	1	Input	Pin for high level reference voltage input to A/D converter
VREFL	1	Input	Pin for low level reference voltage input to A/D converter
P60 to P67	8	I/O	Ports 60 - 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor)
P70 TI0 $\overline{INT9}$	1	I/O Input Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input Interrupt request pin 9: Interrupt request pin with falling edge (TTL level).
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 $\overline{INT5}$	1	I/O Input Input	Port 81: I/O port Timer input 5 : Timer 4 count/capture trigger signal input Interrupt request pin 5 : Interrupt request pin with falling edge (TTL level)
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge

Pin name	Number of pins	I/O	Function
P85 TI7 $\overline{INT7}$	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with falling edge (TTL level)
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 $\overline{INT0}$	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/falling edge (TTL level)
P90 TXD0	1	I/O Input	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91	1	I/O	Port 91: I/O port (with pull-up resistor)
P92	1	I/O	Port 92: I/O port (with pull-up resistor)
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94	1	I/O	Port 94: I/O port (with pull-up resistor)
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
P96	1	I/O	Port 96: I/O port (Open Drain Output)
P97	1	I/O	Port 97: I/O port (Open Drain Output)
PA0 to PA6	7	I/O	Port A0-6: I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System clock output: Outputs f_{FPH} or fSYS clock
$\overline{INT8}$	1	Input	Interrupt request pin 8: Interrupt request pin with falling edge. (TTL level)
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs f_{SYS} clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: "1" should be inputted with TMP93PS42A.
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{RESET}$	1	Input	Reset: Initializes TMP93PS42A. (with pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin (All Vcc pins are connected to the power supply source.)

Pin name	Number of pins	I/O	Function
VSS	3		GND pin (0 V)
AVCC	1		Power supply pin for A/D converter
AVSS	1		GND pin for A/D converter (0 V)

Note : Built-in pull-up / pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

(2) PROM mode

Table 2.2 (2) Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output enable	P30 (72 pin)
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	$\overline{EA}$
VCC	4	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS
Pin function	**Number of pins**	**Input / Output**	**Pin state**	
P34	1	Input	Fix to low level (security pin)	
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Self oscillation with a resonator	
X2	1	Output		
P42 to P40 P37 to P35 $\overline{INT8}$	7	Input	Fix to high level	
TEST1 / TEST2	2	Input / Output	Short	
P57 to P50 P67 to P60 P73 toP70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ P30 (61 pin)	48	I/O	Open	

3. OPERATION

This section describes the functions and basic operational blocks of the TMP93PS42A.

The TMP93PS42A has PROM in place of the mask ROM which is included in the TMP93CS42A. The other configuration and functions are the same as the TMP93CS42A. Regarding the function of the TMP93PS42A, which is not described herein, see the part of TMP93CS42A.

The TMP93PS42A has two operational modes: MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by releasing the CLK pin (pin open). In the MCU mode, the operation is the same as TMP93CS42A.

3.2 Memory Map

Figure 3.1 (1), (2) are the memory map of the TMP93PS42A.

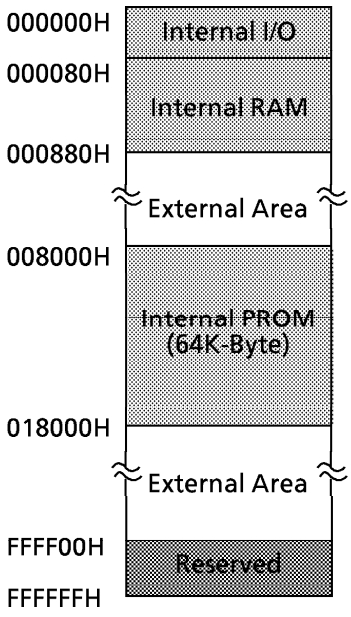


Figure 3.1 (1) Memory map in MCU mode

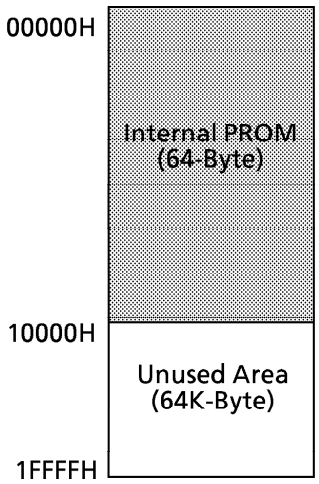


Figure 3.1 (2) Memory map in PROM mode

Figure 3.2 Memory map

3.3 PROM Mode

(1) Mode setting and programming

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

① OTP adaptor

BM11109 : TMP93PS40F adaptor

② Setting OTP adaptor

Set the switch (SW1) to N side.

③ Setting PROM programmer

i) Set PROM type to TC571000D.

Size : 1M bit (128K×8bit)
VPP : 12.75V
tpw : 100 μs

The electric signature mode (hereinafter referred to as "signature".) is not supported. Therefore if signature is used, the device is damaged because 12.75V is applied to A9 of address. Do not use signature.

ii) Transferring the data (copy)

In TMP93PS42A, PROM is placed on addresses 00000 to 0FFFFH in PROM mode, and addresses 08000H to 17FFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 0FFFFH in PROM mode using the object converter(tuconv) or the block transfer mode (see instruction manual of PROM programmer.)

iii) Setting the programming address

Start address : 00000H
End address : 0FFFFH

When the PROM programmer can not set the programming address, set the data of addresses 10000H to 1FFFFH to FFH.

④ Programming

Program/verify according to the procedures of PROM programmer.

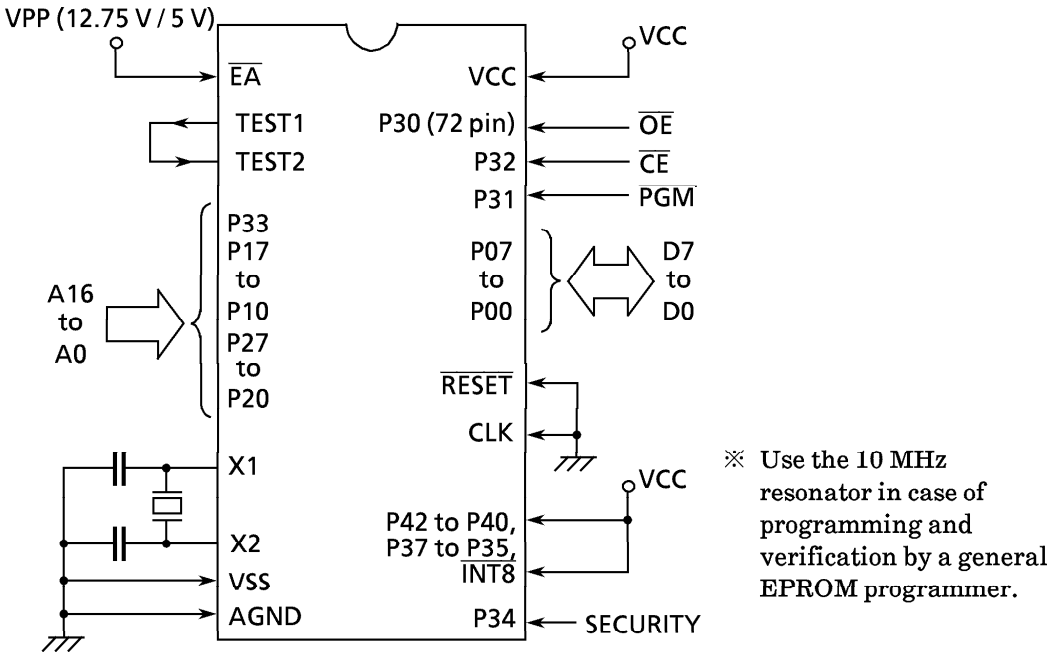


Figure 3.3 (1) PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows,
(VCC : 6.25 V, $\overline{\text{RESET}}$: "L" level, CLK : "L" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of Vpp = Vcc = 5 V after all data were written.

Figure 3.2 (2) shows the programming flow chart.

High Speed Program Writing.

Flow chart

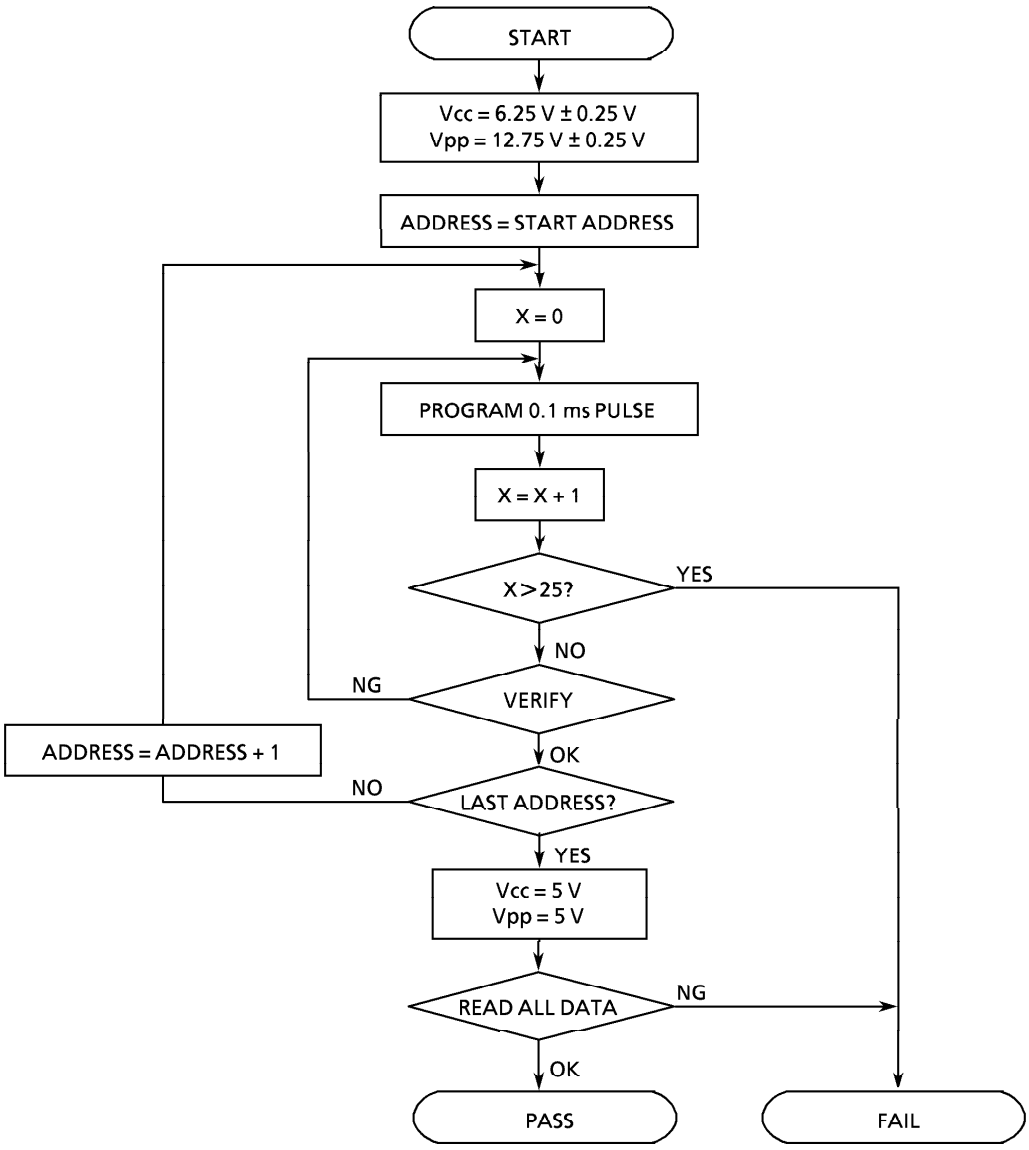


Figure 3.3 (2) Flow chart

(3) Security Bit

The TMP93PS42A has a Security Bit. If the Security Bit is programmed to "0", the content of the PROM is disable to be read in PROM mode.(outputs data FFH)

(How to program the Security Bit)

The differences from the programming procedures described in section 3.3 (1) are follows.

② Setting OTP adapter
Set the switch(SW1) to S side.

③ Setting PROM programmer
ii) Transferring the data
iii) Setting the programming address
The security bit is in bit 0 of address 00000H.
Set the start address 00000H and the end address 00000H.
Set the data FEH at the address 00000H.

4. ELECTRICAL CHARACTERISTIC

"X" used in an expression shows a frequency of clock f_{PPH} selected by SYSCR1<SYSCK>. If a clock gear is selected, a value of "X" is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR2-0> = "000")

4.1 Absolute Maximum Ratings (TMP93PS42AF)

Symbol	Parameter	Rating	Unit
V cc	Power Supply Voltage	– 0.5 to 6.5	V
V IN	Input Voltage	– 0.5 to Vcc + 0.5	V
Σ IOL	Output Current (total)	120	mA
Σ IOH	Output Current (total)	– 80	mA
P D	Power Dissipation (Ta = 85 ℃)	600	mW
T SOLDER	Soldering Temperature (10 s)	260	℃
T STG	Storage Temperature	– 65 to 150	℃
T OPR	Operating Temperature	– 40 to 85	℃

4.2 DC Characteristics (1/2)

Symbol	Parameter		Min.	Typ. (note1)	Max.	Unit	Condition
V CC	Power Supply Voltage (AVcc = Vcc, AVss = Vss)		4.5		5.5	V	fc = 4 to 20 MHz
V IL	Input Low Voltage	AD0 to 15	–0.3		0.8	V	V_{CC} = 5 V ± 10 %
V IL1		Port2 to A (except P87, P5)			0.3Vcc		
V IL2		RESET,NMI			0.25Vcc		
V IL3		EA			0.3		
V IL4		X1			0.2Vcc		
V IL5		INT0,INT5,INT7, INT8, INT9			0.8		
V IH	Input High Voltage	AD0 to 15	2.2		Vcc + 0.3		V_{CC} = 5 V ± 10 %
V IH1		Port2 to A (except P87)	0.7Vcc				
V IH2		RESET, NMI	0.75Vcc				
V IH3		EA	Vcc – 0.3				
V IH4		X1	0.8Vcc				
V IH5		INT0,INT5,INT7, INT8, INT9	2.8				
V OL	Output Low Voltage				0.45	V	I OL = 1.6 mA (V_{CC} = 5 V ± 10 %)
V OH	Output High Voltage		4.2				I OH = – 400 μA (V_{CC} = 5 V ± 10 %)

Note 1 : Typical values are for Ta = 25 °C and VCC = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min.	Typ. (note1)	Max.	Unit	Condition
I DAR (note2)	Darlington Drive Current (8 Output Pins max.)	−1.0		−3.5	mA	V EXT = 1.5 V R EXT = 1.1 kΩ Vcc = 5 V ± 10 %
I LI	Input Leakage Current		0.02	±5	μA	0.0 ≦ V_{IN} ≦ V_{CC}
I LO	Output Leakage Current		0.05	±10		0.2 ≦ V_{IN} ≦ V_{CC} − 0.2
V STOP	Power Down Voltage (at STOP, RAM Back up)	2.0		6.0	V	V IL2 = 0.2Vcc, V IH2 = 0.8Vcc
R RST	$\overline{\text{RESET}}$ Pull Up Resister	50		150	kΩ	Vcc = 5 V ± 10 %
C IO	Pin Capacitance			10	pF	fc = 1 MHz
V TH	Schmitt Width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$	0.4	1.0		V	
RKL	Programmable Pull Down Resistor	10		80	kΩ	Vcc = 5 V ± 10 %
RKH	Programmable Pull Up Resistor	50		150		Vcc = 5 V ± 10 %
I cc	NORMAL (note 3)		19	25	mA	Vcc = 5 V ± 10 % fc = 20 MHz
	NORMAL2 (note 4)		24	30		
	RUN		17	25		
	IDLE2		12	17		
	IDLE1		3.5	5		
	STOP		0.2	10	μA	Vcc = 5 V ± 10 %

(note 1) Typical values are for Ta = 25 °C and VCC = 5 V unless otherwise noted.
(note 2) I-DAR is guranteed for total of up to 8 ports.
(note 3) The condition of measurement of Icc NORMAL.
Only CPU operates. Output ports are open and input ports fixed.
(note 4) The condition of measurement of Icc NORMAL2.
CPU and all peripherals operate. Output ports are open and input ports fixed.

4.3 AC Characteristics

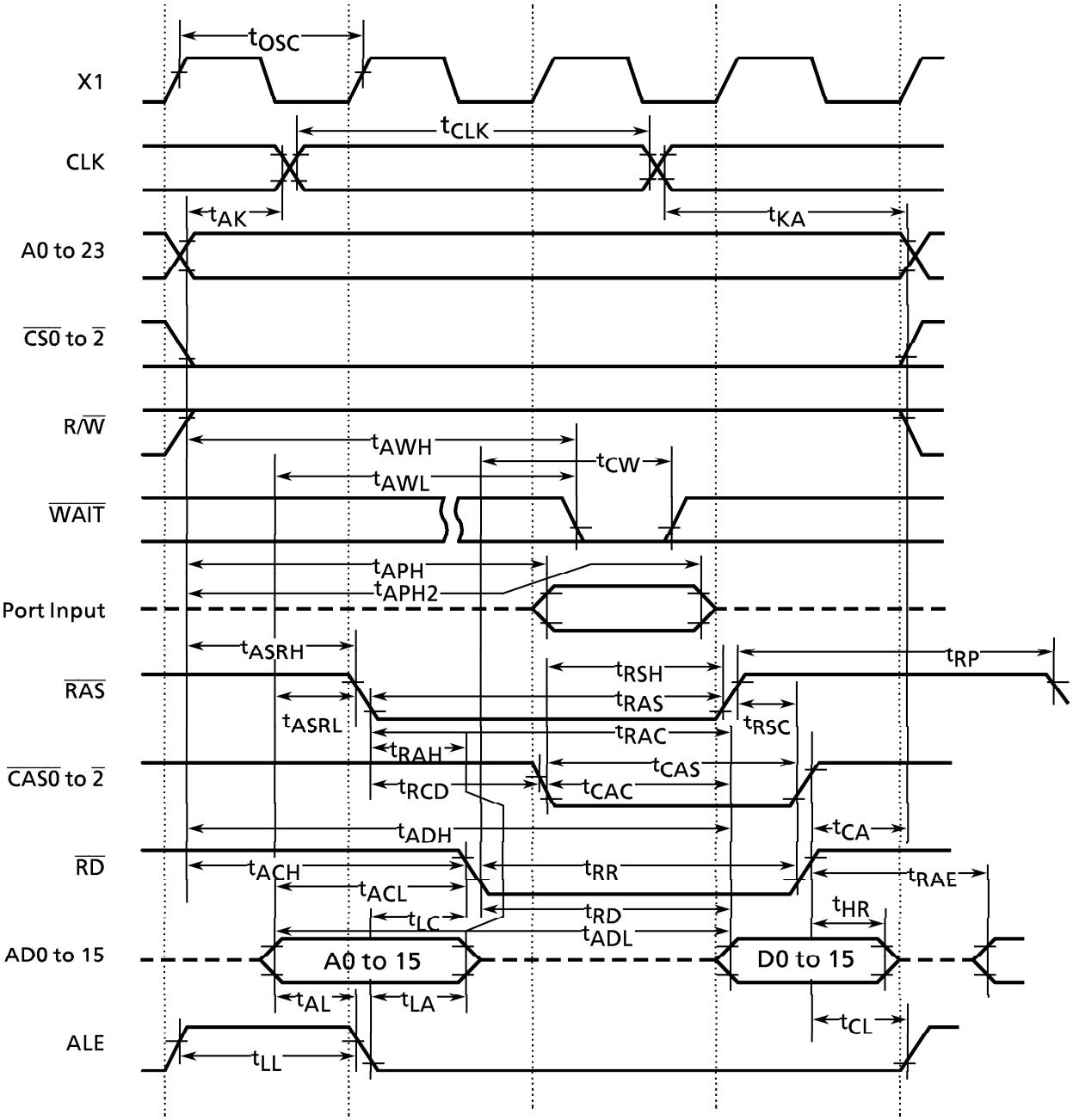
(1) Vcc = 5 V ± 10 %

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	250	62.5		50		ns
2	t_{CLK}	CLK width	2x – 40		85		60		ns
3	t_{AK}	A0-23 Valid→ CLK Hold	0.5x – 20		11		5		ns
4	t_{KA}	CLK Valid→ A0-23 Hold	1.5x – 70		24		5		ns
5	t_{AL}	A0-15 Valid→ ALE fall	0.5x – 15		16		10		ns
6	t_{LA}	ALE fall→ A0-15 Hold	0.5x – 20		11		5		ns
7	t_{LL}	ALE High width	x – 40		23		10		ns
8	t_{LC}	ALE fall→ $\overline{RD}/\overline{WR}$ fall	0.5x – 25		6		0		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ rise→ ALE rise	0.5x – 20		11		5		ns
10	t_{ACL}	A0-15 Valid→ $\overline{RD}/\overline{WR}$ fall	x – 25		38		25		ns
11	t_{ACH}	A0-23 Valid→ $\overline{RD}/\overline{WR}$ fall	1.5x – 50		44		25		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ rise→ A0-23 Hold	0.5x – 25		6		0		ns
13	t_{ADL}	A0-15 Valid→ D0-15 input		3.0x – 55		133		95	ns
14	t_{ADH}	A0-23 Valid→ D0-15 input		3.5x – 65		154		110	ns
15	t_{RD}	$\overline{RD}$fall →D0-15 input		2.0x – 60		65		40	ns
16	t_{RR}	$\overline{RD}$ Low pulse width	2.0x – 40		85		60		ns
17	t_{HR}	$\overline{RD}$rise→ D0-15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$rise→ A0-15output	x – 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low pulse width	2.0x – 40		85		60		ns
20	t_{DW}	D0-15 Valid→ $\overline{WR}$ rise	2.0x – 55		70		45		ns
21	t_{WD}	$\overline{WR}$ rise →D0-15 Hold	0.5x – 15		16		10		ns
22	t_{AWH}	A0-23 Valid→ $\overline{WAIT}$ input (2 WAIT +n mode)		5.5x – 90		254		185	ns
23	t_{AWL}	A0-15 Valid→ $\overline{WAIT}$ input (2 WAIT +n mode)		5.0x – 80		223		170	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold (2 WAIT +n mode)	4.0x + 0		250		200		ns
25	t_{APH}	A0-23 Valid→ PORT input		2.5x – 120		36		5	ns
26	t_{APH2}	A0-23 Valid→ PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ rise→ PORT Valid		200		200		200	ns
28	t_{ASRH}	A0-23 Valid→ $\overline{RAS}$ fall	1.0x – 40		23		10		ns
29	t_{ASRL}	A0-15 Valid→ $\overline{RAS}$ fall	0.5x – 15		16		10		ns
30	t_{RAC}	$\overline{RAS}$ fall→ D0-15 input		2.5x – 70		86		55	ns
31	t_{RAH}	$\overline{RAS}$ fall→ A0-15 Hold	0.5x – 15		16		10		ns
32	t_{RAS}	$\overline{RAS}$ Low pulse width	2.0x – 40		85		60		ns
33	t_{RP}	$\overline{RAS}$ High pulse width	2.0x – 40		85		60		ns
34	t_{RSH}	$\overline{CAS}$ fall→ $\overline{RAS}$ rise	1.0x – 40		23		10		ns
35	t_{RSC}	$\overline{RAS}$ rise→ $\overline{CAS}$ rise	0.5x – 25		6		0		ns
36	t_{RCD}	$\overline{RAS}$ fall→ $\overline{CAS}$ fall	1.0x – 40		23		10		ns
37	t_{CAC}	$\overline{CAS}$ fall→ D0-15 input		1.5x – 65		29		10	ns
38	t_{CAS}	$\overline{CAS}$ Low pulse width	1.5x – 30		64		40		ns

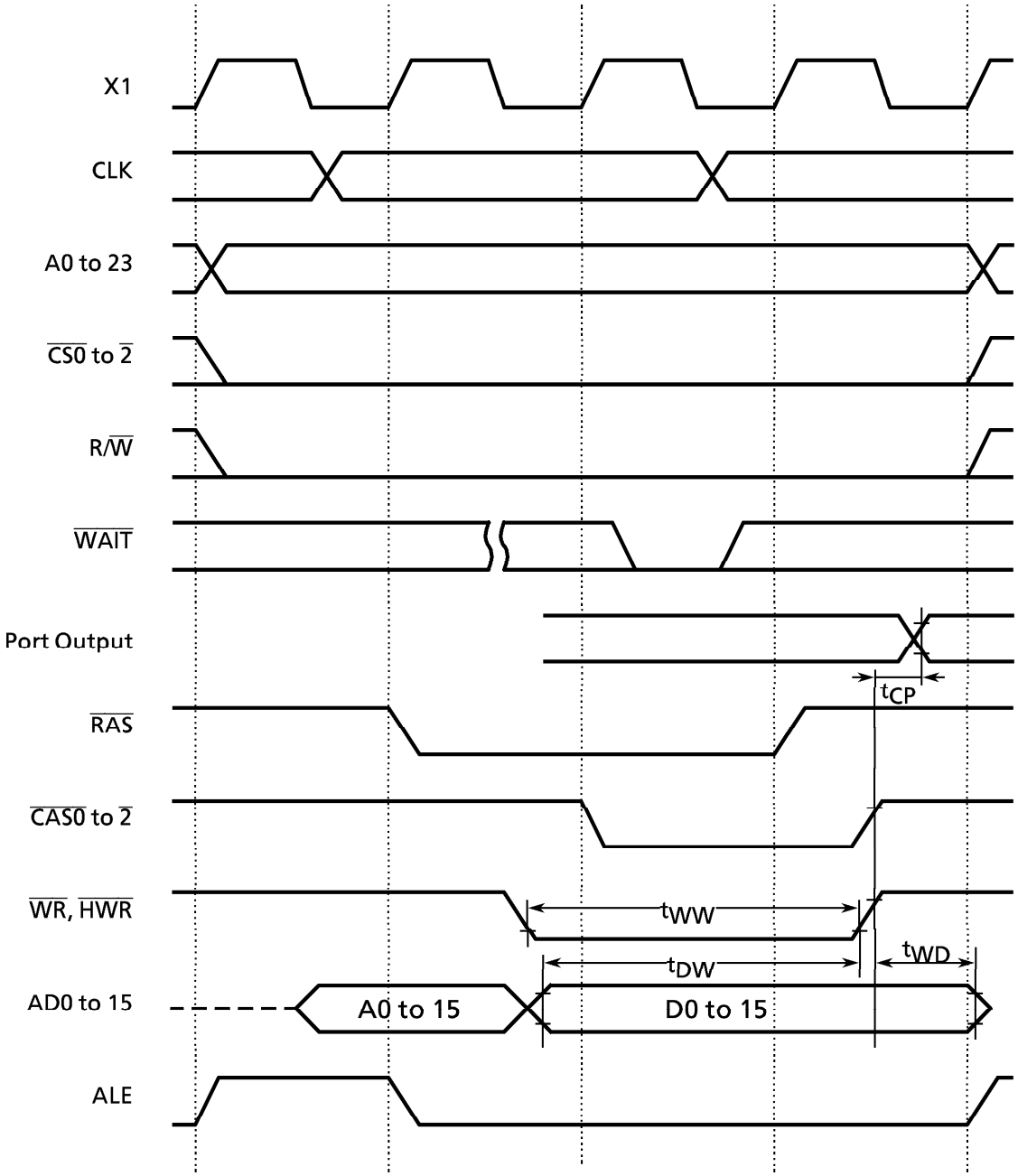
AC Measuring Conditions

- Output Level : High 2.2 V /Low 0.8 V , CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V /Low 0.45 V (AD0~AD15)
  High 0.8Vcc /Low 0.2Vcc (Except for AD0 to AD15)

(1) Read Cycle


X1
CLK
A0 to 23
CS0 to 2
R/W
WAIT
Port Input
RAS
CAS0 to 2
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tASRH
tASRL
tRSH
tRAS
tRAC
tRAH
tRCD
tCAS
tCAC
tRSC
tRP
tADH
tCA
tACH
tACL
tLC
tRR
tRD
tADL
tRAE
tHR
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(2) Write Cycle



4.4 A/D Conversion Characteristics

Symbol	Parameter	Power Supply	Min	Typ	Max	
VREFH	Analog reference voltage (+)	V_{CC} = 5V ± 10 %	V_{CC} – 1.5V	V_{CC}	V_{CC}	V
VREFL	Analog reference voltage (–)		V_{SS}	V_{SS}	V_{SS} + 0.2V	
V_{AIN}	Analog input voltage range		VREFL		VREFH	
I_{REF} (V_{REFL} = 0 V)	Analog current for analog reference voltage <VREFON> = 1			0.5	1.5	mA
	<VREFON> = 0			0.02	5.0	μA
–	Error			± 1.0	± 3.0	LSB

Note 1 : 1LSB = (VREFH – VREFL) / 2^{10} [V]
Note 2 : The operation above is guaranteed with $f_{FPH} \geqq 4$ MHz.
Note 3 : The value I_{CC} includes the current which flows through AV_{CC} pin.

4.5 Serial Channel Timing (I/O Interface Mode)

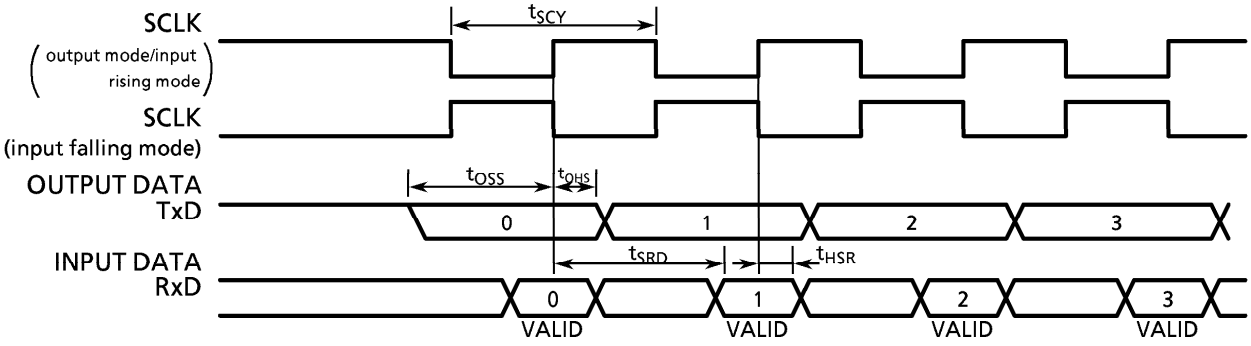
① SCLK Input Mode

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16x		1.28		0.8		μs
t_{OSS}	Output Data → Rising edge of SCLK*	t_{SCY}/2 – 5x – 50		190		100		ns
t_{OHS}	SCLK rising edge* → Output Data hold	5x – 100		300		150		ns
t_{HSR}	SCLK rising edge* → Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge* → effective data input		t_{SCY} – 5x – 100		780		450	ns

*) SCLK rising/falling ··· SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16x	8192x	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data → SCLK rising edge	t_{SCY} – 2x – 150		970		550		ns
t_{OHS}	SCLK rising edge → Output Data hold	2x – 80		80		20		ns
t_{HSR}	SCLK rising edge → Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge → effective data input		t_{SCY} – 2x – 150		970		550	ns



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	8X + 100		740		500		ns
t_{VCKL}	Low level clock Pulse width	4X + 40		360		240		ns
t_{VCKH}	High level clock Pulse width	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, $\overline{INT0}$ interrupt

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, $\overline{INT0}$ Low level Pulse width	4X		320		200		ns
t_{INTAH}	$\overline{NMI}$, $\overline{INT0}$ High level Pulse width	4X		320		200		ns

(2) INT4 to 9 interrupt, capture

Input pulse width of INT4 to 9 depends on the operation clock of CPU and Timer (9 bit prescaler). The following shows the pulse width in each clock.

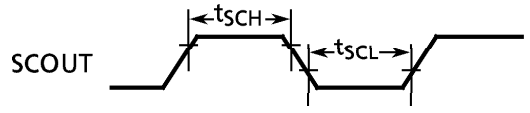
Prescaler clock selection <PRCK1, 0>	t_{INTBL} (INT4 to 9 Low level Pulse width)		t_{INTBH} (INT4 to 9 High level Pulse width)		Unit
	Variable	20 MHz	Variable	20 MHz	
	Min	Min	Min	Min	
00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
10(fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	μs

4.8 SCOUT pin AC characteristics m

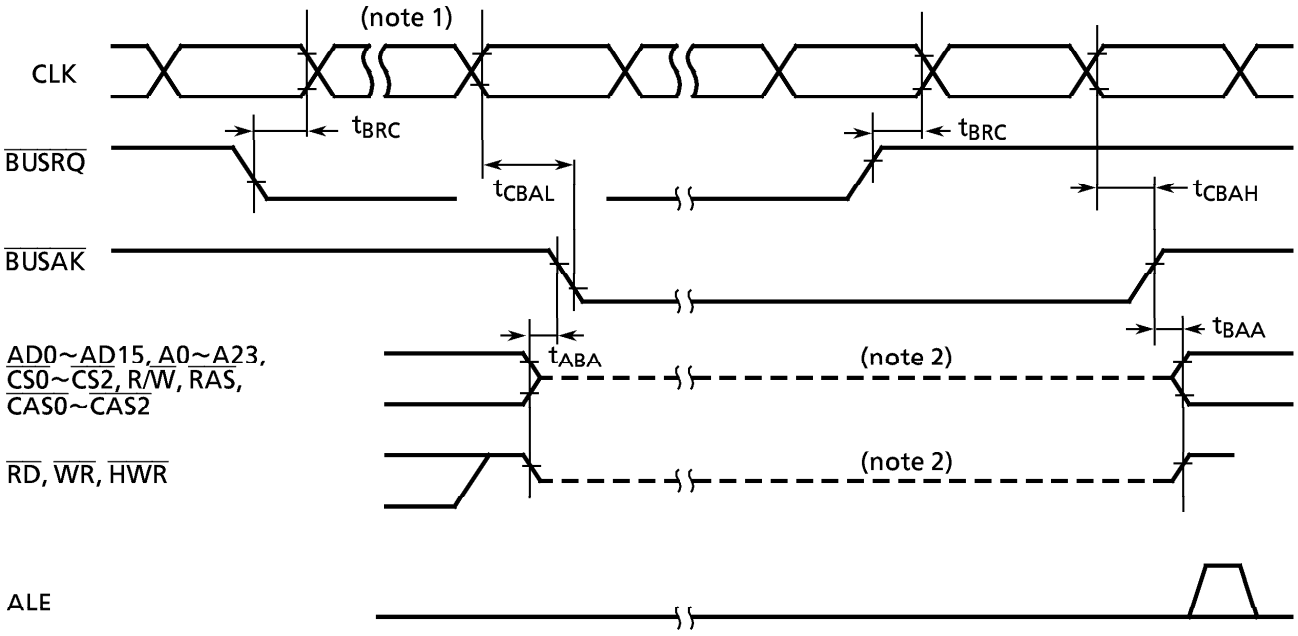
Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCH}	High-level pulse width VCC = 5V ± 10 %	0.5X–10		30		15		ns
t_{SCL}	Low-level pulse width VCC = 5V ± 10 %	0.5X–10		30		15		ns

Measurement condition

- Output level : High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request/Bus Acknowledge



Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{BRC}	$\overline{BUSRQ}$ set-up time to CLK	120		120		120		ns
t_{CBAL}	CLK→ $\overline{BUSAK}$ falling edge		1.5x + 120		240		195	ns
t_{CBAH}	CLK→ $\overline{BUSAK}$ rising edge		0.5x + 40		80		65	ns
t_{ABA}	Output Buffer is off to $\overline{BUSAK}$ ↓	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ ↑ to Output Buffer is on.	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.
It doesn't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.
The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

4.10 Read operation in PROM mode

DC / AC characteristics

TA = 25 ± 5 °C Vcc = 5 V ± 10 %

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.2	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3	0.8	V
t_{ACC}	Address to Output Delay	C_L = 50 pF	–	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

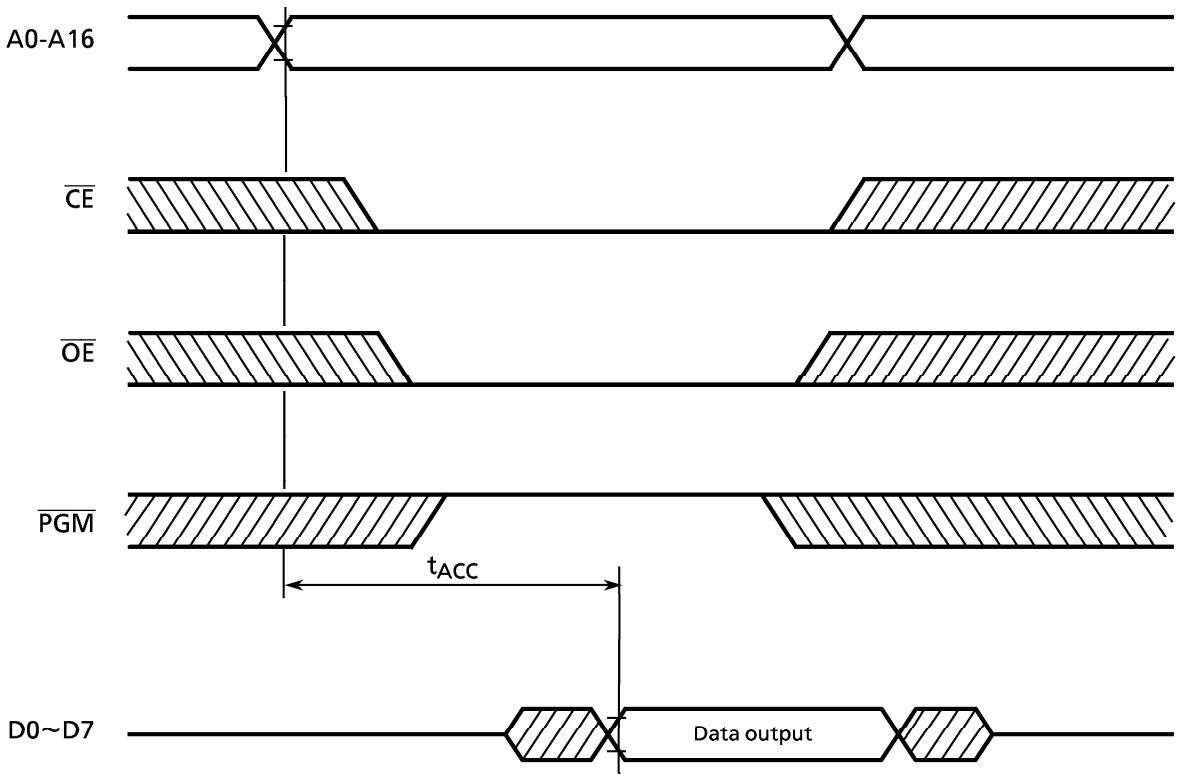
4.11 Program operation in PROM mode

DC / AC characteristics

TA = 25 ± 5 °C Vcc = 6.25 V ± 0.25 V

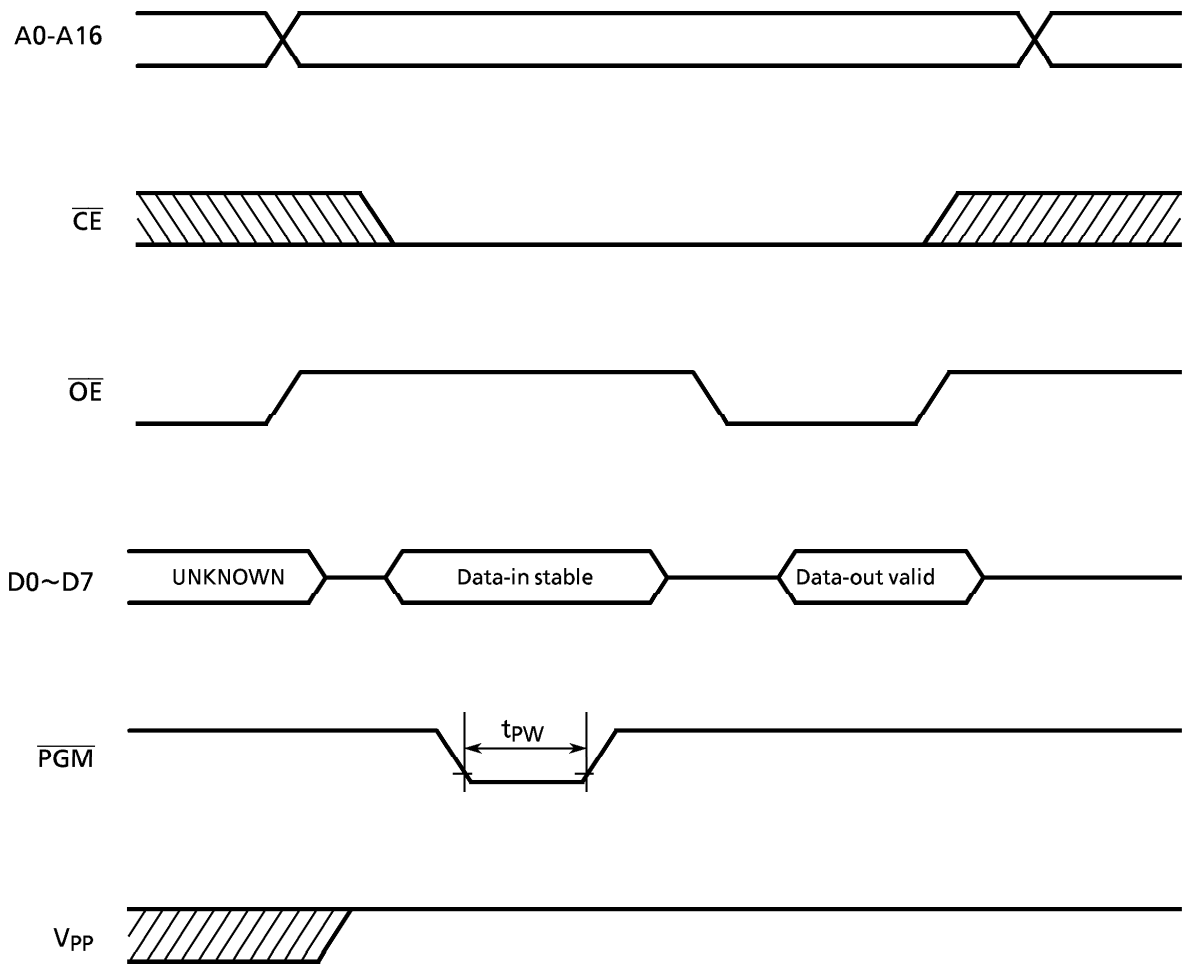
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programing Supply Voltage	–	12.50	12.75	13.00	V
V_{IH}	Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.6		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3		0.8	V
I_{CC}	V_{CC} Supply Current	fc = 10 MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00 V	–		50	mA
t_{PW}	$\overline{PGM}$ Program Pulse Width	C_L = 50 pF	0.095	0.1	0.105	ms

4.12 Timing chart of read operation in PROM mode



4.13 Timing chart of program operation in PROM mode

High-Speed Programing formula



NOTE

1. The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.
2. The pulling up/down device on condition of V_{PP} = 12.75 V suffers a damage for the device.
3. The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the programming.