

Descriptions

The S1117 series of positive adjustable and fixed regulators are designed to provide 1A with high efficiency. All internal circuitry is designed to operate down to 1.3V input to output differential. On-chip trimming adjusts reference voltage to 2%.

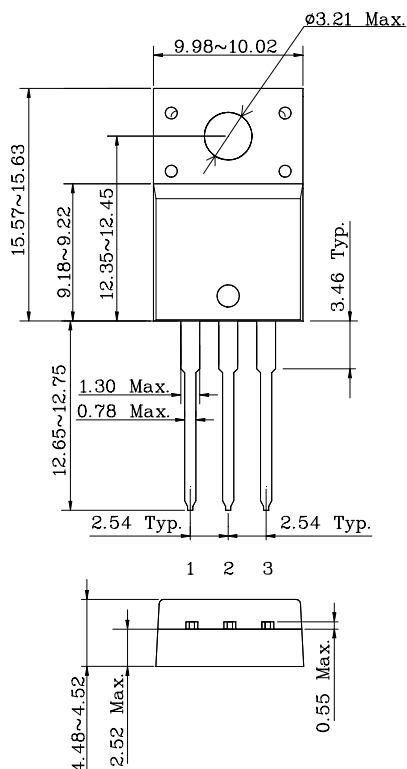
Features

- Adjustable or Fixed output
- Output Current of 1A
- Low Dropout, 1.3V maximum at 1A Output Current
- Thermal Shutdown Protection
- Fast Transient Response

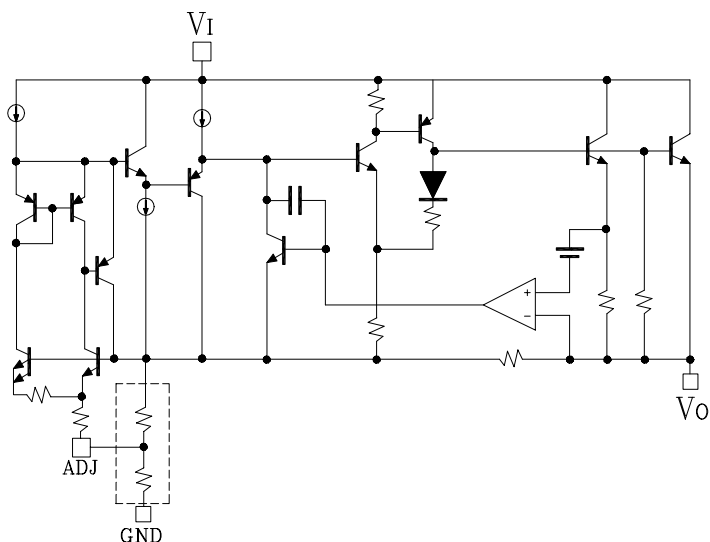
Ordering Information

Type NO.	Marking	Package Code
S1117API/S1117xxPI	S1117□□PI/ S1117□□□PI	TO-220F
□□:Voltage Code (Aj : 1.25V, 15:1.5V,:18: 1.8V, 25:2.5V, 33:3.3V, 50:5.0V)		
□□□:Voltage Code (285:2.85V)		

Outline Dimensions (Unit : mm)



BLOCK DIAGRAM



PIN Connections

1. GND/Adj
2. Output voltage
3. Input voltage

Absolute Maximum Ratings**T_a=25°C**

Characteristic	Symbol	Rating	Unit
Input voltage	V _I	16	V
Power Dissipation	P _D	2.0	W
Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{stg}	-55 ~ 150	°C

Device Selection Guide (NOTE1)

Device	Output Voltage
S1117API	Adjustable
S1117-15PI	1.5V
S1117-18PI	1.8V
S1117-25PI	2.5V
S1117-285PI	2.85V
S1117-33PI	3.3V
S1117-50PI	5.0V

Note 1 : Other fixed versions are available V_O=1.5V to 5V

Electrical Characteristics

(Electrical Characteristics at $T_J = 25^\circ\text{C}$ and $V_I = (V_O + 1.5\text{V})$, $I_L = 10\text{ mA}$, $C_O = 10\text{ }\mu\text{F}$ unless otherwise specified.)

Characteristic	Symbol	Device	Test Condition		Min	Typ	Max	Unit
Output Voltage	V_O	S1117A	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		1.225	1.25	1.275	V
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	1.200		1.300	
		S1117-15	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		1.470	1.5	1.530	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	1.440		1.560	
		S1117-18	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		1.764	1.8	1.836	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	1.728		1.872	
		S1117-25	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		2.450	2.5	2.550	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	2.400		2.600	
		S1117-285	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		2.793	2.85	2.907	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	2.736		2.964	
		S1117-33	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		3.234	3.3	3.366	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	3.168		3.432	
		S1117-50	$V_I = (V_O + 1.5\text{V}), I_O = 10\text{ mA}$		4.900	5.0	5.100	
			$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 0$ to 1000 mA	*	4.800		5.200	
Line Regulation (Note2)	$\Delta V_{O(\Delta V_I)}$	All	$1.5\text{V} \leq V_I - V_O \leq 7\text{V}$ $I_O = 10\text{ mA}$		-	5	10	mV
Load Regulation (Note2)	$\Delta V_{O(\Delta I_L)}$	All	$V_I = (V_O + 1.5\text{V})$ $I_O = 10\text{ mA} \sim 1000\text{ mA}$		-	10	30	mV
Quiescent Current	I_{QC}	All	$V_I = V_O + 1.5\text{V}$ $V_{ADJ} = 0\text{V}$	*	-	7	13	mA
Minimum Load Current	$I_{L(MIN)}$	S1117A	$V_I = (V_O + 1.5\text{V}), V_O = 0\text{V}$	*		3	7	mA
Adjust Pin Current	I_{ADJ}	S1117A	$V_I = (V_O + 1.5\text{V})$ to 7V $I_O = 10\text{ mA}$	*		55	90	μA
Dropout Voltage (Note4)	V_{DROP}	All	$I_O = 1000\text{ mA}$	*	-	1.2	1.3	V
Ripple Rejection (Note3)	RR	All	$V_I - V_O = 1.5\text{V}, I_O = 1000\text{ mA}$ $V_{Ripple} = 1\text{V}_{P-P}, f = 120\text{ Hz}$		60	72	-	dB
Current Limit	I_{LIMIT}	All	$(V_I - V_O) = 1.5\text{V}$	*	1			A

The * denotes the specifications which apply over the full temperature range.

Note 2: Low duty pulse testing with Kelvin connections required.

Note 3: 120 Hz input ripple (C_{ADJ} for ADJ=25 μF)

Note 4: $\Delta V_O = 1\%$

■ Typical Applications

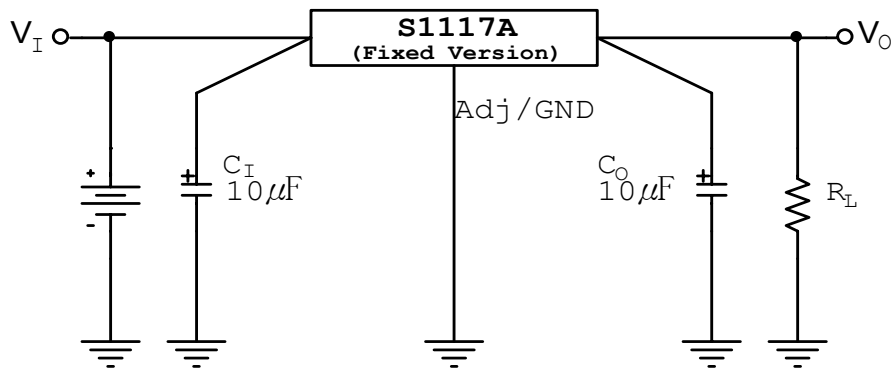
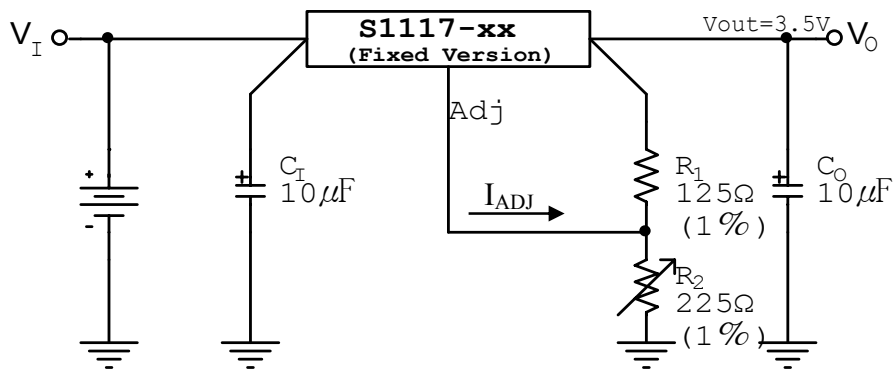


Fig. 1 Fixed Voltage Regulator



$$V_O = V_{ADJ} * (1 + R_2/R_1) + I_{ADJ} * R_2$$

Fig. 2 Adjustable Voltage Regulator

Notes:

- 1) C_I needed if device is far from filter capacitors
- 2) C_O minimum value required for stability

Electrical Characteristic Curves

Fig. 3 V_{DROP} vs. I_O

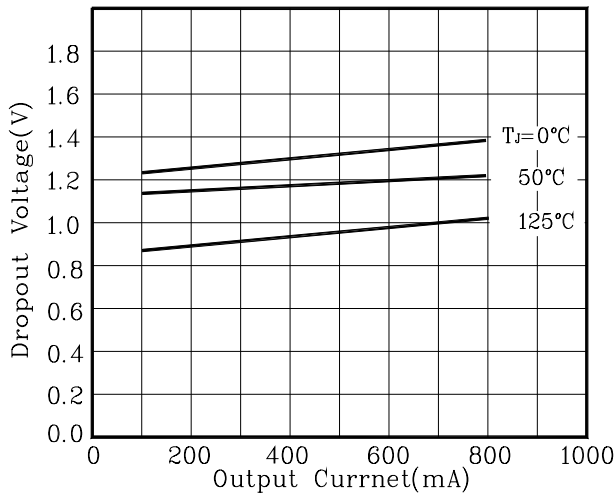


Fig. 4 ΔV_O vs. T_a

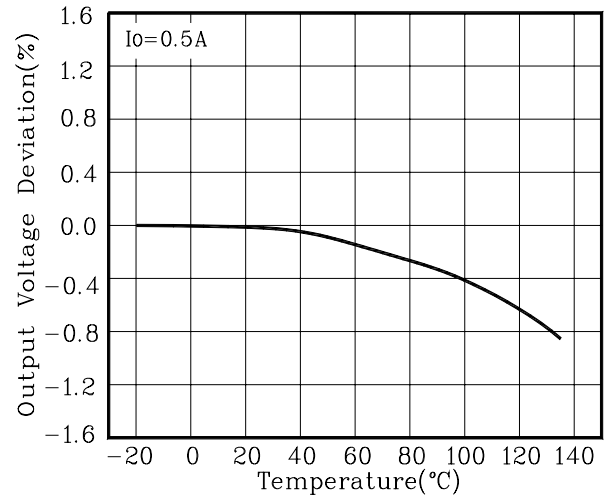


Fig. 5 RR vs. Frequency

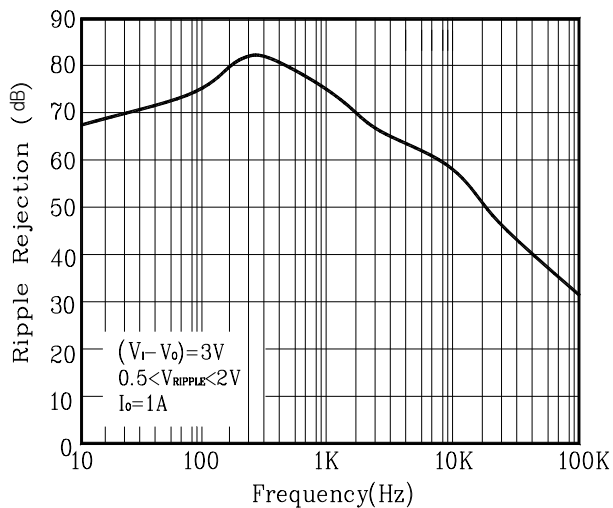


Fig. 6 Temperature Stability

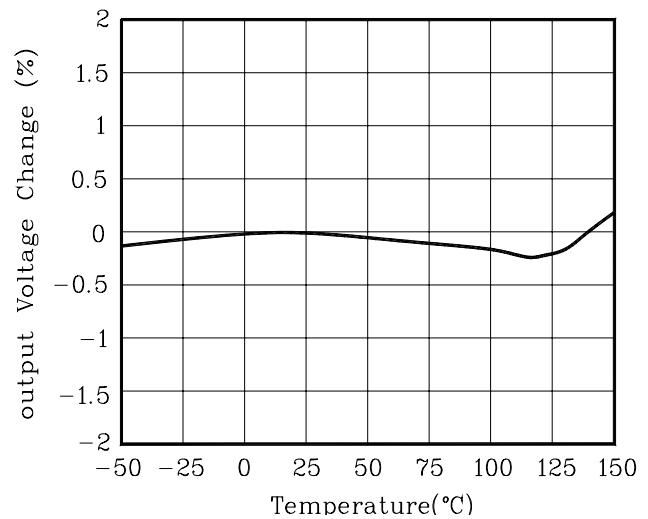


Fig. 7 I_{ADJ} vs. T_a

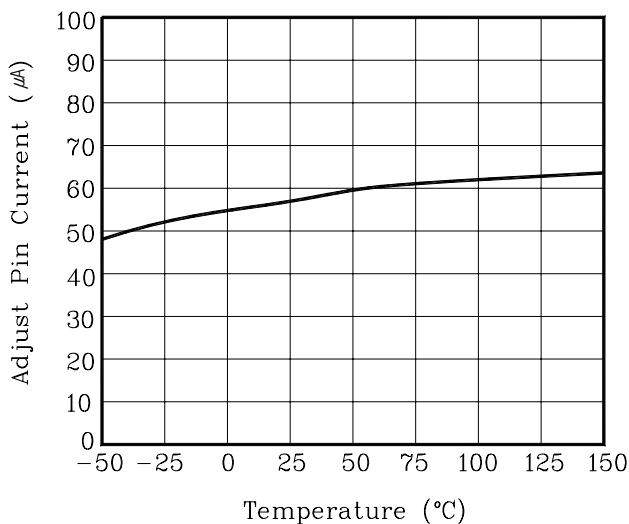
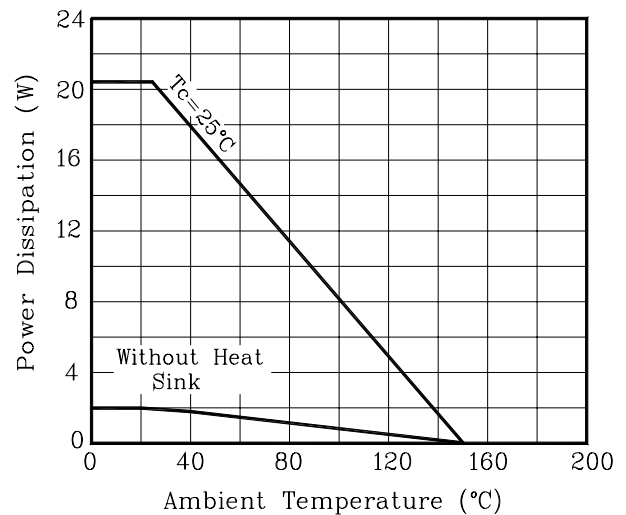


Fig. 8 P_D vs. T_a



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