Preliminary

Ver.: 0.24

TFT LCD Specification

Model Name: TD016THEB2

Customer Signature
Date

This technical specification is subjected to change without notice.

1. FEATURES

The 1.6”(4.06cm) LCD module is an active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used. Vertical drivers are built on the panel.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size (Diagonal)	1.6 (4.06)	Inch (cm)
Display Type	Trans-mission	
Active Area (HxV)	28.608 x 28.608	mm
Number of Dots (HxV)	128 x RGB x 128	dot
Dot Pitch (HxV)	0.0745 x 0.2235	mm
Color Arrangement	RGB Stripe	
Color Numbers	65 K / 262 K	
Outline Dimension (HxVxT) *	34.8 x 41.64 x 3.2	mm
Weight	5.6 +/- 0.5	g

* Exclude protrusions.

3. INPUT/OUTPUT TERMINALS(USE i80 System)

:

Pin No	Symbol	I/O	Description	Remark
1	VSS	-	Ground	
2	ID		PULL LOW	
3	D0	I	Data0	
4	/RESET	I	RESET	
5	D1	I	Data1	
6	/RD	I	Read (Enable)	
7	D2	I	Data2	
8	/WR	I	Write (Write/Read)	
9	D3	I	Data3	
10	NC	--	NC	
11	D4	I	Data4	
12	LED+	I	LED (Anode)	
13	D5	I	Data5	
14	LED-	I	LED (Cathode)	
15	D6	I	Data6	
16	NC	--	NC	
17	D7	I	Data7	
18	VCC(+2.8V)	I	System Power Supply	
19	/CS	I	Chip Select	
20	VCC(+2.8V)	I	System Power Supply	
21	RS	I	Command (L)/Data (H)	
22	VSS	-	Ground	

4. ABSOLUTE MAXIMUM RATINGS

VSS=0V

Item	Symbol	Min	MAX	Unit	Remark
Input voltage	VI	--	+4.6	V	
Back Light Forward Current	I_F	-	--	mA	
Operating temperature	Topr	-20	+70	℃	
Storage temperature	Tstg	-30	+80	℃	

5. ELECTRICAL CHARACTERISTICS

5.1. Driving TFT LCD Panel

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		VCC	2.7	2.8	3.0	V	
Logic Input High Level		VIH	2.7	2.8	3.0	V	
Logic Input Low Level		VIL	0	--	0.25	V	
System Current	Normal mode	Isc		4.2	5	mW	Note 5-1
	8 Color mode			2.5	2.8	mW	
	8 Color Partial mode			1.4	2	mW	
	Sleep mode			0.5	0.7	mW	

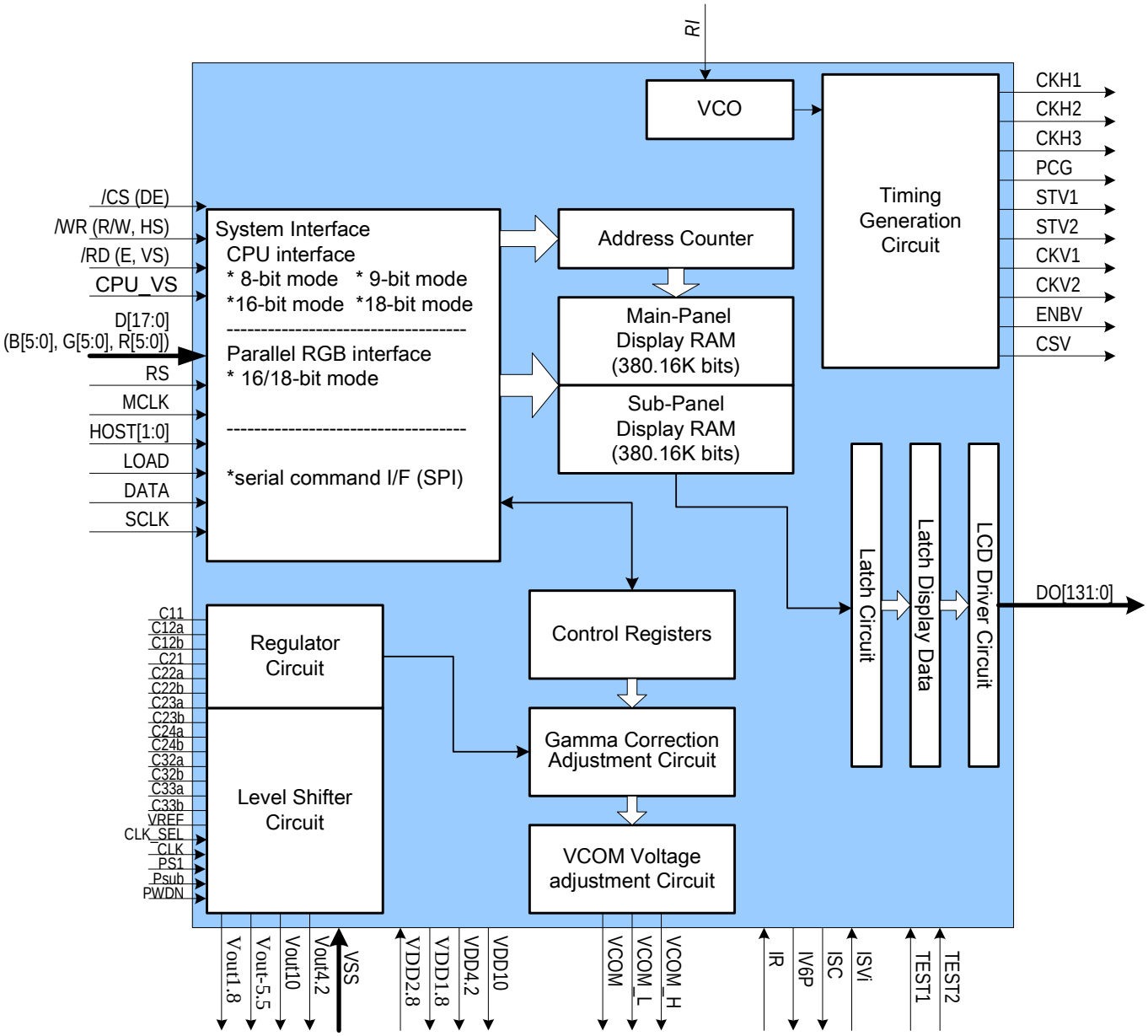
VSS=0V, Ta=25℃

Note: 5-1: Power consumption test condition

a. Input voltage(VCC1): 2.8V

Test pattern:

5.2. Driving TFT LCD Panel Block Diagram



5.3. Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	--	15	25	mA	Note 5-2
Forward Current Voltage	V_F	--	7.2	8.4	V	
Backlight Power Consumption	W_{BL}	--	108	--	mW	

Ta=25℃

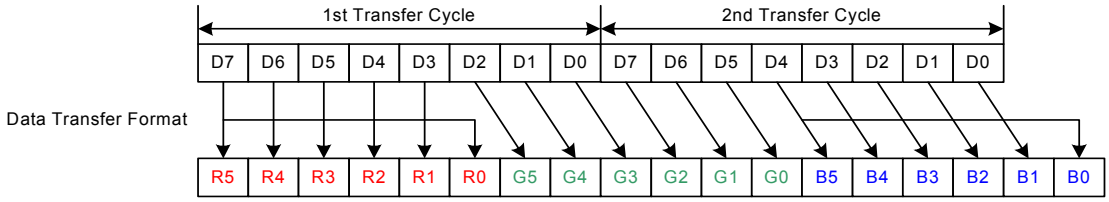
Note 5-2: Backlight driving circuit is recommend as the fix current circuit.

6. TIMING CHART

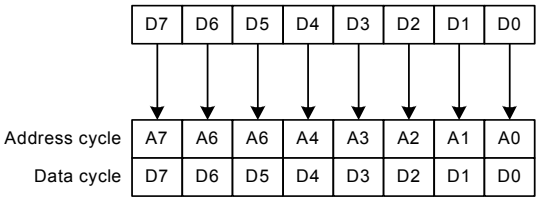
6.1 CPU Interface 8 bit mode

8-Bit Bus Width CPU interface

Memory Access:

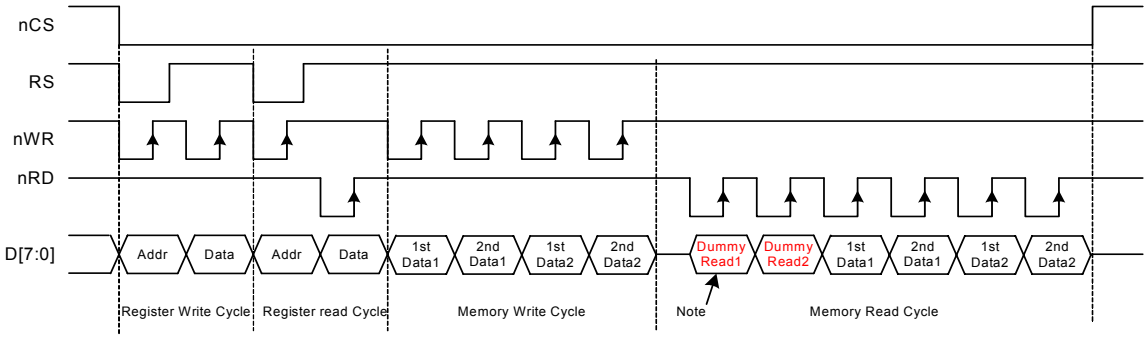


Register Access:

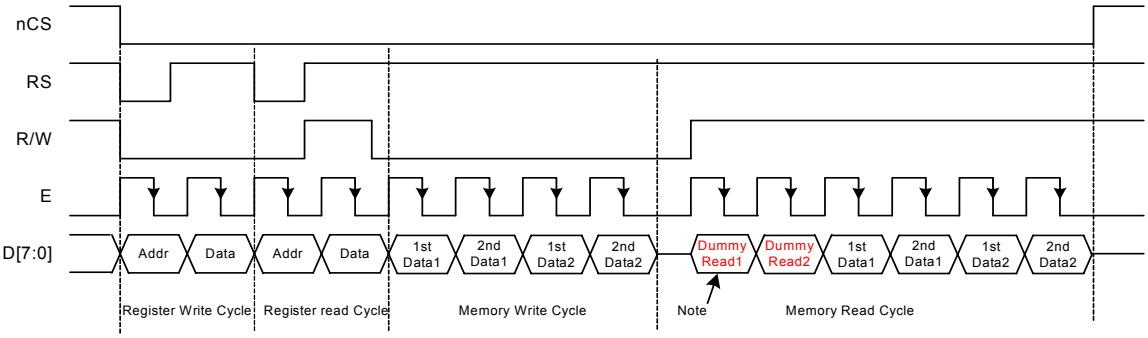


Timing Waveform

Example: i80 CPU



Example: M68 CPU

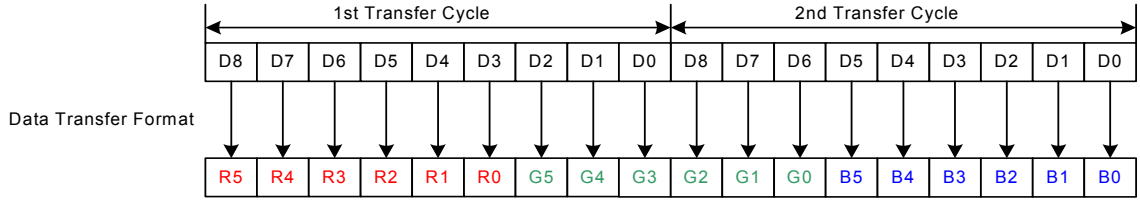


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

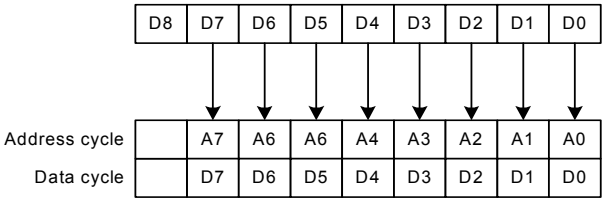
6.2 CPU Interface 9 bit mode

9-Bit Bus Width CPU interface

Memory Access:

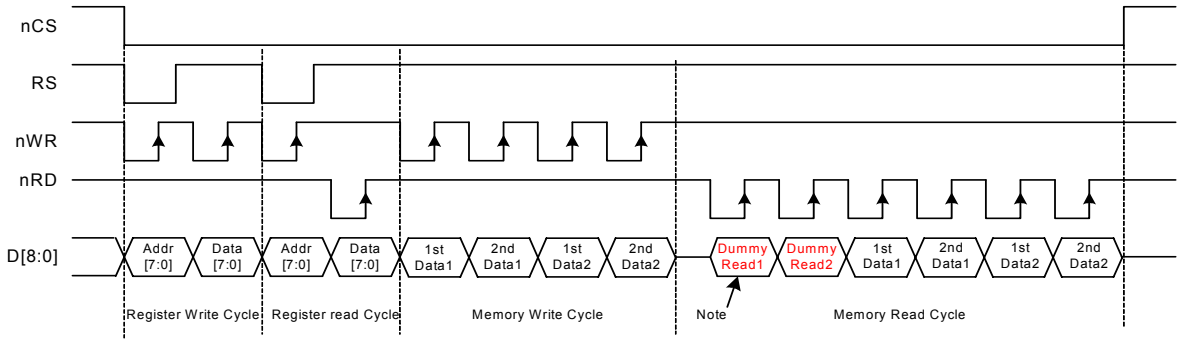


Register Access:

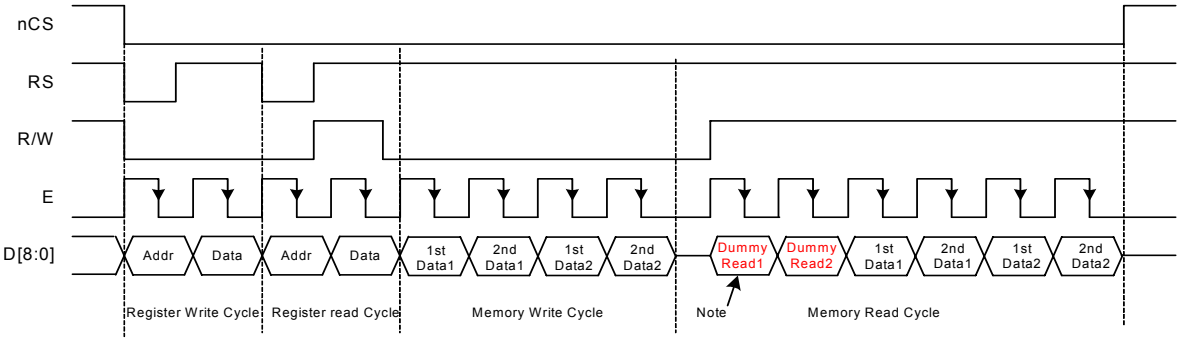


Timing Waveform

Example: i80 CPU



Example: M68 CPU

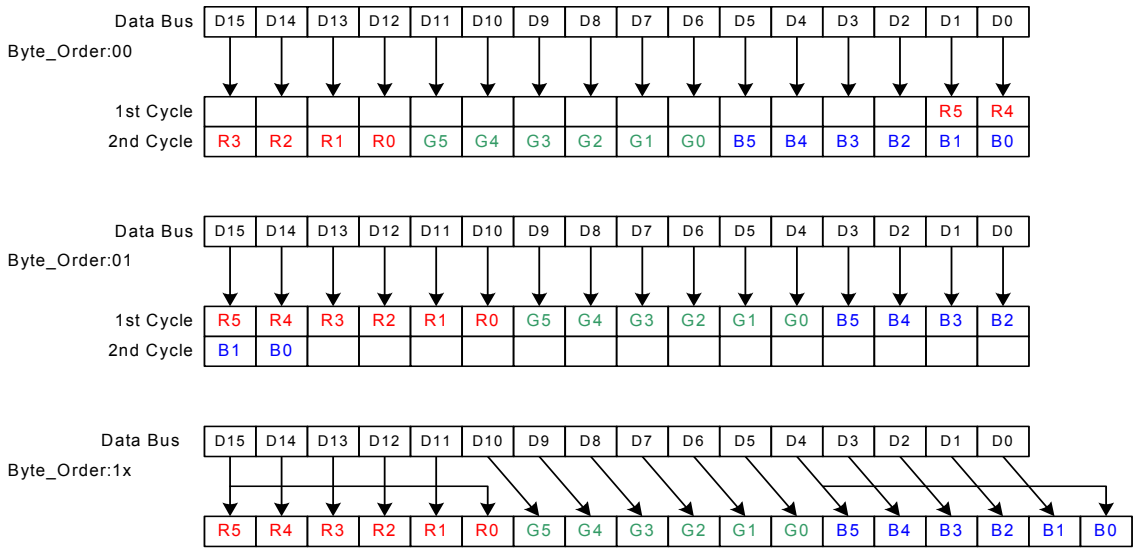


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

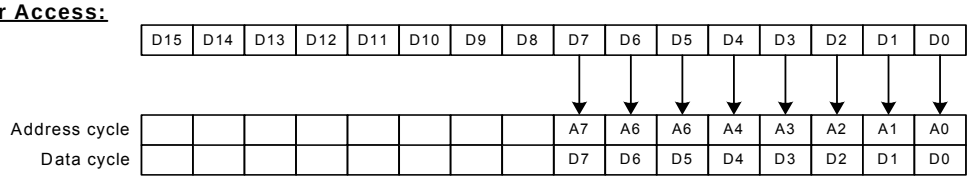
6.3 CPU Interface 16 bit mode

16-Bit Bus Width CPU interface

Memory Access:

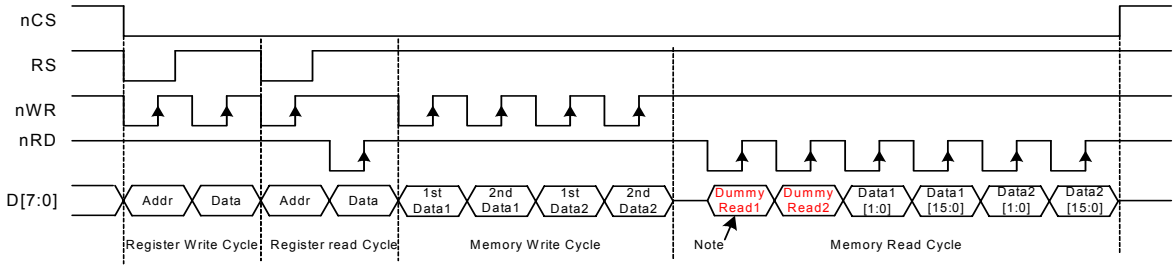


Register Access:

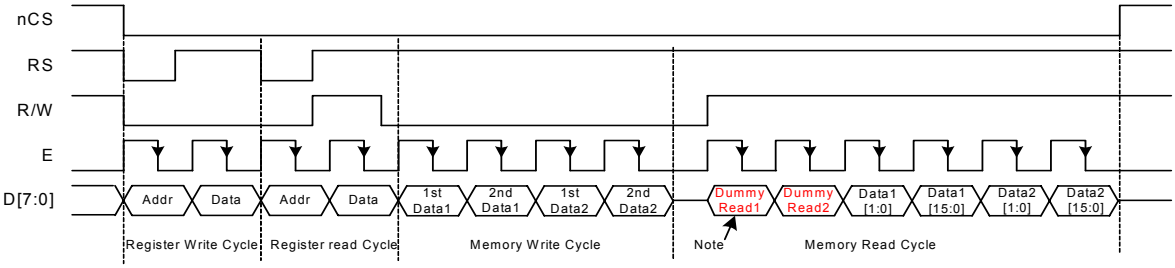


Timing Waveform

Example: i80 CPU, 16-bit, Byte Order=00

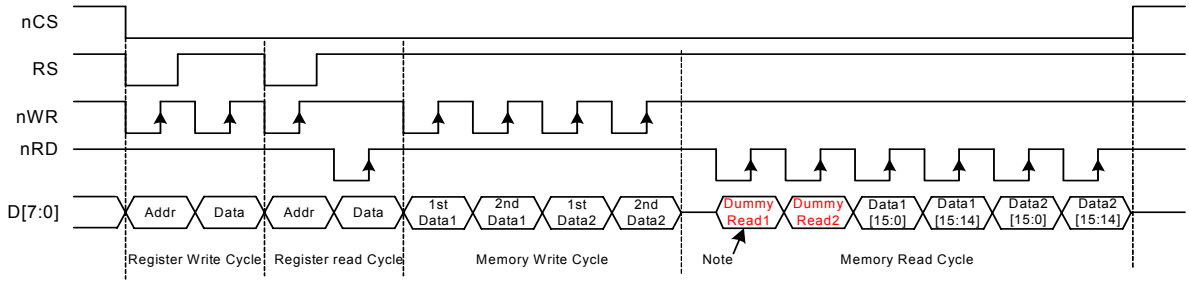


Example: M68 CPU, 16-bit, Byte Order=00

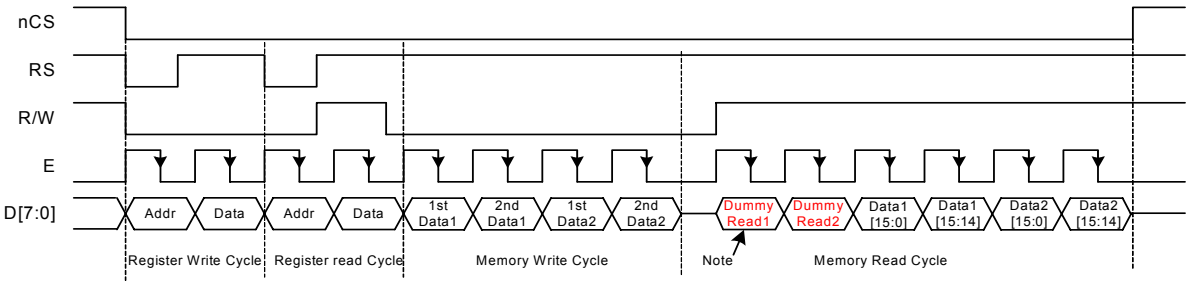


Timing Waveform

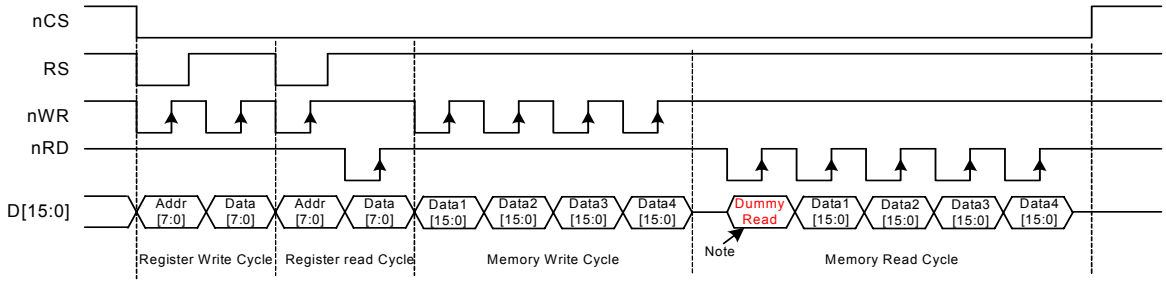
Example: i80 CPU, 16-bit, Byte_Order=01



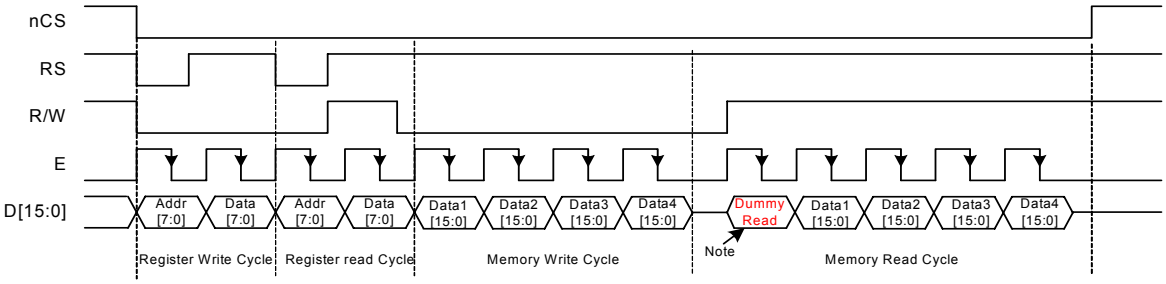
Example: M68 CPU, 16-bit, Byte_Order=01



Example: i80 CPU, 16bit, Byte_Order=1x



Example: M68 CPU, 16-bit, Byte_Order=1x

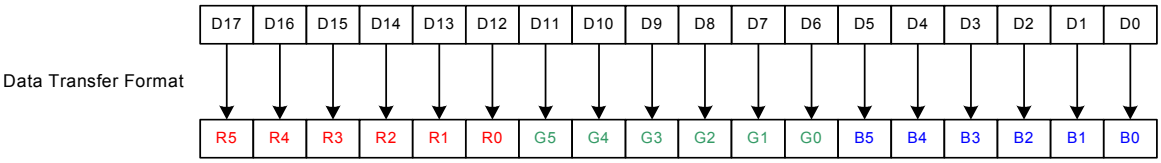


Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

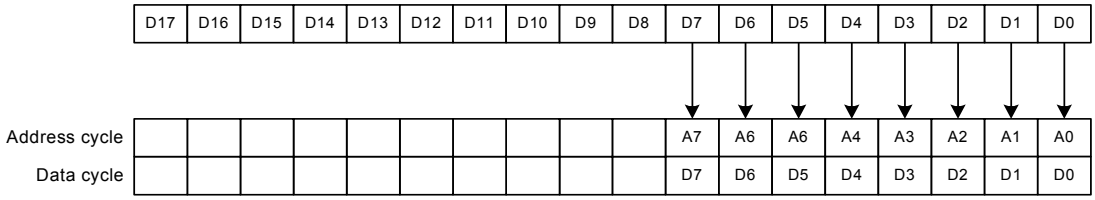
6.4 CPU Interface 18 bit mode

18-Bit Bus Width CPU interface

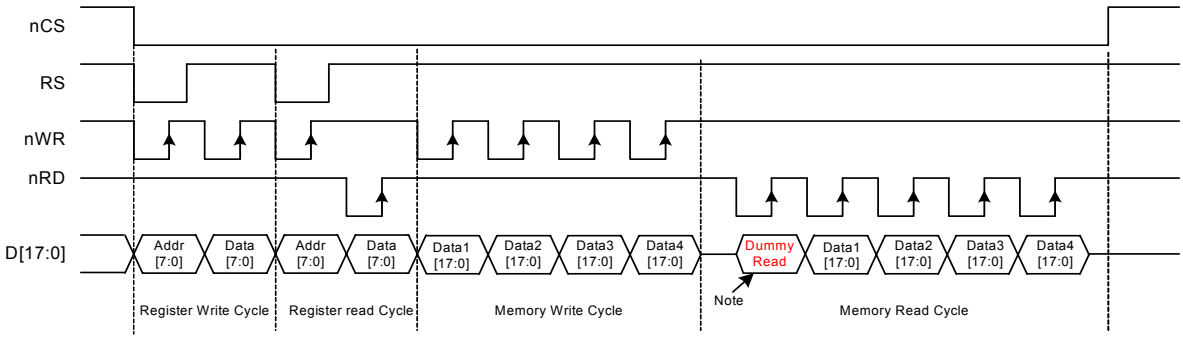
Memory Access:



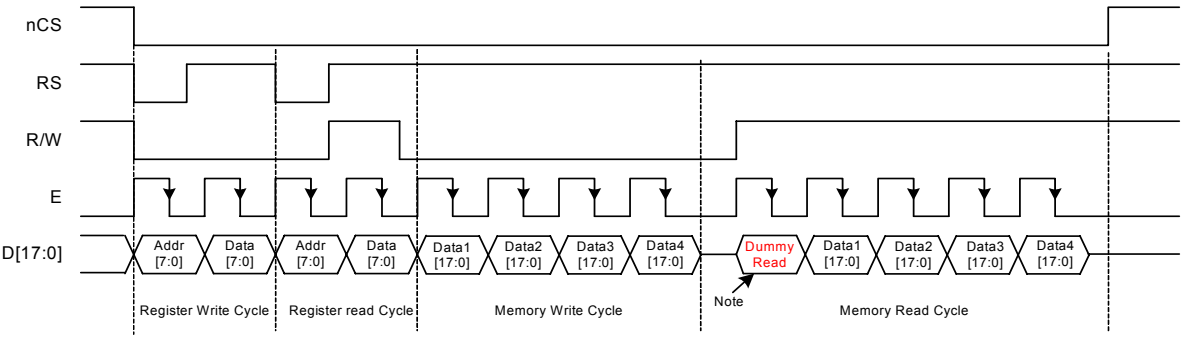
Register Access:



Example: i80 CPU



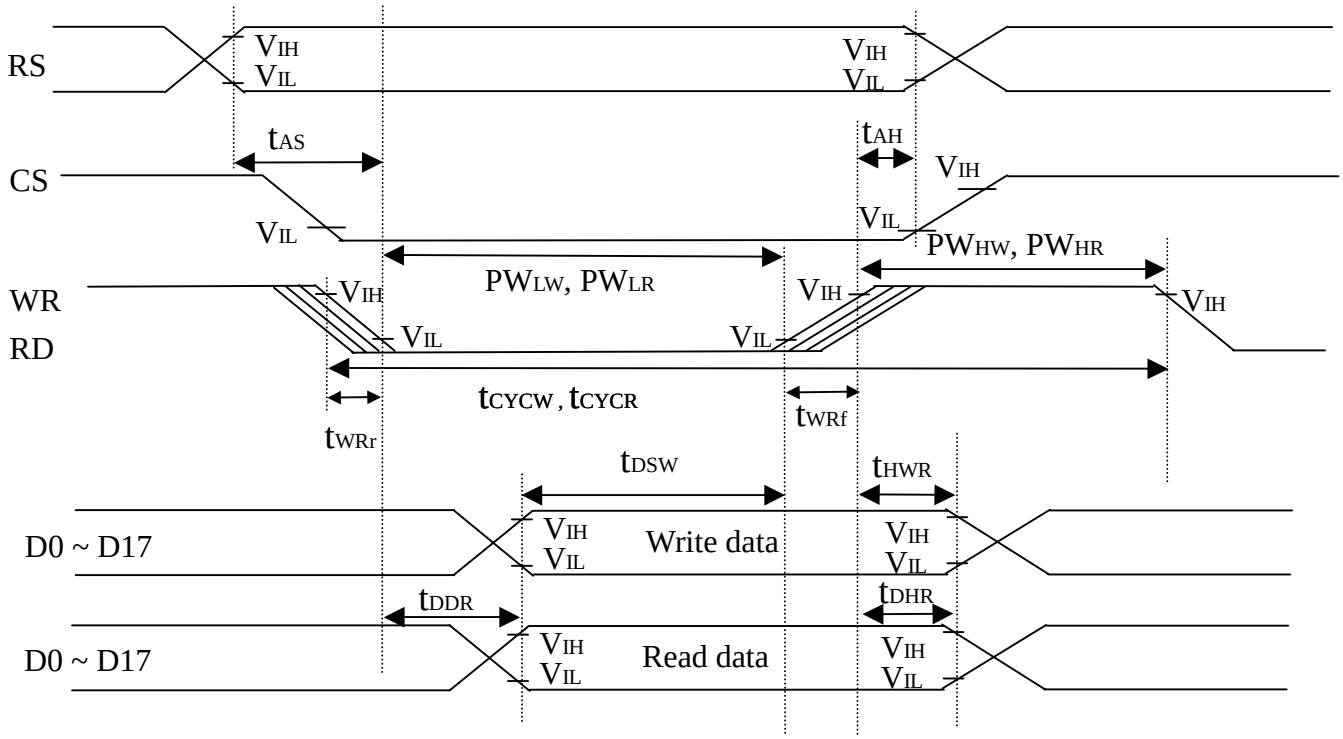
Example: M68 CPU



Note:
1. Since the content of memory is latch into output buffer first, the dummy read operation is necessary to let the latch data send to the output bus when the write cycle is changed to read cycle.
2, The content of address counter increases automatically based on the interface configuration.

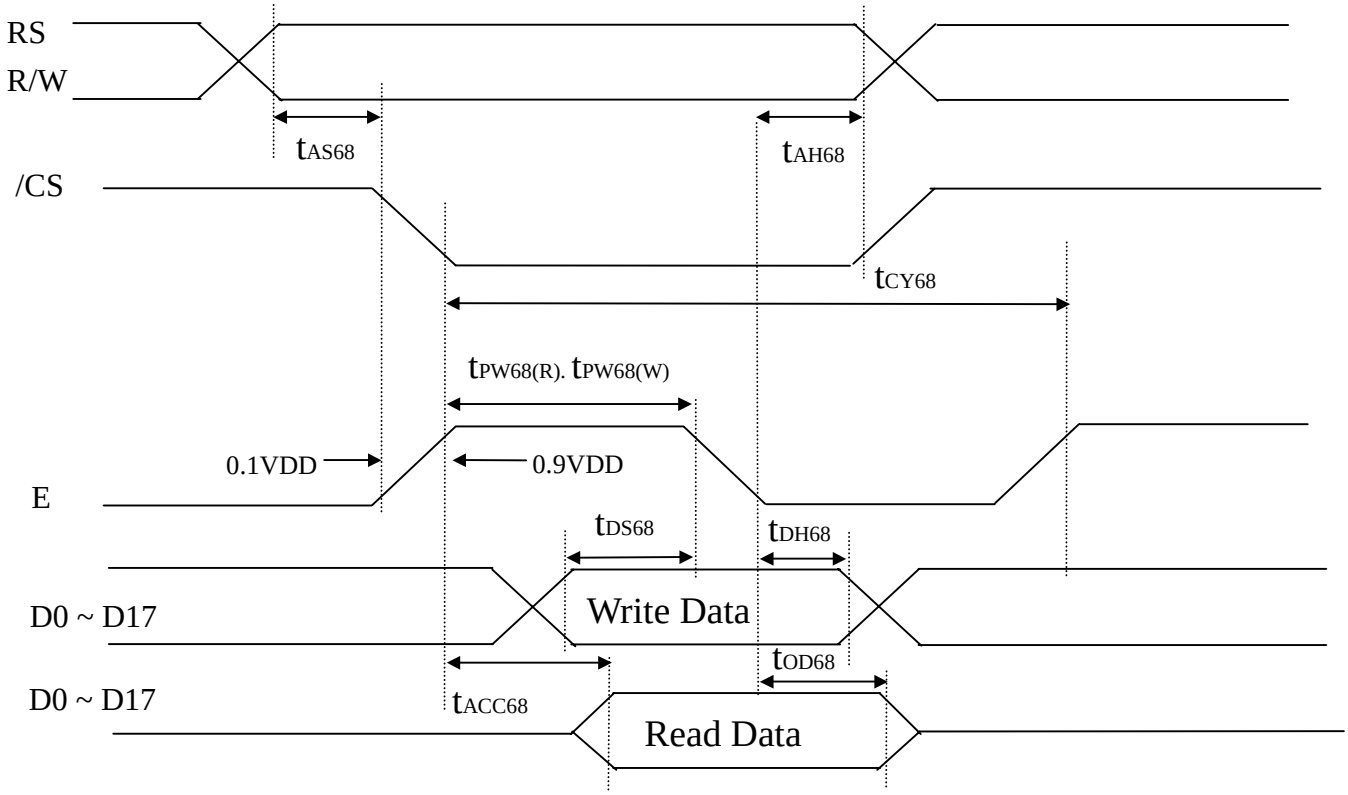
6.5 CPU Interface input timing

I80 System Timing Diagram



Item	Symbol	Min	Typ	Max	unit
Bus cycle time	t_{CYCW}	200	—	—	ns
	t_{CYCR}	300	—	—	ns
E_RD pulse width low	PW_{LW}	40	—	—	ns
	PW_{LR}	150	—	—	ns
E_RD pulse width high	PW_{HW}	100	—	—	ns
	PW_{HR}	100			
Pulse rise/fall time	t_{WRr}, t_{WRf}	—	—	25	ns
Setup time(RS,CS,WR,RD)	t_{AS}	10	—	—	ns
Hold time(RS,CS,WR,RD)	t_{AH}	2	—	—	ns
Data setup time	t_{DSW}	60	—	—	ns
Data hold time	t_{HWR}	2	—	—	ns
Data output setup time	t_{DDR}	—	—	100	ns
Data output hold time	t_{DHR}	5	—	—	ns

M68 System Timing Diagram



Item		Signal	Symbol	Min	Typ	Max.	Unit	Remark
Address setup time Address hold time		RS R/W	t_{AS68} t_{AH68}	13 17	—	—	ns	
System cycle time		RS R/W	t_{CY68}	400	—	—	ns	
Data setup time Data hold time		D[17:0]	t_{DS68} t_{DH68}	35 13	—	—	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	— 10	— —	125 90	ns	C_L = 100pF
Enable pulseWidth	Read Write		$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	—	—	—	

6.6 Input Timing Characteristics

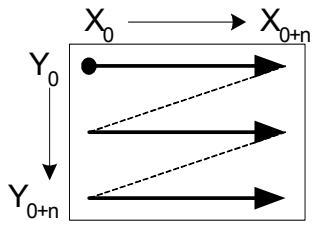
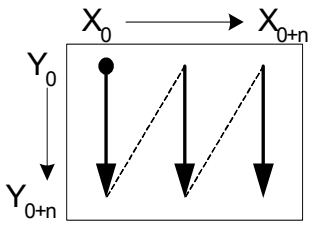
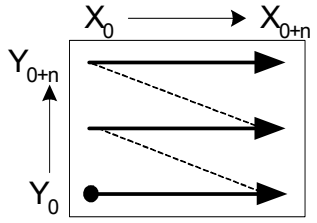
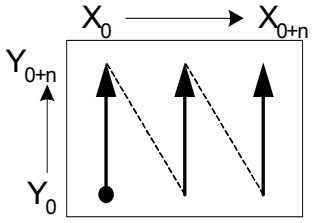
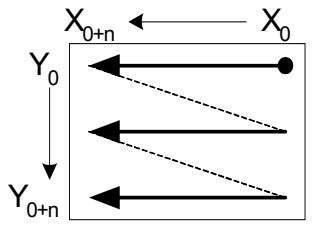
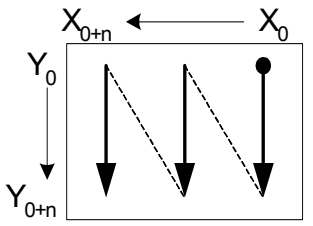
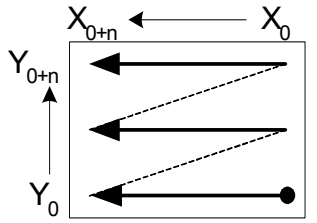
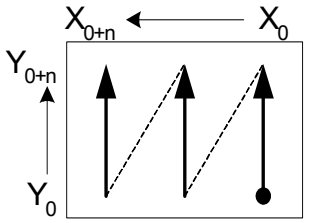
128 x 128

Line No.	R0	G0	B0	R1	G1	B1	.....	R126	G126	B126	R127	G127	B127
	D17.....D0			D17.....D0				D17.....D0			D17.....D0		
L1	"0000"H			"0001"H			.....	"007E"H			"007F"H		
L2	"0100"H			"0101"H			.....	"017E"H			"017F"H		
L3	"0200"H			"0201"H			.....	"027E"H			"027F"H		
L4	"0300"H			"0301"H			.....	"037E"H			"037F"H		
L5	"0400"H			"0401"H			.....	"047E"H			"047F"H		
.....	.....	.....	.....	.....	.....	.....		.....	.....	.....	.....	.....	.....
L123	"7A00"H			"7A01"H			.....	"7A7E"H			"7A7F"H		
L124	"7B00"H			"7B01"H			.....	"7B7E"H			"7B7F"H		
L125	"7C00"H			"7C01"H			.....	"7C7E"H			"7C7F"H		
L126	"7D00"H			"7D01"H			.....	"7D7E"H			"7D7F"H		
L127	"7E00"H			"7E01"H			.....	"7E7E"H			"7E7F"H		
L128	"7F00"H			"7F01"H			.....	"7F7E"H			"7F7F"H		

96 x 96

Line No.	R0	G0	B0	R1	G1	B1	.....	R94	G94	B94	R95	G95	B95
	D17.....D0			D17.....D0				D17.....D0			D17.....D0		
L1	"0000"H			"0001"H			.....	"005E"H			"005F"H		
L2	"0100"H			"0101"H			.....	"015E"H			"015F"H		
L3	"0200"H			"0201"H			.....	"025E"H			"025F"H		
L4	"0300"H			"0301"H			.....	"035E"H			"035F"H		
L5	"0400"H			"0401"H			.....	"045E"H			"045F"H		
.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
L91	"5A00"H			"5A01"H			.....	"5A5E"H			"5A5F"H		
L92	"5B00"H			"5B01"H			.....	"5B5E"H			"5B5F"H		
L93	"5C00"H			"5C01"H			.....	"5C5E"H			"5C5F"H		
L94	"5D00"H			"5D01"H			.....	"5D5E"H			"5D5F"H		
L95	"5E00"H			"5E01"H			.....	"5E5E"H			"5E5F"H		
L96	"5F00"H			"5F01"H			.....	"5F5E"H			"5F5F"H		

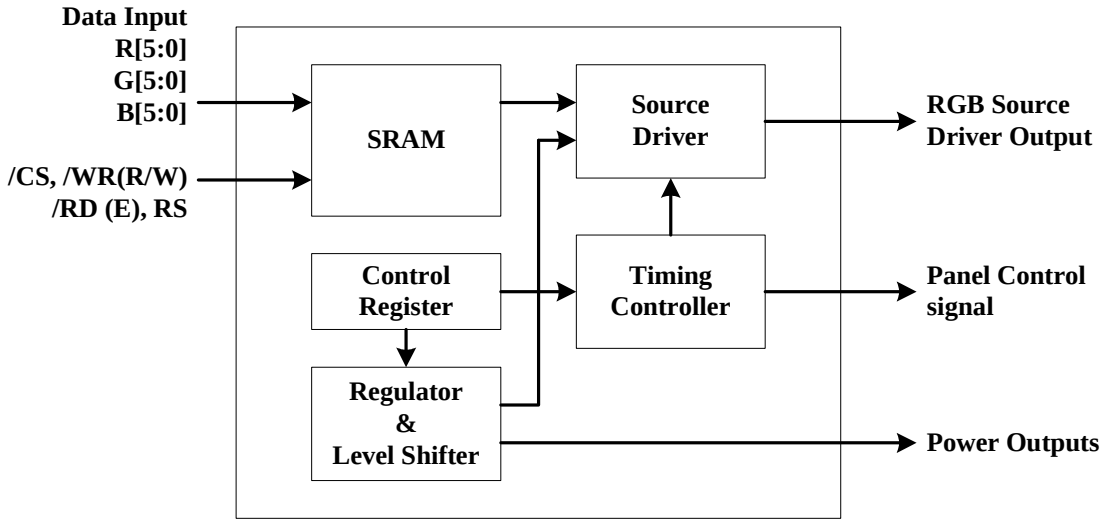
6.7 SRAM Access Mode

ADDR_CTRL_X	ADDR_CTRL_Y	ADDR_CTRL_XY	Scan Types	ADDR_CTRL_X	ADDR_CTRL_Y	ADDR_CTRL_XY	Scan Types
*0	*0	*0		0	0	1	
0	1	0		0	1	1	
1	0	0		1	0	1	
1	1	0		1	1	1	

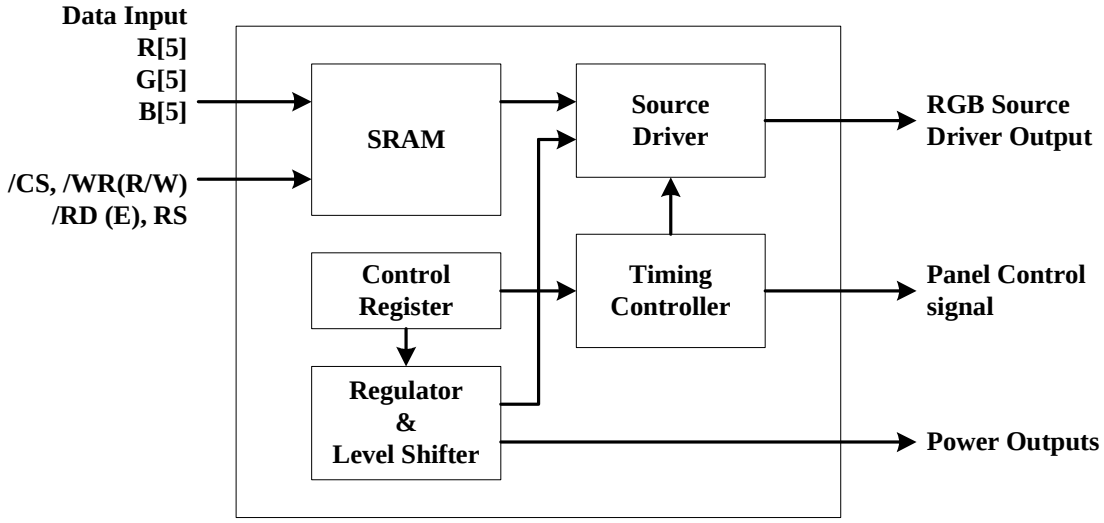
** [ADDR_CTRL_X, ADDR_CTRL_Y, ADDR_CTRL_XY] = "000" mode can operate in the CPU and parallel RGB mode, and the other modes can operate in the CPU mode only.*

6.8 Mode Setup

6.8.1 Normal (Moving) Mode



6.8.2 8 color Mode



(1) Reduce Frame rate, 60Hz→40Hz, so change time step up 60/40

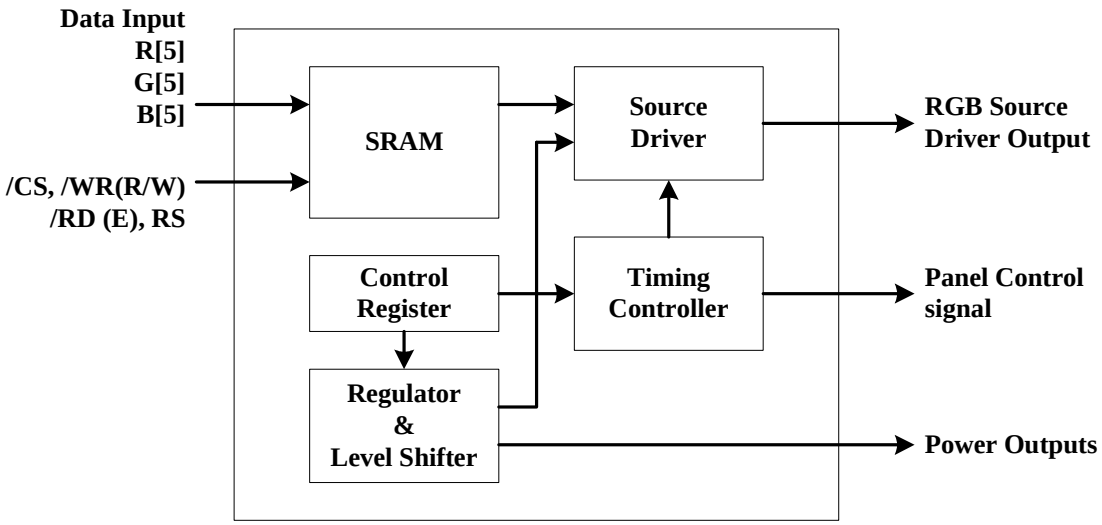
(2) Vcom & source driver DC bias current reduce 40/60

(3) Reduce RGB swing voltage 4V →2.8V

(4) Reduce Vcom swing voltage 4V → 2.2V max. (adjustable)

	Data (white)	Data (black)
Vcom high(+2.2V)	2.8V	0V
Vcom low(0.2V)	0V	2.8V

6.8.3 8 Color Dithering Mode



(1) Reduce Frame rate, 60Hz →40Hz, so change time step up 60/40

(2) Vcom & source driver DC bias current reduce 40/60

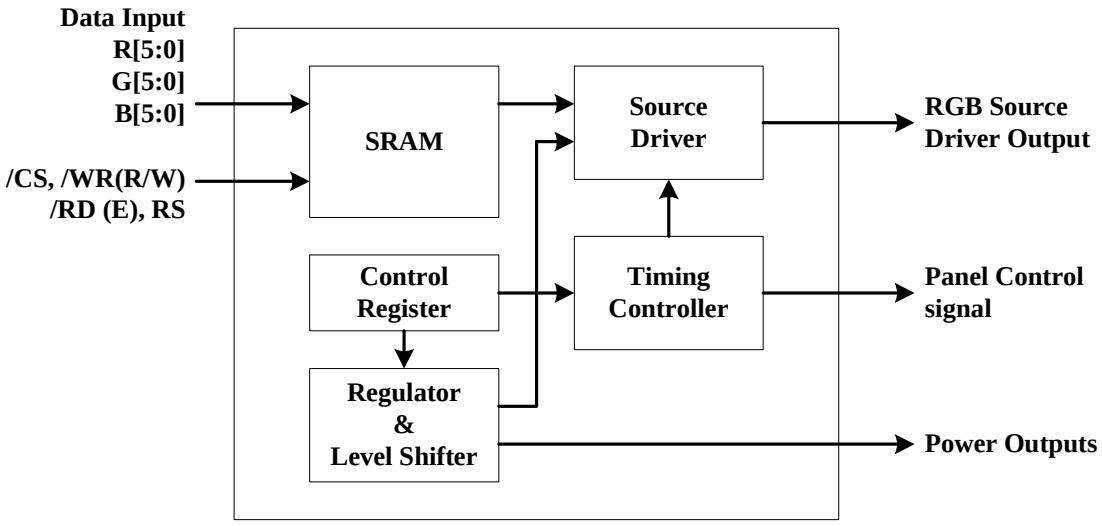
(3) Reduce RGB swing voltage 4V →2.8V

(4) Reduce Vcom swing voltage 4V → 2.2V max. (adjustable)

	Data (white)	Data (black)
Vcom high(+2.2V)	2.8V	0V
Vcom low(0.2V)	0V	2.8V

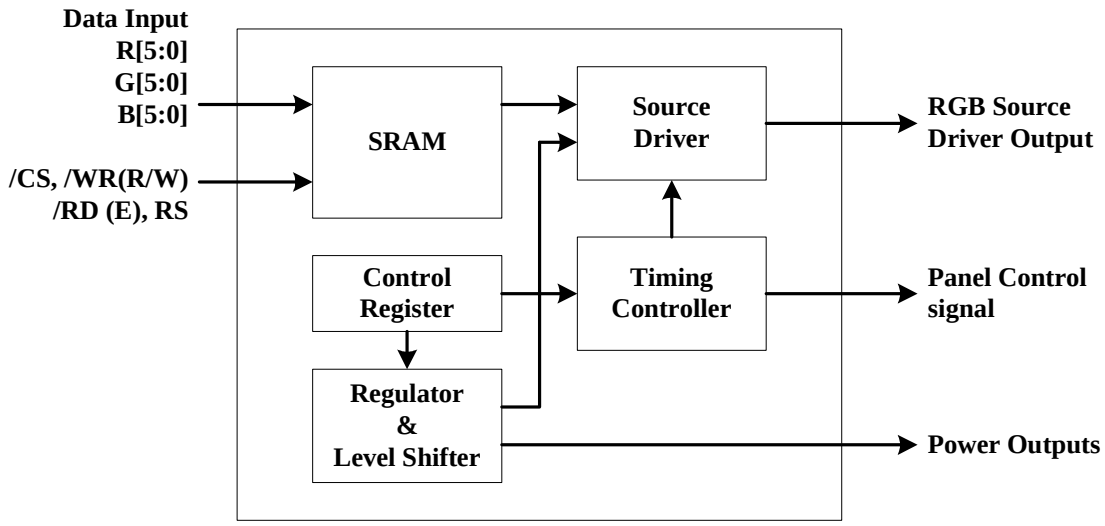
6.8.4 Partial Mode

(16/18bit color or 8 color mode)



Only display area, other area have no signal and no display

6.8.5 Sleep Mode

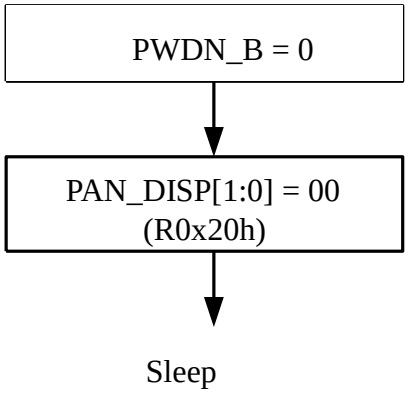


Note 1: Only receive register data. SRAM data can be retained.

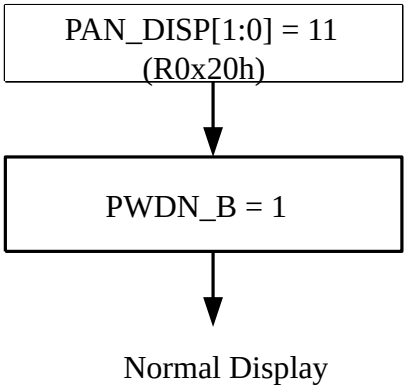
Note 2: The VCO is stopped in sleep mode.

Note 3: The power Vout1.6 is not off in sleep mode and is controlled by PS1 input.

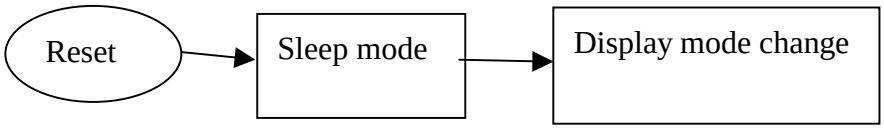
Sleep Mode Setting Flow



Sleep Mode Cancel Flow



6.9 Control Flow



6.10 Input Signals, Basic Display Color and Gray Scale of Each Color

6.10.1 65K

Color	Display	Data Signal																Gray Scale
		Red					Green						Blue					
		R0	R1	R2	R3	R4	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	-
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	-
	Cyan	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
																		R3~
																		R28
	↓	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R29
	Light	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R30
	Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	R31
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	G2
																		G3~
																		G60
	↓	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	G62
	Green	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	G63
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	B2
																		B3~
																		B28
	↓	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	B29
	Light	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	B30
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B31

6.10.2 262K

Color	Display	Data Signal																		Gray Scale
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
																				R3~
																				R60
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
																				G3~
																				G60
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
																				B3~
																				B60
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

7 OPTICAL CHARACTERISTICS

7.1 Main panel Optical Specification (LED current =15mA)

Ta=25℃

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ_{right}	CR ≥ 2	60	>60	—	Degree	Note 7-1
	Θ_{left}		60	>60	—		
	Θ_{up}		30	35	—		
	Θ_{down}		60	>60	—		
Contrast Ratio	CR	Θ=0°	200	300	—	—	Note 7-2
Response Time	Tr+Tf	Θ=0°	—	35	45	ms	Note 7-3
Luminance (I_F=15mA)	L	Θ=0°	200	240	—	cd/m^2	Note 7-4
White Chromaticity	x_W	Θ=0°	0.283	0.326	0.350	—	Note 7-5
	y_W		0.298	0.341	0.365		
Red Chromaticity	x_R	Θ=0°	0.565	0.615	0.665	—	Note 7-5
	y_R		0.300	0.350	0.400		
Green Chromaticity	x_G	Θ=0°	0.267	0.317	0.367	—	Note 7-5
	y_G		0.529	0.579	0.629		
Blue Chromaticity	x_B	Θ=0°	0.096	0.146	0.196	—	Note 7-5
	y_B		0.090	0.140	0.190		
NTSC	NTSC	Θ=0°	45	50	--	%	Note 7-5
Uniformity	U_L	Θ=0°	78	>80	--	%	Note 7-9
MicroReflectance	R	Θ=10°	1.5	2	--	%	Note 7-8

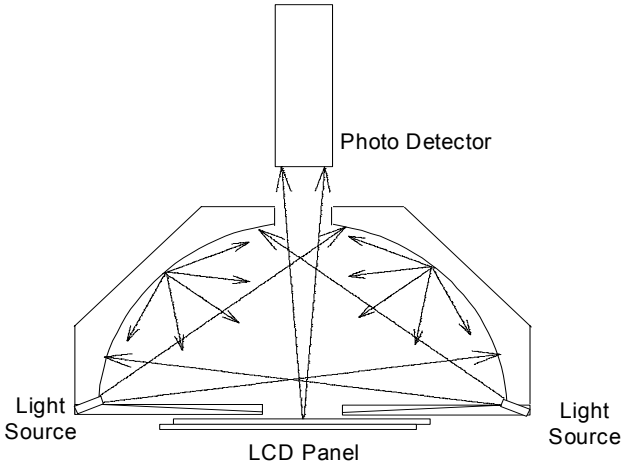
7.2 Basic Measure Condition

(1) Ambient Temperature: Ta=25℃

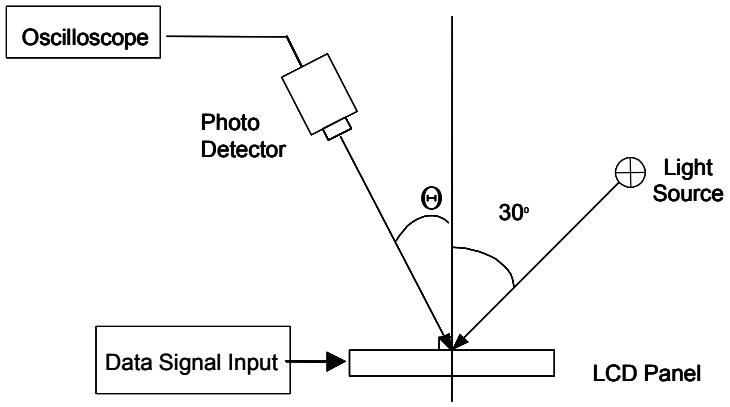
(2) Testing Point: Measure in the display center point and the test angle Θ=10°

(3) Measuring System

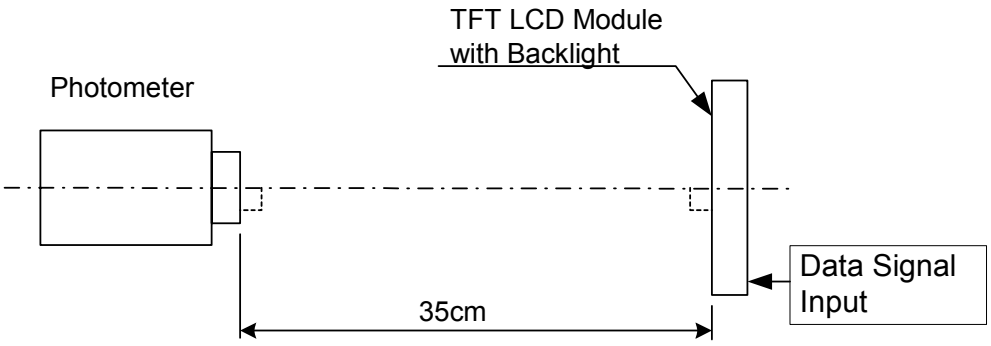
a. Measure System A



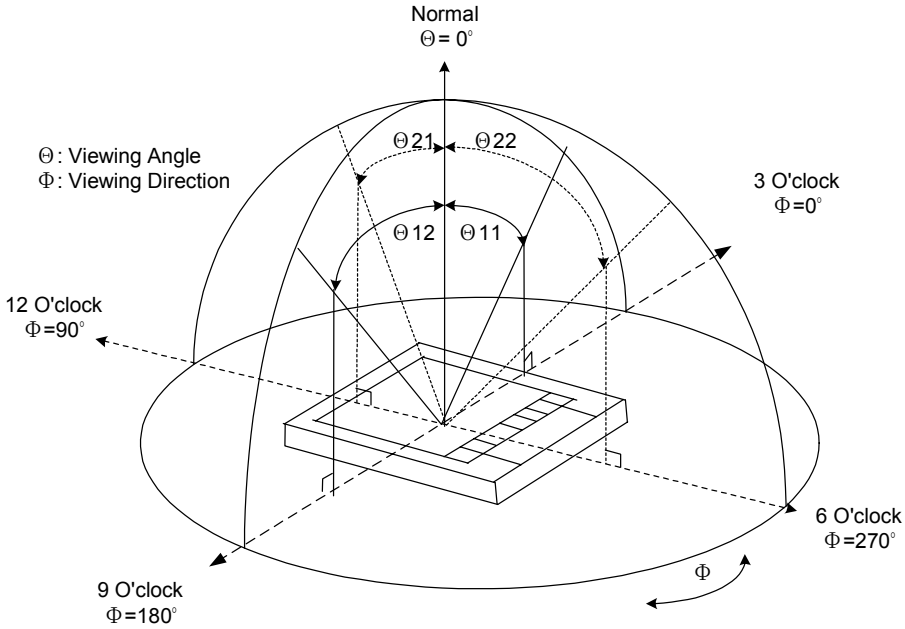
b. Measure System B (θ =10deg)



c. Measure System C



Note 7-1: Viewing angle diagram:

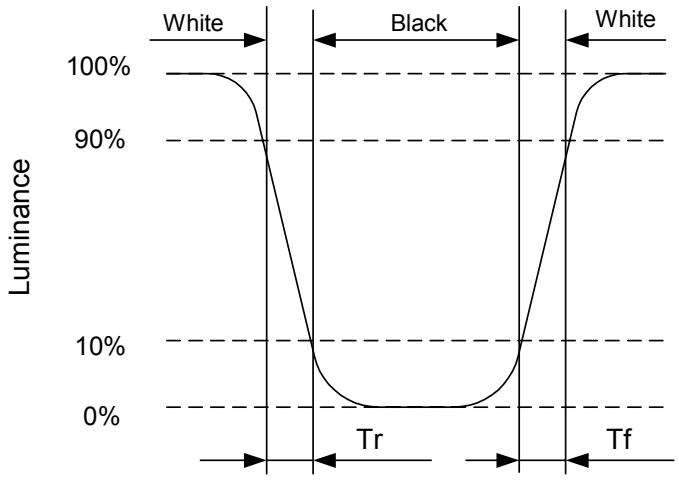


Note 7-2: Contrast Ratio as Backlight On: (Measure System C)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time: (Measure System C)



Note 7-4: Luminance: (Measure System C)

Test Point: Display Center

LED Current If = **15 mA**

Note 7-5: Chromaticity: The same test condition as Note 7-4.

Note: 7-6: Contrast Ratio as Backlight Off: (Measure System B)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-7: White chromaticity as back light off: (Measure System A)

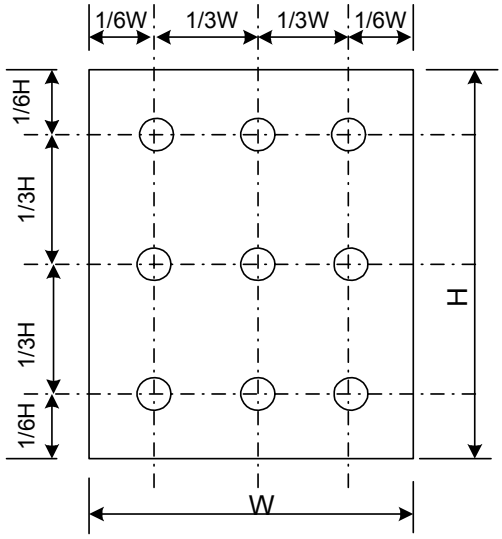
Note 7-8: Reflectance: (Measure System B)

$$\text{Reflection ratio(R)} = \frac{\text{Light detected level of refection by the LCD module}}{\text{Light detected level of refection by the standard white}}$$

Notes 7-9: Definition of uniformity: Light on backlight 5 minutes before test.

$$\text{Uniformity (Lu)} = \frac{\text{Minimum Luminance of 9 test points}}{\text{Center Point Luminance of 9 test points}} \text{X100\%}$$

The definition of 9 test points:



8 RELIABILITY

No	Test Item	Condition
1	High Temperature Operation	Ta = +70℃, 240hrs
2	High Temperature & High Humidity Operation	Ta = +40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta = -20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta = +70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta = -30℃, 240hrs
6	Thermal Shock (non-operation)	-30℃ ←→ 70℃, 30 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0Ω; Discharge: ±150V 3 times / Terminal
8	Surface Discharge (non-operation)	C=150pF, R=330Ω(Non-OP) Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel(System) MM(Machine Mode)
9	Vibration (non-operation)	Frequency: 10~55~10Hz; Amplitude: 1.5mm Sweep Time: 11 min Test Time: 2 hrs for each direction of X, Y, Z
10	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles(Once for each direction)

Ta: Ambient Temperature

9 HANDLING CAUTIONS

9.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. Connect the wrist conduction ring to the earth and the conducting shoes to the earth are necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, using ionized air to decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

9.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) The front polarizer is easy damaged. Handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface. Please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

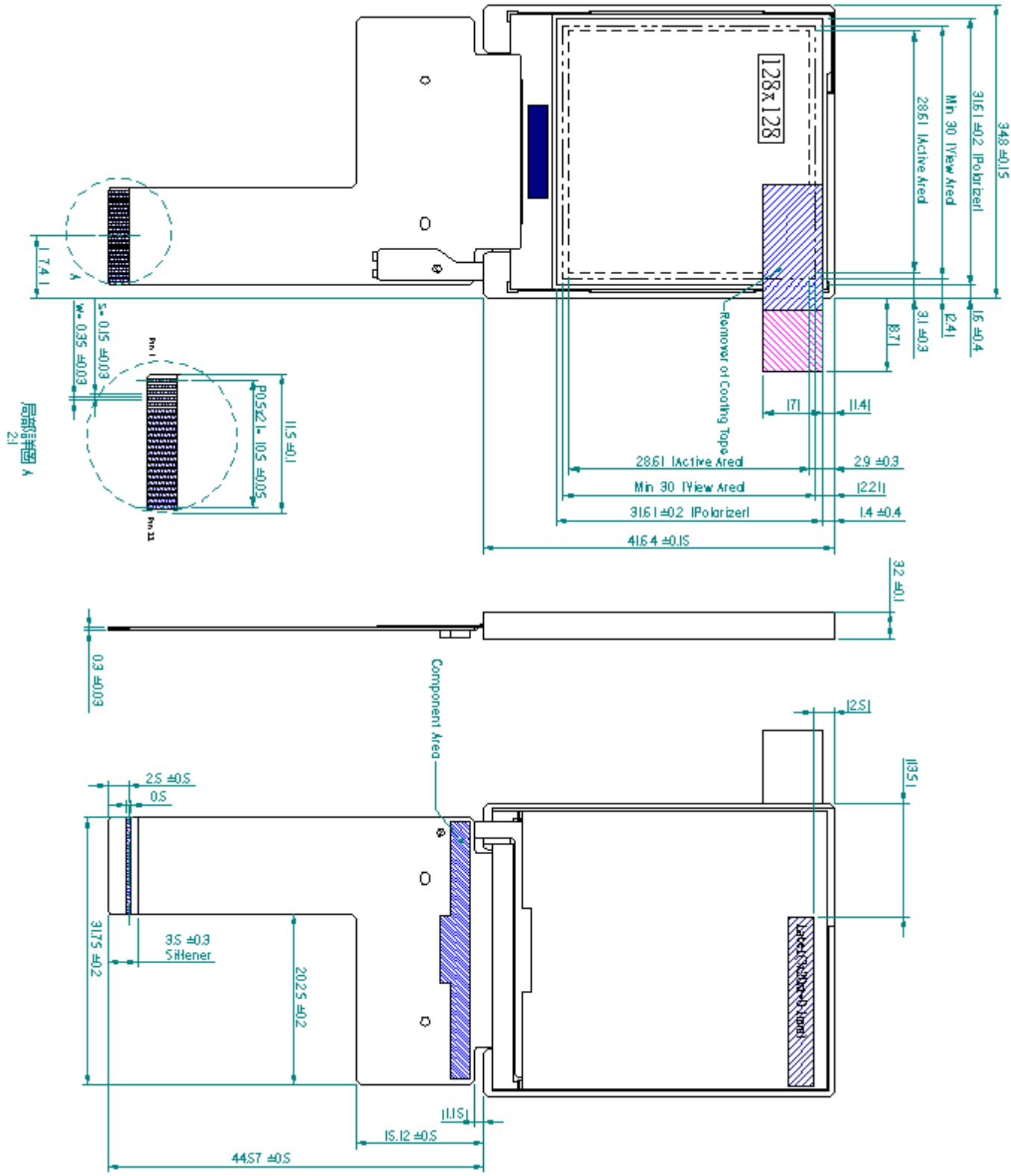
(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(3) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

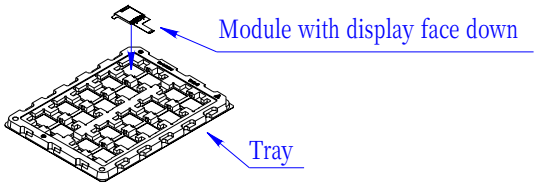
(4) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

10 MECHANICAL DRAWING



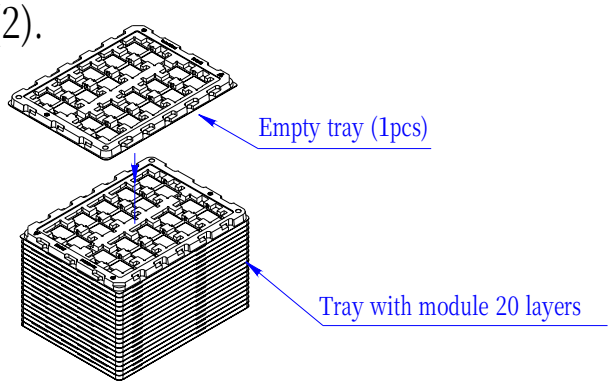
11 PACKING DRAWING

(1).

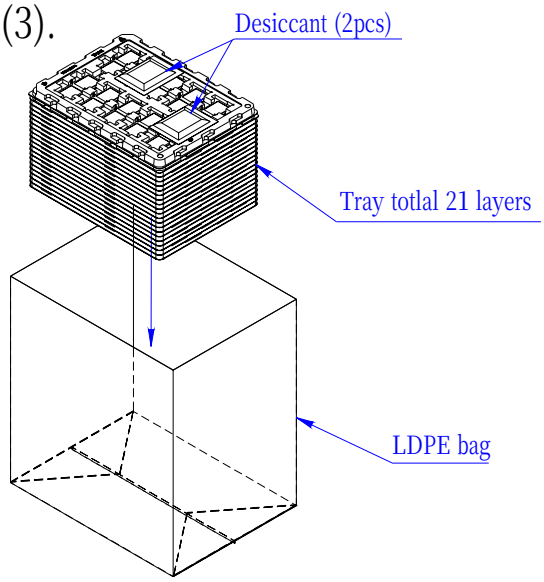


Module Qt'y on 1 tray =10pcs

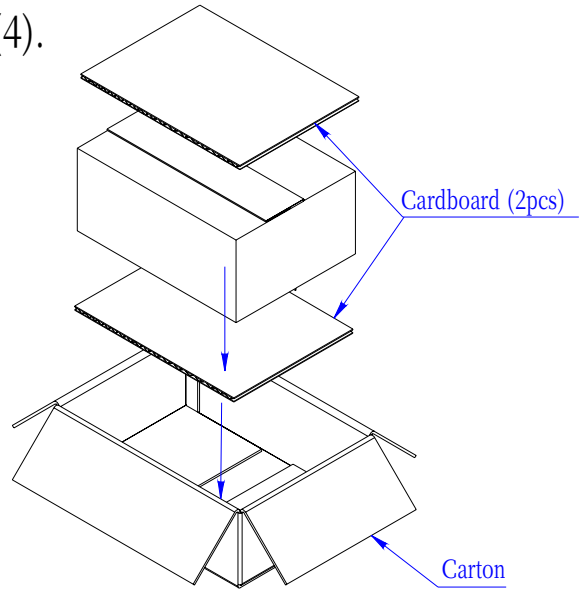
(2).



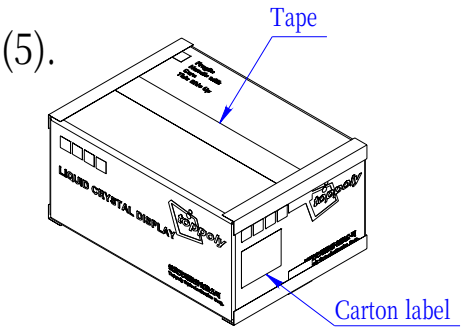
(3).



(4).



(5).



Module Qt'y = 200pcs

TD016THEB2 Module delivery packing method

1. Module packed into tray cavity (with Module display face down).
2. Tray pack with module (Tray stacking with 20 layers) and with 1 empty tray above
3. The stacking tray unit.2pcs desiccant put above the empty tray. Stacking tray unit put into the LDPE bag and fixed by adhesive tape.
4. Pack the package unit into the carton, and with 2pcs cardboard under the package unit.
5. Carton tapping with adhesive tape.