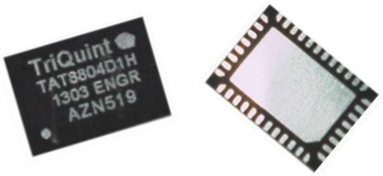
TAT8804D1H

21 dB CATV 12V Power Doubler

Applications

- HFC Nodes
- CATV Line Amplifiers
- Head End Equipment
- 50 to 1000 MHz 75 Ohm Amplifier

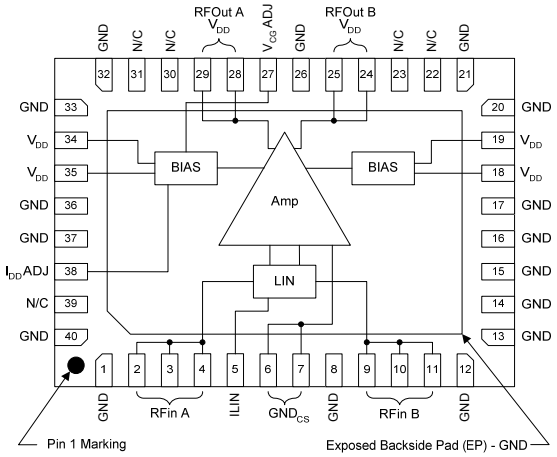


40 Pin 5x7 mm QFN Package

Product Features

- 50 to 1000 MHz Bandwidth
- Excellent High Output Linearity at Reduced Supply Voltages
- Ultra-Low CSO / CTB / XMOD
- Low Noise through 1.2 GHz
- Excellent Input/Output Return Loss
- High Gain, 21 dB typ. at 1.2 GHz
- Variable Bias Control
- Compact 5 X 7 mm QFN Package
- High Reliability with RF ESD protection
- +12 V Supply Voltage
- 650 mA Operating Current

Functional Block Diagram



General Description

The TAT8804 is an ultra-linear, QFN GaAs amplifier MMIC intended for output stage amplification in CATV infrastructure applications.

The device features a push-pull cascode design which provides flat gain along with ultra-low distortion, making it ideal for use in CATV distribution systems requiring high output power capability. ESD protection is also provided at the output of the device.

The TAT8804 draws approximately 650 mA from a single +12 V supply providing 21 dB gain with excellent linearity.

Users may adjust the bias current with external voltage enabling the TAT8804 to be used in applications such as doublers or for lower power system applications.

The TAT8804 is packaged in an industry standard 40 pin 5 x 7 mm QFN package with exposed paddle (EP) beneath the device for thermal and electrical grounding.

For applications requiring demanding VSWR tolerance at high input overdrive conditions, an EVB with level protection is available (TAT8804D1H-EBP).

Pin Configuration

Pin No.	Label
18-19, 34-35	V_{DD}
2-4	RFin A
9-11	RFin B
28-29	RFout A/V_{DD}
24-25	RFout B/V_{DD}
5	ILIN
27	V_{CG} ADJ
38	I_{DD} ADJ
1,8,12-17, 20-21, 26, 32-33, 36-37, 40, EP	GND
6-7	GND_{CS}
22-23, 30-31, 39	N/C

Ordering Information

Part No.	Description
TAT8804D1H	GaAs Power Doubler MMIC
TAT8804D1H-EB	50−1200 MHz Evaluation Board
TAT8804D1H-EBP	50−1200 MHz EVB + Protection

Standard T/R size = 1000 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to 100 °C
Operating Temperature	−40 to 85 °C
Device Voltage (V_{DD})	+18 V
Device Current (I_{DD})	750 mA

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})		12		V
Tj for >10^6 hours MTTF			165	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

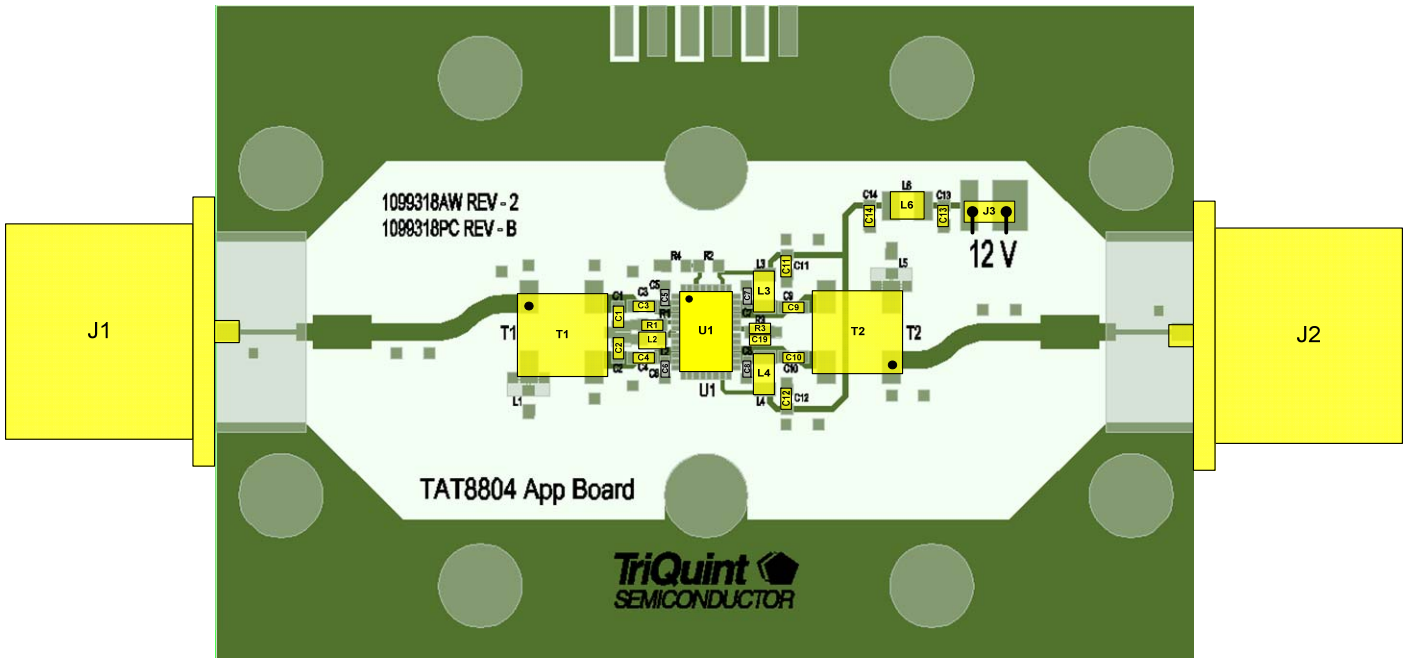
Electrical Specifications

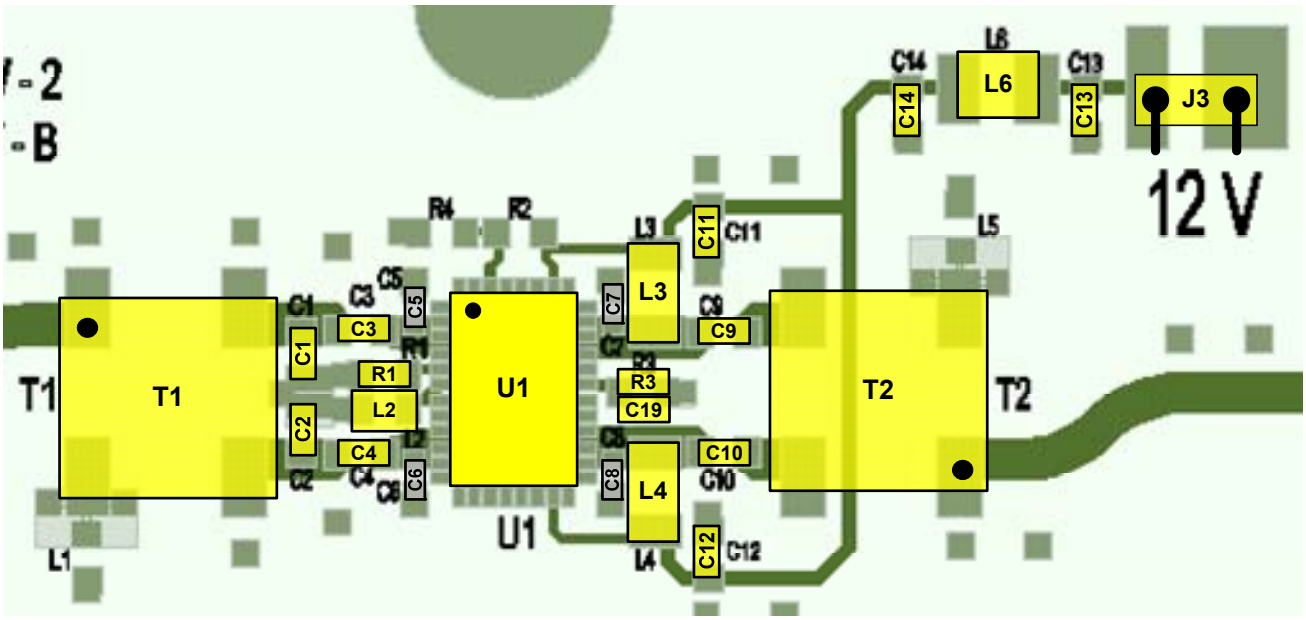
Test conditions unless otherwise noted: V_{DD} = +12 V, Heatsink Temp. = +35°C, $Z_{In/Out}$ = 75 Ω using evaluation board EB
Includes input and output balun/transformer losses of tuned application circuit,

Parameter	Conditions		Min	Typ	Max	Units
Operational Frequency Range			50		1003(1)	MHz
Current (I_{DD})			550	650	720	mA
Gain	f_o= 50 & 1003 MHz	EVB: EB		21		dB
		EVB: EBP[5]		19.5		
Gain Flatness	50 to 1003 MHz(2)		-0.5		+0.5	
Gain Tilt	50 to 1003 MHz(3)			+0.6		
Input Return Loss	f_o= 50 MHz			25		dB
	f_o= 1003 MHz			17		
Output Return Loss	f_o= 50 MHz			20		dB
	f_o= 1003 MHz			17		
Overdrive VSWR Mismatch Tolerance	79 Ch. NTSC + 75 Ch. QAM, −6 dB offset, Vin = +44 dBmV per channel	EVB: EB			1.37:1 (16)	VSWR (dB)
		EVB: EBP[5]			5.85:1 (3)	
CSO	79 Ch. NTSC + 75 Ch. QAM, −6 dB offset EQ Vout = +58 dBmV with 15.6 dB tilt	Note 4		−73	−68	dBc
CTB				−79	−70	dBc
XMOD				−62		dBc
CCN			60	64		dB
OIP2	f_1- f_2= 50 MHz, +17 dBm / tone	Note 4		85		dBm
OIP3				49		dBm
P1dB				34		dBm
Noise Figure				4.5		dB
Thermal Resistance, θjb	Junction to base			5.5		°C/W

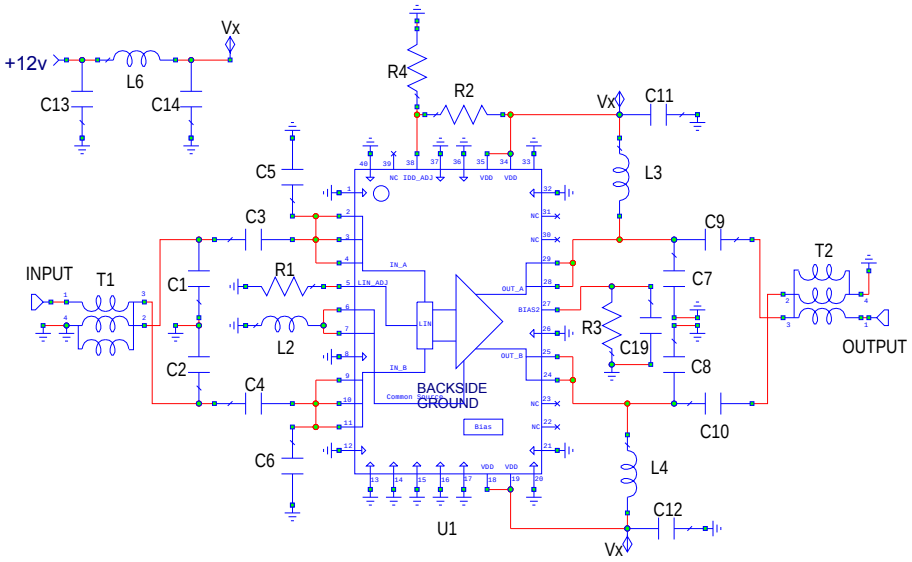
Notes:
1. Useable S21 Bandwidth can extend to 1200 MHz with some S11 & S22 degradation
2. Using least squares fit across the band 50 to 1003 MHz
3. Gain of $S21_{1003MHz}$ - $S21_{50MHz}$
4. Standard EB configuration (EVB without protection).
5. EBP – Evaluation board with protection

TAT8804D1H-EB Evaluation Board





TAT8804D1H-EB Evaluation Board Schematic



Bill of Material – TAT8804D1H-EB

Reference Des.	Value	Description	Manuf.	Part Number
PCB	Rev B	PCB TAT8804 - EVB	TriQuint	1099318
U1	n/a	TAT8804D1H Sample	TriQuint	TAT8804D1H
T1-2	1:1 BALUN, 75Ω	MABA-009210-CT1760	MACOM	MABA-009210-CT1760
C11-12	0.01 uF	CAP, 0603, 10%, 50V, X7R	TDK	C1608X7R1H103J
C3-4	270 pF	CAP, 0603, 5%, 50V, NPO	TDK	C1608C0G1H271J080AA
C9-10	330 pF	CAP, 0603, 5%, 50V, NPO	TDK	CGJ3E2C0G1H331J080AA
C13-14	0.1 uF	CAP, 0603, 10%, 50V, X7R	TDK	C1608X7R1H104K
C19	4.7uF	CAP, 0603, 10%, 10V, Y5V	Murata	GRM188F51A475ZE20D
L2[1]	680 nH	IND, 0805, 5%, 355 MHz SRF, 660mA	Coilcraft	0805AF-681XJR
L3-4	500 nH	IND, 1206, 10%, 270 MHz SRF, 260mA	Murata	CGJ3E2C0G1H331J080AA
R1	2.4K Ω	RES, 0603, 1%, 1/10W	Panasonic	ERJ3EKF2401V
R3	680 Ω	RES, 0603,1%, 1/10W	Panasonic	ERJ3EKF6800V
L6	900 nH	IND, 1008, 10%, 1008AF-901X	Coilcraft	022-28-8021
J1-2	75 Ω	N-TYPE MALE, PANEL MOUNT	Pasternack	PE4504
J3	2 pin 0.1" RA	Molex SMT connector	Molex	022-28-8021
R2, R4-5, C1-2, C5-6, C7-8, L1, L5	n/a	Do Not Insert	N/A	N/A
PH 4-40	4-40, 0.25",	Pan Head Screw w/ lock washer	various	
SH 4-40	4-40, 0.25",	Socket Head Screw	various	
	Cut to 0.25" x 0.4"	Indium foil 1"x1" x 0.004"	Indium Corp	IND4HSD004
Heatsink	Aluminum	Heatsink for 62 mil board	TriQuint	1094050

Notes:
1. Output source degeneration inductor must be rated for 650mA min for I_{DD} flowing through RF output devices

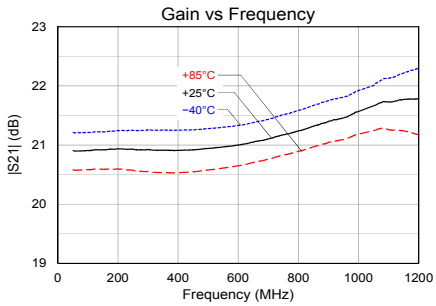
Typical Performance – TAT8804D1H-EB

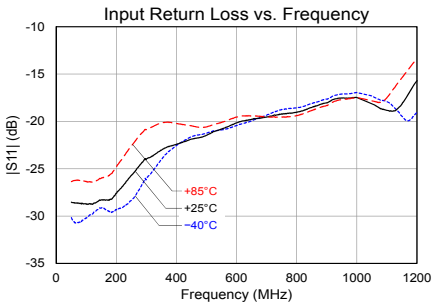
Test conditions unless otherwise noted: V_{DD} = +12 V, Heatsink Temp. = +35 °C, $Z_{In/Out}$=75 Ω using evaluation board EB
Includes input and output balun/transformer losses of tuned application circuit,

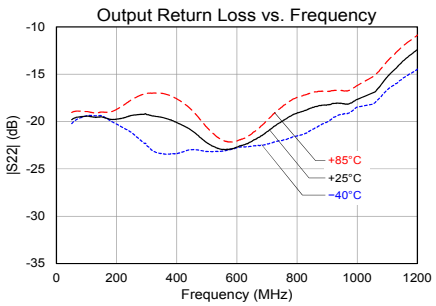
Parameter	Conditions	Typical Value				Units
Frequency		50	550	1003	1200	MHz
Gain	Ptest = −20 dBm	21.2	21.1	21.3	21.5	dB
Input Return Loss		25	20	17	16	dB
Output Return Loss		20	19	17	12	dB
CSO	79 Ch. NTSC + 75 Ch. QAM, −6 dB offset, EQ Vout = +58 dBmV with 15.6 dB tilt	−73	−78			dBc
CTB		−79	−82			dBc
XMOD		−65	−62			dBc
CCN		64	66			dB
CIN		64	66			dB
Output P1dB		+34.2	+35.2	+35	+31.4	dBm
Output IP3	Pout = +17 dBm / tone, Δf = 50 MHz		+55	+50	+45.5	dBm
Noise Figure		5.8	2.5	3	3.3	dB
Current (I_{DD})		650				mA

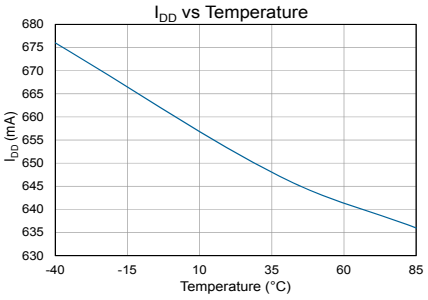
Performance Plots – TAT8804D1H-EB

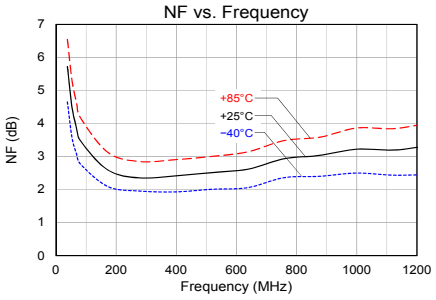
Test conditions unless otherwise noted: V_{DD} = +12 V, Heatsink Temp. = +35 °C, Z_0 = 75 Ω

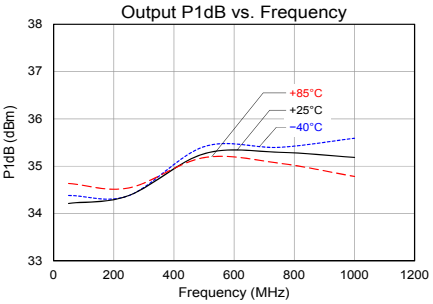






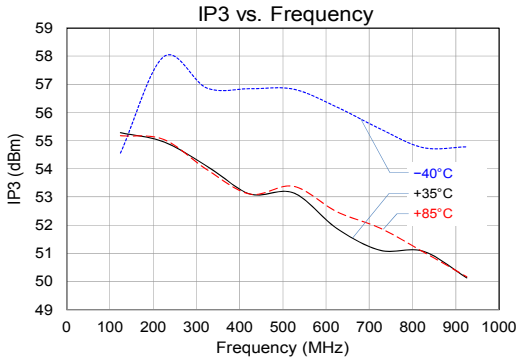


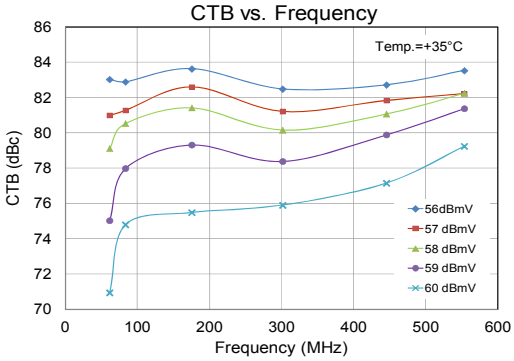


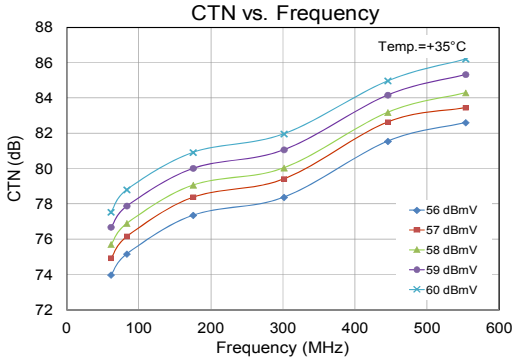


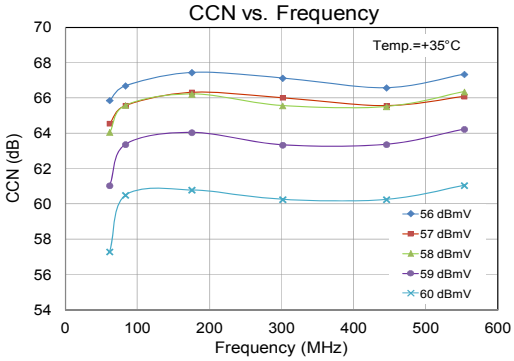
Performance Plots – TAT8804D1H-EB

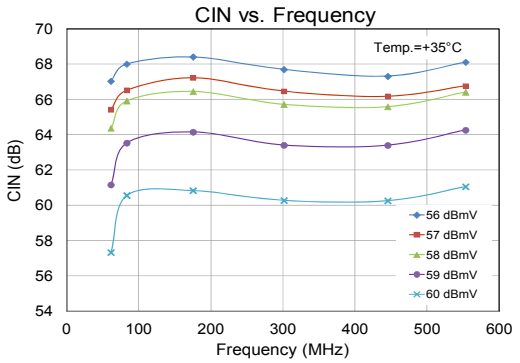
Test conditions unless otherwise noted: V_{DD} = +12 V, Heatsink Temp. = +35 °C
79 Chan. NTSC + 75 Chan. QAM (−6 dB offset), EQ Vout = +56 to +60 dBmV with 15.6 dB tilt

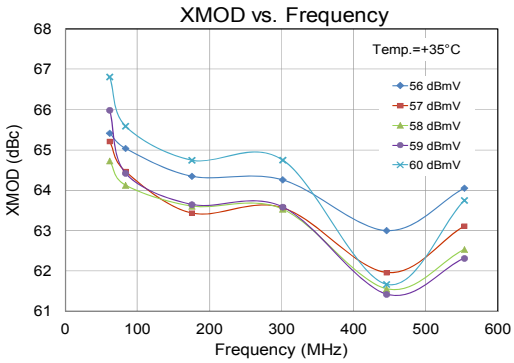


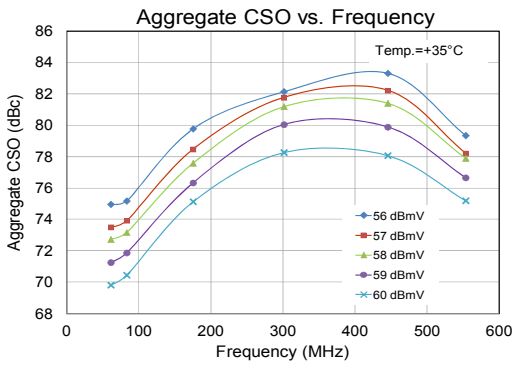








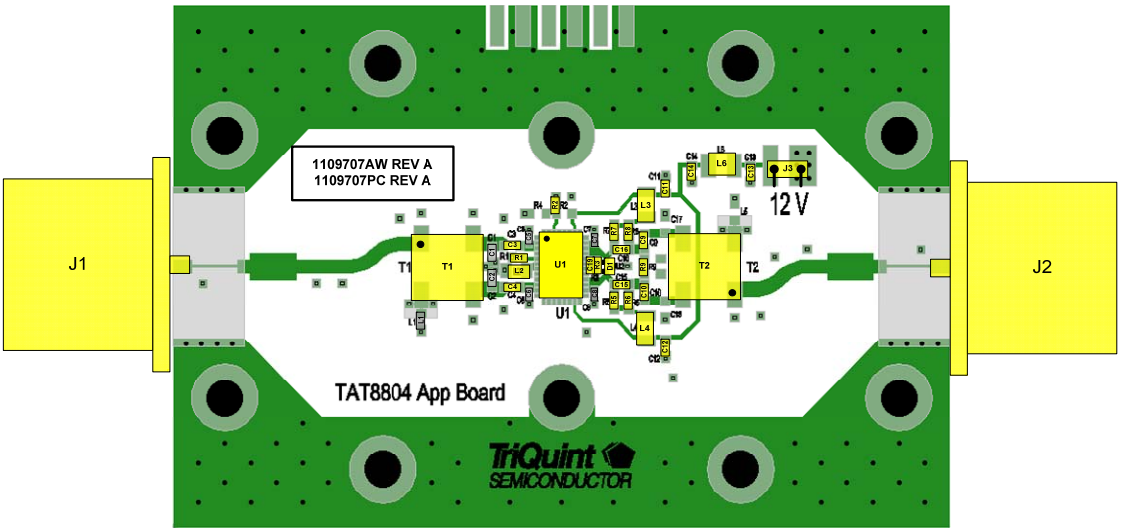


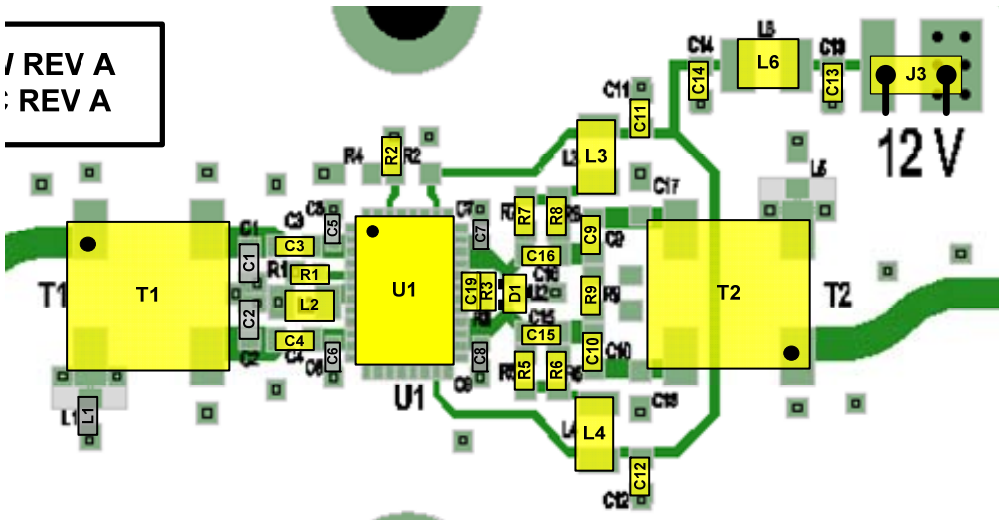


TAT8804D1H-EBP Evaluation Board (With VSWR & Overdrive Protection)

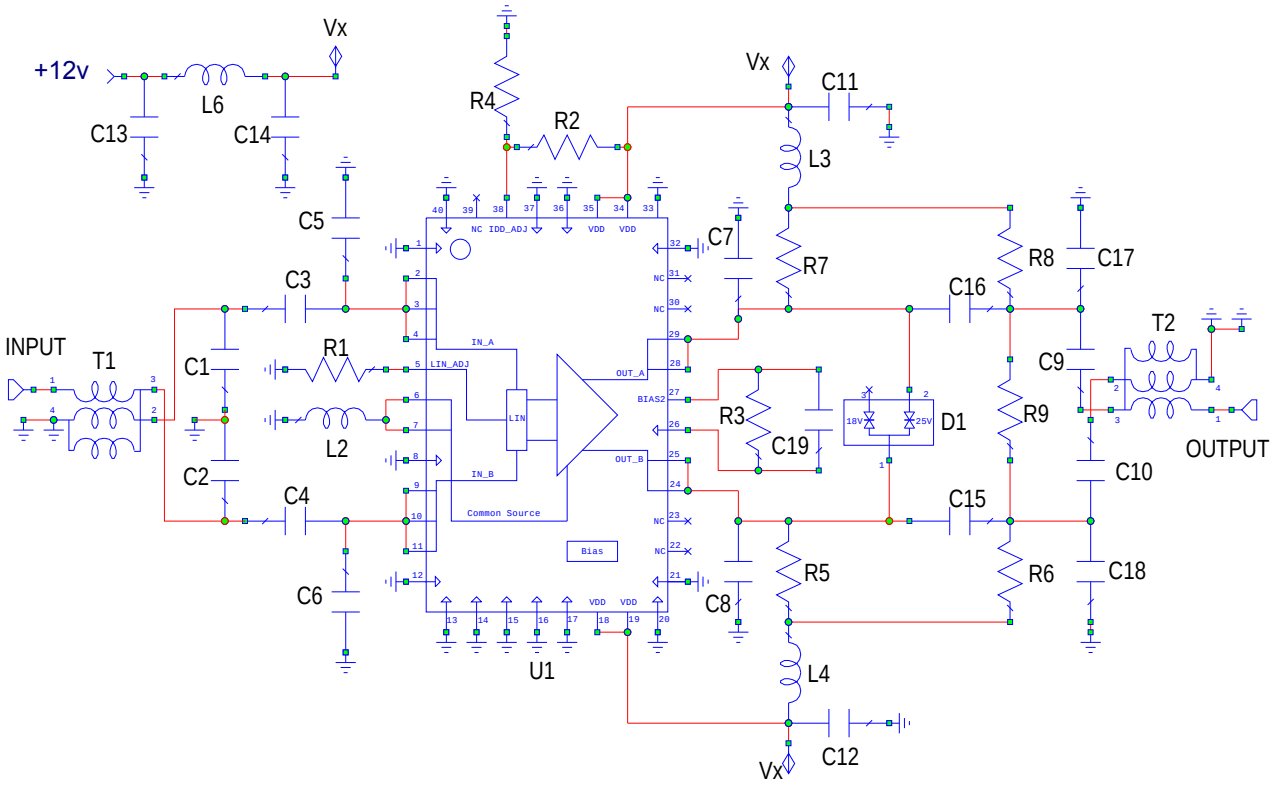
An RF overdrive situation exists if the tilt and pads commonly used before an output doubler are set to low levels during system turn up. Normally such overdrive is not a problem except when the output coax is not terminated. A full reflection at worst case phase may damage unprotected and overdriven amplifiers.

An output protection scheme has been worked out for cases where customers cannot ensure that input RF overdrive and full reflections from the output coaxial network will not simultaneously occur. The scheme works by adding additional protection elements to the TAT8804 application circuit and in conjunction with the nominal 2.5 to 3.0 dB loss from output couplers, power inserters, and diplexer filters present in nearly all actives today. The circuit below protects the TAT8804 for an input +44 dBmV/ch FLAT (79 Ch. NTSC+ 75 Ch. QAM at -6 dB offset) condition and a full reflection of any phase after a 3 dB output loss. The inclusion of additional protection elements to this application circuit results in a small degradation in output performance. For more detailed discussion of this application, consult TriQuint Applications Engineering.





TAT8804D1H-EBP Schematic (With VSWR & Overdrive protection)

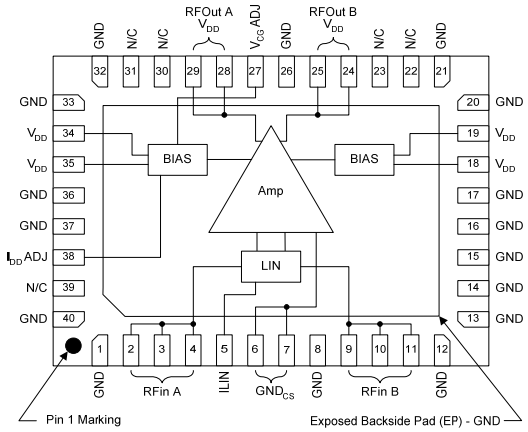


Bill of Material – TAT8804D1H-EBP (With VSWR & Overdrive protection)

Reference Des.	Value	Description	Manuf.	Part Number
PCB	Rev A	PCB TAT8804 - EVB Protected	TriQuint	1109707
U1	n/a	TAT8804D1H Sample	TriQuint	TAT8804D1H
D1	25V	ESD Clamp diode	TriQuint	TQP200002
T1-2	1:1 BALUN, 75 Ω	MABA-009210-CT1760	MACOM	MABA-009210-CT1760
C3-4	270pF	CAP, 0603, 5%, 50V, NPO	TDK	C1608C0G1H271J080AA
C9-10	330 pF	CAP, 0603, 5%, 50V, NPO	TDK	CGJ3E2C0G1H331J080AA
C11-12	0.01 uF	CAP, 0603, 10%, 50V, X7R	TDK	C1608X7R1H103J
C13-14	0.1 uF	CAP, 0603, 10%, 50V, X7R	TDK	C1608X7R1H104K
C15-16	56 pF	CAP, 0603, 10%, 50V, NPO	TDK	CGJ3E2C0G1H560J080AA
C19	4.7uF	CAP, 0603, 10%, 10V, Y5V	Murata	GRM188F51A475ZE20D
R1	2.4K Ω	RES, 0603, 1%, 1/10W	Panasonic	ERJ3EKF2401V
R3	680 Ω	RES, 0603,1%, 1/10W	Panasonic	ERJ3EKF6800V
R5, R7	2.2 ohm	RES, 0603, 1%, 1/16W	Panasonic	ERJ3GSYJ2R2H
R6, R8	5.1 ohm	RES, 0603, 1%, 1/10W	Panasonic	ERJ-3GSYJ5R1V
R9	475 Ω	RES, 0603, 1%, 1/10W	Panasonic	ERJ3EKF4750H
L2[1]	680 nH	IND, 0805, 5%, 355 MHz SRF, 660mA	Coilcraft	0805AF-681XJR
L3-4	500 nH	IND, 1206, 10%, 270 MHz SRF, 260mA	Murata	CGJ3E2C0G1H331J080AA
L6	900 nH	IND, 1008, 10%, 1008AF-901X	Coilcraft	1008AF-901X
R2, R4, C1-2, C5-8, C17-C18, L1, L5	n/a	Do Not Insert	N/A	N/A
J1-2	75 Ω	N-TYPE MALE, PANEL MOUNT	Pasternack	PE4504
J3	2 pin 0.1" RA	Molex SMT connector	Molex	022-28-8021
PH 4-40	4-40, 0.25”,	Pan Head Screw w/ lock washer	various	
SH 4-40	4-40, 0.25”,	Socket Head Screw	various	
	Cut to 0.25" x 0.4"	Indium foil 1"x1" x 0.004"	Indium Corp	IND4HSD004
Heatsink	Aluminum	Heatsink for 62 mil board	TriQuint	1094050

Notes:
1. Output source degeneration inductor must be rated for 650mA min for I_{DD} flowing through RF output devices

Pin Configuration and Description

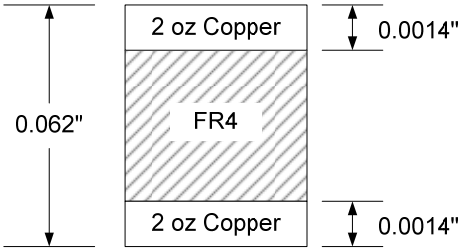


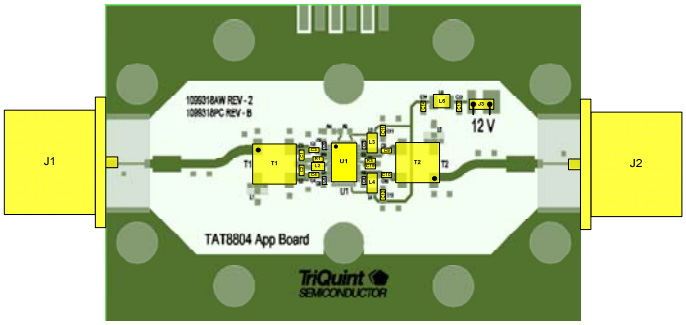
Pin No.	Label	Description
2-4	RFin A	RF in A, requires external Balun. External DC Block required.
9-11	RFin B	RF in B, requires external Balun. External DC Block required.
5	ILIN	Current adjust pin to optimize Linearity
28-29	RFout A/V_{DD}	RF Out A and supply voltage, external DC block & Balun required.
24-25	RFout B/V_{DD}	RF Out B and supply voltage, external DC block & Balun required.
18-19, 34-35	V_{DD}	Bias controller supply voltage
27	V_{CG} ADJ	Common Gate adjustment to optimize common gate amplifier bias voltage (normally open)
38	I_{DD} ADJ	I_{DD} current control (normally open), pulling to gnd lowers I_{DD} current
1,8,12-17, 20-21, 26, 32-33, 36-37, 39-40	GND	RF/DC Ground Connection
6-7	GND_{CS}	Common Source ground degeneration, grounded with inductor. Full DC current flows through this pin, inductor must handle total I_{DD} current.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
22-23, 30-31, 39	N/C	No connection

Evaluation Board PCB Information

EB & EBP EVB PCB Material and Stack-up

Board Material: 0.062" FR4 , ε_r=4.25
Plating: 2oz Copper
Board Dimension: 3" x 2"

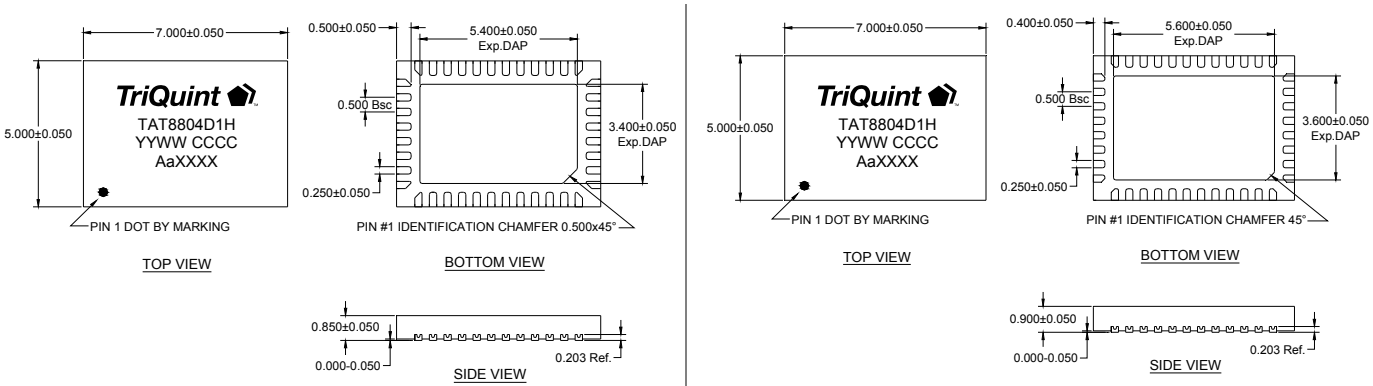




Package Marking and Dimensions

Marking: Part Number – TAT8804D1H
Date Code – YYWW
Country Code - CCCC
Lot code – AaXXXX

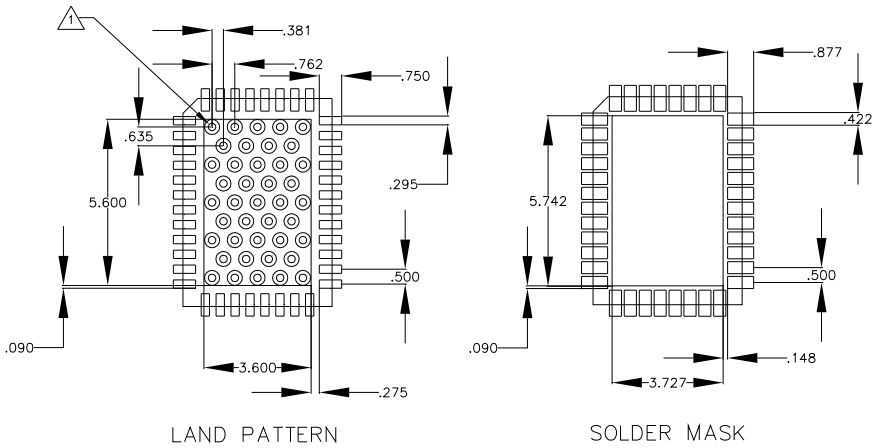
The TAT8804D1H may be supplied in either of the following compatible packages.



Notes:

1. Dimension and tolerance formats conform to ASME Y14.4M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 2 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Place mounting screws near the part to fasten a back side heat sink.
6. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
7. Ensure that the backside via region makes good physical contact with the heat sink.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥250 volts to < 500 volts
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥1000 volts
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with J-STD-020, Lead free solder, (260° maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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