

GENERAL DESCRIPTION

C1003 is a poly gate CMOS integrated circuit which is designed to drive an Electroluminescence Lamp (EL) to light with flashing. It supplies three input pins to control three ELs or four ELs to flash, which is selected by OP3. C1003 also can flash with two functions: one direction or bi-directions flash which is selected by OP2. C1003 can flash during six cycles then full on during three cycles, or all flash during 9 cycles which is decided by OP1. The flash time can be decided by built-in oscillator. Positive and negative triggers are available.

C1003 series product can be widely used in the back light of digital watch, analogy watch, calculator etc.

FUNCTIONS

- Power supply: 1.5V ~ 4.5V
- DC to AC conversion by a few external components
- Built-in RC oscillator
- Three internal function control inputs:
 OP1: flashing mode control
 OP2: flashing in one or bi-directions control
 OP3: 3 or 4 ELS flashing control

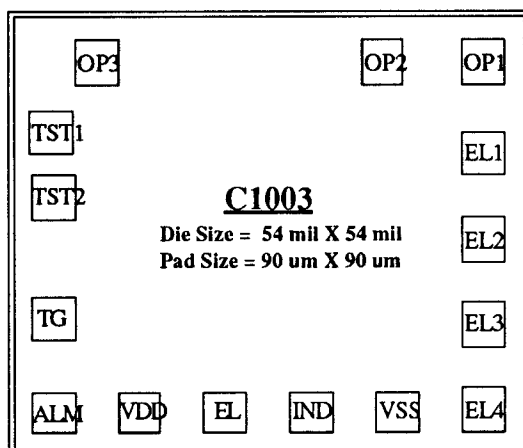
FEATURES

- Economical solution for EL display
- CMOS process with low power consumption and high stability
- Min. external components application.

FUNCTION CONTROL TABLE

Pin Name	Function Description
OP1	When OP1 is open, C1003 flashes 6 cycles and keeps on 3 cycles then turns off; when it is connected to Vss, C1003 will flashed 9 cycles then off.
OP2	When OP2 is open, C1003 flashes in one-direction; when it is connected to Vss, C1003 flashed in bi-direction
OP3	When OP3 is open, there are 3 ELs output in C1003 when it is connected to Vss, there are 4 ELs output in C1003

PAD DIAGRAM



PIN	DESCRIPTION
TST1, TST2	Test Pins
TG	Trigger input pin active at high
ALM	Trigger input pin active at low
VDD	Positive power supply
EL	DC to AC converter output
IND	DC to AC converter output
Vss	Negative power supply
EL1 ~ EL4	EL output control pins
OP1 ~ OP3	Option pins for flash function

Note: Substrate should be connected to VDD

ABSOLUTE MAXIMUM RATINGS

(Ta = 25 °C)

Parameter	Symbol	Limits
Power supply voltage range	V _{DD} - V _{SS}	- 0.3V to + 5.0V
Input voltage range	V _{in}	V _{SS} - 0.3 to V _{DD} + 0.3
Operating temperature range	T _A	0 to +60°C
Storage temperature range	T _{stg}	-40 to +70°C

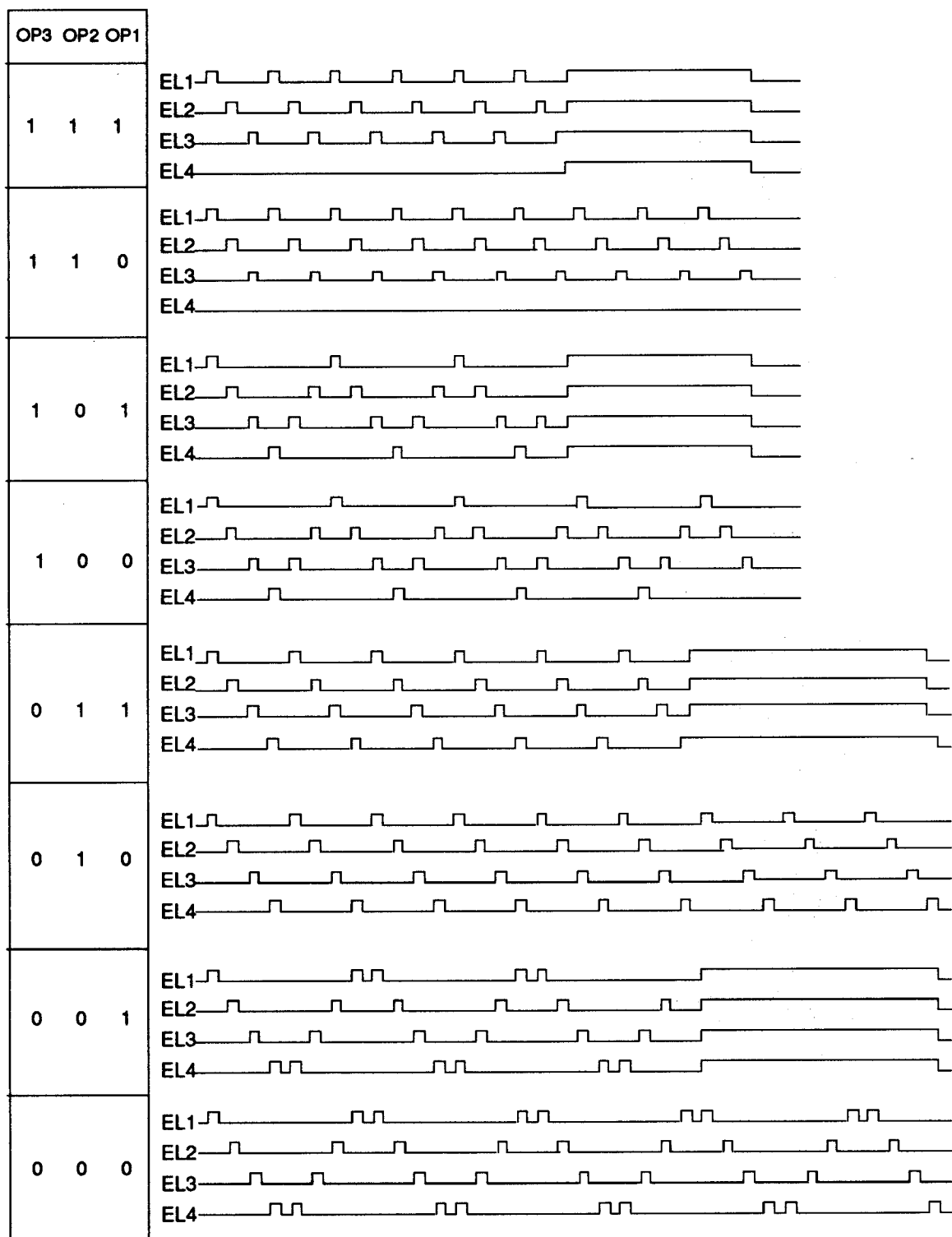
DC ELECTRICAL CHARACTERISTICSUnless otherwise specified, Ta = 25°C, V_{DD} = 3.0V, V_{SS} = 0V

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating voltage range	V _{DD}	1.3	3.0	4.5	V	—
Standard current	I _{DD}	--	0.1	1	μA	*no load
IND Output Source Current	I _{OH1}	3.0	4.6	--	mA	V _{OH} = 0.8V
EL Output Source Current	I _{OH2}	1.0	2.2	--	mA	V _{OH} = 0.8V
IND Output Sink Current	I _{OL1}	10	20	--	mA	V _{OL} = 0.8V
EL Output Sink Current	I _{OL2}	2.0	4.0	--	mA	V _{OL} = 0.8V
Oscillator Starting Voltage	V _{STP}	1.3	--	--	V	—
Oscillator Frequency	F _{osc}	400	500	670	KHZ	V _{DD} = 3.0V

Unless otherwise specified, Ta = 25°C, V_{DD} = 1.5V, V_{SS} = 0V

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating voltage range	V _{DD}	1.3	1.5	4.5	V	—
Standard current	I _{DD}	--	0.1	1	μA	*no load
IND Output Source Current	I _{OH1}	0.5	0.8	--	mA	V _{OH} = 0.8V
EL Output Source Current	I _{OH2}	0.2	0.4	--	mA	V _{OH} = 0.8V
IND Output Sink Current	I _{OL1}	3.0	10	--	mA	V _{OL} = 0.8V
EL Output Sink Current	I _{OL2}	0.3	0.8	--	mA	V _{OL} = 0.8V
Oscillator Starting Voltage	V _{STP}	1.3	--	--	V	—
Oscillator Frequency	F _{osc}	400	500	670	KHZ	V _{DD} = 1.5V

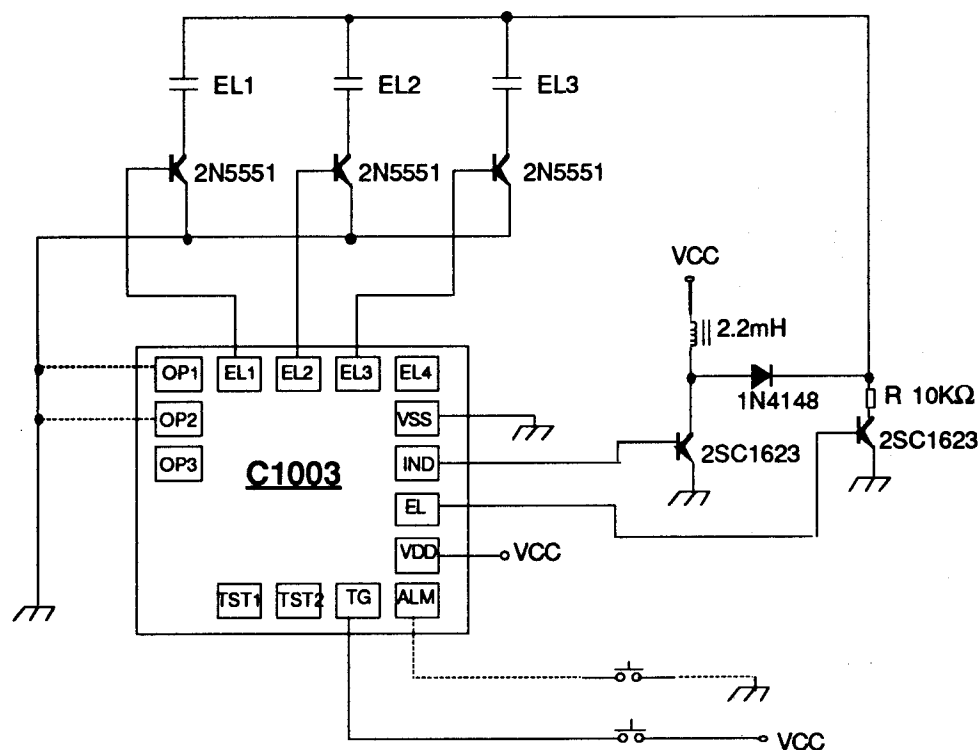
C1003 Waveform



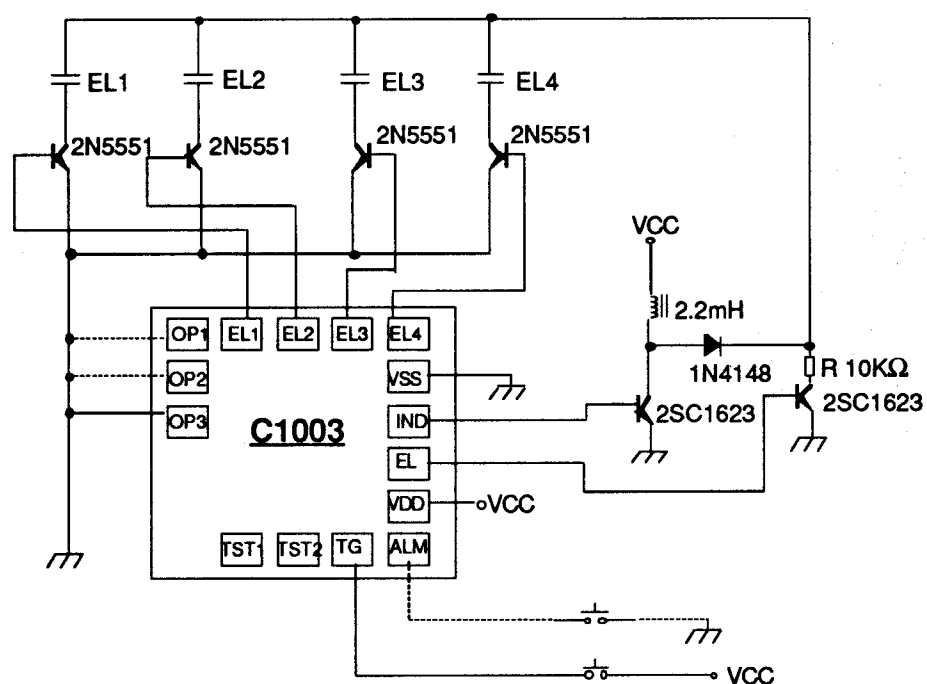
Note : 0 = VSS; 1 = Open

APPLICATION CIRCUITS

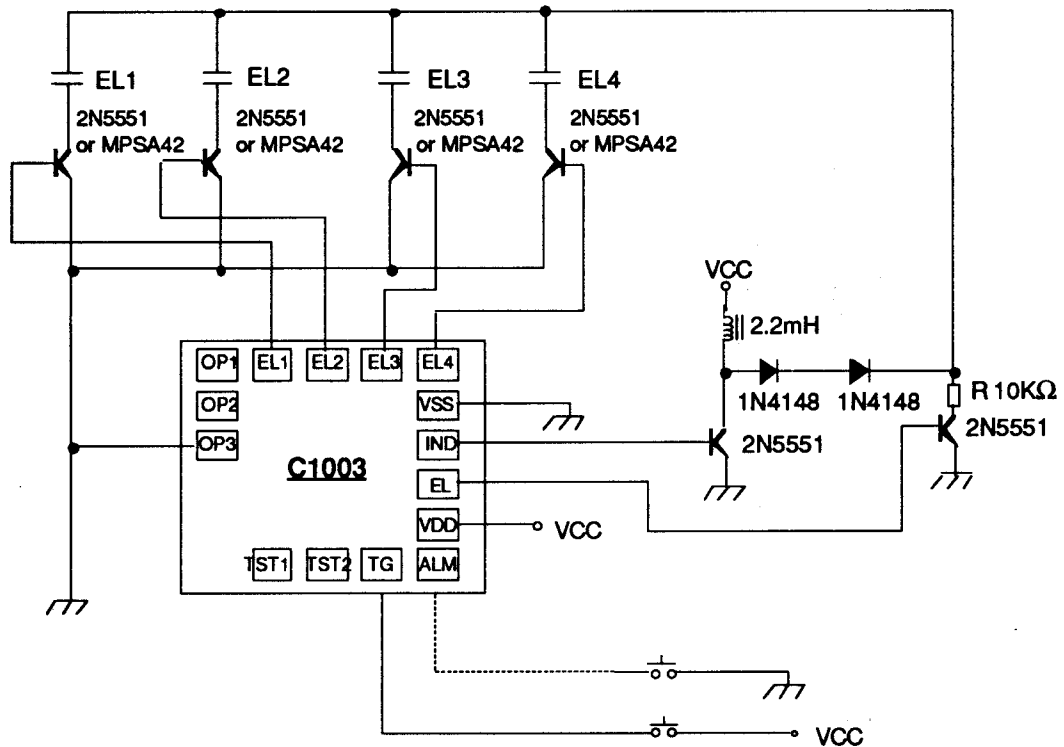
1) 3 ELS output with build-in flash time



2) 4 ELS output with build-in flash time



3) 4 ELS output with build-in flash time and super brightness circuit



PCB LAYOUT RULE

1. VDD and VSS must be separate by different path for routing between high voltage signal and IC. Like shown below.
2. Between VDD and VSS nearest IC pre-placement a cap. space for reduce noise interference. The cap value may be $0.1\mu\text{F}$ or $0.2\mu\text{F}$.
3. If there is a crystal must be far away from high voltage signal.
4. If space is enough please placing VSS signal between high voltage signal and digital signal.

