

#### FEATURES

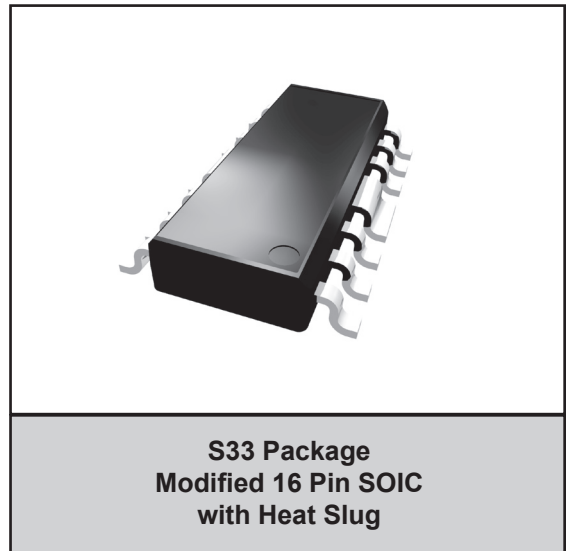
- 12 dB Gain
- +8 V Nominal Supply Operation
- High Linearity
- Low Noise Figure: 2.7 dB (typ.)
- Characterized at +34 dBmV output power
- Wide Band Operation to Beyond 1 GHz
- -40 to +85°C
- RoHS-Compliant Package
- Heat Slug Package for enhanced Thermal Management

#### APPLICATIONS

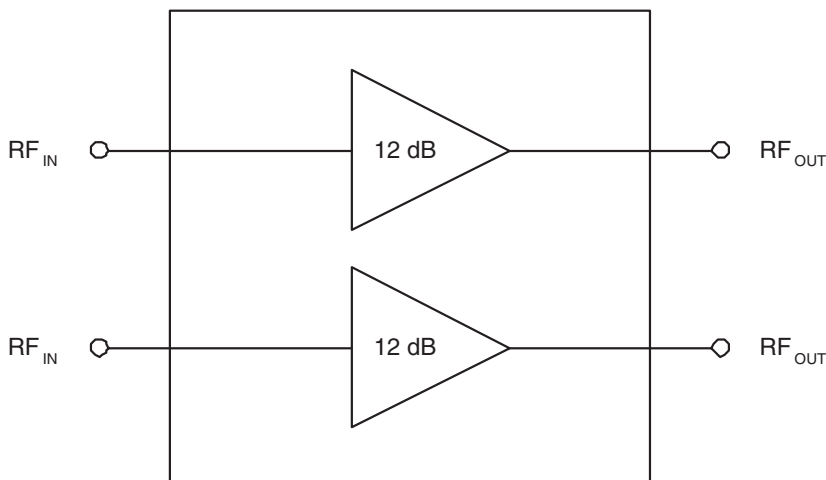
- Driver Amplifier
- CATV - Distribution / Drop Amplifiers
- Set Top Boxes
- Home Gateway

#### PRODUCT DESCRIPTION

The ABA3101 is a monolithic IC intended for use in applications requiring high linearity, such as Cellular Telephone Base Station Driver Amplifiers, CATV Fiber Receiver and Distribution Amplifiers, CATV Drop Am-



plifiers, CATV Set Top Boxes, and Home Gateways. Offered in a modified 16 lead surface mount SOIC package with a heat slug, it is well suited for use in amplifiers where small size, reduced component count, and high reliability are important.



**Figure 1: Block Diagram**

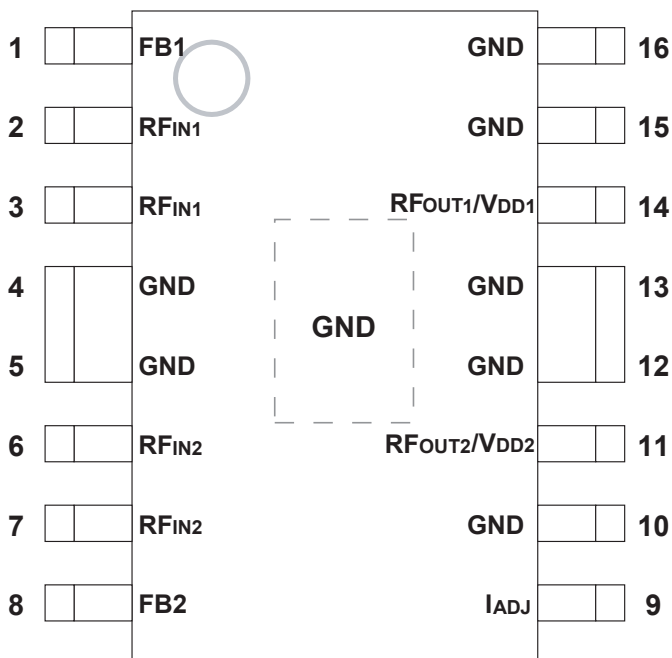


Figure 2: Pin Out

Table 1: Pin Description

| PIN | NAME              | DESCRIPTION               | PIN | NAME                                 | DESCRIPTION                       |
|-----|-------------------|---------------------------|-----|--------------------------------------|-----------------------------------|
| 1   | FB1               | Feedback for Amplifier A1 | 9   | IADJ                                 | Current Adjust                    |
| 2   | RF <sub>IN1</sub> | RF Input of Amplifier A1  | 10  | GND                                  | Ground                            |
| 3   | RF <sub>IN1</sub> | RF Input of Amplifier A1  | 11  | RF <sub>OUT2</sub> /V <sub>DD2</sub> | RF Output and VDD of Amplifier A2 |
| 4   | GND               | Ground                    | 12  | GND                                  | Ground                            |
| 5   | GND               | Ground                    | 13  | GND                                  | Ground                            |
| 6   | RF <sub>IN2</sub> | RF Input of Amplifier A2  | 14  | RF <sub>OUT1</sub> /V <sub>DD1</sub> | RF Output and VDD of Amplifier A1 |
| 7   | RF <sub>IN2</sub> | RF Input of Amplifier A2  | 15  | GND                                  | Ground                            |
| 8   | FB2               | Feedback for Amplifier A2 | 16  | GND                                  | Ground                            |

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

| PARAMETER                            | MIN | MAX  | UNIT |
|--------------------------------------|-----|------|------|
| Analog Supply (pins 11, 14)          | 0   | +12  | VDC  |
| RF Power at Inputs (pins 2, 3, 6, 7) | -   | +15  | dBm  |
| Storage Temperature                  | -65 | +150 | °C   |
| Soldering Temperature                | -   | 260  | °C   |
| Soldering Time                       | -   | 5    | sec  |

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 1, 2, 3, 6, 7 and 8 should be AC-coupled. No external DC bias should be applied.
2. Pin 9 should be AC-grounded. No external DC bias should be applied.

Table 3: Operating Ranges

| PARAMETER                             | MIN  | TYP | MAX  | UNIT |
|---------------------------------------|------|-----|------|------|
| RF Input / Output Frequency           | 50   | -   | 1000 | MHz  |
| Analog Supply: $V_{DD}$ (pins 11, 14) | +4.5 | +8  | +9   | VDC  |
| Case Temperature: $T_C$               | -40  | -   | +100 | °C   |

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

**Table 4: Electrical Specifications**  
**(T<sub>A</sub> = +25 °C, V<sub>DD</sub> = + 8 VDC, Test System = 75Ω)**

| PARAMETER                                              | MIN | TYP               | MAX               | UNIT | COMMENTS                                        |
|--------------------------------------------------------|-----|-------------------|-------------------|------|-------------------------------------------------|
| Gain at 1 GHz                                          | 12  | 12.5              | 13.2              | dB   | at 1 GHz                                        |
| Noise Figure                                           | -   | 2.5<br>2.7<br>3.2 | 3.5<br>3.5<br>3.5 | dB   | 50 - 550 MHz<br>550 - 800 MHz<br>800 - 1002 MHz |
| Input / Output Return Loss                             | 20  | 22                | -                 | dB   |                                                 |
| CSO <sup>(1)</sup>                                     | -   | -70               | -69               | dBc  |                                                 |
| CTB <sup>(1)</sup>                                     | -   | -72               | -70               | dBc  |                                                 |
| 2nd Order Output Intercept Point (OIP2) <sup>(2)</sup> | -   | +70               | -                 | dBm  |                                                 |
| 3rd Order Output Intercept Point (OIP3) <sup>(2)</sup> | -   | +40               | -                 | dBm  |                                                 |
| Thermal Resistance                                     | -   | -                 | 10                | °C/W |                                                 |
| Current Consumption <sup>(3)(4)</sup>                  | 200 | 212               | 225               | mA   |                                                 |

**Notes:**

(1) 112 channels, +34 dBmV per channel (measured at the output), 3 dB tilt, 6 MHz channel spacing.

(2) Two tones: 500 MHz and 501 MHz, +4 dBm per tone.

(3) Characterized with I<sub>ADJ</sub> pin floating.

(4) Adding a shunt resistor from the I<sub>ADJ</sub> pin to ground will lower current, but with some decrease in performance.

## PERFORMANCE DATA

Figure 3: Typical Gain (S21) vs. Frequency

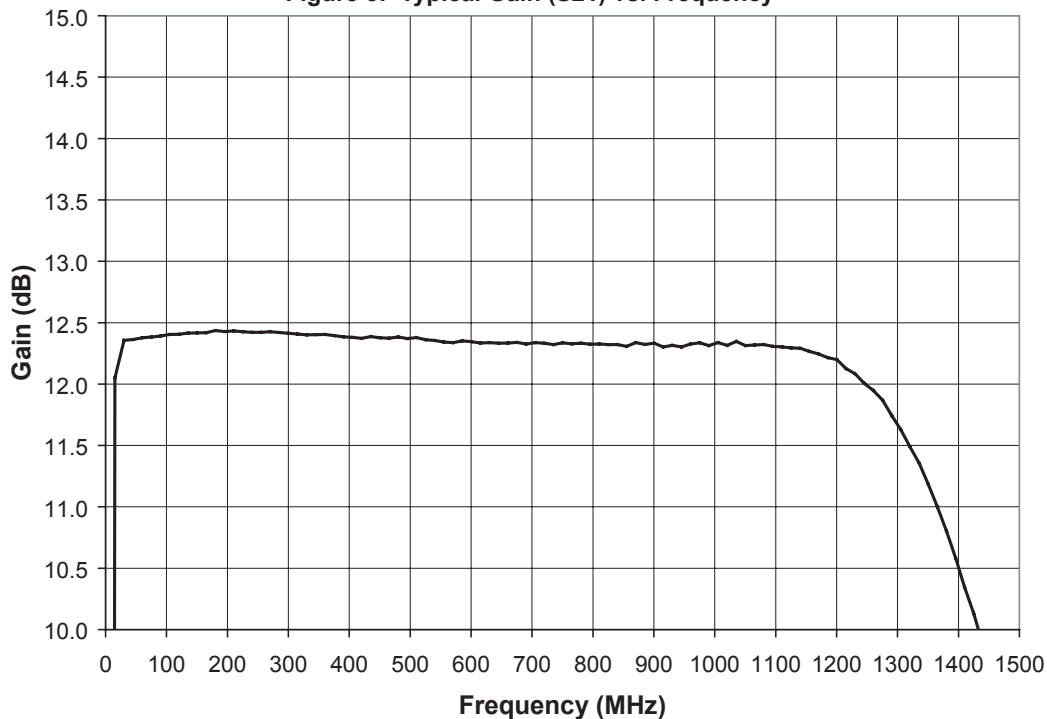


Figure 4: Typical Input and Output Return Loss (S11 and S22) vs. Frequency

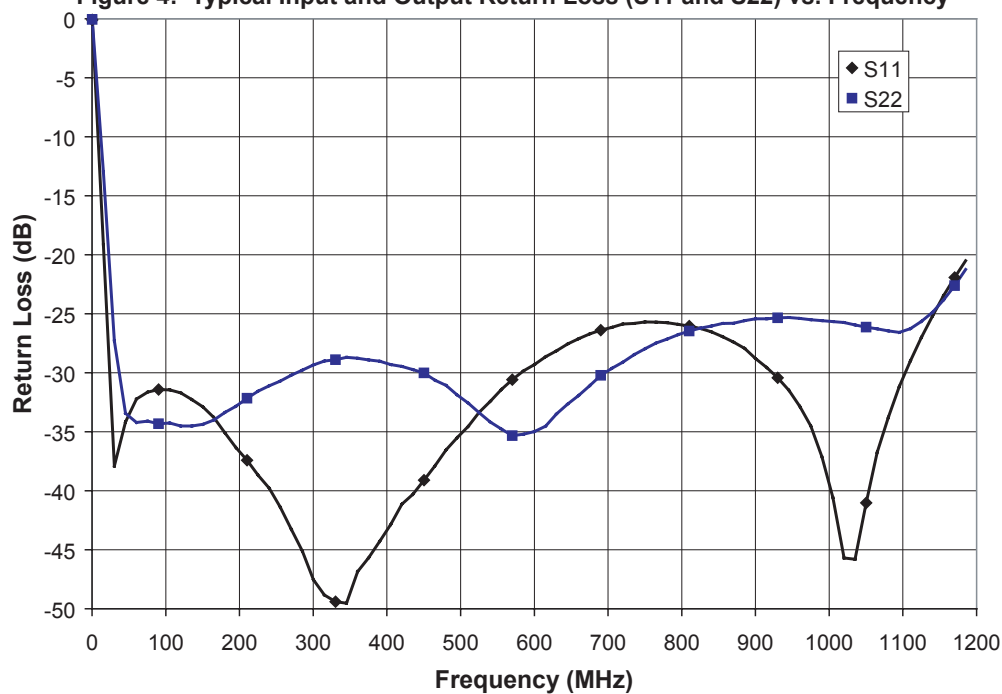


Figure 5: Typical Isolation (S12) vs. Frequency

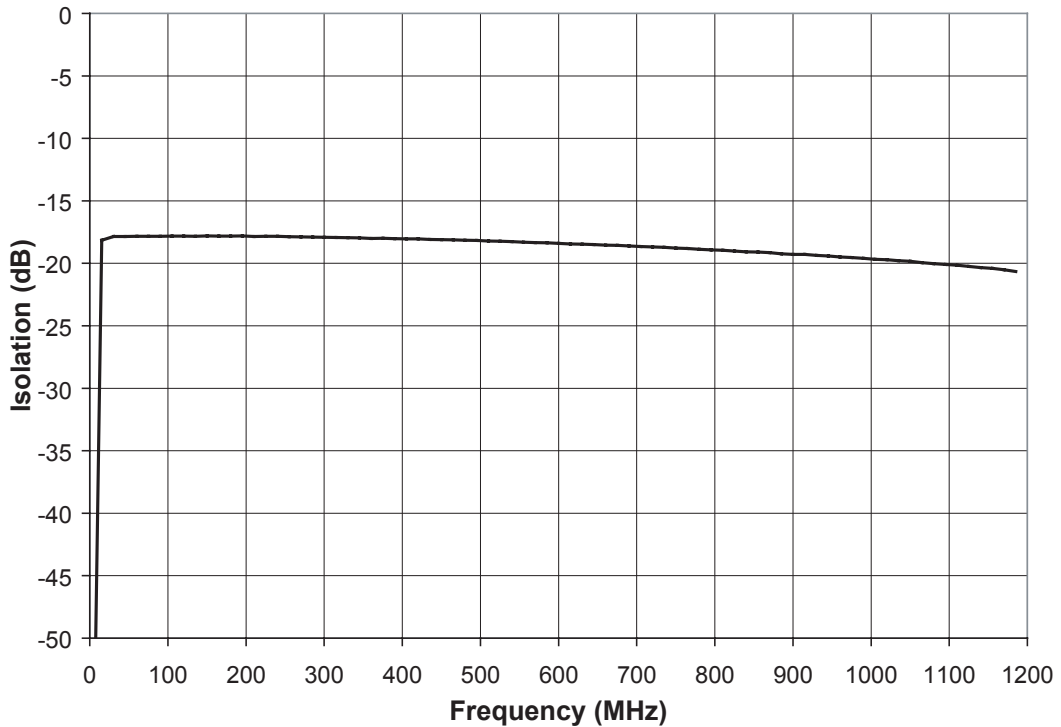
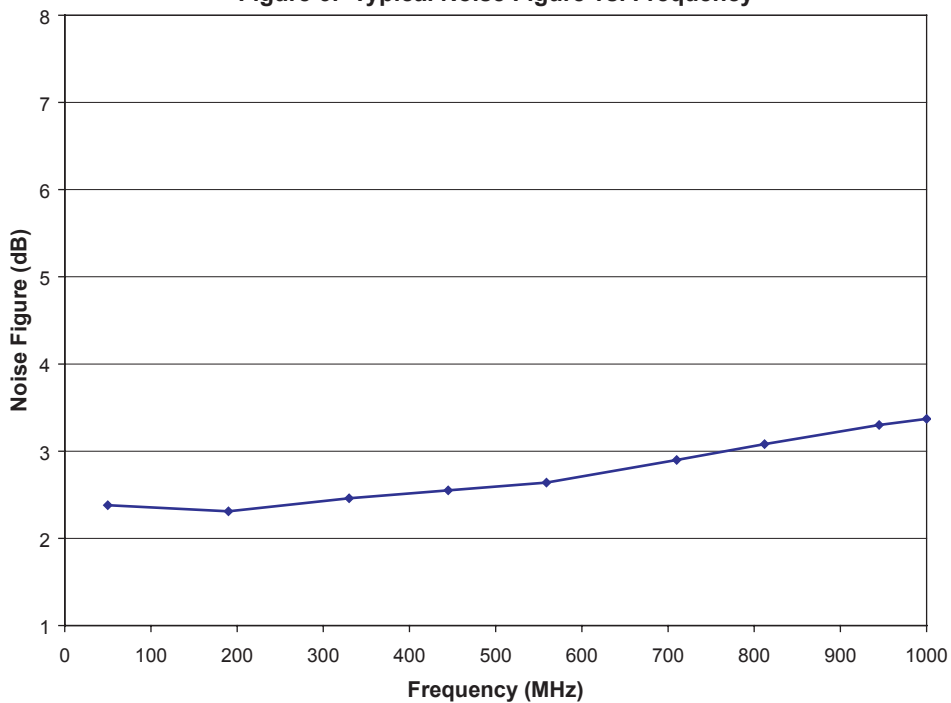
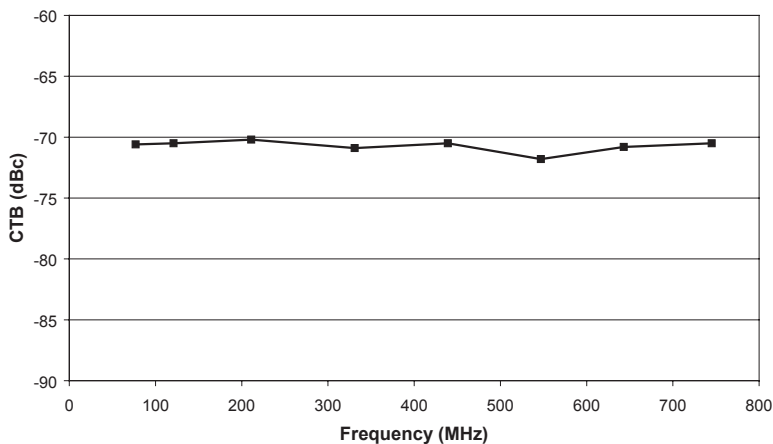
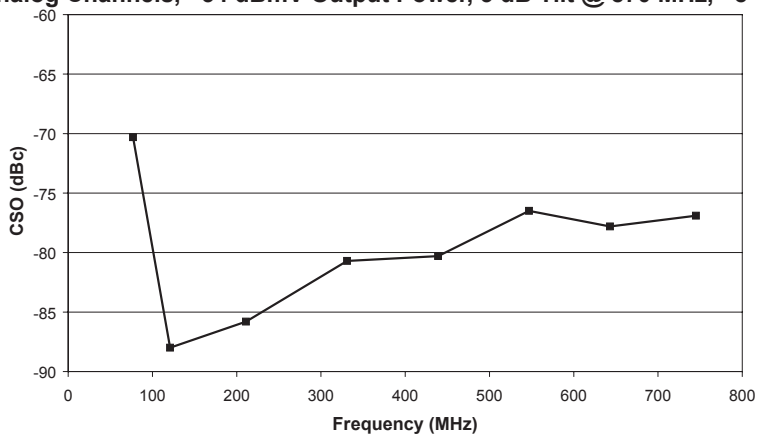
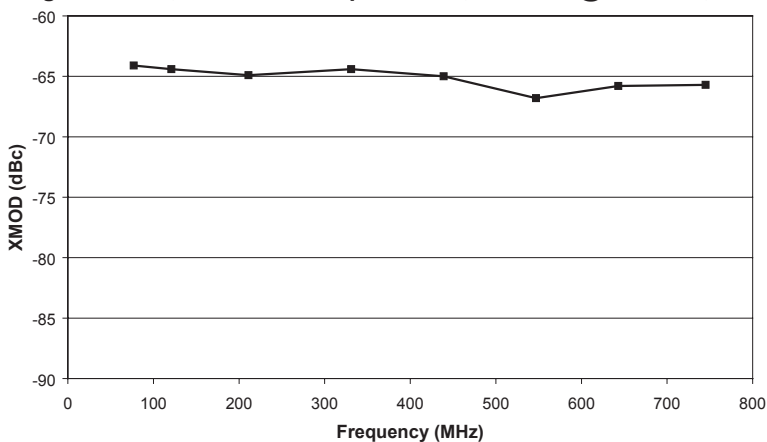
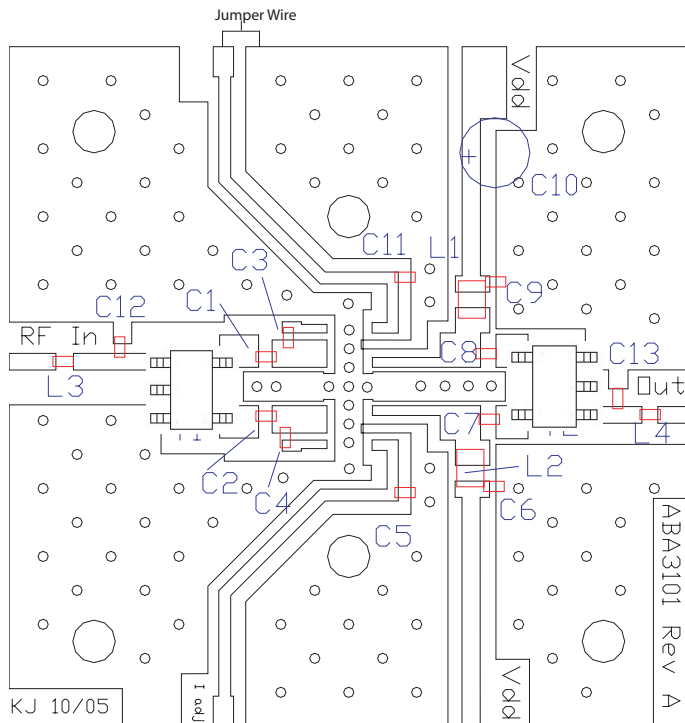


Figure 6: Typical Noise Figure vs. Frequency



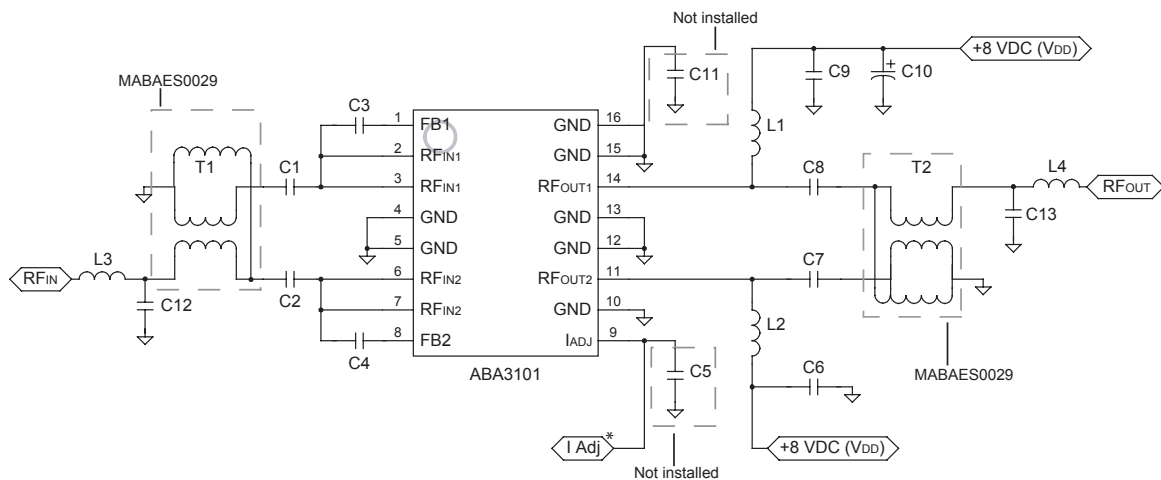
**Figure 7: CTB vs. Frequency****112 Analog Channels, +34 dBmV Output Power, 3 dB Tilt @ 870 MHz, +8 V, 200 mA****Figure 8: CSO vs. Frequency****112 Analog Channels, +34 dBmV Output Power, 3 dB Tilt @ 870 MHz, +8 V, 200 mA****Figure 9: XMOD vs. Frequency****112 Analog Channels, +34 dBmV Output Power, 3 dB Tilt @ 870 MHz, +8 V, 200 mA**

## APPLICATION INFORMATION



**Figure 10: Evaluation Board Layout**

*Note: Pin 16 of the ABA3101 is connected to ground internally. Do not apply voltage to the  $V_{ADJ}$  input of the evaluation board.*



**Figure 11: Evaluation Board Schematic**

*Note:*

*\* connecting a resistor from  $I_{ADJ}$  to ground lowers current; normal operation is with  $I_{ADJ}$  floating.*

Table 5: Evaluation Board Parts List

| ITEM          | DESCRIPTION                    | QTY | VENDOR                          | VENDOR PART NUMBER        |
|---------------|--------------------------------|-----|---------------------------------|---------------------------|
| C1-C4, C6, C9 | 0.01uF CHIP CAP.               | 6   | MURATA                          | GRM39X7R1103K25V          |
| C7, C8        | 330 pF CHIP CAP.               | 2   | MURATA                          | GRM39COG471J25V           |
| C10           | 47 uF ELEC. CAP.               | 1   | DIGI-KEY CORP                   | P5275-ND                  |
| C5, C11       | (not installed)                |     |                                 |                           |
| C12, C13      | 1.0 pF CHIP CAP.               | 2   | MURATA                          | GRM1885C1H1ROCZ01B        |
| L1, L2        | 470 nH CHIP INDUCTOR           | 2   | MURATA                          | LQH1WA47KONOO03/4052      |
| L3, L4        | 5.6 nH CHIP INDUCTOR           | 2   | TOKO                            | PTL2012-F5N6C             |
| CONNECTORS    | 75 $\Omega$ N MALE PANEL MOUNT | 2   | PASTERNAK ENTERPRISES           | PE4504                    |
| T1, T2        | BALUN                          | 2   | MACOM                           | MABAES0029 <sup>(4)</sup> |
|               | PCB                            | 1   | STANDARD PRINTED CIRCUITS, INC. |                           |

## Notes:

1. "N" Connector center pin should be approximately 80 mils in length.

2. Connector tabs must be reduced by 150 mils.

3. Device must be soldered on PC board.

(4) MABAES0029 is not RoHS compliant. For RoHS, the user should evaluate M/A-COM MABACT0069 balun or other similar replacement.

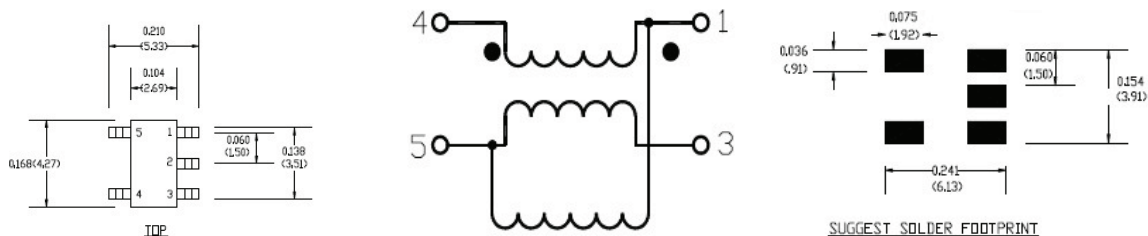
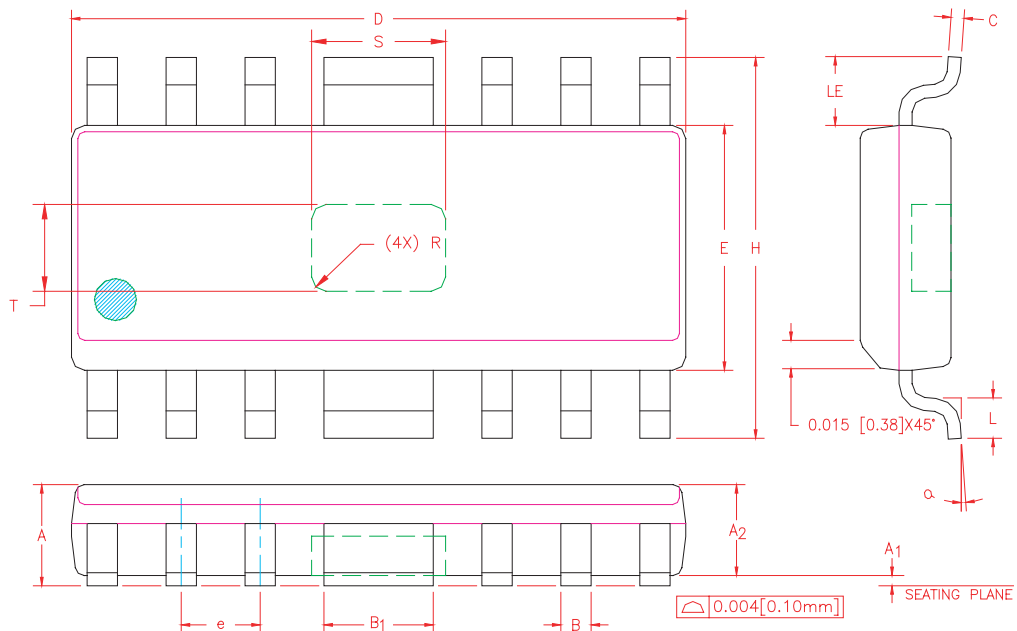


Figure 12: M/A-COM MABAES0029 Balun

## Notes:

1. Consult M/A-COM data sheet for more details.

## PACKAGE OUTLINE



| SYMBOL | INCHES |       | MILLIMETERS |       | NOTE |
|--------|--------|-------|-------------|-------|------|
|        | MIN.   | MAX.  | MIN.        | MAX.  |      |
| A      | 0.058  | 0.068 | 1.47        | 1.73  |      |
| A1     | 0.000  | 0.004 | 0.00        | 0.10  | 7    |
| A2     | 0.054  | 0.065 | 1.37        | 1.65  |      |
| B      | 0.013  | 0.020 | 0.33        | 0.50  |      |
| B1     | 0.062  | 0.070 | 1.58        | 1.78  |      |
| C      | 0.008  | 0.010 | 0.20        | 0.25  | 4    |
| D      | 0.380  | 0.400 | 9.66        | 10.16 | 2    |
| E      | 0.150  | 0.160 | 3.81        | 4.06  | 3    |
| e      | 0.050  | BSC   | 1.27        | BSC   |      |
| H      | 0.226  | 0.244 | 5.74        | 6.20  |      |
| L      | 0.016  | 0.040 | 0.41        | 1.02  |      |
| LE     | 0.030  | —     | 0.76        | —     |      |
| α      | 0°     | 8°    | 0°          | 8°    |      |
| S      | 0.070  | 0.100 | 1.78        | 2.54  | 6    |
| T      | 0.040  | 0.070 | 1.02        | 1.78  | 6    |
| R      | 0.015  | REF.  | 0.38        | REF.  | 6    |

## NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE  $\pm 0.005$  [0.13mm].
5. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.
6. DIMENSIONS "S", "T" AND "R" INDICATE EXPOSED SLUG AREA.
7. A1 STAND OFF IS MEASURED FROM BOTTOM OF HEAT SLUG TO THE SEATING PLANE.

Figure 13: S33 Package Outline - Modified 16 Pin SOIC with Heat Slug

NOTES

**ORDERING INFORMATION**

| ORDER NUMBER  | TEMPERATURE RANGE | PACKAGE DESCRIPTION                    | COMPONENT PACKAGING       |
|---------------|-------------------|----------------------------------------|---------------------------|
| ABA3101RS33P1 | -40 to +100 °C    | RoHS Compliant<br>Modified 16 Pin SOIC | 3,500 piece Tape and Reel |

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