AAm®
Advanced Design
Advanced Microcontroller

Understanding of
ADAM81 Series Architecture

A Guide to

ADAM81P12XX

User's Manual

(V0.8-2010.05)

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0. User's Manual Revision History

8. [V0.8-2010.05]
   → 1.7.3. DC Characteristics (DC Current Value is modified.)

7. [V0.7-2009.11]
   → Code Option Bit Default value define.

6. [V0.6-2009.07]
   → R3FN2 function is modified.

5. [V0.5-2009.07]
   → Code Option Bit Mapping is modified.
   → Internal RC-OSC Spec is modified.

4. [V0.4-2009.02]
   → 12. Voltage Detection Indicator Mode
   12.3. Timming Diagram (VDI RESET mode, Must set (ENST=1))

3. [V0.3-2008.12]
   → 1.7.3. DC Characteristics
   DC Current Value is modified.

2. [V0.2-2008.11]
   → 1.7.3. DC Characteristics
   VOH/VOL Typ. Value is modified as 0.7v <- 0.4v .

1. [V0.1-2008.11]
   → 2.7 Peripheral Registers
   *bit is read-modified operation. (SETR1/CLRR1 instruction)

0. [V0.0-2008.10]
   → 1'st release

1. OVERVIEW

The ADAM81 is the High Speed and Low Voltage operating 8-bit single chip microcomputer.
The ADAM81 contains ADAM80 CPU, RAM, Timer/PWM, Interrupt, Watch Dog Timer, 12-bit ADC, Input/Output Ports and Oscillation Circuit.

1.1. Features

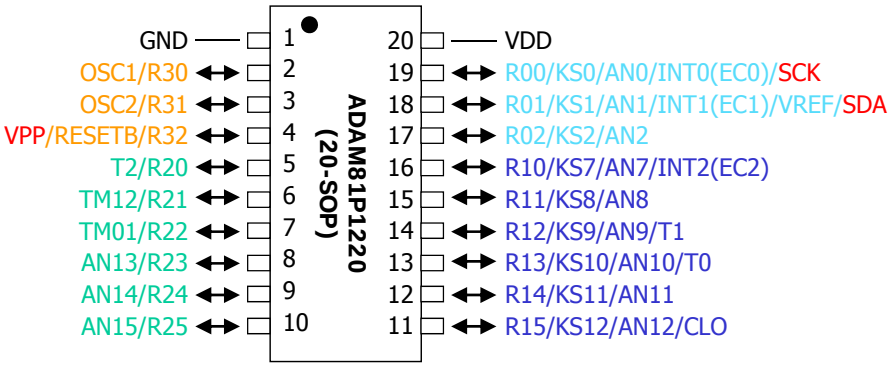
▪ High Performance 8-bit RISC CPU	55 - Instructions (most single cycle)
▪ General Purpose Registers	8bit x 8 (A, B, C, D, E, F, G, H)
▪ Program Stack Level	16 level
▪ Interrupt Stack Level	8 level
▪ SRAM Indirect Addressing Register (X, A) SRAM Indirect Addressing Pointer (Y)	8bit x 1 (Addressing 192bytes) 5bit x 1 (Addressing 32bytes)
▪ Instruction Execution Time	0.5us @8MHz
▪ Program Memory Area	8K bytes (4K x 16bit)
▪ Data Memory Area	192bytes
▪ Timer (Include function : Timer/PWM/Counter/Capture)	16bit x 3ch [PWM: (8+8)bit x 3ch]
▪ Watch-Dog Timer (with RCWDT=32us)	19bit
▪ Interrupt Source	External 4ch (KS, INT0, INT1, INT2) Internal 6ch (T0, T1, T2, ADC, WDT, VDI)
▪ Analog-Digital Converter	12bit x 12ch
▪ Internal RCOSC	typ. 16/8/4/2/1MHz
▪ Internal RCWDT	typ. 32KHz
▪ External R-OSC	
▪ Power Saving Operation Modes	STOP, SLEEP, RC-WDT
▪ Power-On Reset	
▪ Low Voltage Detector	
▪ Voltage Detection Indicator	3 level (2.3V/3.0V/3.8V)
▪ Operating Voltage	1.8V ~ 5.5V @(1 ~ 4MHz, 32KHz) 2.2V ~ 5.5V @(1 ~ 8MHz) 2.7V ~ 5.5V @(1 ~ 20MHz)
▪ Operating Temperature	-40^{O}C ~ 85^{O}C
▪ Package	20/16 SOP

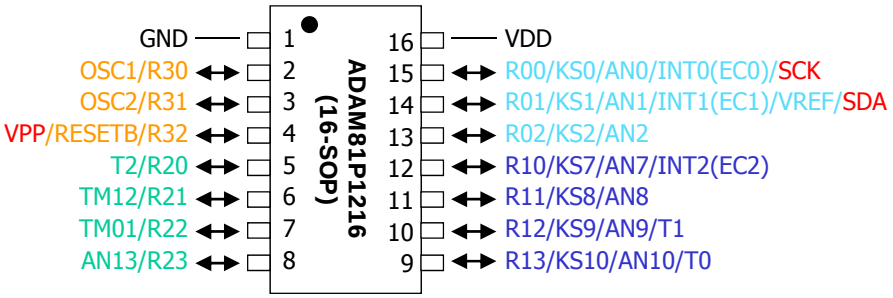
☑ ADAM81P12XX Series members

Series	ADAM81P1220	ADAM81P1216
Program memory	4,096 x 16	4,096 x 16
Data memory	192 x 8	192 x 8
I/O ports (max.)	*14 (18)	*10 (14)
Package	20SOP	16SOP

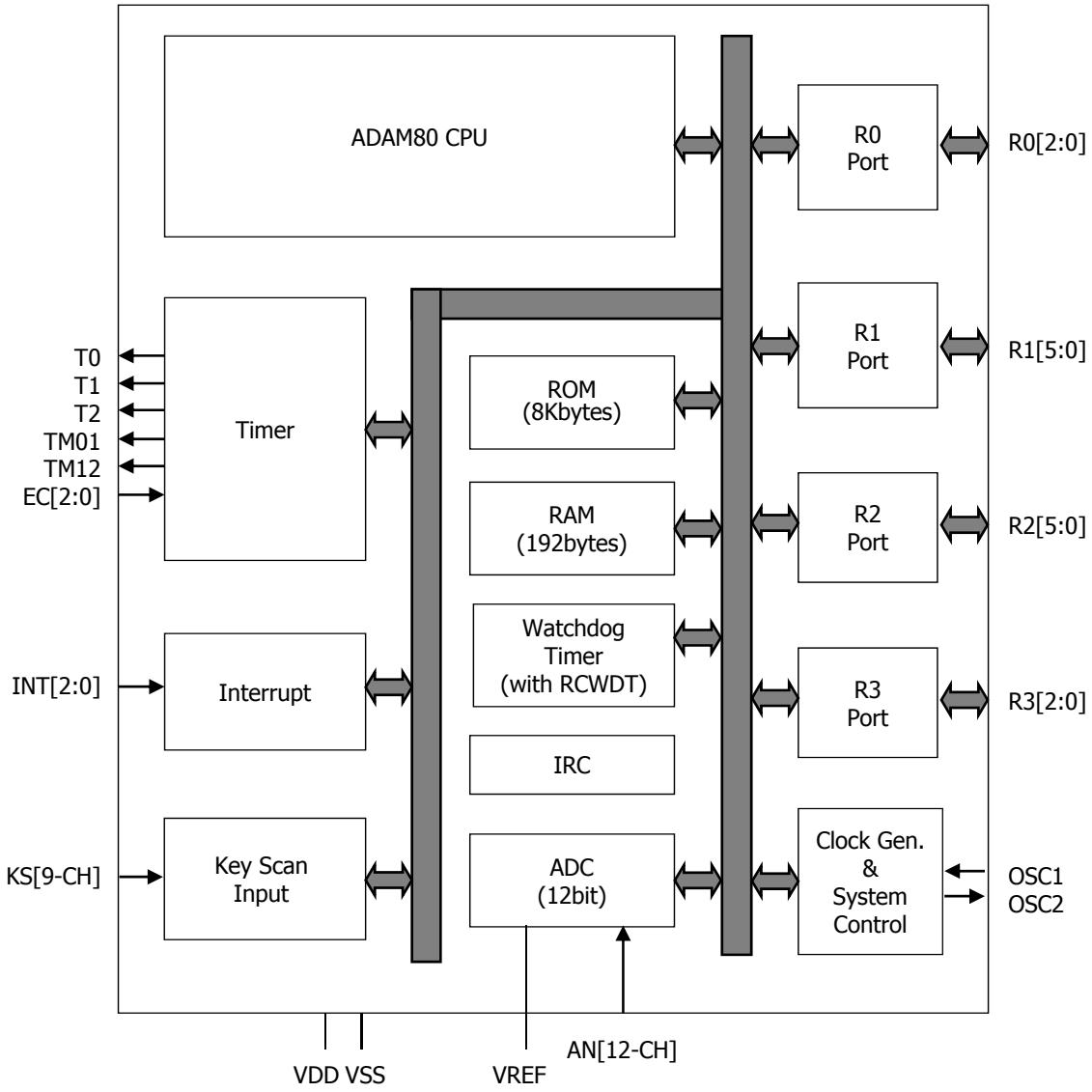
* OSC1/OSC2/RESETB/VREF

1.2. Pin Assignments

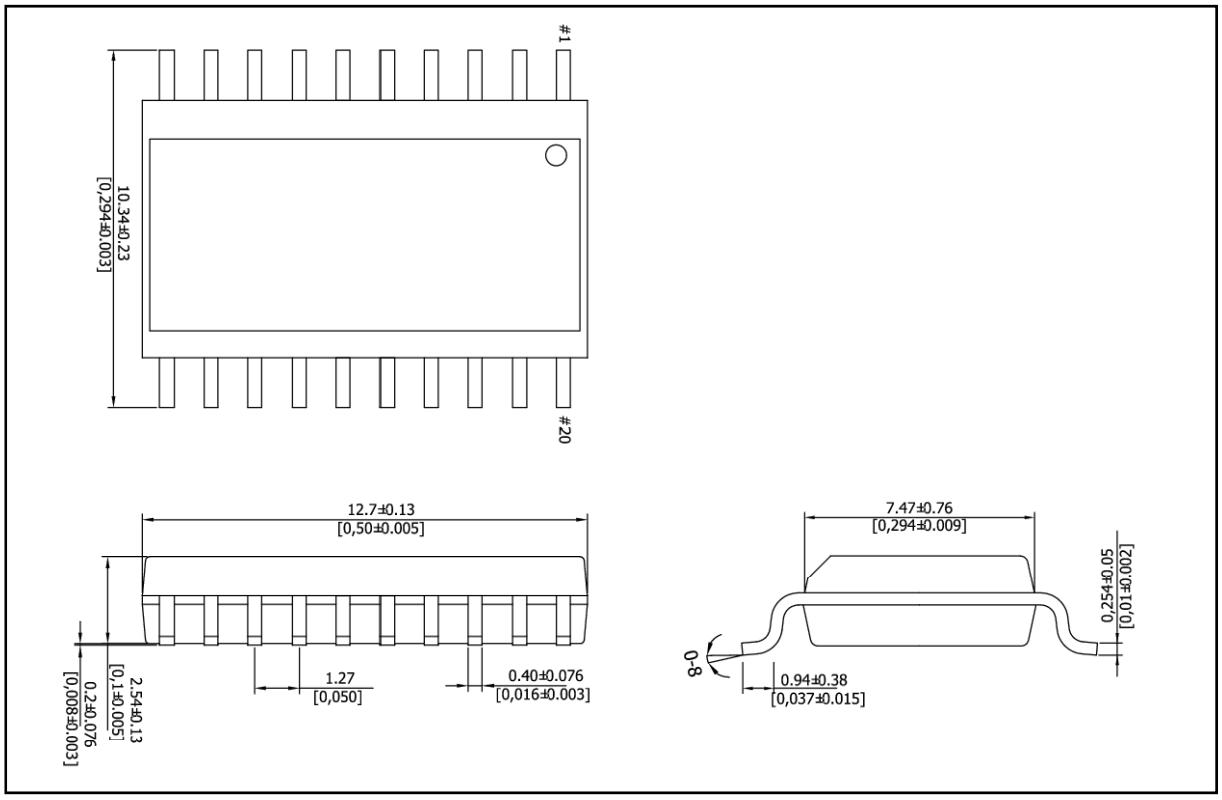




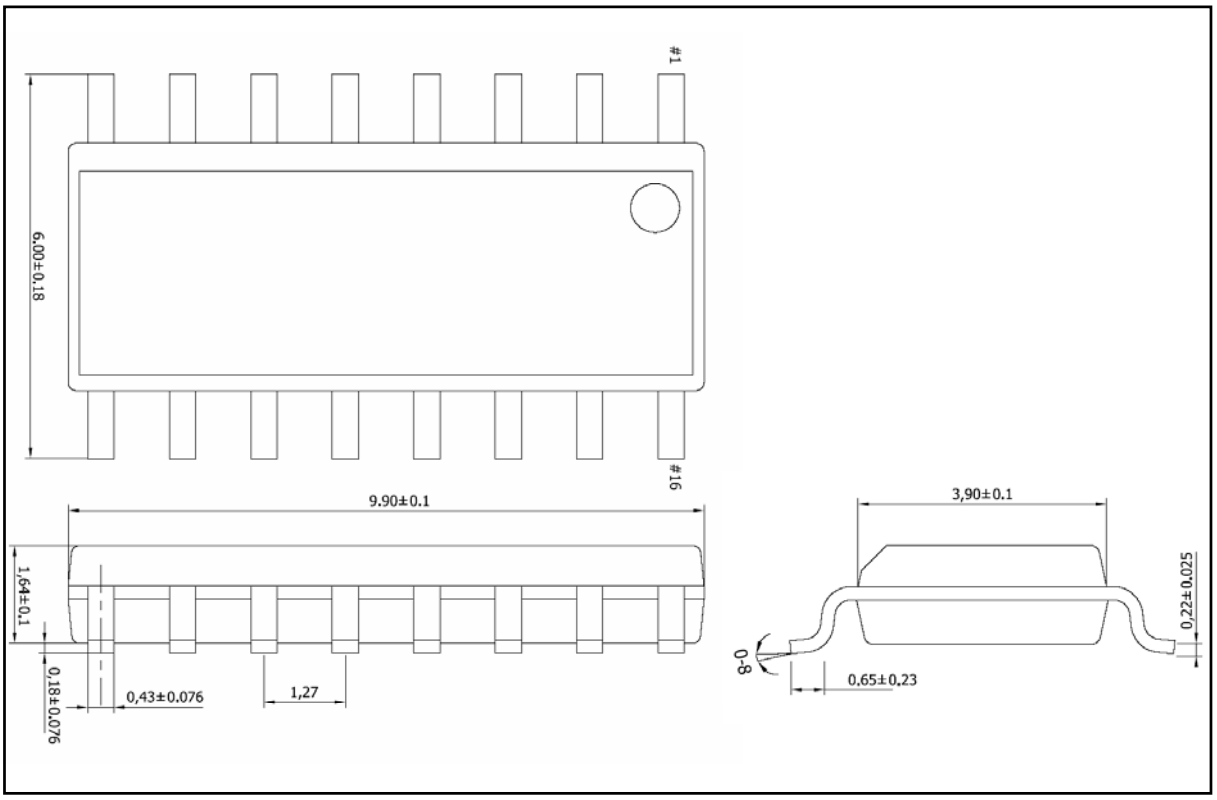
1.3. Block Diagram



1.4. Package Dimension



20 SOP (300MIL) Pin Dimension (dimensions in mm)

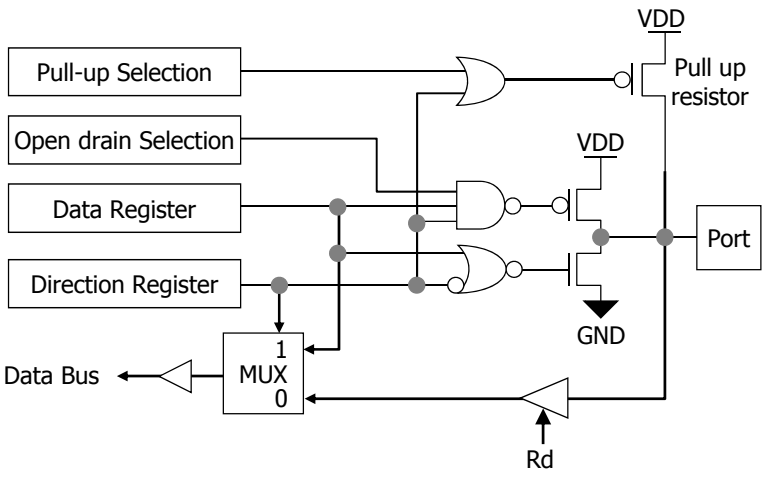


16 SOP (150MIL) Pin Dimension (dimensions in mm)

1.5. Pin Function

Pin Name	I/O	Function	@RESET	@STOP
R02/KS2/AN2 R01/KS1/AN1/INT1(EC1)/VREF R00/KS0/AN0/INT0(EC0)	I/O	- 3-bit I/O Port. - CMOS input with pull-up resistor. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/KS/AN/INT(EC). - Direct Driving of LED.	Input	State of before STOP
R15/KS12/CLO R14/KS11 R13/KS10/AN10/T0 R12/KS9/AN9/T1 R11/KS8/AN8 R10/KS7/AN7/INT2(EC2)	I/O	- 6-bit I/O Port. - CMOS input with pull-up resistor. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/KS/AN/INT(EC)/TIMER/CLO. - Direct Driving of LED.	Input	State of before STOP
R25/AN15 R24/AN14 R23/AN13 R22/TM01 R21/TM12 R20/T2	I/O	- 8-bit I/O Port. - CMOS input with pull-up resistor. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/AN/TIMER. - Direct Driving of LED.	Input	State of before STOP
R32/RESETB R31/OSC2 R30/OSC1	I/O	- 3-bit I/O Port. - CMOS input with pull-up resistor. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/Pull-down/N-ch open drain. - R32 is open-drain output. - Direct Driving of LED.	Input	State of before STOP
RESETB	I	- External RESETB Input by Code/Register Option.	Input	
OSC1	I	- Oscillator Input.	Input	Low
OSC2	O	- Oscillator Output.	Output	High
VREF	P	- ADC Positive Power Supply.		
VDD	P	- Positive Power Supply.		
GND	P	- Ground.		

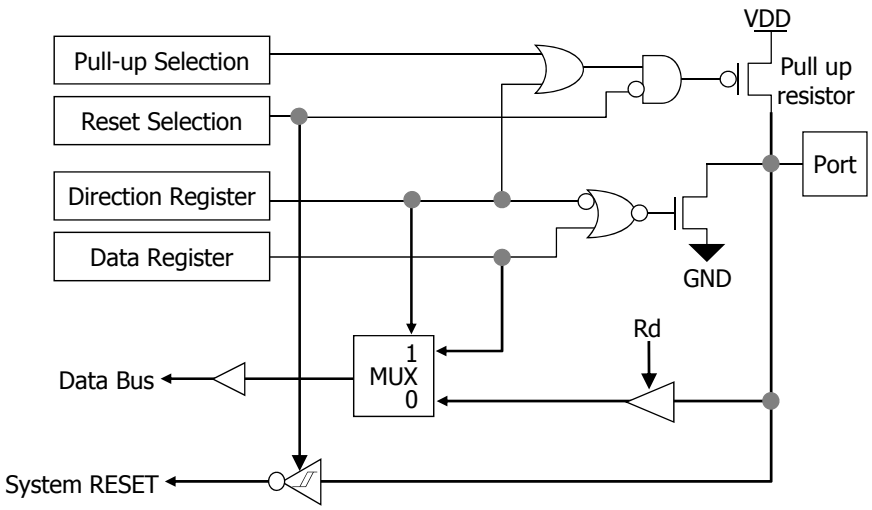
1.6. Port Structure (Normal I/O mode with Pull-Up & Open-Drain)

Pin Name	Circuit Type	RESET
R0[2:0] R1[5:0] R2[5:0] R3[2:0]		Input
Shared Function	KS/AN/INT(EC)/VREF/TIMER/CLO/OSC1/OSC2	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KS	Input	*	Port	Data	KS		
AN	Input	Off	Port(Analog Input) =unknown=	Data	AN		
INT(EC)	Input	*	Port	Data	INT(EC)		
VREF	Input	Off	Port(Analog Power) =unknown=	Port(Analog Power) =unknown=	VREF	R0[1] RESET	
TIMER	Output	Off	Port	Data	TIMER		
CLO	Output	Off	Port	Data	CLO		

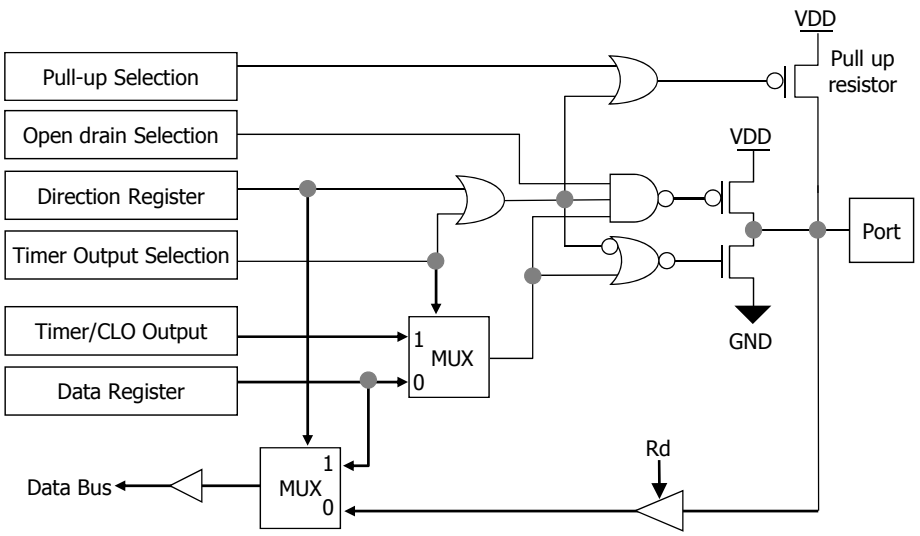
* : It is depend on user definition.

1.6. Port Structure (RESETB mode)

Pin Name	Circuit Type	RESET
R3[2]		Input
Shared Function	RESETB (Input with Pull-up)	

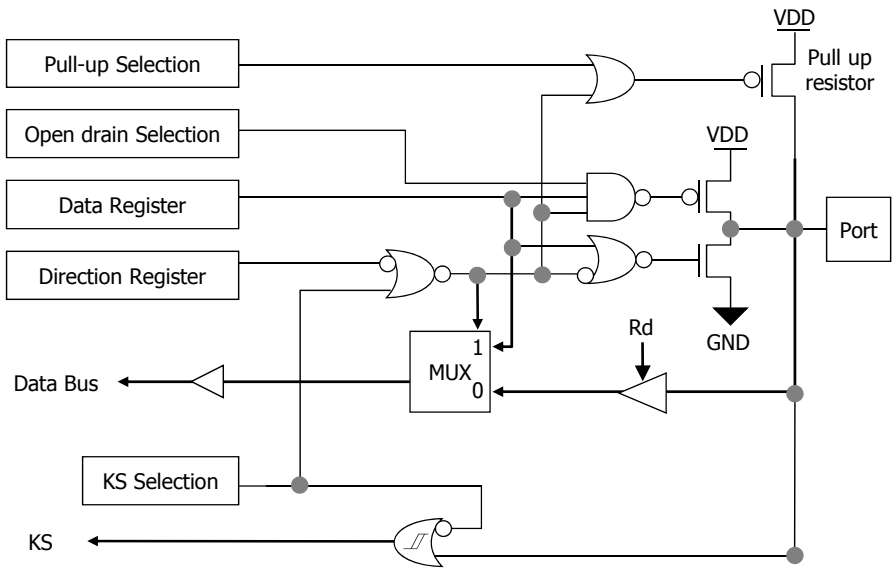
Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	-			
RESETB	Input	On	Port	-	Pull-up RESETB	R3[2] RESET	

1.6. Port Structure (Timer, CLO output mode)

Pin Name	Circuit Type	RESET
R1[3]/T0 R1[2]/T1 R2[0]/T2 R2[1]/TM12 R2[2]/TM01 R1[5]/CLO		Input
Shared Function	T0/T1/T2/TM01/TM12, CLO	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
TIMER	Output	Off	Port	Data	TIMER		
CLO	Output	Off	Port	Data	CLO		

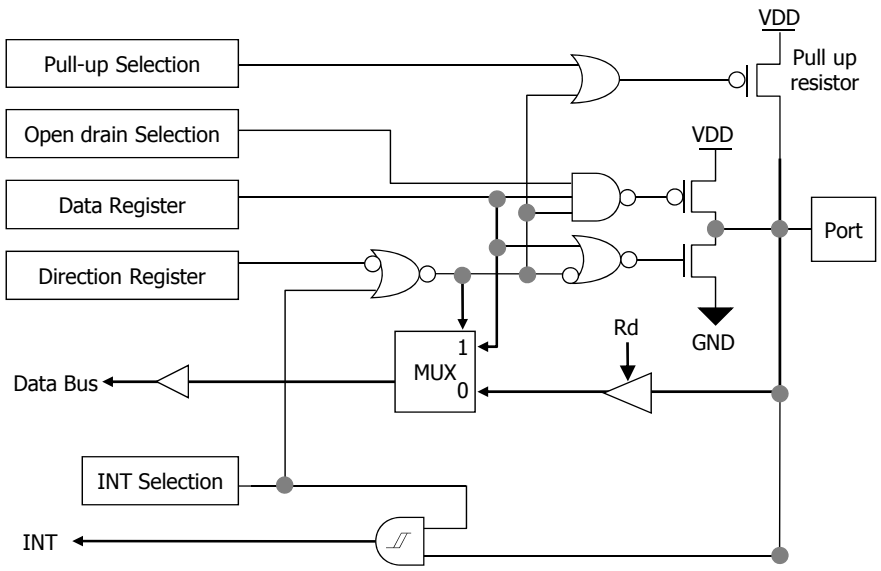
1.6. Port Structure (Key-Scan mode)

Pin Name	Circuit Type	RESET
R0[2:0]/KS[2:0] R1[5:0]/KS[12:7]		Input
Shared Function	KS	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KS	Input	*	Port	Data	KS		

* : It is depend on user definition.

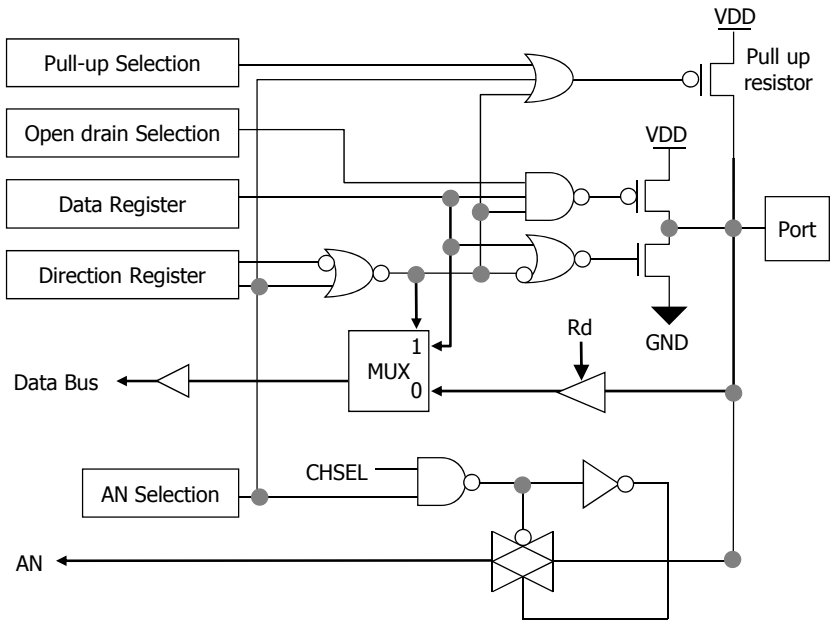
1.6. Port Structure (External Interrupt [INT] mode)

Pin Name	Circuit Type	RESET
R0[0]/INT0(EC0) R0[1]/INT1(EC1) R1[0]/INT2(EC2)		Input
Shared Function	INT(EC)	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
INT(EC)	Input	*	Port	Data	INT(EC)		

* : It is depend on user definition.

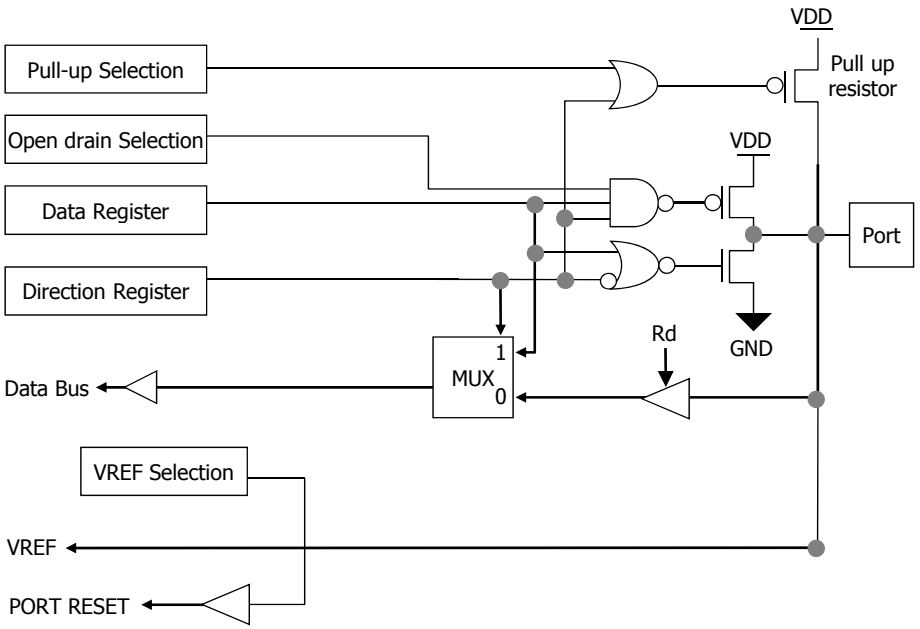
1.6. Port Structure (Analog Input [AN] mode)

Pin Name	Circuit Type	RESET
R0[2:0]/AN[2:0] R1[5:0]/AN[12:7] R2[5:3]/AN[15:13]		Input
Shared Function	AN	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
AN	Input	Off	Port(Analog Input) =unknown=	Data	AN		

* : It is depend on user definition.

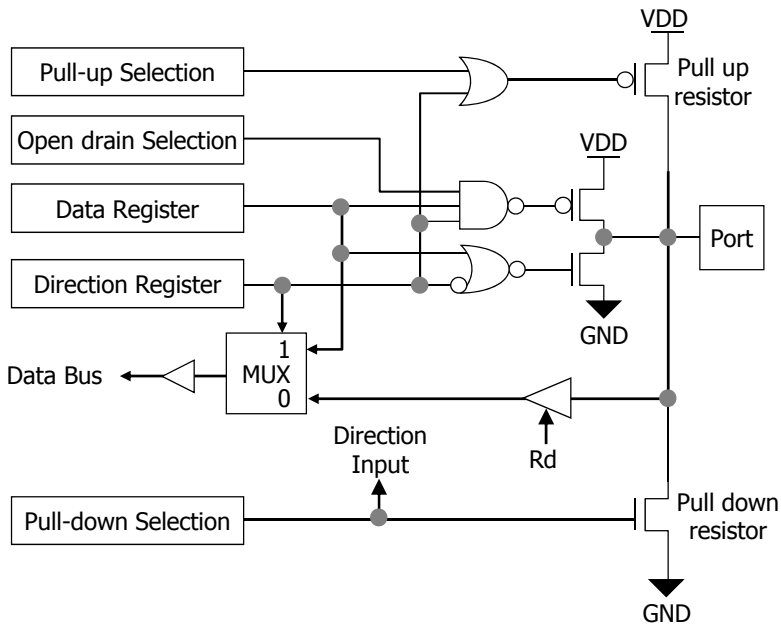
1.6. Port Structure (VREF mode)

Pin Name	Circuit Type	RESET
R0[1]		Input
Shared Function	KS/AN/INT(EC)/VREF	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
VREF	Input	Off	Port(Analog Power) =unknown=	Port(Analog Power) =unknown=	VREF	R0[1] RESET	

* : It is depend on user definition.

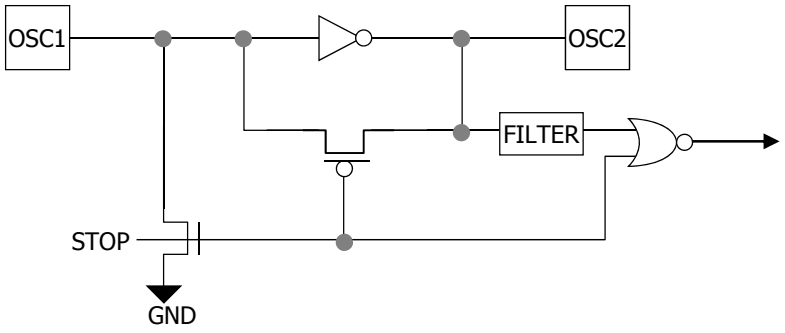
1.6. Port Structure (Normal I/O mode with Pull-Down)

Pin Name	Circuit Type	RESET
R3[0]/OSC1 R3[1]/OSC2		Input
Shared Function	OSC1/OSC2	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
OSC1	Input	Off	=unknown=	=unknown=	OSC1	R3[0] RESET	Disable
OSC2	Input	Off	=unknown=	=unknown=	OSC2	R3[1] RESET	
Pull-down	Input	*	*	*	*		

* : It is depend on user definition.

1.6. Port Structure (OSC1/OSC2 mode)

Pin Name	Circuit Type	RESET
OSC1 OSC2		Oscillation

1.7. Electrical Characteristics

1.7.1. Absolute Maximum Ratings (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +6.0	V
Input Voltage	V_I	-0.3 ~ VDD + 0.3	V
Output Voltage	V_O	-0.3 ~ VDD + 0.3	V
Storage Temperature	T_{STG}	-65 ~ 150	°C
Power Dissipation	P_D	700	mW

1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	f_{OSC} = 4MHz	1.8	-	5.5	V
		f_{OSC} = 8MHz	2.2	-	5.5	V
		f_{OSC} = 20MHz	2.7	-	5.5	V
Oscillation Frequency	f_{OSC}		1	4	20	MHz
Operating Temperature	T_{OPR}		-40		85	°C

1.7.3. DC Characteristics (Ta = 25℃)

PARAMETER	Symbol	Condition			Specification			UNIT
					MIN.	TYP.	MAX.	
High level input voltage	V_{IHX}	OSC1			0.9VDD		VDD	V
	V_{IH1}	RESETB, KS, INT0, INT1, INT2, EC0, EC1, EC2			0.8VDD		VDD	V
	V_{IH2}	R0, R1, R2, R3			0.7VDD		VDD	V
Low level input voltage	V_{ILX}	OSC1			0		0.1VDD	V
	V_{IL1}	RESETB, KS, INT0, INT1, INT2, EC0, EC1, EC2			0		0.2VDD	V
	V_{IL2}	R0, R1, R2, R3			0		0.3VDD	V
High level input leakage current	I_{IH}	R0, R1, R2, R3		VIH = VDD			1	uA
Low level input leakage current	I_{IL}	R0, R1, R2, R3		VIL = 0V			-1	uA
High level output voltage	V_{OH1}	R0, R1, R2, R3	VDD = 5V	IOH = -10mA	VDD-1.0	VDD-0.7		V
	V_{OHX}	OSC2	VDD = 5V	IOH = -0.2mA	VDD-1.0	VDD-0.7		V
Low level output voltage	V_{OL1}	R0, R1, R2, R3	VDD = 5V	IOL = 25mA		0.7	1.0	V
	V_{OL2}	OSC2	VDD = 5V	IOL = 0.2mA		0.7	1.0	V
High level output leakage current	I_{OHL}	R0, R1, R2, R3		VOH = VDD			1	uA
Low level output leakage current	I_{OLL}	R0, R1, R2, R3		VOL = 0V			-1	uA
Input Pull-up current	I_{PU}	R0, R1, R2, R3	VDD = 5V		-48	-60	-72	uA
Input Pull-down current	I_{PD}	R30, R31	VDD = 5V		48	60	72	uA
Power supply current `	I_{DD}	Operating current	VDD = 5V	fXIN = 8MHz		3	5	mA
	I_{SLEEP}	Sleep mode current	VDD = 5V	fXIN = 8MHz		2	3	mA
	I_{STOP}	Stop mode current	VDD = 5V	Oscillator stop		2.5	5	uA
			VDD = 5V	with RCWDT		10	20	uA
			VDD = 5V	with VDI		100	200	uA
IRC Frequency	F_{IRC}	IRC	VDD = 5V		3.92	4	4.08	MHz
RCWDT Frequency	F_{RCWDT}	RCWDT	VDD = 5V		25.6	32	38.4	KHz
ERC Frequency	F_{ERC}	ERC	VDD = 5V	R=4.7kΩ	15.2	16	16.8	MHz
			VDD = 5V	R=94kΩ	1.425	1.5	1.575	MHz
		Reference Resistor Selection Guide (An approximate value). R=4.7kΩ (16MHz) R=10kΩ (12MHz) R=15kΩ (8MHz) R=30kΩ (4.5MHz) R=47kΩ (3MHz) R=94kΩ (1.5MHz)						
RAM retention supply voltage	V_{RET}				0.7			V

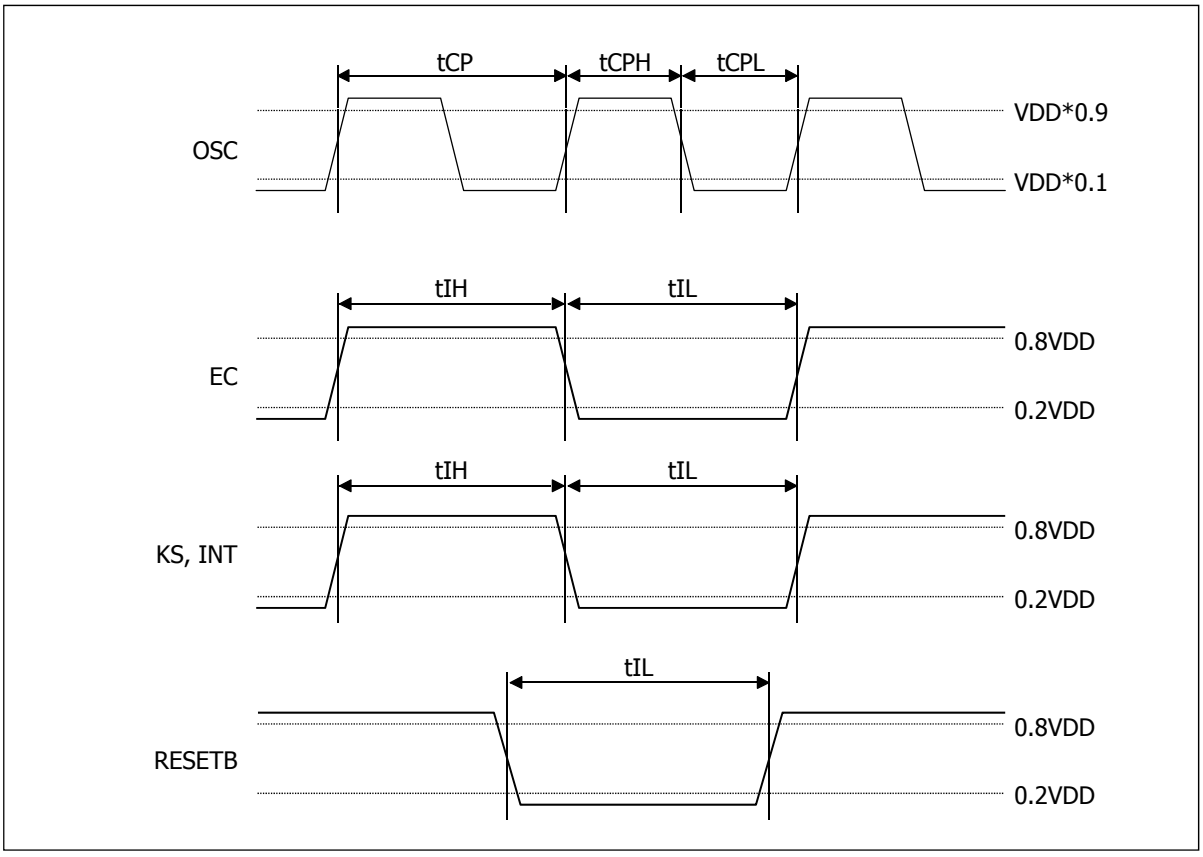
1.7.4. A/D Conversion Characteristics

PARAMETER	Symbol	Condition	Specification			UNIT
			MIN.	TYP.	MAX.	
Resolution	R_{ADC}		-	12	-	bit
Analog Input Voltage Range	V_{AIN}	AVREFS = 0	VSS	-	VDD	V
		AVREFS = 1	VSS	-	AVREF	V
Analog Input Power Supply Voltage Range	V_{REF}	VDD = 5V	2.7	-	VDD	V
		VDD = 3V	2.4	-	VDD	V
Overall Accuracy	E_{ADC}	VDD=4.096V, f_{OSC}=4MHz	-	±3	±4	lsb
Non-Linearity Error	E_{NE}		-	±3	±4	lsb
Differential Non-Linearity Error	E_{DE}		-	±3	±4	lsb
Zero Offset Error	E_{OFF}		-	±3	±4	lsb
Full Scale Error	E_{OFF}		-	±3	±4	lsb
Conversion Time	T_{CONV}	VDD = 5.5V ~ 2.7V	29	-	-	uS
		VDD = 5.5V ~ 2.4V	58	-	-	uS
AVREF Input Current	I_{REF}	AVREFS = 1	-	0.8	2.0	mA

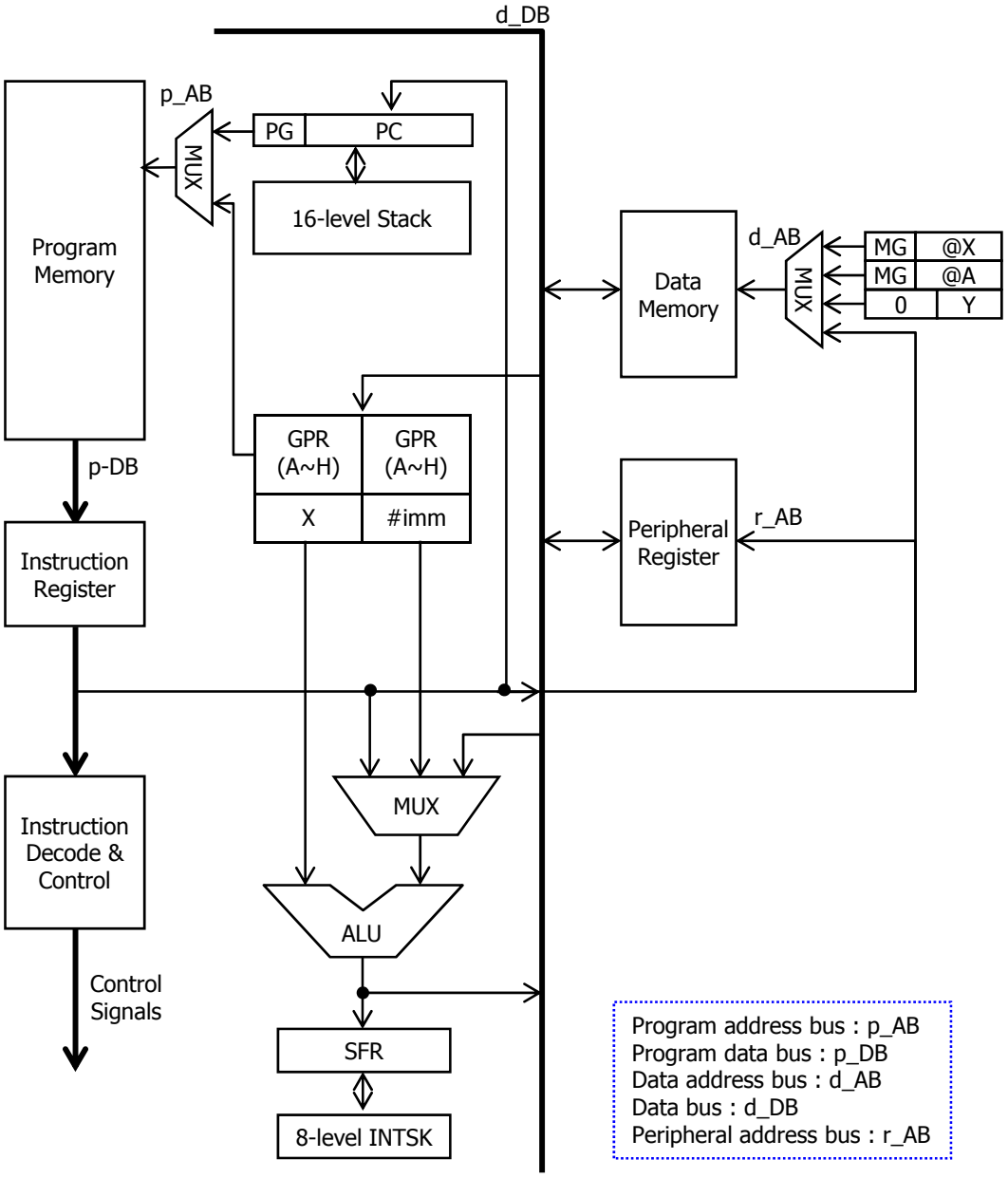
1.7.5. AC Characteristics (Ta = 25℃)

Parameter	Symbol	Pin	Specification			Unit
			min.	typ.	max.	
External clock input cycle time	tCP	OSC	50	250	1000	ns
External clock input High	tCPH	OSC		0.5		tCP
External clock input Low	tCPL	OSC		0.5		tCP
System clock cycle time	tSYS	-		4		tCP
External pulse width High	tIH	EC	1			tCP
External pulse width Low	tIL	EC	1			tCP
Interrupt pulse width High	tIH	KS, INT	2			tSYS
Interrupt pulse width Low	tIL	KS, INT	2			tSYS
RESETB pulse width Low	tIL	RESETB	8			tSYS

Minimum pulse width



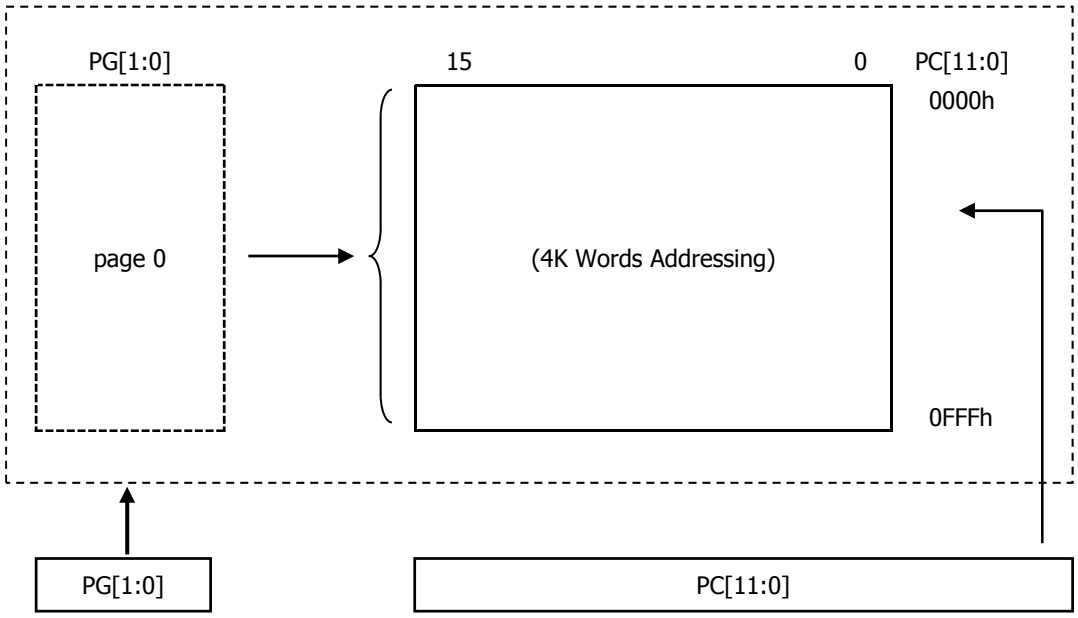
2.0. CPU Function Diagram



2.1. Program Memory Map

The ADAM81 can address up to Maximum 8Kbytes (4K x 16bits) for Program Memory.
Program Counter(PC[11:0]) is used to address the whole area of Program Memory having an instruction (16bit) to be next executed.
The Program Memory consists of 8K words on each page, and thus each page can hold up to 8K steps of instructions.

• The program memory is composed as shown below.



* don't change the page.

Mode of Program Memory Addressing

	11	10	9	8	7	6	5	4	3	2	1	0
4K words Addressing	PC[11:0]											

2.2. Program page Register

The following registers are used to address the Program Memory.

• Program page Register (PG) :
Holds ROM's page number (page 0 ~ page 3) to be addressed.
it is writable by MOVPG instruction Only.

* To change the page,
1) MOVPG #pageNo.
2) CALL or BR instruction execute.

	7	6	5	4	3	2	1	0	
PG	-	-	PG1	PG0	-	-	PC14	PC13	79h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R	R	-	-	R	R	

Selection Mode of PG

Bit Name	Selection Mode		Remarks
PG[1:0]	00	Program Memory page 0	
	01	Program Memory page 1	
	10	Program Memory page 2	
	11	Program Memory page 3	
PC14:13]	-	Program Counter	read only

• Program counter (PC) :
Available for addressing word on each page.

This 13-bit binary counter increments for fetching a word to be addressed in the currently addressed page having an instruction to be next executed. For easier programming, at turning on the power, the program counter is reset to the zero location(0000h). The PG is also set to "0h". Then the program counter specifies the next address. When BR, CALL or RET, RETI instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CALL, address data are taken in from the instruction operands (A0 to A11), or for RET, RETI and address including page address is fetched from stack register.

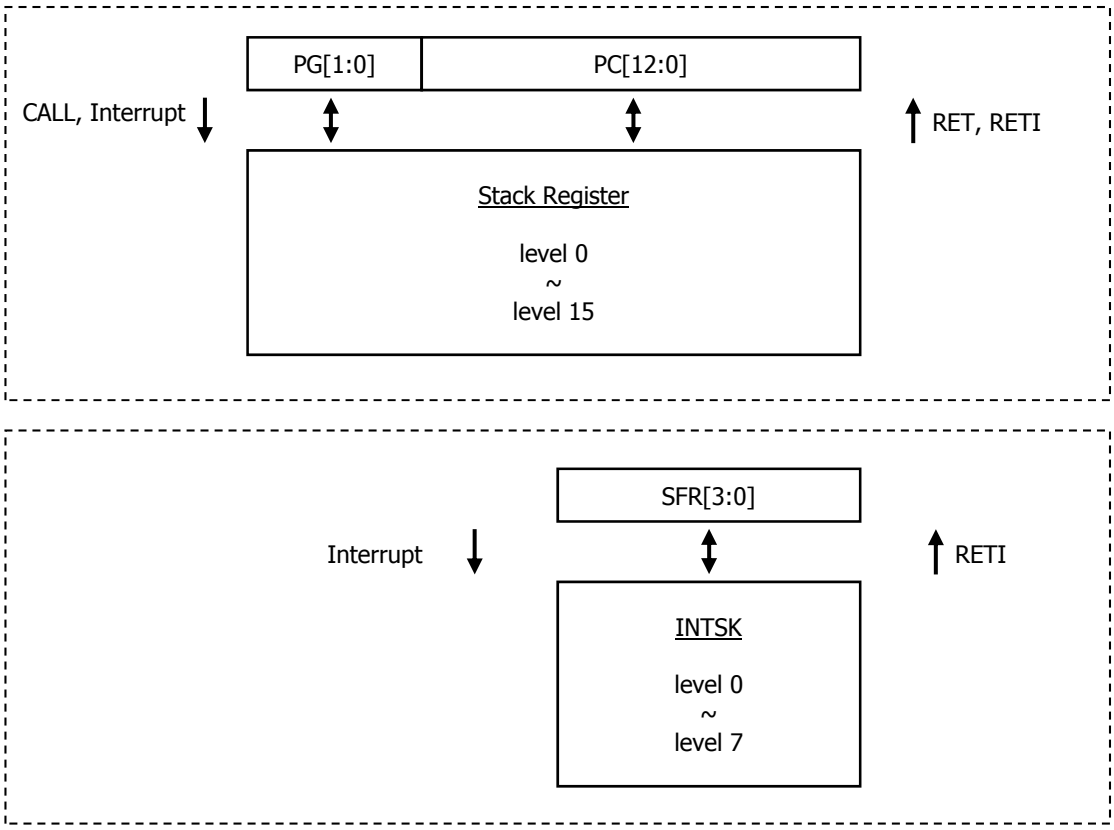
bit	11		0
PC	PC		
initial value	0000h		

Selection Mode of PC

PC[11:0]	Program Counter	0000h ~ 0FFFh	4K words Addressing

• Stack Register (SR) :
Stores returned-word address in the subroutine call mode.

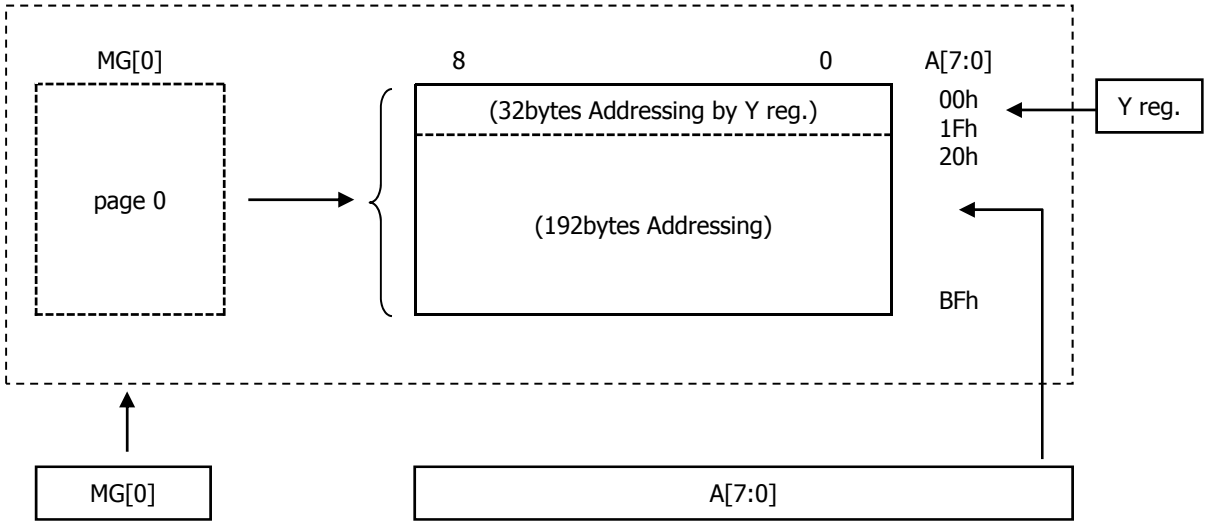
The Stack register stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.
If subroutine or interrupts are nested to more than 16 levels, internal reset is occurred.
The interrupt stack register(INTSK) Saves the contents of Status flag register(SFR) when an interrupt is acknowledged.
The Saved contents are restored when an interrupt return(RETI) instruction is executed.
INTSK Saves data each time an interrupt is acknowledged. but the data stored first is lost if more than 8 levels of interrupts occur.



2.3. DATA Memory Map

The ADAM81 can address up to Maximum 192bytes for Data Memory.
Data Memory Address[7:0] is used to address the whole area of Data Memory .
The Data Memory consists of 192bytes on each page.
Y register can address up to 32bytes (Page 0 : 00h ~ 1fh) for SRAM backup mode.

• The data memory is composed as shown below.



* don't change the page.

The following register is used to address the RAM.

- Memory page Register (MG) :
  Holds RAM's page number (page 0 ~ page 1) to be addressed.
  It is writable with MOVMG instruction only.

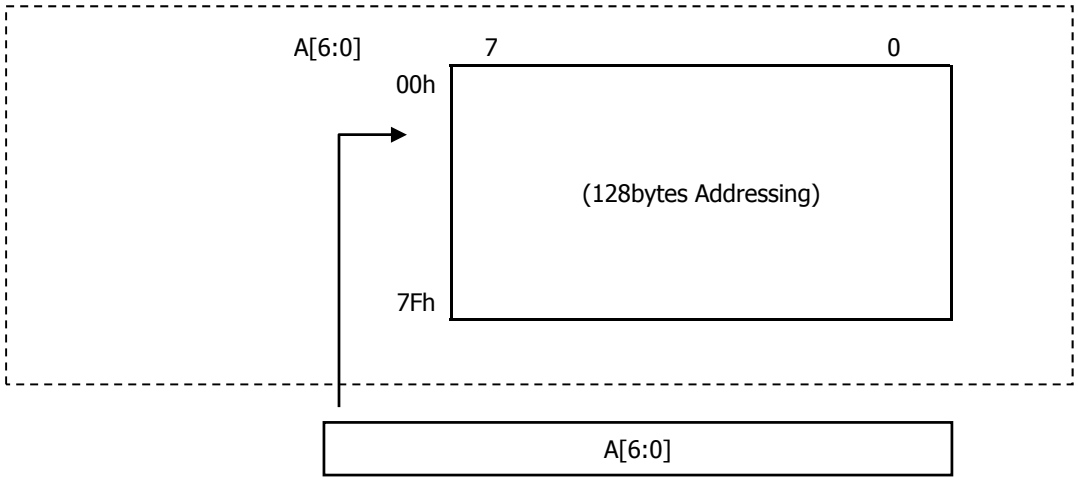
Selection Mode of MG

MG[0]	Data Memory page Register	0	page 0

2.4. Peripheral Memory Map

The ADAM81 can address up to Maximum 128bytes for Peripheral Control Registers.
Peripheral Address[6:0] is used to address the whole area of Registers .

• The Peripheral Register is composed as shown below.



2.5. General Purpose Registers

2.5.1. X-register (X)

X-register is consist of 8 bits. It can used for a general-purpose register.
X-register also used for data memory indirect addressing mode register.

2.5.2. Y-register (Y)

Y-register is consist of 5 bits. It is read-only.
Y-register used for data memory (0-page) indirect addressing pointer.

	7	6	5	4	3	2	1	0	
Y	-	-	-	Y4	Y3	Y2	Y1	Y0	78h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	R	R	R	R	R	

2.5.3. GPR (A, B, C, D, E, F, G, H)

GPR is consist of 8 x 8bits. It can used for a general-purpose register.
GPR also used for program memory indirect addressing mode register.
A (GPR) also used for data memory indirect addressing mode register.

2.5.4 PC & PG Buffer Register (read only)

it is writable by MOVPG instruction Only.

PC is the program counter, PG is the program page buffer.
PG is updated to PC when call or br executed.

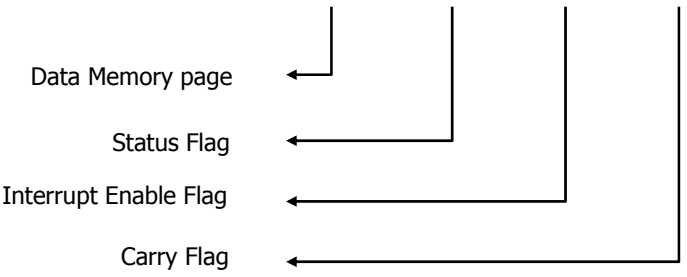
	7	6	5	4	3	2	1	0	
PG	-	-	PG1	PG0	-	-	PC14	PC13	79h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R	R	-	-	R	R	

2.6. Status Flag Register (SFR)

Status Flag Register (SFR) is consist of 4-bit register.

Consisted of the flags showing the post state of operation and the flags determining the CPU operation, initialized as 0h in reset state.

	7	6	5	4	3	2	1	0	
SFR	-	-	-	-	MG0	S	I	Cy	7Ah
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	R	R	R	R	



- Data Memory page (MG)
  - 0 : page 0
  - 1 : page 1

- Status flag (S)
  - According to the condition after executing an instruction , set or clear.
  - Can not be set or clear by any instruction.

- Interrupt enable flag (I)
  - Master enable flag of interrupt.
  - Set and cleared by EI, DI
  - This Flag immediately becomes "0" when an interrupt is served.
  - After interrupt service routine, restored I flag to INTSK.

- Carry flag (Cy)
  - Carry flag bit is set when there is carry or borrow After executing ADD / SUB / SHIFT / ROTATE / LDC / STC instructions.
  - Set by SETC and clear by CLRC.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
00h	PORT R0 DATA REG.								R/W	R0	1111_1111	*bit/byte
	-	-	-	-	-	R02	R01	R00				
01h	PORT R0 PULL UP SELECTION REG.								W	R0PU	1111_1111	byte
	-	-	-	-	-	R02PU	R01PU	R00PU				
02h	PORT R0 OPEN DRAIN SELECTION REG.								W	R0OD	0000_0000	byte
	-	-	-	-	-	R02OD	R01OD	R00OD				
03h	PORT R0 DIRECTION REG.								R/W	R0DD	0000_0000	bit/byte
	-	-	-	-	-	R02DD	R01DD	R00DD				
04h	PORT R0 FUNCTION SELECTION REG LOW.								R/W	R0FL	0000_0000	bit/byte
	-		R02		R01		R00					
-	-								-	-	-	-
08h	PORT R1 DATA REG.								R/W	R1	1111_1111	*bit/byte
	-	-	R15	R14	R13	R12	R11	R10				
09h	PORT R1 PULL UP SELECTION REG.								W	R1PU	1111_1111	byte
	-	-	R15PU	R14PU	R13PU	R12PU	R11PU	R10PU				
0Ah	PORT R1 OPEN DRAIN SELECTION REG.								W	R1OD	0000_0000	byte
	-	-	R15OD	R14OD	R13OD	R12OD	R11OD	R10OD				
0Bh	PORT R1 DIRECTION REG.								R/W	R1DD	0000_0000	bit/byte
	-	-	R15DD	R14DD	R13DD	R12DD	R11DD	R10DD				
0Ch	PORT R1 FUNCTION SELECTION REG LOW.								R/W	R1FL	0000_0000	bit/byte
	R13		R12		R11		R10					
0Dh	PORT R1 FUNCTION SELECTION REG HIGH.								R/W	R1FH	0000_0000	bit/byte
	-		-		R15		R14					
-	-								-	-	-	-
10h	PORT R2 DATA REG.								R/W	R2	1111_1111	*bit/byte
	-	-	R25	R24	R23	R22	R21	R20				
11h	PORT R2 PULL UP SELECTION REG.								W	R2PU	1111_1111	byte
	-	-	R25PU	R24PU	R23PU	R22PU	R21PU	R20PU				
12h	PORT R2 OPEN DRAIN SELECTION REG.								W	R2OD	0000_0000	byte
	-	-	R25OD	R24OD	R23OD	R22OD	R21OD	R20OD				
13h	PORT R2 DIRECTION REG.								R/W	R2DD	0000_0000	bit/byte
	-	-	R25DD	R24DD	R23DD	R22DD	R21DD	R20DD				
14h	PORT R2 FUNCTION SELECTION REG.								R/W	R2FN	0000_0000	bit/byte
	-	-	R2FN5	R2FN4	R2FN3	R2FN2	R2FN1	R2FN0				
-	-								-	-	-	-

Caution :
Before operating pheriperals, Must be initialize undefined registers.
*bit is read-modified operation. (SETR1/CLRR1 instruction)

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
18h	PORT R3 DATA REG.								R/W	R3	1111_1111	*bit/byte
	-	-	-	-	-	R32	R31	R30				
19h	PORT R3 PULL UP SELECTION REG.								W	R3PU	1111_1111	byte
	-	-	-	-	-	R32PU	R31PU	R30PU				
1Ah	PORT R3 OPEN DRAIN SELECTION REG.								W	R3OD	0000_0000	byte
	-	-	-	-	-	R32OD	R31OD	R30OD				
1Bh	PORT R3 DIRECTION REG.								R/W	R3DD	0000_0000	bit/byte
	-	-	-	-	-	R32DD	R31DD	R30DD				
1Ch	PORT R3 FUNCTION SELECTION REG.								R/W	R3FN	0000_0000	bit/byte
	-	-	-	-	-	R3FN2	R3FN1	R3FN0				
-	-								-	-	-	-
40h	EXTERNAL INTERRUPT EDGE SELECTION REG 0.								W	IEDS0	----_--00	byte
	-			-		-		IEDK				
41h	EXTERNAL INTERRUPT EDGE SELECTION REG 1.								W	IEDS1	0000_0000	byte
	-			IED2		IED1		IED0				
42h	INTERRUPT ENABLE REG 0.								R/W	IENR0	0000_0000	bit/byte
	-	-	-	-	INT2E	INT1E	INT0E	KSE				
43h	INTERRUPT REQUEST FLAG REG 0.								R/W	IRQR0	0000_0000	bit/byte
	-	-	-	-	INT2F	INT1F	INT0F	KSF				
44h	INTERRUPT ENABLE REG 1.								R/W	IENR1	0000_0000	bit/byte
	-	VDIE	WDTE	ADCE	-	T2E	T1E	T0E				
45h	INTERRUPT REQUEST FLAG REG 1.								R/W	IRQR1	0000_0000	bit/byte
	-	VDIF	WDTF	ADCF	-	T2F	T1F	T0F				
-	-								-	-	-	-
51h	TIMER0 MODE REG 0.								R/W	T0MR0	0000_0000	bit/byte
	T0CS	T0CN	T0EG	T0CPE1	T0CPE0	T0CK2	T0CK1	T0CK0				
52h	TIMER0 MODE REG 1.								R/W	T0MR1	0000_0000	bit/byte
	T0MC1	T0MC0	PWME0	WRAM0	FMOD0	INTS0	OUTC0	CKC0				
53h	TIMER0 DATA0 REG LOW. (PWM0 DUTY)								W	T0D0L	undefined	byte
	T0D0L7	T0D0L6	T0D0L5	T0D0L4	T0D0L3	T0D0L2	T0D0L1	T0D0L0				
	TIMER0 COUNT REG LOW.								R	T0CRL	undefined	byte
	T0CRL7	T0CRL6	T0CRL5	T0CRL4	T0CRL3	T0CRL2	T0CRL1	T0CRL0				
54h	TIMER0 DATA1 REG LOW. (PWM0 PERIOD)								W	T0D1L	undefined	byte
	T0D1L7	T0D1L6	T0D1L5	T0D1L4	T0D1L3	T0D1L2	T0D1L1	T0D1L0				
55h	TIMER0 DATA0 REG HIGH. (PWM0 DUTY EXTENSION)								W	T0D0H	undefined	byte
	T0D0H7	T0D0H6	T0D0H5	T0D0H4	T0D0H3	T0D0H2	T0D0H1	T0D0H0				
	TIMER0 COUNT REG HIGH.								R	T0CRH	undefined	byte
	T0CRH7	T0CRH6	T0CRH5	T0CRH4	T0CRH3	T0CRH2	T0CRH1	T0CRH0				
56h	TIMER0 DATA1 REG HIGH. (PWM0 PERIOD)								W	T0D1H	undefined	byte
	T0D1H7	T0D1H6	T0D1H5	T0D1H4	T0D1H3	T0D1H2	T0D1H1	T0D1H0				

Caution :
Before operating pheripherals, Must be initialize undefined registers.
*bit is read-modified operation. (SETR1/CLRR1 instruction)

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
57h	TIMER1 MODE REG 0.								R/W	T1MR0	0000_0000	bit/ byte
	T1CS	T1CN	T1EG	T1CPE1	T1CPE0	T1CK2	T1CK1	T1CK0				
58h	TIMER1 MODE REG 1.								R/W	T1MR1	0000_0000	bit/byte
	-	-	PWME1	WRAM1	FMOD1	INTS1	OUTC1	CKC1				
59h	TIMER1 DATA0 REG LOW. (PWM1 DUTY)								W	T1D0L	undefined	byte
	T1D0L7	T1D0L6	T1D0L5	T1D0L4	T1D0L3	T1D0L2	T1D0L1	T1D0L0				
	TIMER1 COUNT REG LOW.								R	T1CRL	undefined	byte
	T1CRL7	T1CRL6	T1CRL5	T1CRL4	T1CRL3	T1CRL2	T1CRL1	T1CRL0				
5Ah	TIMER1 DATA1 REG LOW. (PWM1 PERIOD)								W	T1D1L	undefined	byte
	T1D1L7	T1D1L6	T1D1L5	T1D1L4	T1D1L3	T1D1L2	T1D1L1	T1D1L0				
5Bh	TIMER1 DATA0 REG HIGH. (PWM1 DUTY EXTENSION)								W	T1D0H	undefined	byte
	T1D0H7	T1D0H6	T1D0H5	T1D0H4	T1D0H3	T1D0H2	T1D0H1	T1D0H0				
	TIMER1 COUNT REG HIGH.								R	T1CRH	undefined	byte
	T1CRH7	T1CRH6	T1CRH5	T1CRH4	T1CRH3	T1CRH2	T1CRH1	T1CRH0				
5Ch	TIMER1 DATA1 REG HIGH. (PWM1 PERIOD)								W	T1D1H	undefined	byte
	T1D1H7	T1D1H6	T1D1H5	T1D1H4	T1D1H3	T1D1H2	T1D1H1	T1D1H0				
5Dh	TIMER2 MODE REG 0.								R/W	T2MR0	0000_0000	bit/ byte
	T2CS	T2CN	T2EG	T2CPE1	T2CPE0	T2CK2	T2CK1	T2CK0				
5Eh	TIMER2 MODE REG 1.								R/W	T2MR1	0000_0000	bit/byte
	T2MC2	T2MC1	PWME2	WRAM2	FMOD2	INTS2	OUTC2	CKC2				
5Fh	TIMER2 DATA0 REG LOW. (PWM2 DUTY)								W	T2D0L	undefined	byte
	T2D0L7	T2D0L6	T2D0L5	T2D0L4	T2D0L3	T2D0L2	T2D0L1	T2D0L0				
	TIMER2 COUNT REG LOW.								R	T2CRL	undefined	byte
	T2CRL7	T2CRL6	T2CRL5	T2CRL4	T2CRL3	T2CRL2	T2CRL1	T2CRL0				
60h	TIMER2 DATA1 REG LOW. (PWM2 PERIOD)								W	T2D1L	undefined	byte
	T2D1L7	T2D1L6	T2D1L5	T2D1L4	T2D1L3	T2D1L2	T2D1L1	T2D1L0				
61h	TIMER2 DATA0 REG HIGH. (PWM2 DUTY EXTENSION)								W	T2D0H	undefined	byte
	T2D0H7	T2D0H6	T2D0H5	T2D0H4	T2D0H3	T2D0H2	T2D0H1	T2D0H0				
	TIMER2 COUNT REG HIGH.								R	T2CRH	undefined	byte
	T2CRH7	T2CRH6	T2CRH5	T2CRH4	T2CRH3	T2CRH2	T2CRH1	T2CRH0				
62h	TIMER2 DATA1 REG HIGH. (PWM2 PERIOD)								W	T2D1H	undefined	byte
	T2D1H7	T2D1H6	T2D1H5	T2D1H4	T2D1H3	T2D1H2	T2D1H1	T2D1H0				
63h	SYSTEM CONTROL REG.								R/W	SCR	0000_0000	bit/ byte
	-	-	LVDDIS	OSCNF	PSS	OCS	DRS1	DRS0				
64h	WATCH DOG TIMER CONTROL REG.								R/W	WDTR	0000_0000	bit/ byte
	-	RCWDTEN	WDTRST	WDTCK	WAKEUP1	WAKEUP0	-	-				
65h	A/D CONVERTER MODE REG 0.								R/W	ADCM0	0000_0001	bit/ byte
	-	-	-	-	-	ADEN	ADST	ADSF				
66h	A/D CONVERTER DATA REG LOW.								R	ADCRL	undefined	byte
	ADCRL7	ADCRL6	ADCRL5	ADCRL4	ADCRL3	ADCRL2	ADCRL1	ADCRL0				
67h	A/D CONVERTER DATA REG HIGH.								R	ADCRH	undefined	byte
	-	-	-	-	ADCRH3	ADCRH2	ADCRH1	ADCRH0				
	A/D CONVERTER MODE REG 1.								W	ADCM1	0000_0000	byte
	CHSEL3	CHSEL2	CHSEL1	CHSEL0	ADCK2	ADCK1	ADCK0	AVREFS				

Caution :
Before operating pheriperals, Must be initialize undefined registers.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
78h	Y REG.								R	Y	0000_0000	byte
	-	-	-	Y4	Y3	Y2	Y1	Y0				
79h	Program Page Reg. (PG[1:0], ADDR[14:13])								R	PG	0000_0000	byte
	-	-	PG1	PG0	-	-	PC14	PC13				
7Ah	STATUS FLAG REG.								R	SFR	0000_0000	byte
	-	-	-	-	MG0	S	I	Cy				
7Bh	*PROHIBIT*								-	-	-	-
7CH	*PROHIBIT*								-	-	-	-
7Dh	*PROHIBIT*								-	-	-	-
7Eh	VTG. DETECTION INDICATOR ENABLE REG.								W	WDIER	0000_0000	byte
	-	-	-	SNST	VDIRST	VDIER2	VDIER1	VDIER0				
	VTG. DETECTION INDICATOR DATA REG.								R	VDIR	0000_0000	byte
	-	VDIR6	VDIR5	VDIR4	-	VDIR2	VDIR1	VDIR0				
7Fh	*PROHIBIT*								-	-	-	-

Caution :
Before operating pheriperals, Must be initialize undefined registers.

The ADAM81 has 18 I/O ports which are R0 (3 I/O), R1 (6 I/O), R2 (6 I/O), R3 (3 I/O).
R0 and R1 Port have Stop Release selection register.
Pull-up resistor of R0, R1, R2 and R3 ports can be selectable by program.
Pull-down resistor of R30 and R31 ports can be selectable by program.
R0, R1, R2 and R3 ports contains data direction register which controls I/O and data register which stores port data.
R0, R1, R2 and R3 Ports have Open Drain selection register and Data register.

*R32 is Open Drain output.

I/O Ports Registers

Port	Data Reg.	Pull-up Reg.	Open-Drain Reg.	Direction Reg.	Function Reg.
port R0	R0	R0PU	R0OD	R0DD	R0FL
port R1	R1	R1PU	R1OD	R1DD	R1FH/R1FL
port R2	R2	R2PU	R2OD	R2DD	R2FN
port R3	R3	R3PU	R3OD	R3DD	R3FN

R/W	R/W	W	W	R/W	R/W
Initial value	1111_1111	1111_1111	0000_0000	0000_0000	0000_0000
default	ffh	disable	enable	input	disable

3.1. Port R0

• R0 Data Register (R0)

	7	6	5	4	3	2	1	0	
R0	-	-	-	-	-	R02	R01	R00	00h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	-	-	-	R/W	R/W	R/W	

R0 data register (R0) is 3-bit register to store data of port R0.
When set as the output state by R0DD, and data is written in R0, data is outputted into port R0.
When set as the input state, input state of port R0 is readed.
bit is read-modified operation. (SETR1/CLRR1 instruction)
At output state, if port R0 is readed, R0 is readed instead of port R0.

• R0 Pull-up Selection Register (R0PU)

	7	6	5	4	3	2	1	0	
R0PU	-	-	-	-	-	R0PU2	R0PU1	R0PU0	01h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	-	-	-	W	W	W	

R0 pull-up resistor control register (R0PU) is 3-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R0PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R0 Open Drain Selection Register (R0OD)

	7	6	5	4	3	2	1	0	
R0OD	-	-	-	-	-	R0OD2	R0OD1	R0OD0	02h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	-	W	W	W	

R0 Open Drain Selection Register (R0OD) is 3-bit register, and can assign R0 port as open drain output port each bit. If R0OD is selected as "0", port R0 is open drain output, and if selected as "1", it is push-pull output.

• R0 I/O Data Direction Register (R0DD)

	7	6	5	4	3	2	1	0	
R0DD	-	-	-	-	-	R0DD2	R0DD1	R0DD0	03h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	-	R/W	R/W	R/W	

R0 I/O Data Direction Register (R0DD) is 3-bit register, and can assign input state or output state to each bit. If R0DD is "0", port R0 is in the input state, and if "1", it is in the output state.

• R0 Function Selection Register Low (R0FL)

	7	6	5	4	3	2	1	0	
R0FL	-		R02		R01		R00		04h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of R0FL

Bit Name	Selection Mode		Remarks
-	-	-	
	-	-	
	-	-	
	-	-	
R02	00	R02	
	01	KS2	
	10	-	
	11	AN2	
R01	00	R01	
	01	KS1	
	10	INT1(EC1)	
	11	AN1	
R00	00	R00	
	01	KS0	
	10	INT0(EC0)	
	11	AN0	

3.2. Port R1

• R1 Data Register (R1)

	7	6	5	4	3	2	1	0	
R1	-	-	R15	R14	R13	R12	R11	R10	08h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

R1 data register (R1) is 6-bit register to store data of port R1.
When set as the output state by R1DD, and data is written in R1, data is outputted into port R1.
When set as the input state, input state of port R1 is readed.
bit is read-modified operation. (SETR1/CLRR1 instruction)
At output state, if port R1 is readed, R1 is readed instead of port R1.

• R1 Pull-up Selection Register (R1PU)

	7	6	5	4	3	2	1	0	
R1PU	-	-	R1PU5	R1PU4	R1PU3	R1PU2	R1PU1	R1PU0	09h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	W	W	W	W	W	W	

R1 pull-up resistor control register (R1PU) is 6-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R1PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R1 Open Drain Selection Register (R1OD)

	7	6	5	4	3	2	1	0	
R1OD	-	-	R1OD5	R1OD4	R1OD3	R1OD2	R1OD1	R1OD0	0ah
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	W	W	W	W	W	W	

R1 Open Drain Selection Register (R1OD) is 6-bit register, and can assign R1 port as open drain output port each bit. If R1OD is selected as "0", port R1 is open drain output, and if selected as "1", it is push-pull output.

• R1 I/O Data Direction Register (R1DD)

	7	6	5	4	3	2	1	0	
R1DD	-	-	R1DD5	R1DD4	R1DD3	R1DD2	R1DD1	R1DD0	0bh
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

R1 I/O Data Direction Register (R1DD) is 6-bit register, and can assign input state or output state to each bit. If R1DD is "0", port R1 is in the input state, and if "1", it is in the output state.

• R1 Function Selection Register Low (R1FL)

	7	6	5	4	3	2	1	0	
R1FL	R13		R12		R11		R10		0ch
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

• R1 Function Selection Register High (R1FH)

	7	6	5	4	3	2	1	0	
R1FH	-		-		R15		R14		0dh
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	R/W	R/W	R/W	R/W	

Selection Mode of R1FL

Bit Name	Selection Mode		Remarks
R13	00	R13	
	01	KS10	
	10	T0	
	11	AN10	
R12	00	R12	
	01	KS9	
	10	T1	
	11	AN9	
R11	00	R11	
	01	KS8	
	10	-	
	11	AN8	
R10	00	R10	
	01	KS7	
	10	INT2(EC2)	
	11	AN7	

Selection Mode of R1FH

Bit Name	Selection Mode		Remarks
-	00	-	
	01	-	
	10	-	
	11	-	
-	00	-	
	01	-	
	10	-	
	11	-	
R15	00	R15	
	01	KS12	
	10	CLO	
	11	AN12	
R14	00	R14	
	01	KS11	
	10	-	
	11	AN11	

3.3. Port R2

• R2 Data Register (R2)

	7	6	5	4	3	2	1	0	
R2	-	-	R25	R24	R23	R22	R21	R20	10h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

R2 data register (R2) is 6-bit register to store data of port R2.
When set as the output state by R2DD, and data is written in R2, data is outputted into port R2.
When set as the input state, input state of port R2 is readed.
bit is read-modified operation. (SETR1/CLRR1 instruction)
At output state, if port R2 is readed, R2 is readed instead of port R2.

• R2 Pull-up Selection Register (R2PU)

	7	6	5	4	3	2	1	0	
R2PU	-	-	R2PU5	R2PU4	R2PU3	R2PU2	R2PU1	R2PU0	11h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	W	W	W	W	W	W	

R2 pull-up resistor control register (R2PU) is 6-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R2PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R2 Open Drain Selection Register (R2OD)

	7	6	5	4	3	2	1	0	
R2OD	-	-	R2OD5	R2OD4	R2OD3	R2OD2	R2OD1	R2OD0	12h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	W	W	W	W	W	W	

R2 Open Drain Selection Register (R2OD) is 6-bit register, and can assign R2 port as open drain output port each bit. If R2OD is selected as "0", port R2 is open drain output, and if selected as "1", it is push-pull output.

• R2 I/O Data Direction Register (R2DD)

	7	6	5	4	3	2	1	0	
R2DD	-	-	R2DD5	R2DD4	R2DD3	R2DD2	R2DD1	R2DD0	13h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

R2 I/O Data Direction Register (R2DD) is 6-bit register, and can assign input state or output state to each bit. If R2DD is "0", port R2 is in the input state, and if "1", it is in the output state.

• R2 Function selection Register (R2FN)

	7	6	5	4	3	2	1	0	
R2FN	-	-	R2FN5	R2FN4	R2FN3	R2FN2	R2FN1	R2FN0	14h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of R2FN

Bit Name	Selection Mode		Remarks
-	0	-	
	1	-	
-	0	-	
	1	-	
R2FN5	0	R25	
	1	AN15	
R2FN4	0	R24	
	1	AN14	
R2FN3	0	R23	
	1	AN13	
R2FN2	0	R22	
	1	TM01	
R2FN1	0	R21	
	1	TM12	
R2FN0	0	R20	
	1	T2	

3.4. Port R3

• R3 Data Register (R3)

	7	6	5	4	3	2	1	0	
R3	-	-	-	-	-	R32	R31	R30	18h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	-	-	-	R/W	R/W	R/W	

R3 data register (R3) is 3-bit register to store data of port R3.
When set as the output state by R3DD, and data is written in R3, data is outputted into port R3.
When set as the input state, input state of port R3 is readed.
bit is read-modified operation. (SETR1/CLRR1 instruction)
At output state, if port R3 is readed, R3 is readed instead of port R3.

• R3 Pull-up Selection Register (R3PU)

	7	6	5	4	3	2	1	0	
R3PU	-	-	-	-	-	R3PU2	R3PU1	R3PU0	19h
initial value	1	1	1	1	1	1	1	1	
R/W	-	-	-	-	-	W	W	W	

R3 pull-up resistor control register (R3PU) is 3-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R3PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R3 Open Drain Selection Register (R3OD)

	7	6	5	4	3	2	1	0	
R3OD	-	-	-	-	-	R3OD2	R3OD1	R3OD0	1ah
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	-	W	W	W	

R3 Open Drain Selection Register (R3OD) is 3-bit register, and can assign R3 port as open drain output port each bit. If R3OD is selected as "0", port R3 is open drain output, and if selected as "1", it is push-pull output.

• R3 I/O Data Direction Register (R3DD)

	7	6	5	4	3	2	1	0	
R3DD	-	-	-	-	-	R3DD2	R3DD1	R3DD0	1bh
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	-	R/W	R/W	R/W	

R3 I/O Data Direction Register (R3DD) is 3-bit register, and can assign input state or output state to each bit. If R3DD is "0", port R3 is in the input state, and if "1", it is in the output state.

• R3 Function selection Register (R3FN)

	7	6	5	4	3	2	1	0	
R3FN	-	-	-	-	-	R3FN2	R3FN1	R3FN0	1ch
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	-	R/W	R/W	R/W	

Selection Mode of R3FN

Bit Name	Selection Mode		Remarks
-	0	-	
	1	-	
-	0	-	
	1	-	
-	0	-	
	1	-	
-	0	-	
	1	-	
-	0	-	
	1	-	
R3FN2	0	High Voltage RESET Enable	if (V_{R32} >> VDD)
	1	High Voltage RESET Disable	
R3FN1	0	R31	
	1	Input with Pull-down	
R3FN0	0	R30	
	1	Input with Pull-down	

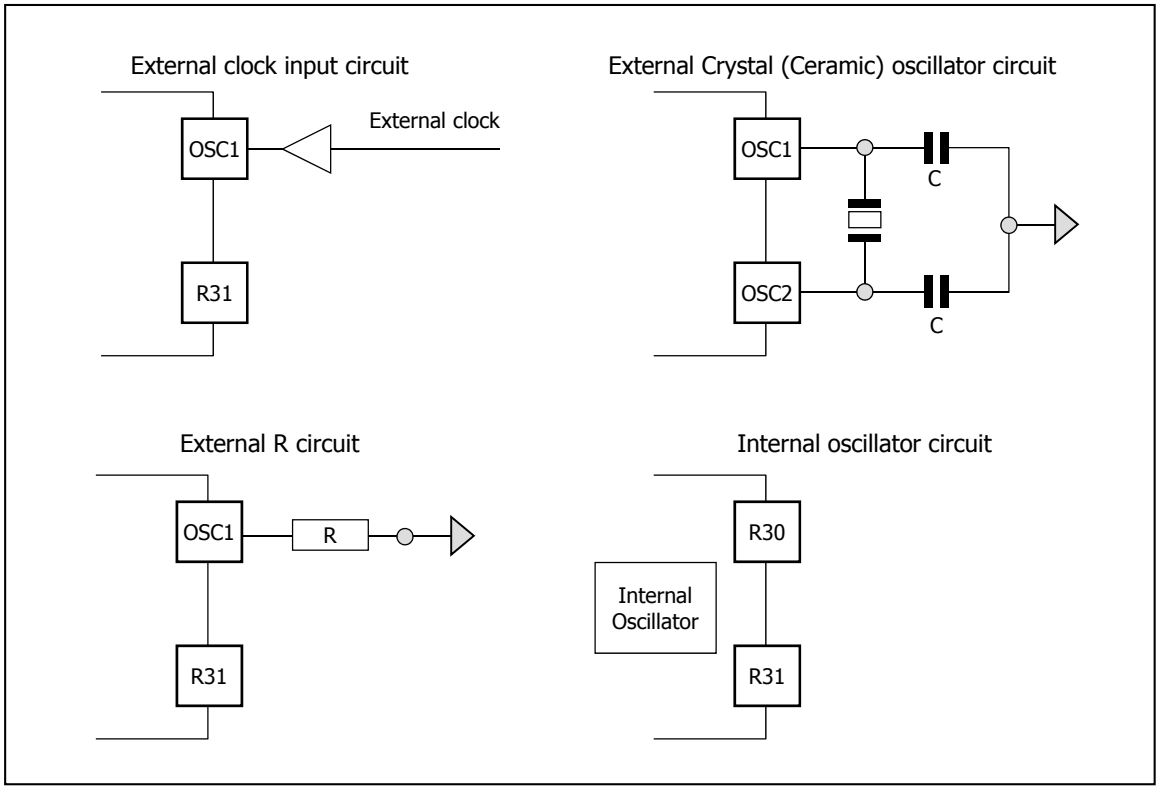
• Code Option (RESETB Selection)

Name	Option Value	Code Option Description	Operation
RSTS	1	RESETB/R32 Selection	RESETB
	0		R32

4.1. Oscillation Circuit

Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator. Fig. 4.1 shows circuit diagrams using a crystal (or ceramic) oscillator and external clock. Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.
Alternately, the oscillator may be driven from an external source as shown is Fig. 4.1.
In the STOP mode, oscillation stop, OSC2 state goes to "High", OSC1 state goes to "Low", and built-in feed back resistor is disabled.

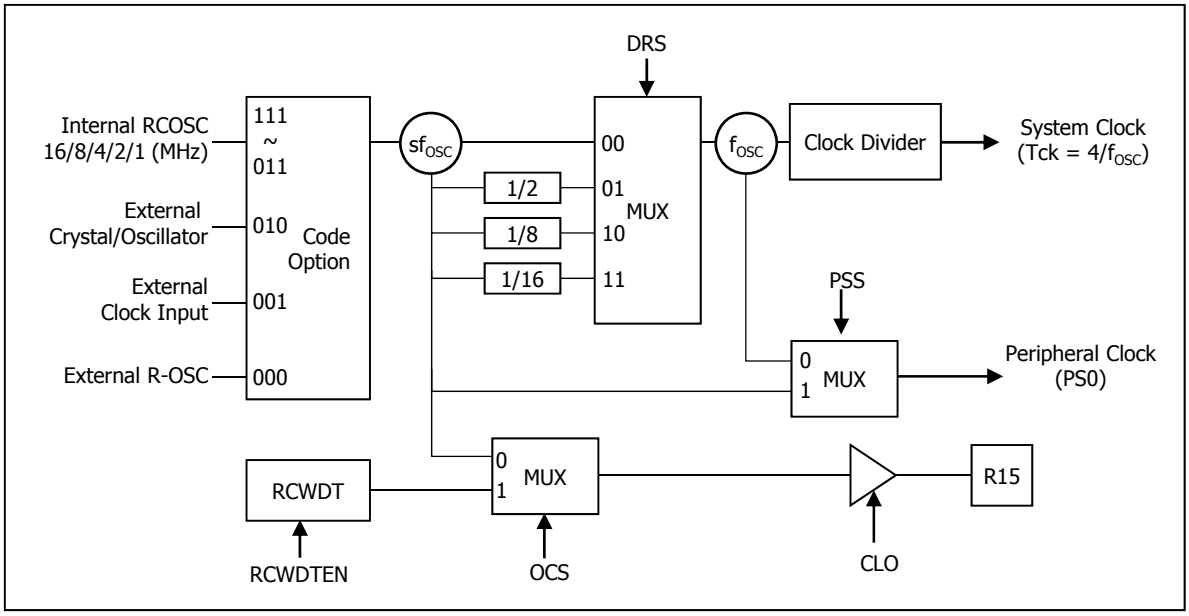
Fig. Pin Assignments of Oscillator configuration



• Code Option (Oscillator Selection)

Name	XTS[2:0]	SXT	Code Option Description	R30 Assign	R31 Assign
XTS	111	1	Internal RC 4MHz	R30(I/O)	R31(I/O)
	110	1	Internal RC 2MHz	R30(I/O)	R31(I/O)
	101	1	Internal RC 1MHz	R30(I/O)	R31(I/O)
	100	1	Internal RC 8MHz	R30(I/O)	R31(I/O)
	011	1	Internal RC 16MHz	R30(I/O)	R31(I/O)
	010	1	XT Oscillator	OSC1(I)	OSC2(O)
	001	1	External Clock Input	OSC1(I)	R31(I/O)
	000	1	External RC Oscillator	OSC1(I)	R31(I/O)
SXT	010	0	32.768KHz Oscillator	OSC1(I)	OSC2(O)

4.2. System Clock & Peripheral Clock Generator Block Diagram



• System Control Register

	7	6	5	4	3	2	1	0	
SCR	-	-	LVDDIS	OSCNF	PSS	OCS	DRS1	DRS0	63h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

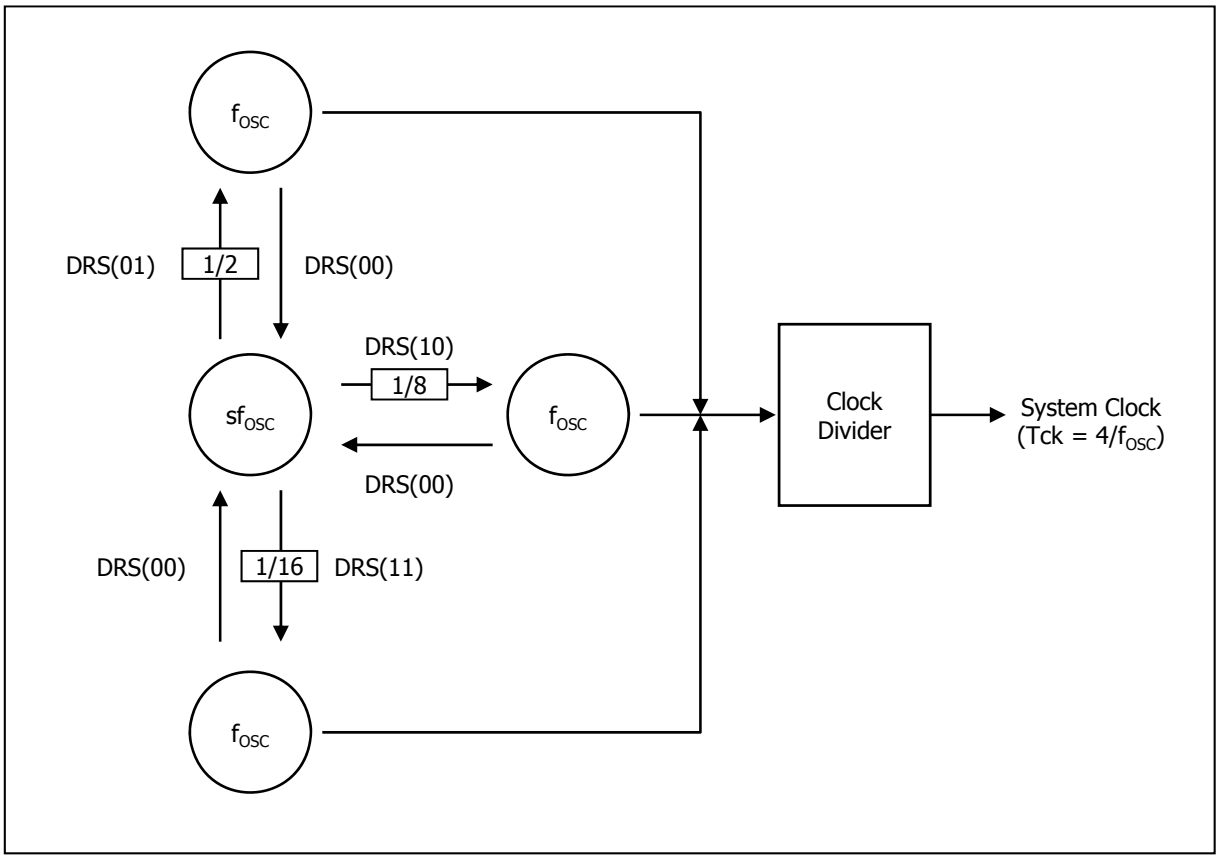
Selection Mode of SCR

Bit Name		Selection Mode		Remarks
LVDDIS	LVD Disable	0	Enable	*
		1	Disable	
OSCNF	OSC. Noise Filter Enable	0	Disable	*
		1	Enable	
PSS	Peripheral Clock Selection	0	f_{OSC} to PS0	*
		1	sf_{OSC} to PS0	
OCS	Output Clock Selection	0	sf_{OSC} Output	
		1	RCWDT Output	
DRS[1:0]	Divide Ratio Selection	00	sf_{OSC}	f_{OSC}
		01	$sf_{OSC}/2$	
		10	$sf_{OSC}/8$	
		11	$sf_{OSC}/16$	

• Selection of Peripheral Clock

Peripheral Clock Source	PSS=0				PSS=1	Remarks
	DRS=0 (fOSC=sfOSC)	DRS=1 (fOSC=sfOSC/2)	DRS=2 (fOSC=sfOSC/8)	DRS=3 (fOSC=sfOSC/16)	DRS=x (fOSC=sfOSC)	
PS0	fOSC	fOSC/2	fOSC/8	fOSC/16	fOSC	
PS1	fOSC/2	fOSC/4	fOSC/16	fOSC/32	fOSC/2	
PS2	fOSC/4	fOSC/8	fOSC/32	fOSC/64	fOSC/4	
PS3	fOSC/8	fOSC/16	fOSC/64	fOSC/128	fOSC/8	
PS4	fOSC/16	fOSC/32	fOSC/128	fOSC/256	fOSC/16	
PS5	fOSC/32	fOSC/64	fOSC/256	fOSC/512	fOSC/32	
PS6	fOSC/64	fOSC/128	fOSC/512	fOSC/1024	fOSC/64	
PS7	fOSC/128	fOSC/256	fOSC/1024	fOSC/2048	fOSC/128	
PS8	fOSC/256	fOSC/512	fOSC/2048	fOSC/4096	fOSC/256	

4.2.2. f_{OSC} Change Method



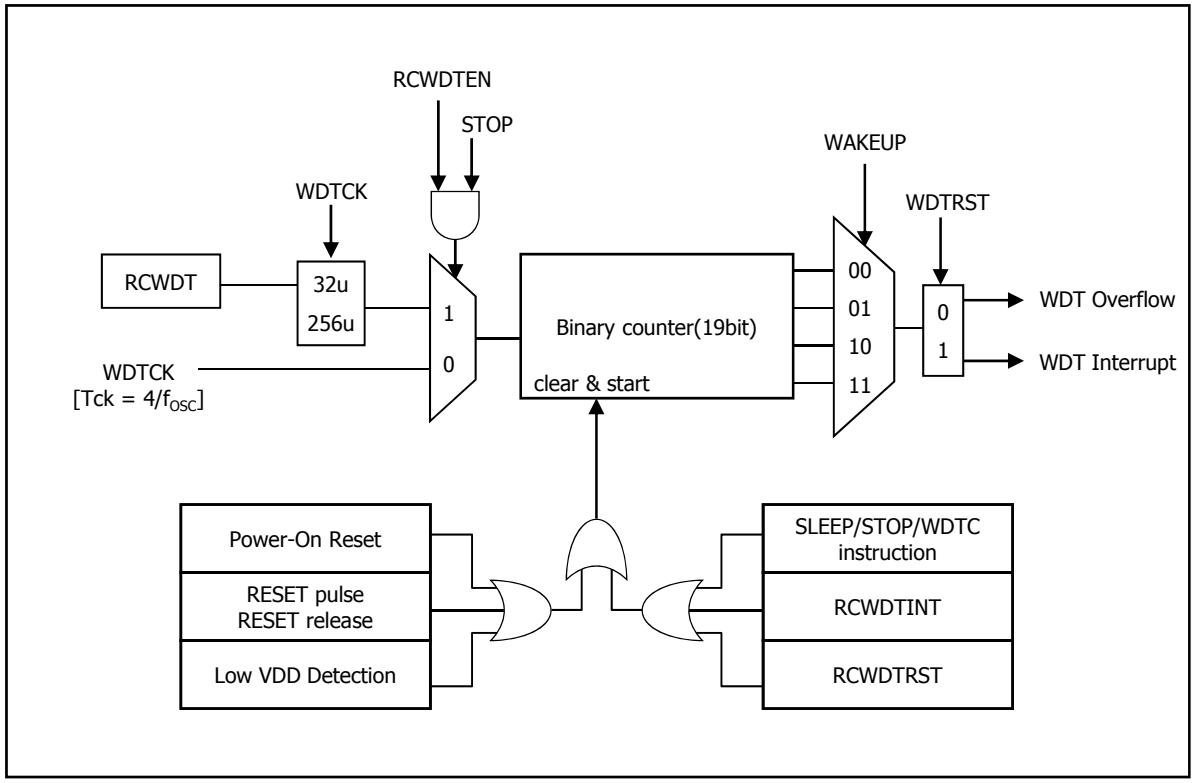
5.1. Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of Tck cycle comes in the first step of WDT after WDT reset.
If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized.
The overflow time is $2^{19} \times$ (Tck/2) (262.144ms at f_{OSC} = 4MHz) Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse.

* Tck = $4/f_{OSC}$

* It is constantly reset in STOP mode.
  When STOP is released by any stop release source, counting is restarted.
  After oscillation stabilization time $2^{15} \times$ (Tck/2) [16.384ms at f_{OSC} = 4MHz],
  STOP is released.

Fig. Block Diagram of Watch-dog Timer



• Watch Dog Timer overflow priod is

2^{19} x (Tck/2)

where, Tck = $4/f_{OSC}$

• WDT Control Register

	7	6	5	4	3	2	1	0	
WDTR	-	RCWDTEN	WDTRST	WDTCK	WAKEUP1	WAKEUP0	-	-	64h
initial value	0	0	0	0	0	0	0	0	
R/W	-	R/W	R/W	R/W	R/W	R/W	-	-	

Selection Mode of WDTR

Bit Name		Selection Mode		Remarks
RCWDTEN	WDT Mode Contol	0	WDT mode	
		1	RCWDT mode	@STOP
WDTRST	WDT Reset or Interrupt Control	0	WDT Reset	
		1	WDT Interrupt	
WDTCK	WDT Clock Selection	0	1us	(@4MHz)
		0	≒ 32us RCWDT	RCWDT mode
		1	≒ 256us RCWDT	
WAKEUP[1:0]	Reset or Interrupt Wakeup Time	00	(Tck/2) * 2^{19}	
		01	(Tck/2) * 2^{18}	
		10	(Tck/2) * 2^{17}	
		11	(Tck/2) * 2^{16}	
[1:0]	-	-	-	-

Reset or Interrupt Wakeup Time (f_{OSC})

(Tck = $4/f_{OSC}$ @4MHz)

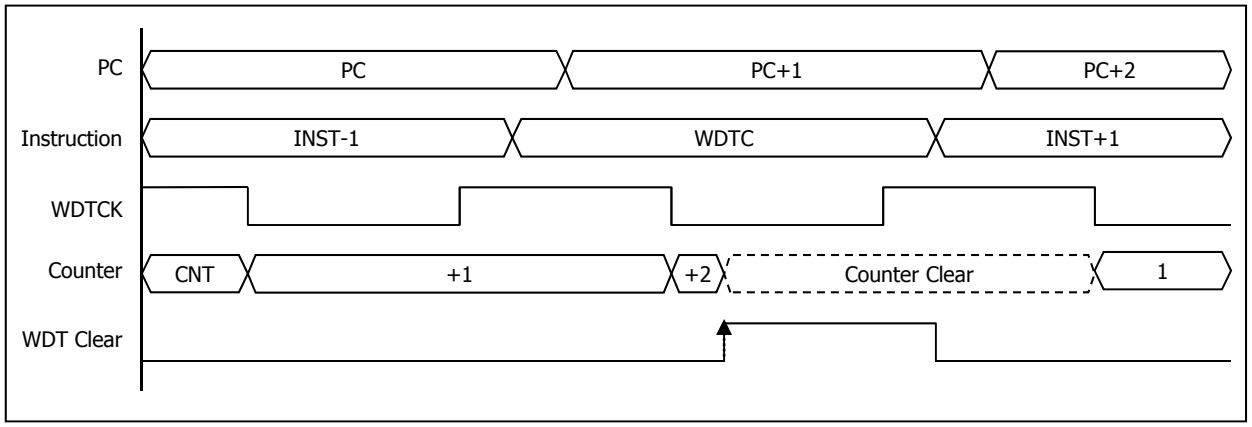
	(Tck/2) * 2^{19}	(Tck/2) * 2^{18}	(Tck/2) * 2^{17}	(Tck/2) * 2^{16}	Unit
Tck = 1us	262.144	131.072	65.536	32.768	ms

Reset or Interrupt Wakeup Time (f_{RCWDT})

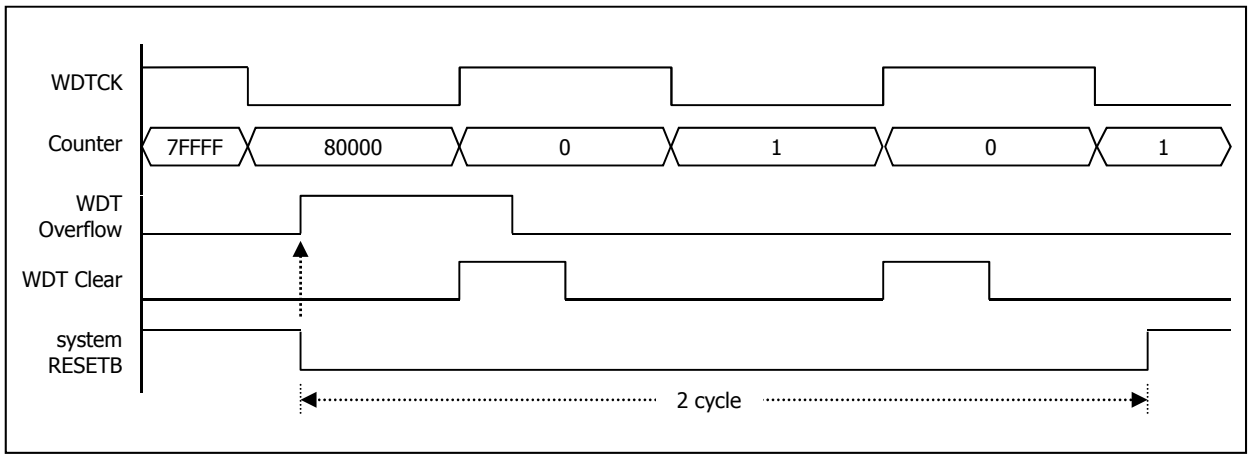
(T_{RCWDT})

	(T_{RCWDT}/2) * 2^{19}	(T_{RCWDT}/2) * 2^{18}	(T_{RCWDT}/2) * 2^{17}	(T_{RCWDT}/2) * 2^{16}	Unit
T_{RCWDT} ≒32us	≒ 8	≒ 4	≒ 2	≒ 1	s
T_{RCWDT} ≒ 256us	≒ 65	≒ 32	≒ 16	≒ 8	

* WDTC Timing Diagram



* Watch dog timer overflow RESET Timing Diagram



6.1. Timer

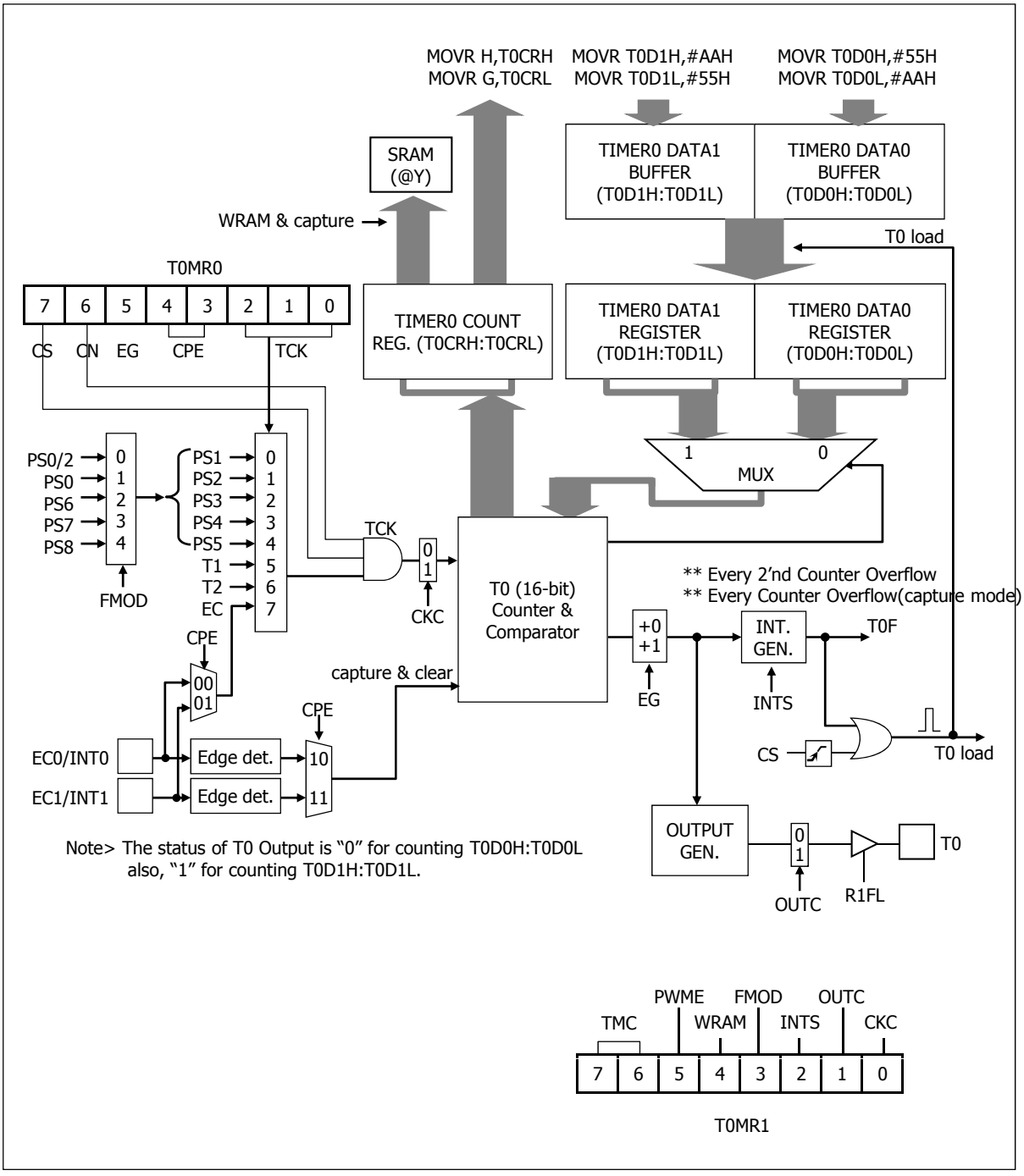
6.1.1. Timer operation mode

Timer is basically made of Timer Data/Counter Register, Timer Mode Register and control circuit. The types of Timer are 16bit Timer/Counter (Timer0, Timer1, Timer2).

Timer0	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output
Timer1	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output
Timer2	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output

6.2. Timer0

6.2.1. Timer0(T0) Block Diagram



6.2.2. Timer0 Control Register

• Timer0 Mode Register 0 (T0MR0)

	7	6	5	4	3	2	1	0	
T0MR0	T0CS	T0CN	T0EG	T0CPE1	T0CPE0	T0CK2	T0CK1	T0CK0	51h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR0 (f_{OSC} = 4MHz)

Bit Name			Selection Mode		Remarks
T0CS	Timer0 Clear / start Control	0	Timer0 Stop		
		1	Timer0 Clear and Start		
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause		
		1	Timer0 continue		
T0EG	Timer0 Count Control	0	Timer0 Count		
		1	Timer0 Count + 1		
T0CPE1 T0CPE0	Input capture & Event Count selection	00	EC0		
		01	EC1		
		10	Capture 0 (INT0)		
		11	Capture 1 (INT1)		
T0CK2 T0CK1 T0CK0	Input clock selection	000	PS1 (0.5us)	*PS0/2	*FMODE
		001	PS2 (1us)	*PS0 (0.25us)	
		010	PS3 (2us)	*PS6 (16us)	
		011	PS4 (4us)	*PS7 (32us)	
		100	PS5 (8us)	*PS8 (64us)	
		101	T1		
		110	T2		
		111	EC (EC0 or EC1)		

• Timer0 Mode Register 1 (T0MR1)

	7	6	5	4	3	2	1	0	
T0MR1	T0MC1	T0MC0	PWME0	WRAM0	FMOD0	INTS0	OUTC0	CKC0	52h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR1

Bit Name			Selection Mode	Remarks
T0MC1 T0MC0	mPWM Control	00	Logical 'AND' of Timer0 output and Timer1 output	
		01	Logical 'OR' of Timer0 output and Timer1 output	
		10	Logical 'NAND' of Timer0 output and Timer1 output	
		11	Logical 'NOR' of Timer0 output and Timer1 output	
PWME0	Timer/PWM Mode Selection	0	Timer0 Normal Mode	
		1	Timer0 PWM Mode	
WRAM0	Automatically Save Capture data to RAM	0	Disable	
		1	Timer0 Automatically Save Capture data to RAM	
FMOD0	Fast Mode Selection	0	Timer0 Normal Mode	
		1	Timer0 Fast Mode	
INTS0	Timer0 Interrupt Overflow Control	0	Timer0 Interrupt Every 2nd Overflow	
		1	Timer0 Interrupt Every Overflow	
OUTC0	Timer0 Output Control	0	Timer0 Output Normal	
		1	Timer0 Output Reverse	
CKC0	Timer0 Input Clock Control	0	Timer0 Input Clock Normal	
		1	Timer0 Input Clock Reverse	

Note: Save 2bytes capture data to RAM (2cycle) - addressed by @Y++., T0CRL saved first.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T0CRL	T0CRH	T0CRL	T0CRH	T0CRL	T0CRH	T0CRL	T0CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

- Timer0 Data0 Register Low (T0D0L) = PWM0 DUTY

	7	6	5	4	3	2	1	0	
T0D0L	T0D0L7	T0D0L6	T0D0L5	T0D0L4	T0D0L3	T0D0L2	T0D0L1	T0D0L0	53h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

- Timer0 Count Register Low (T0CRL)

	7	6	5	4	3	2	1	0	
T0CRL	T0CRL7	T0CRL6	T0CRL5	T0CRL4	T0CRL3	T0CRL2	T0CRL1	T0CRL0	53h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

Note: At 16bit counter value read, Must be read T0CRL first.

- Timer0 Data1 Register Low (T0D1L) = PWM0 PERIOD

	7	6	5	4	3	2	1	0	
T0D1L	T0D1L7	T0D1L6	T0D1L5	T0D1L4	T0D1L3	T0D1L2	T0D1L1	T0D1L0	54h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer0 Data0 Register High (T0D0H) = PWM0 DUTY EXTENSION

	7	6	5	4	3	2	1	0	
T0D0H	T0D0H7	T0D0H6	T0D0H5	T0D0H4	T0D0H3	T0D0H2	T0D0H1	T0D0H0	55h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer0 Count Register High (T0CRH)

	7	6	5	4	3	2	1	0	
T0CRH	T0CRH7	T0CRH6	T0CRH5	T0CRH4	T0CRH3	T0CRH2	T0CRH1	T0CRH0	55h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

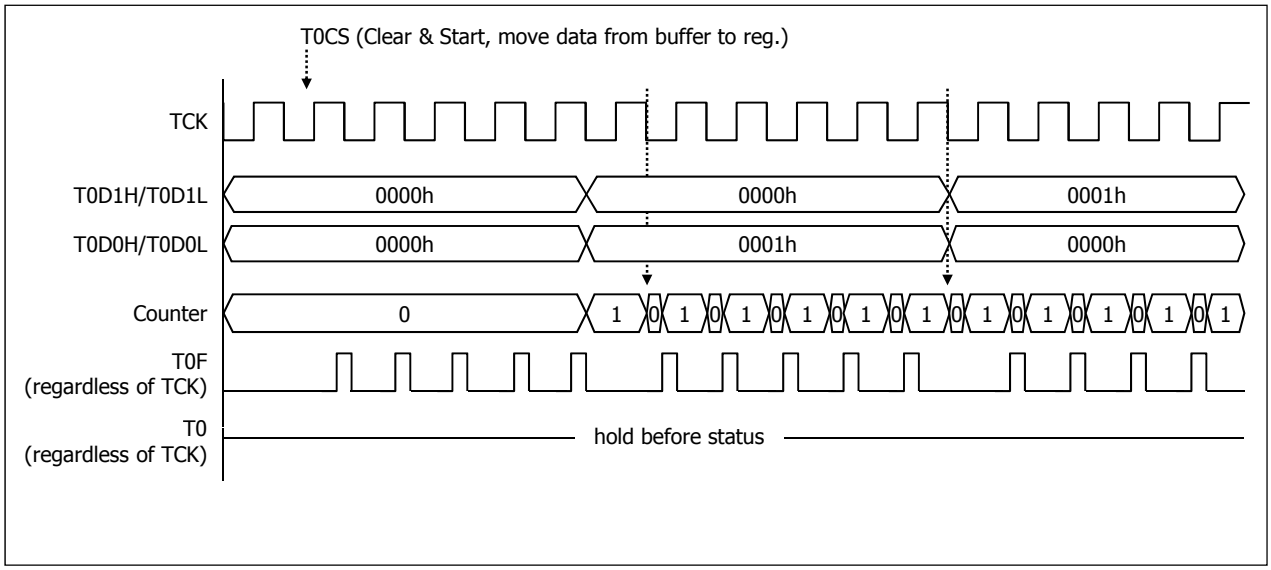
Note: At 16bit counter value read, Must be read T0CRL first.

• Timer0 Data1 Register High (T0D1H) = PWM0 CYCLE

	7	6	5	4	3	2	1	0	
T0D1H	T0D1H7	T0D1H6	T0D1H5	T0D1H4	T0D1H3	T0D1H2	T0D1H1	T0D1H0	56h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

6.2.3. Timer0 Caution

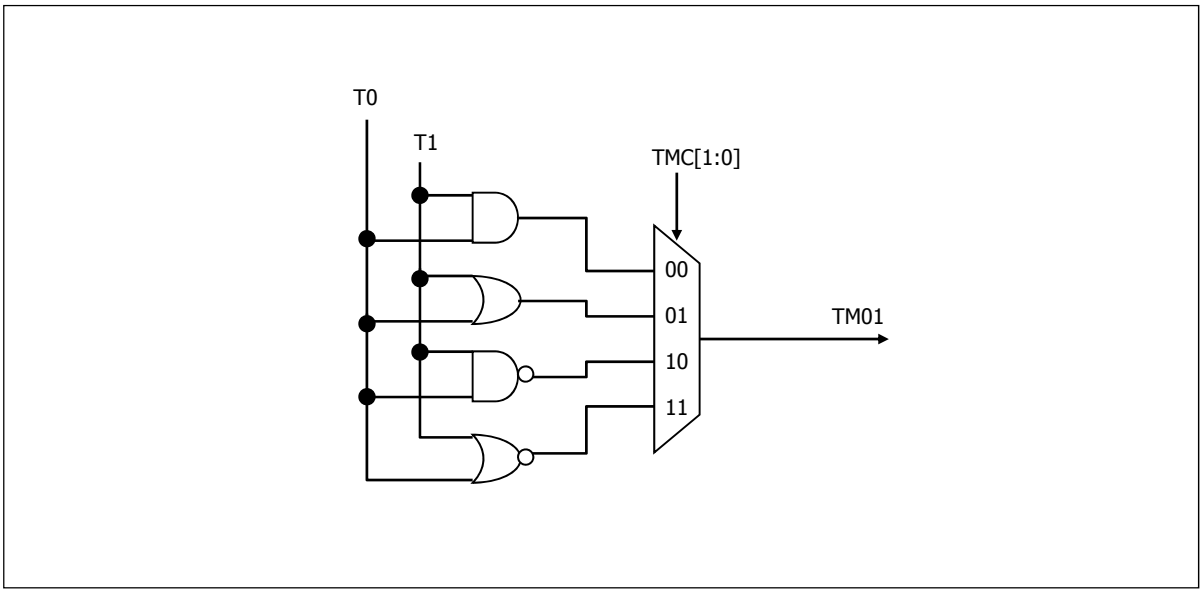
Caution : In the case of T0EG is "0",



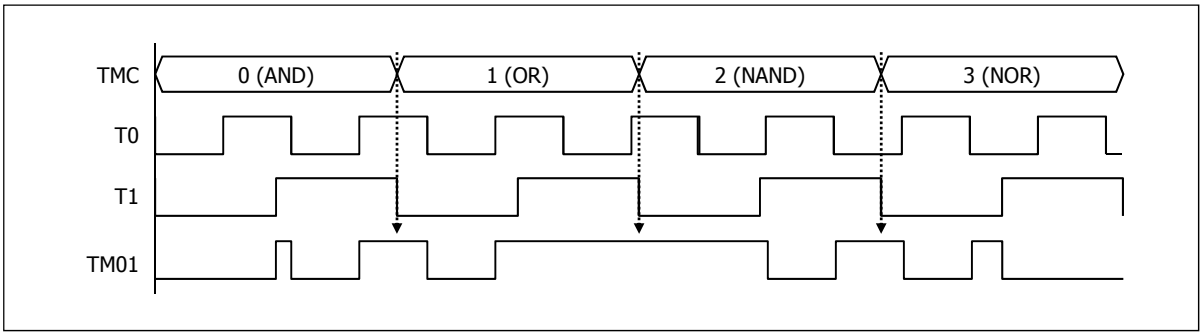
Want to count "0", set T0EG=1

6.2.4. TM01 Mode

* TM01 Logical Output Control

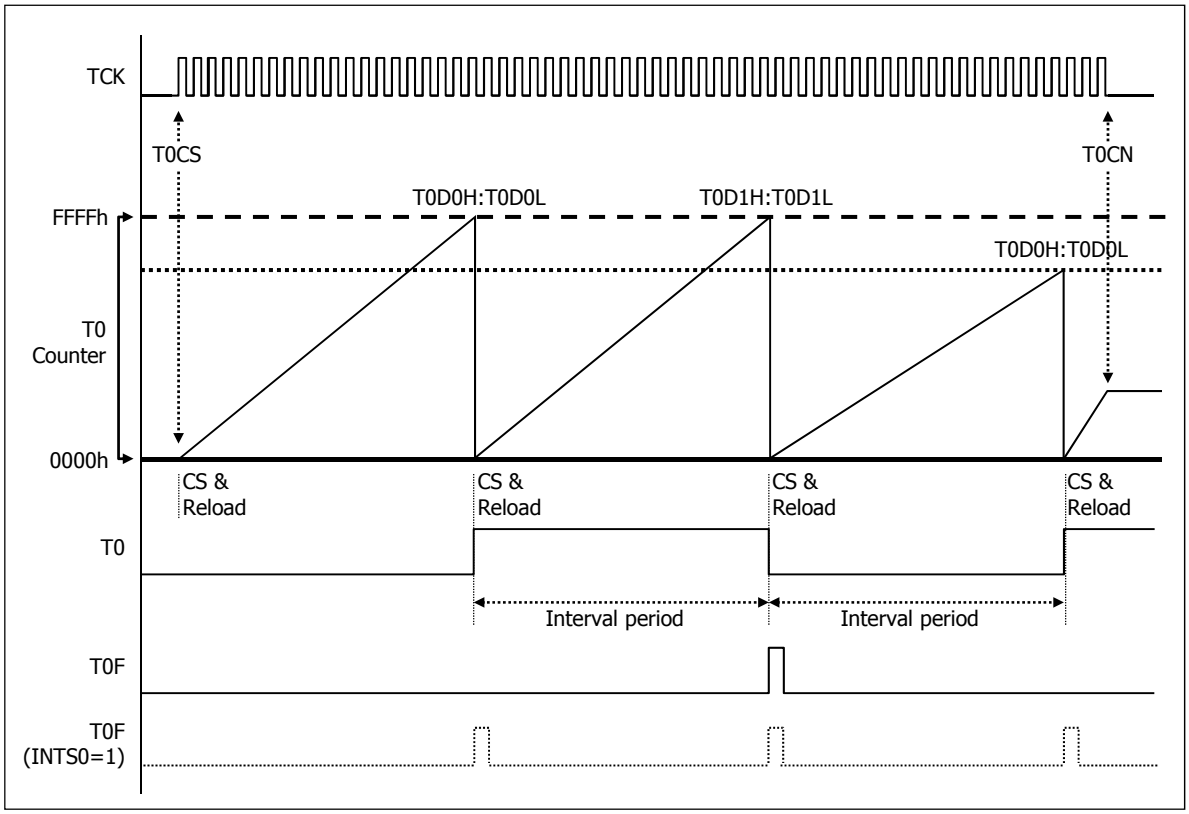


* TM01 mode Timing Diagram



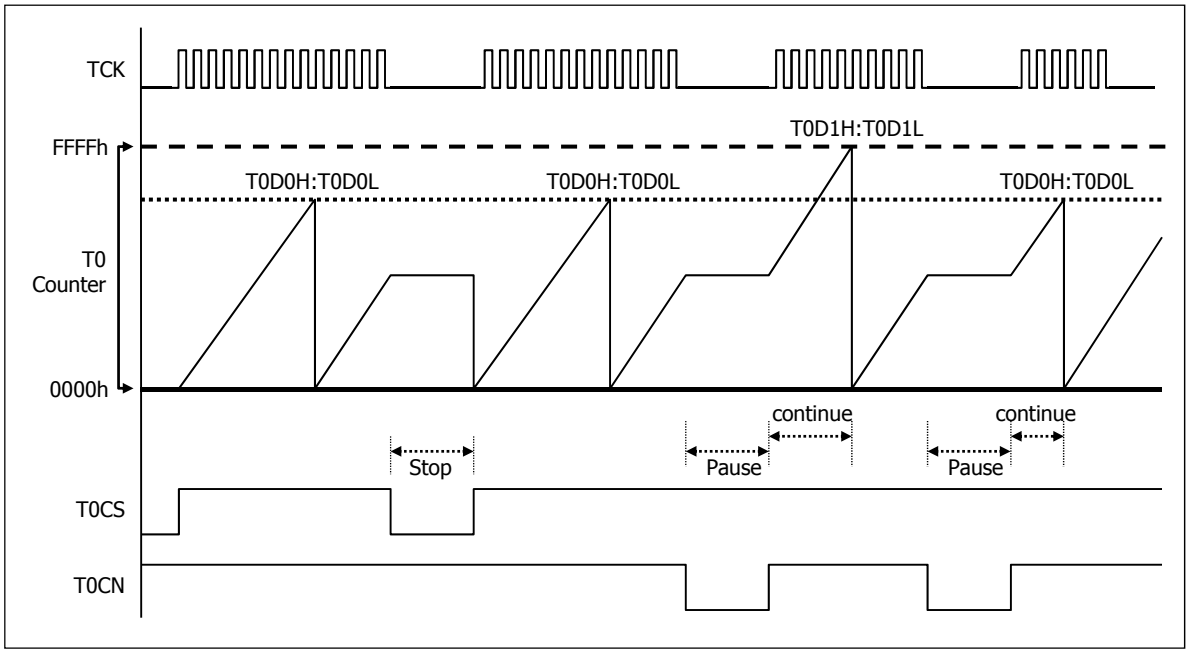
6.2.5. Timer0 Timing Diagram

* 16-bit Timer/Counter mode Timing Diagram

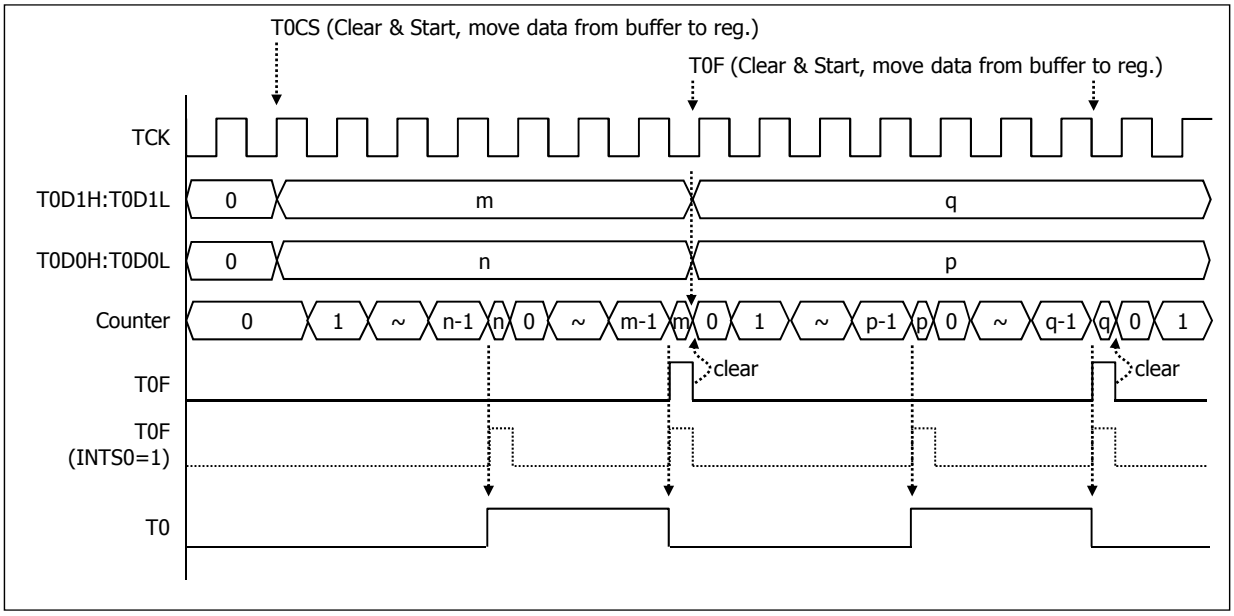


Note > CS : Timer0 Counter Clear & Start.
Reload : Timer0 Data move from Data buffer to Data register.

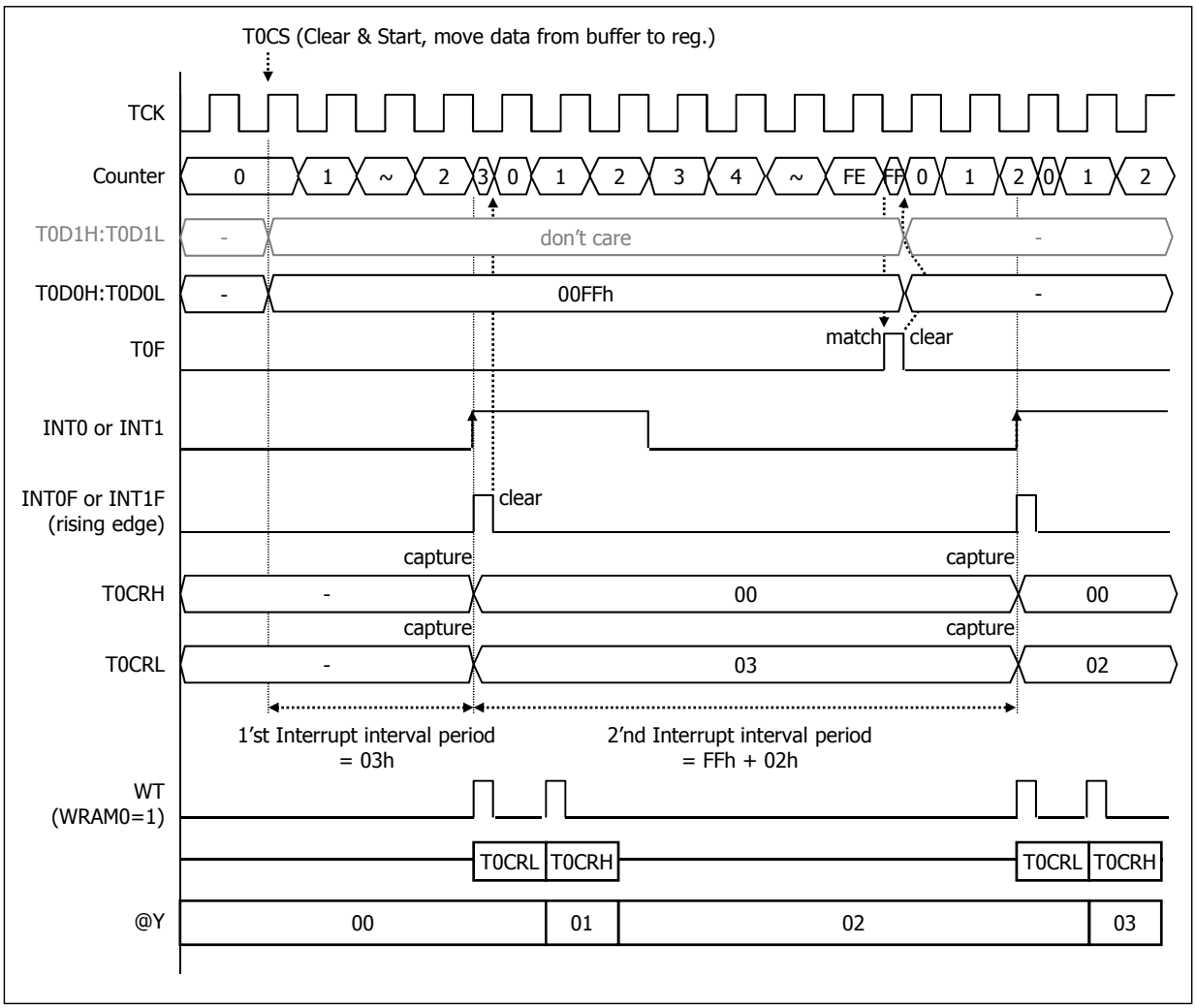
* Start / Stop operation



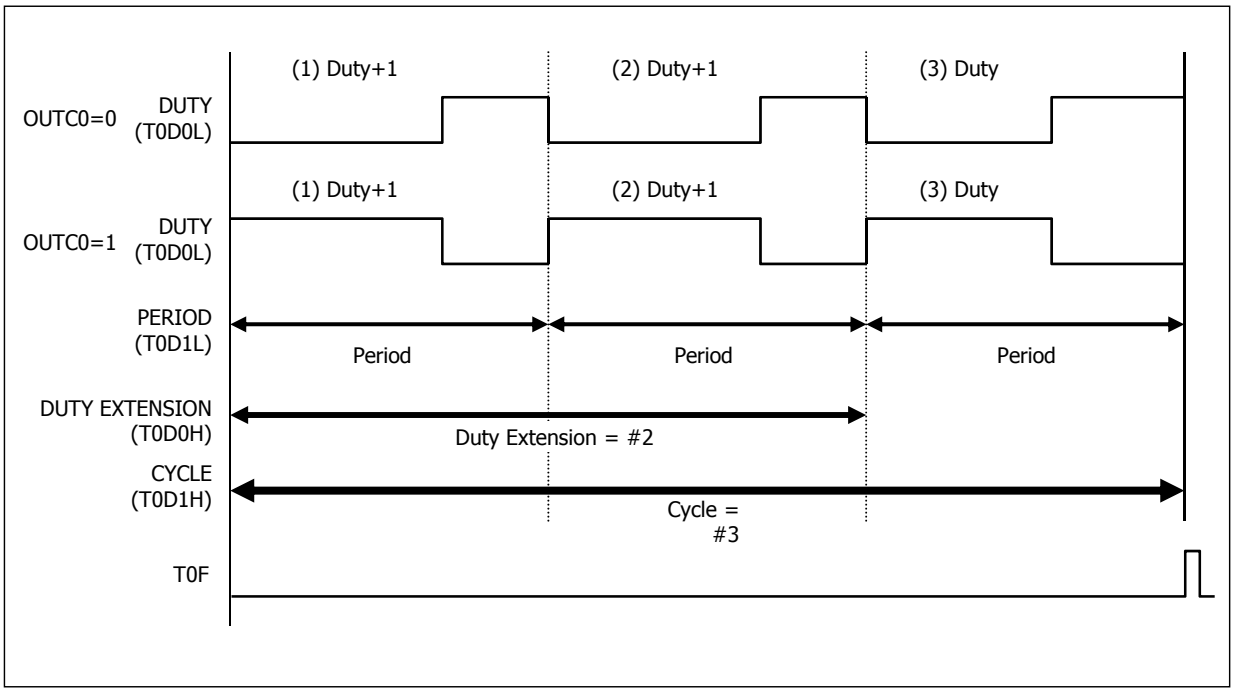
* 16-bit Timer/Counter mode Timing Diagram



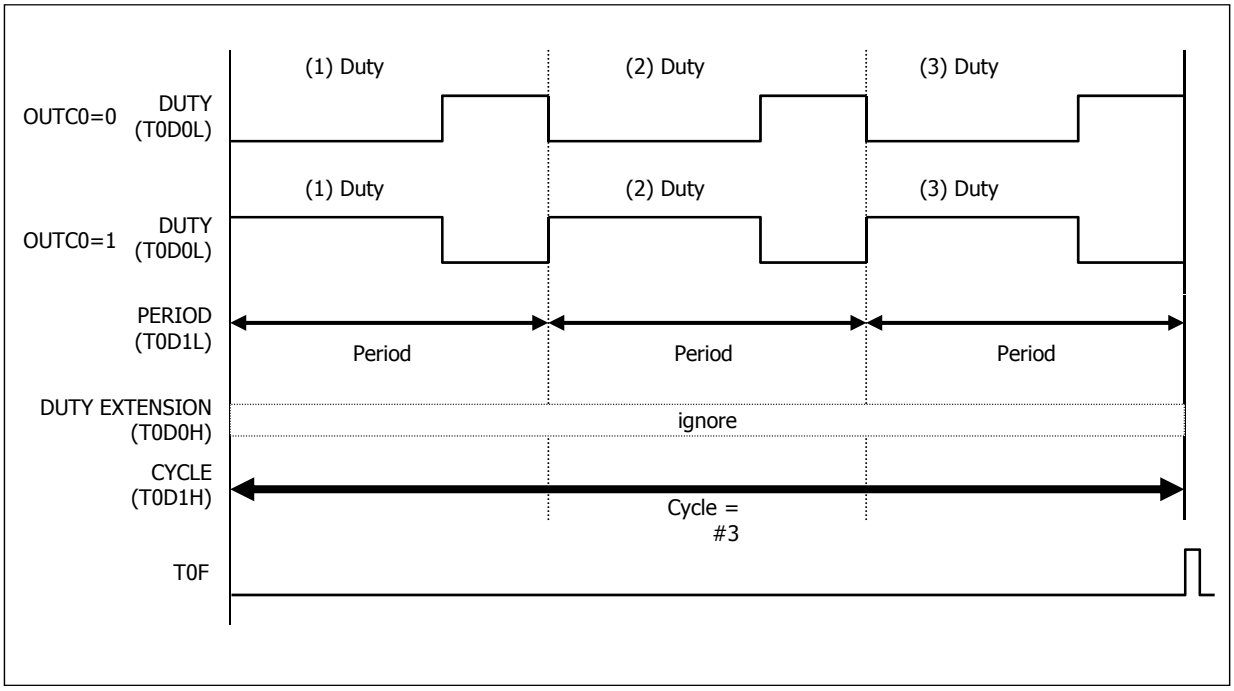
* 16-bit Capture mode Timing Diagram



• PWM mode Timing Diagram : (T0EG=0)



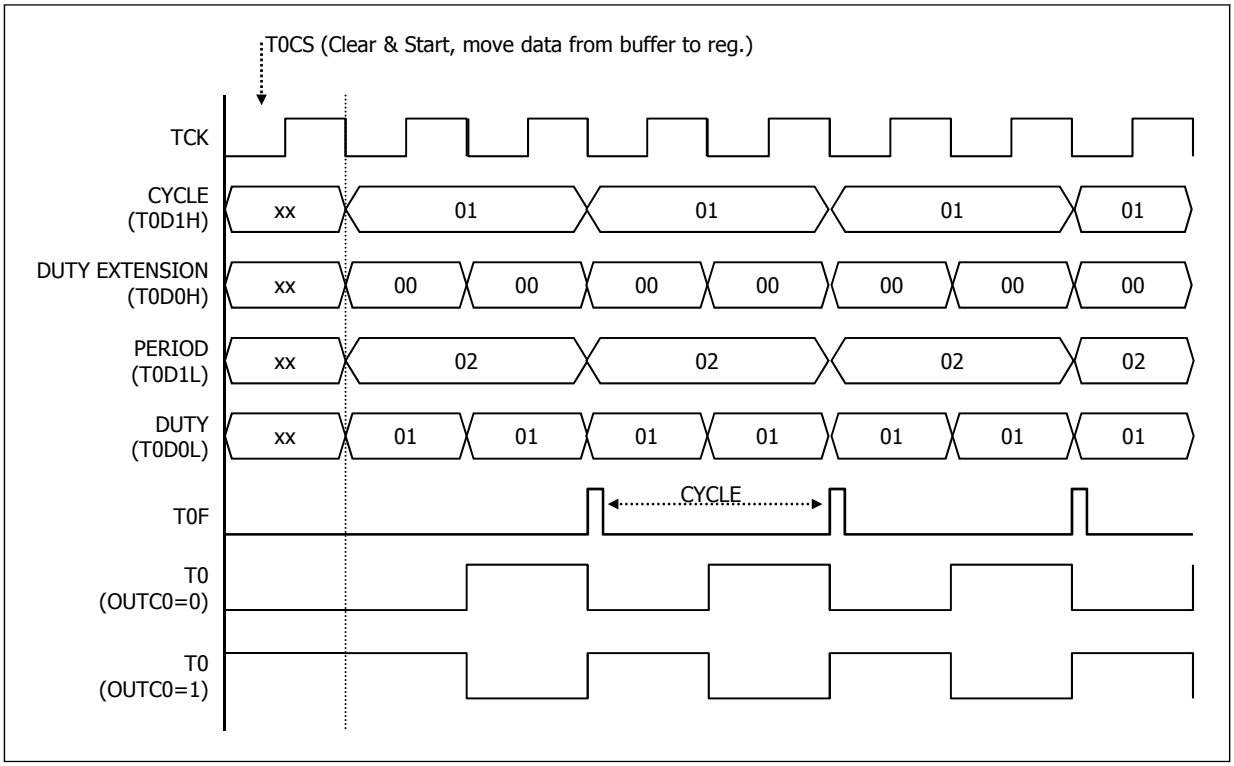
• PWM mode Timing Diagram : (T0EG=1)



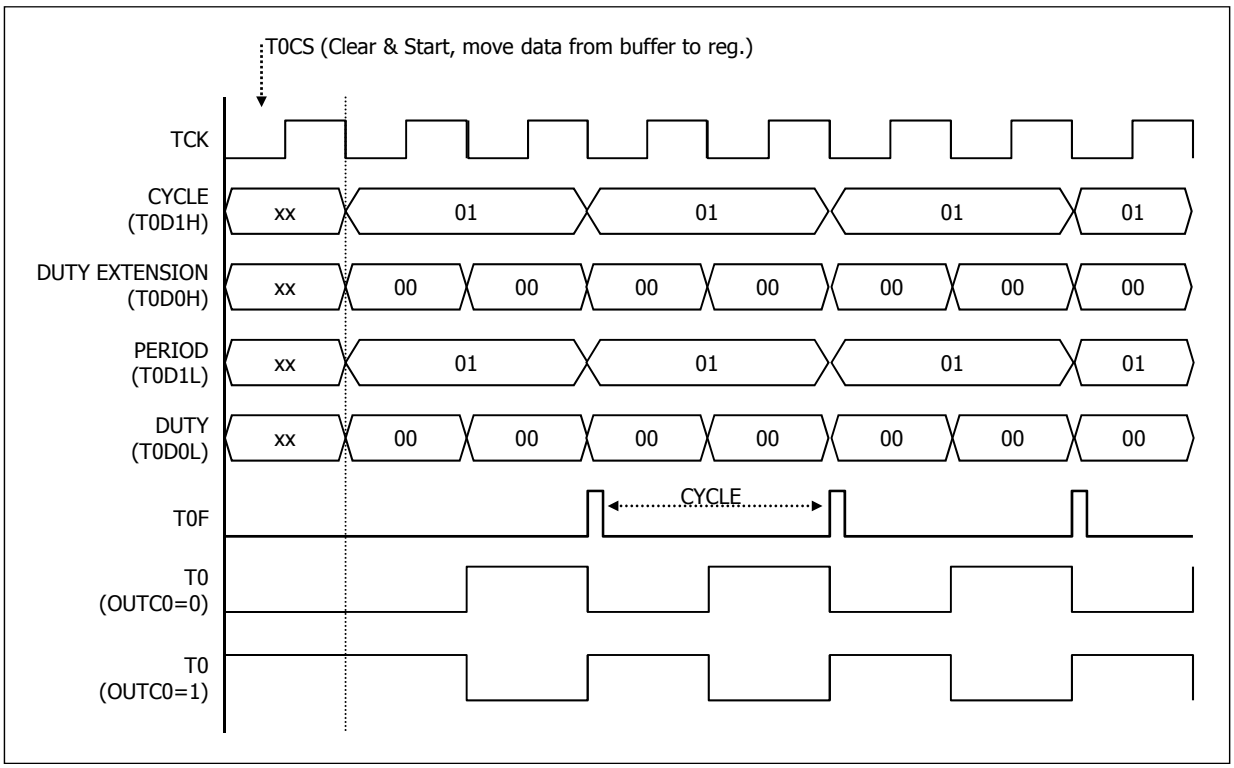
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• PWM mode Timing Diagram : (T0EG=0, DUTY EXTENSION=0)



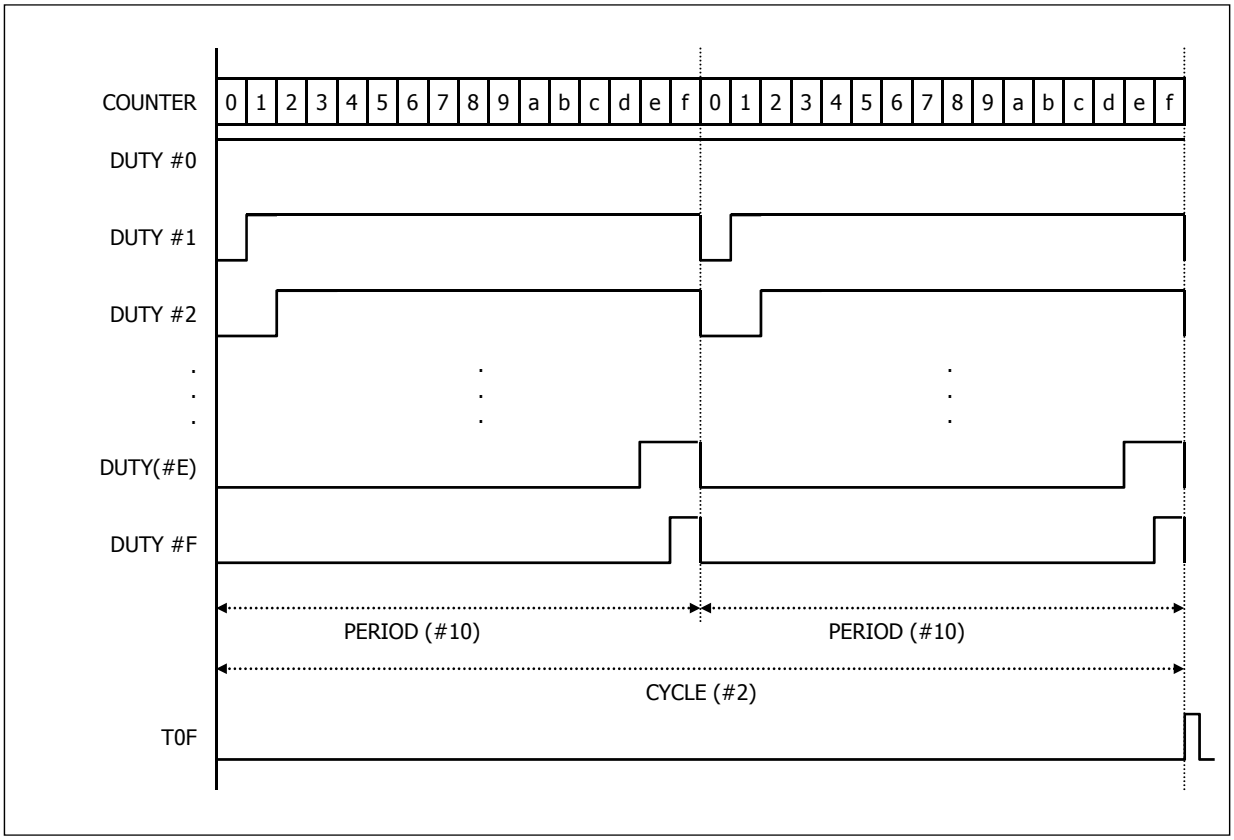
• PWM mode Timing Diagram : (T0EG=1, DUTY EXTENSION=0)



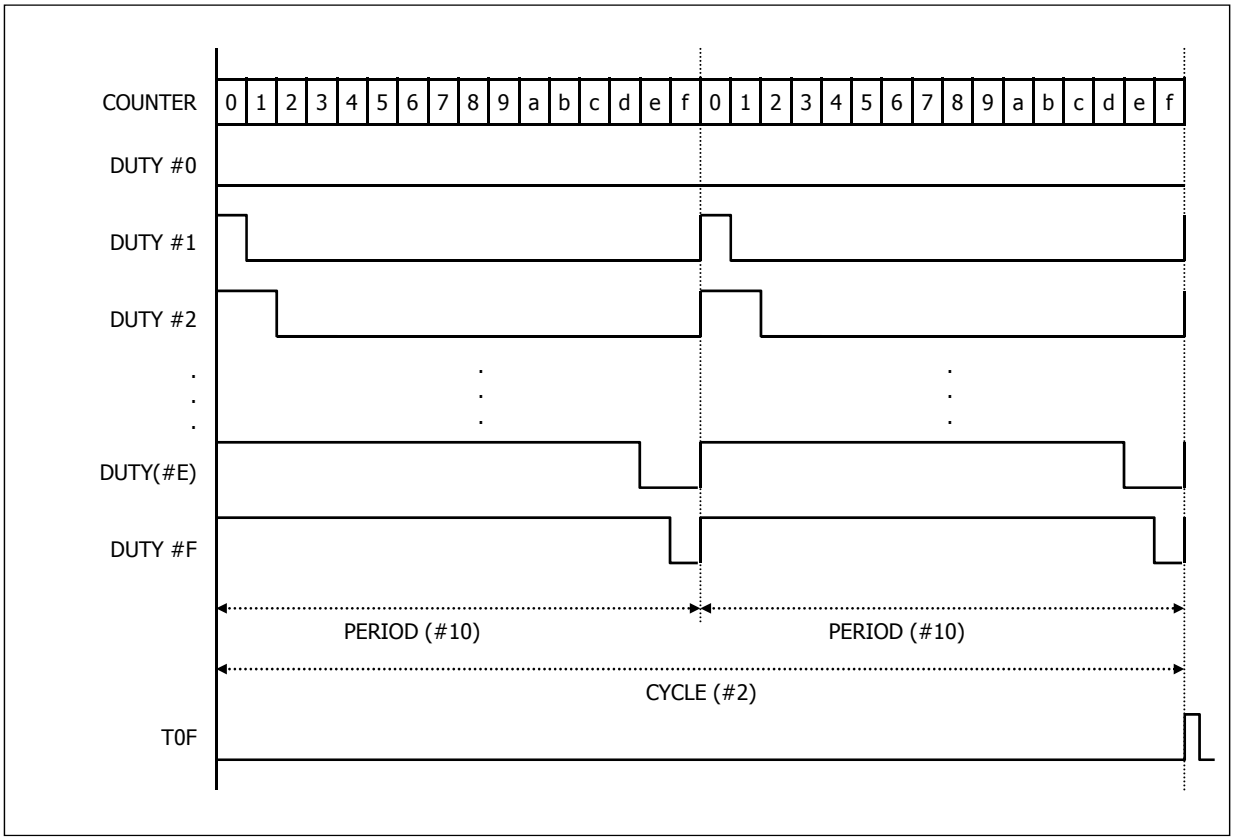
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

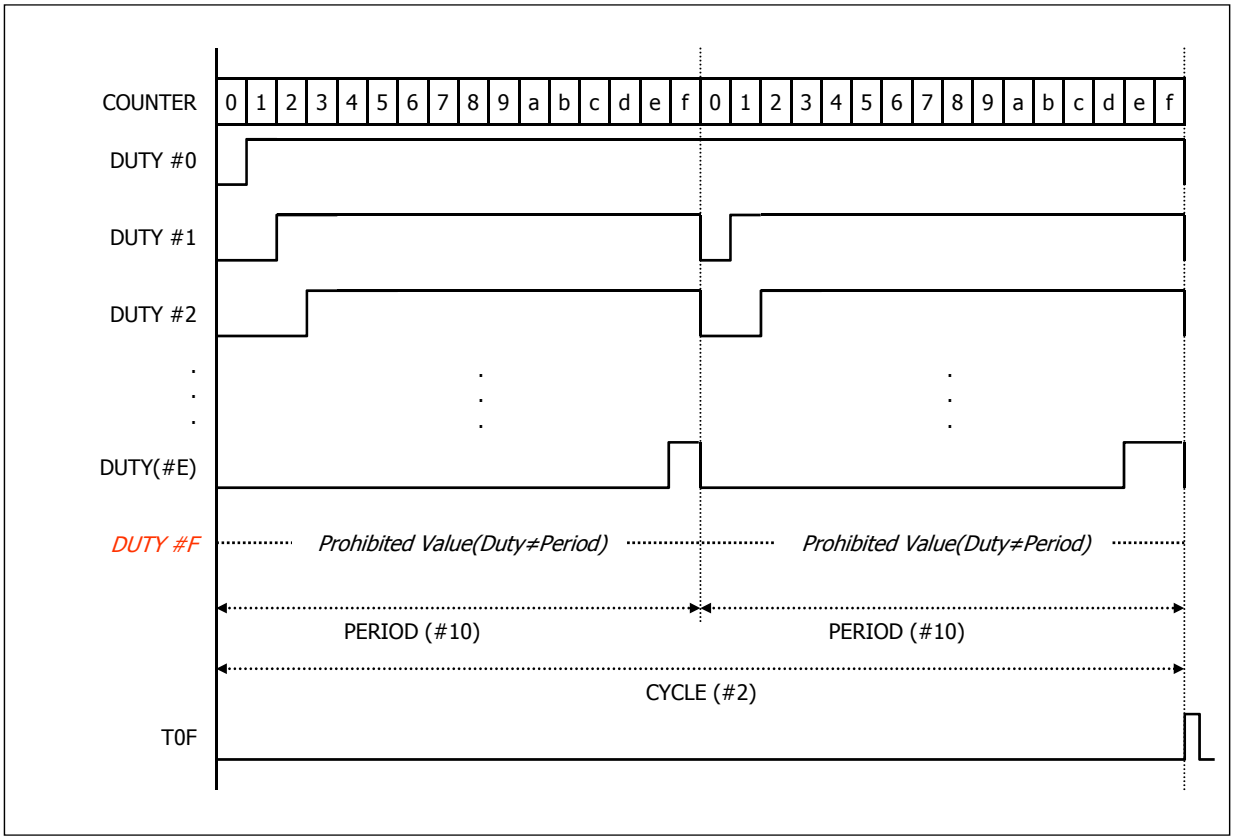
• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=0)



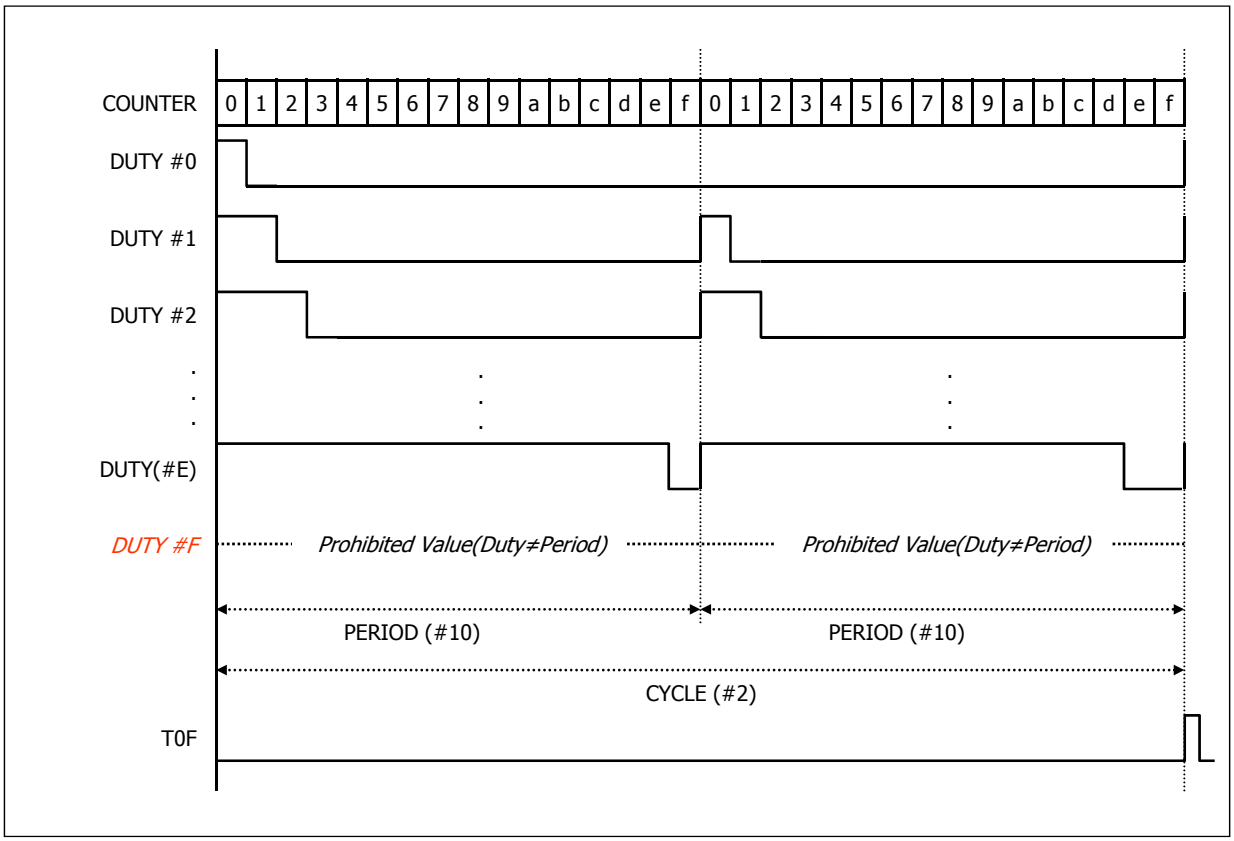
• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=0)



• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=1)

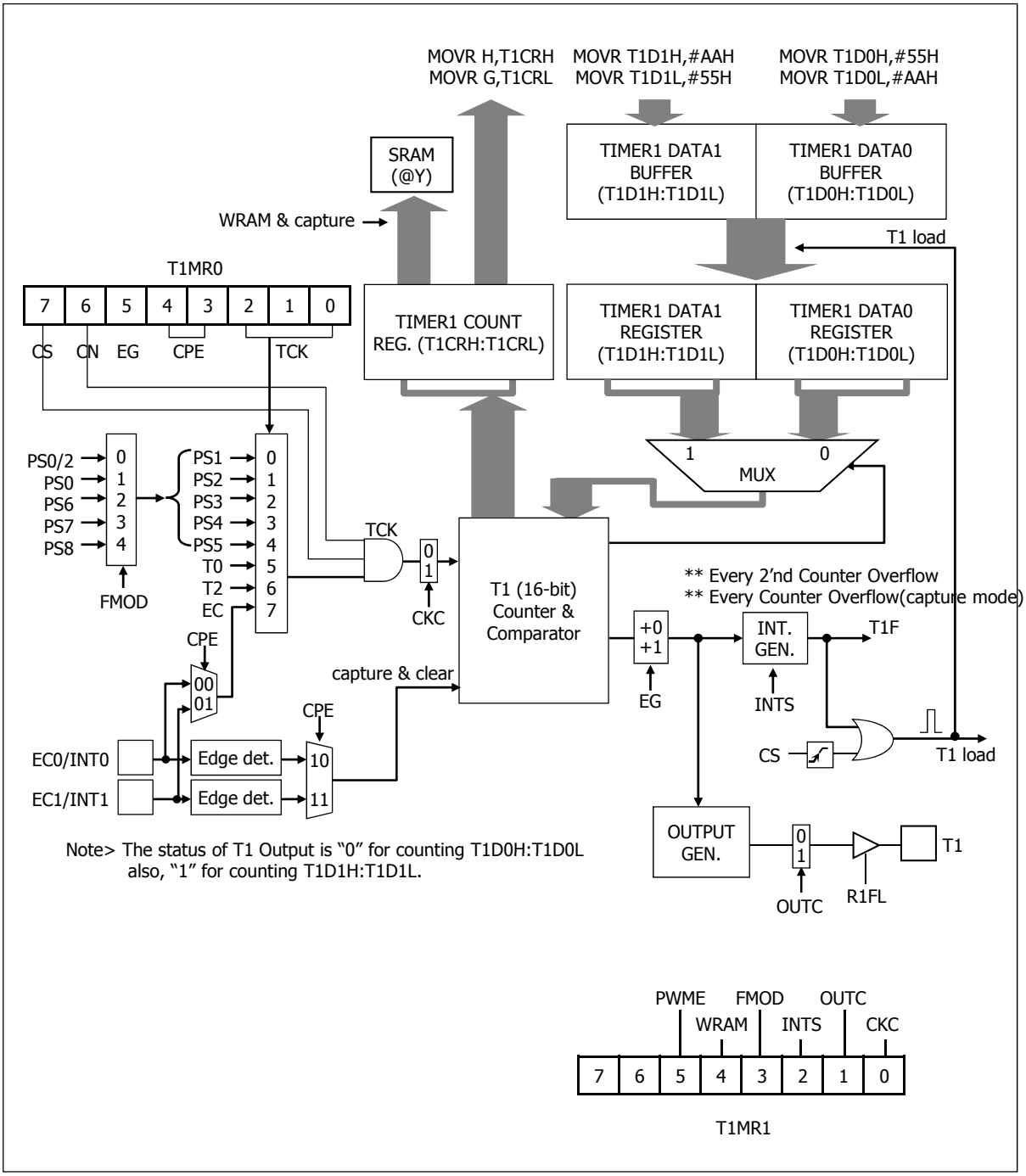


• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=1)



6.3. Timer1

6.3.1. Timer1(T1) Block Diagram



6.3.2. Timer1 Control Register

• Timer1 Mode Register 0 (T1MR0)

	7	6	5	4	3	2	1	0	
T1MR0	T1CS	T1CN	T1EG	T1CPE1	T1CPE0	T1CK2	T1CK1	T1CK0	57h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR0 (f_{OSC} = 4MHz)

Bit Name			Selection Mode		Remarks
T1CS	Timer1 Clear / start Control	0	Timer1 Stop		
		1	Timer1 Clear and Start		
T1CN	Timer1 Pause / Continue Control	0	Timer1 Pause		
		1	Timer1 continue		
T1EG	Timer1 Count Control	0	Timer1 Count		
		1	Timer1 Count + 1		
T1CPE1 T1CPE0	Input capture & Event Count selection	00	EC0		
		01	EC1		
		10	Capture 0 (INT0)		
		11	Capture 1 (INT1)		
T1CK2 T1CK1 T1CK0	Input clock selection	000	PS1 (0.5us)	*PS0/2	*FMODE
		001	PS2 (1us)	*PS0 (0.25us)	
		010	PS3 (2us)	*PS6 (16us)	
		011	PS4 (4us)	*PS7 (32us)	
		100	PS5 (8us)	*PS8 (64us)	
		101	T0		
		110	T2		
		111	EC (EC0 or EC1)		

• Timer1 Mode Register 1 (T1MR1)

	7	6	5	4	3	2	1	0	
T1MR1	-	-	PWME1	WRAM1	FMOD1	INTS1	OUTC1	CKC1	58h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR1

Bit Name			Selection Mode	Remarks
PWME1	Timer/PWM Mode Selection	0	Timer1 Normal Mode	
		1	Timer1 PWM Mode	
WRAM1	Automatically Save Capture data to RAM	0	Disable	
		1	Timer1 Automatically Save Capture data to RAM	
FMOD1	Fast Mode Selection	0	Timer1 Normal Mode	
		1	Timer1 Fast Mode	
INTS1	Timer1 Interrupt Overflow Control	0	Timer1 Interrupt Every 2nd Overflow	
		1	Timer1 Interrupt Every Overflow	
OUTC1	Timer1 Output Control	0	Timer1 Output Normal	
		1	Timer1 Output Reverse	
CKC1	Timer1 Input Clock Control	0	Timer1 Input Clock Normal	
		1	Timer1 Input Clock Reverse	

Note: 16bit Timer : Save 2bytes capture data to RAM (2cycle) - addressed by @Y++.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

• Timer1 Data0 Register Low (T1D0L) = PWM1 DUTY

	7	6	5	4	3	2	1	0	
T1D0L	T1D0L7	T1D0L6	T1D0L5	T1D0L4	T1D0L3	T1D0L2	T1D0L1	T1D0L0	59h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer1 Count Register Low (T1CRL)

	7	6	5	4	3	2	1	0	
T1CRL	T1CRL7	T1CRL6	T1CRL5	T1CRL4	T1CRL3	T1CRL2	T1CRL1	T1CRL0	59h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

Note: At 16bit counter value read, Must be read T1CRL first.

• Timer1 Data1 Register Low (T1D1L) = PWM1 PERIOD

	7	6	5	4	3	2	1	0	
T1D1L	T1D1L7	T1D1L6	T1D1L5	T1D1L4	T1D1L3	T1D1L2	T1D1L1	T1D1L0	5ah
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer1 Data0 Register High (T1D0H) = PWM1 DUTY EXTENSION

	7	6	5	4	3	2	1	0	
T1D0H	T1D0H7	T1D0H6	T1D0H5	T1D0H4	T1D0H3	T1D0H2	T1D0H1	T1D0H0	5bh
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer1 Count Register High (T1CRH)

	7	6	5	4	3	2	1	0	
T1CRH	T1CRH7	T1CRH6	T1CRH5	T1CRH4	T1CRH3	T1CRH2	T1CRH1	T1CRH0	5bh
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

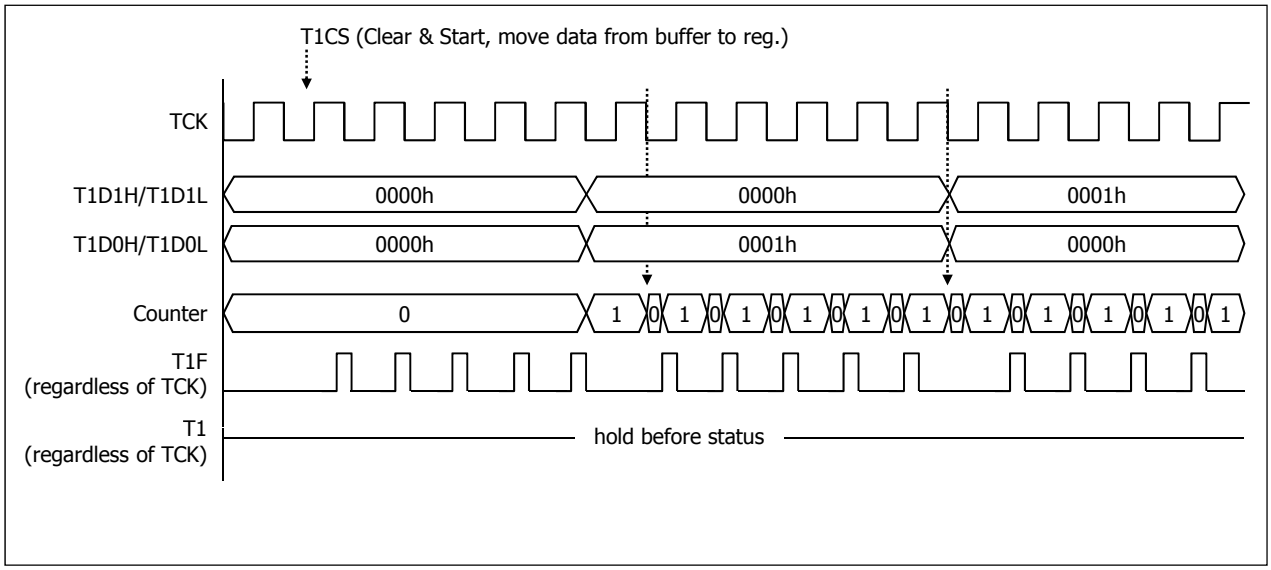
Note: At 16bit counter value read, Must be read T1CRL first.

• Timer1 Data1 Register High (T1D1H) = PWM1 CYCLE

	7	6	5	4	3	2	1	0	
T1D1H	T1D1H7	T1D1H6	T1D1H5	T1D1H4	T1D1H3	T1D1H2	T1D1H1	T1D1H0	5ch
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

6.3.3. Timer1 Caution

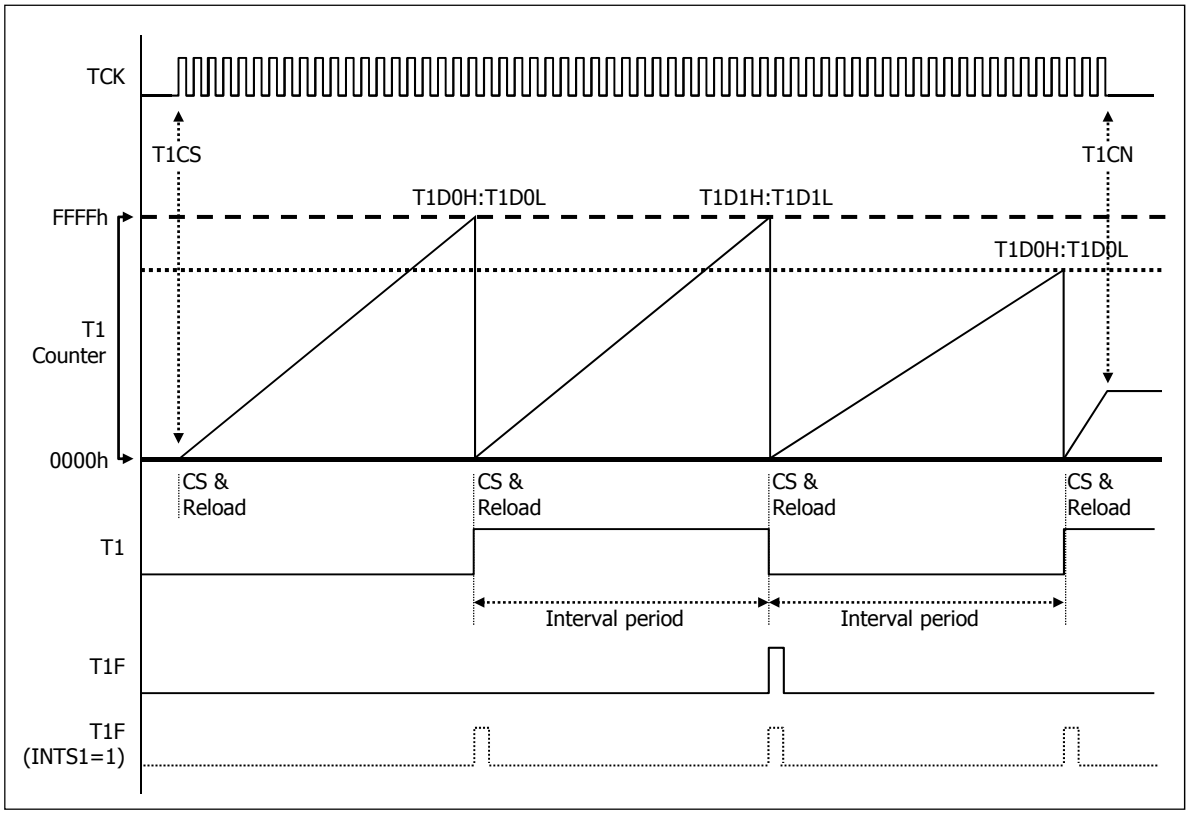
Caution : In the case of T1EG is "0",



Want to count "0", set T1EG=1

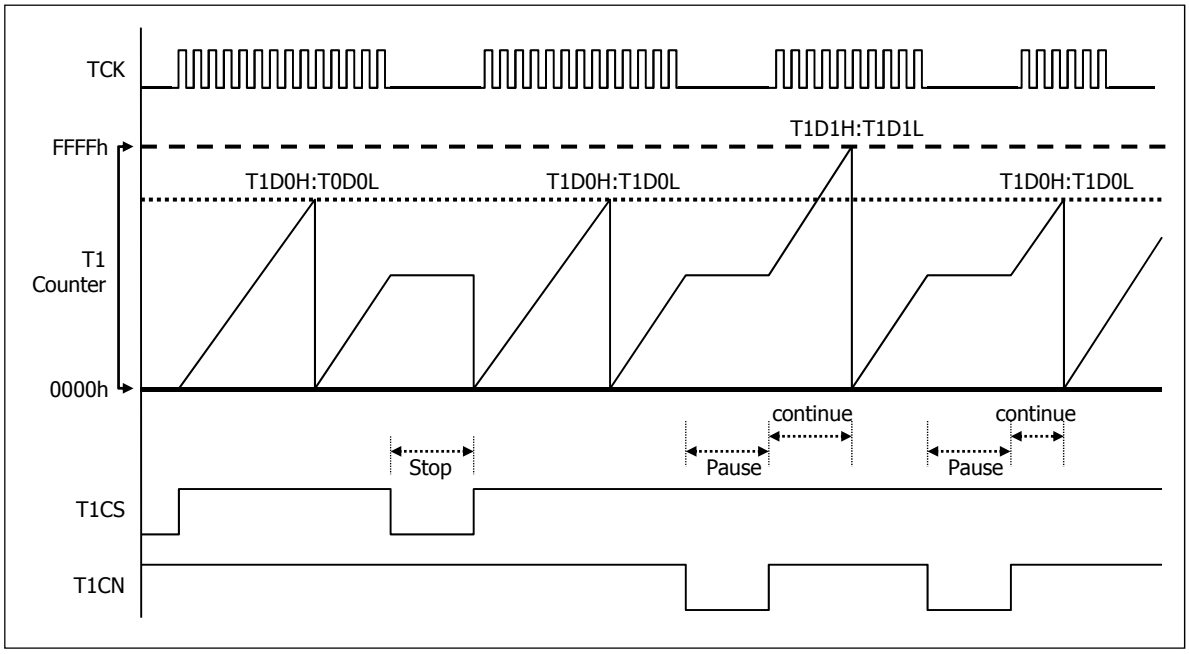
6.3.4. Timer1 Timing Diagram

* 16-bit Timer/Counter mode Timing Diagram

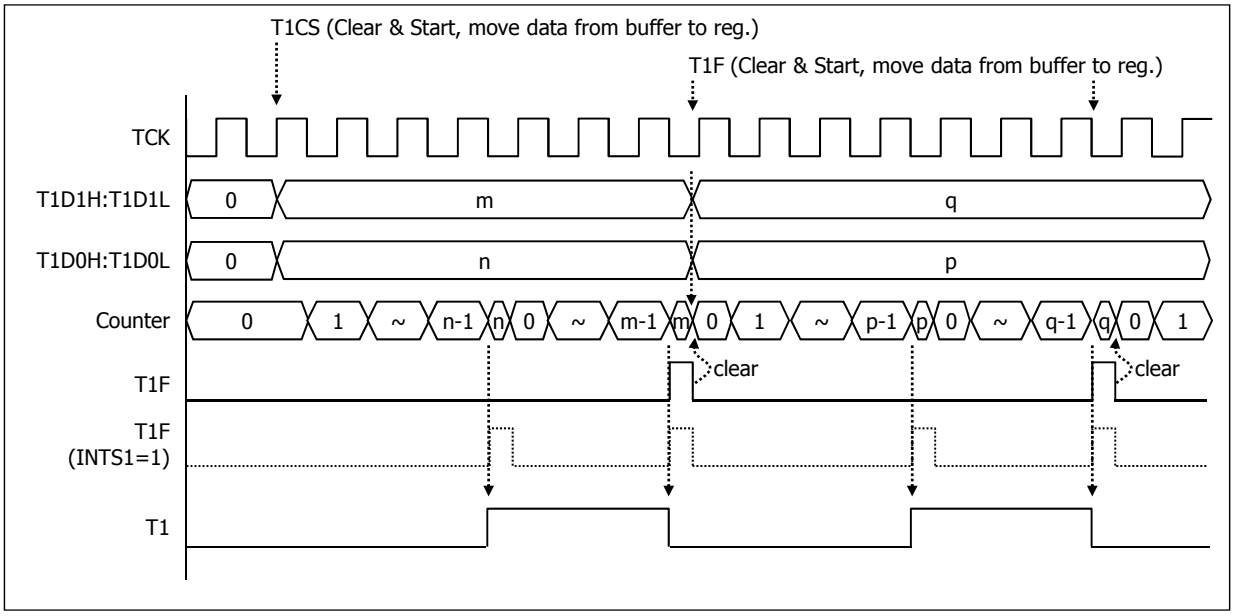


Note > CS : Timer1 Counter Clear & Start.
Reload : Timer1 Data move from Data buffer to Data register.

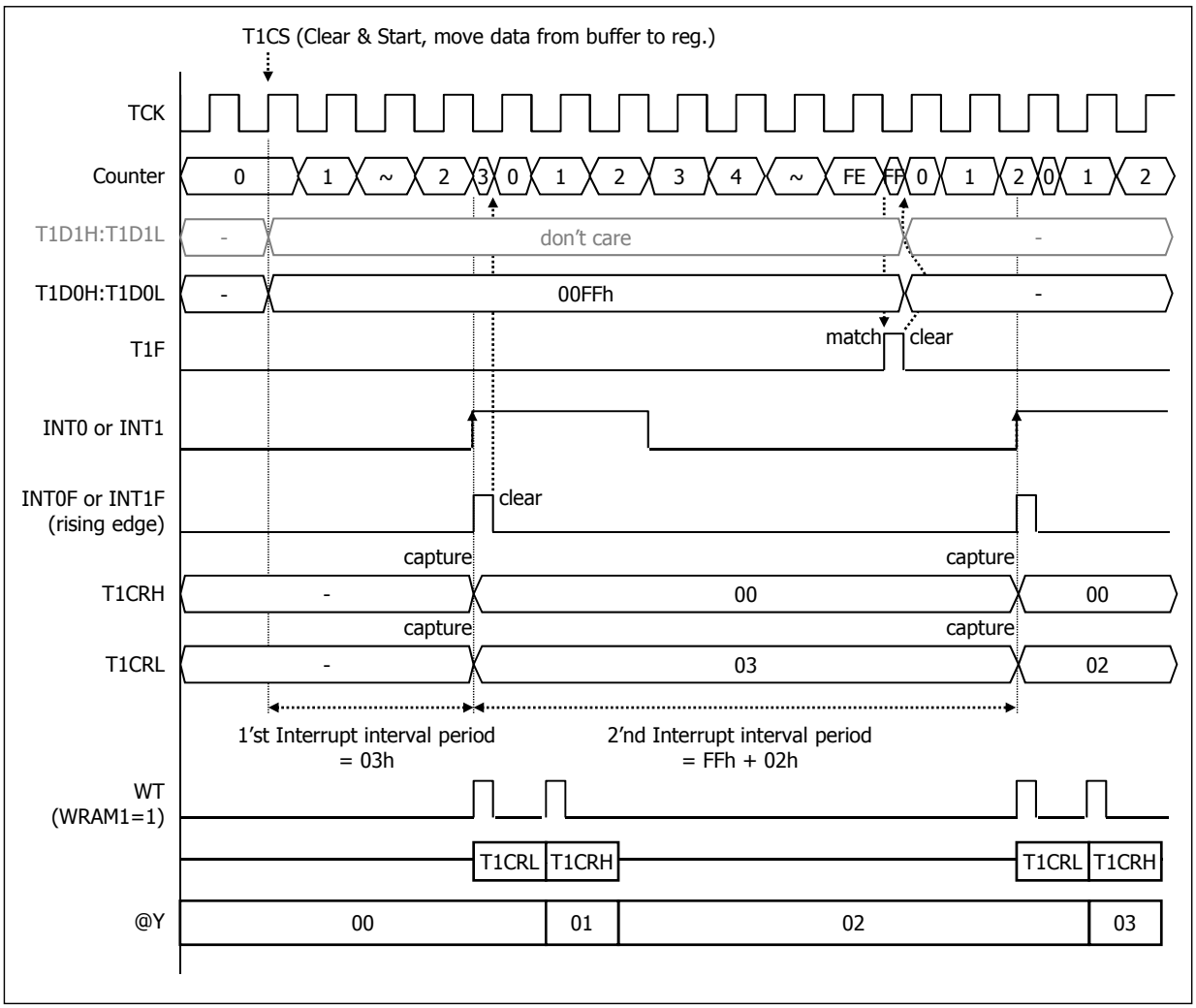
* Start / Stop operation



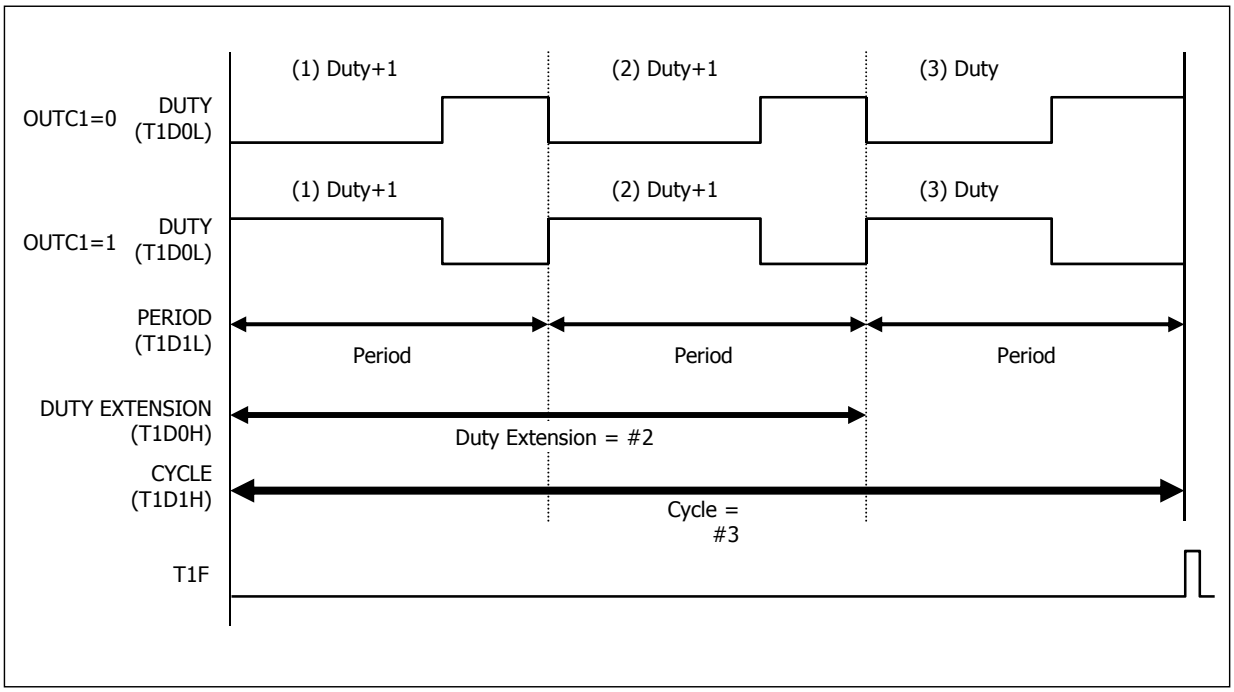
* 16-bit Timer/Counter mode Timing Diagram



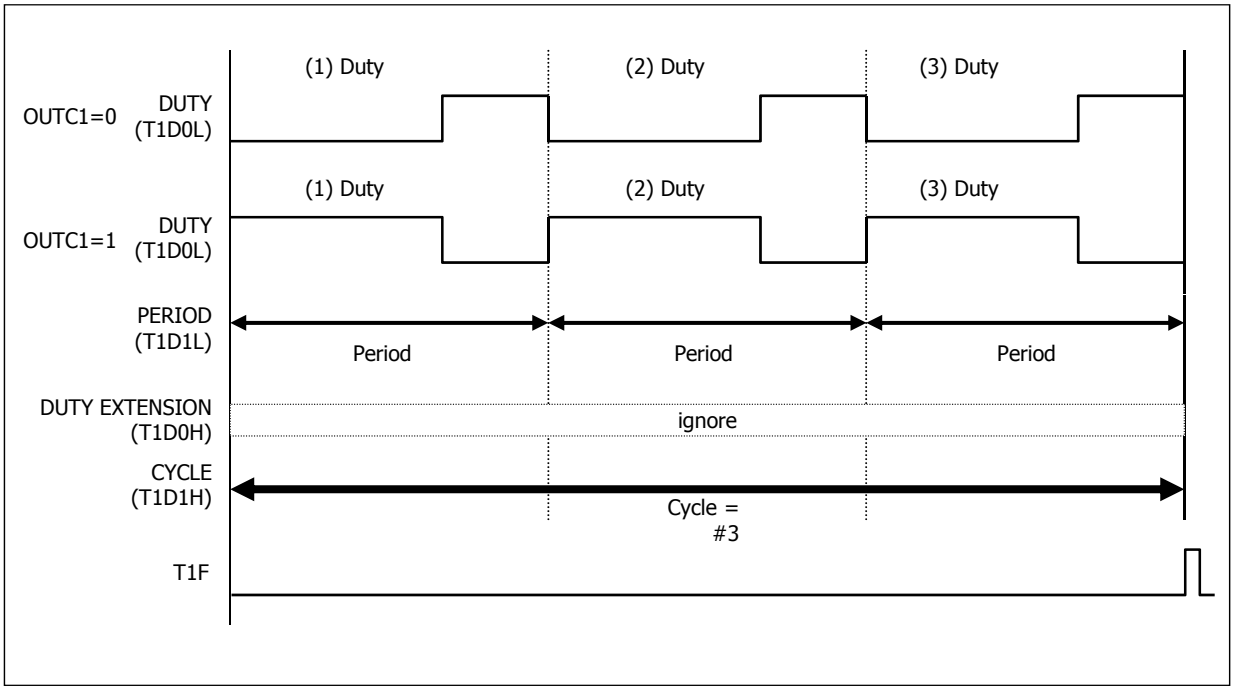
* 16-bit Capture mode Timing Diagram



• PWM mode Timing Diagram : (T1EG=0)



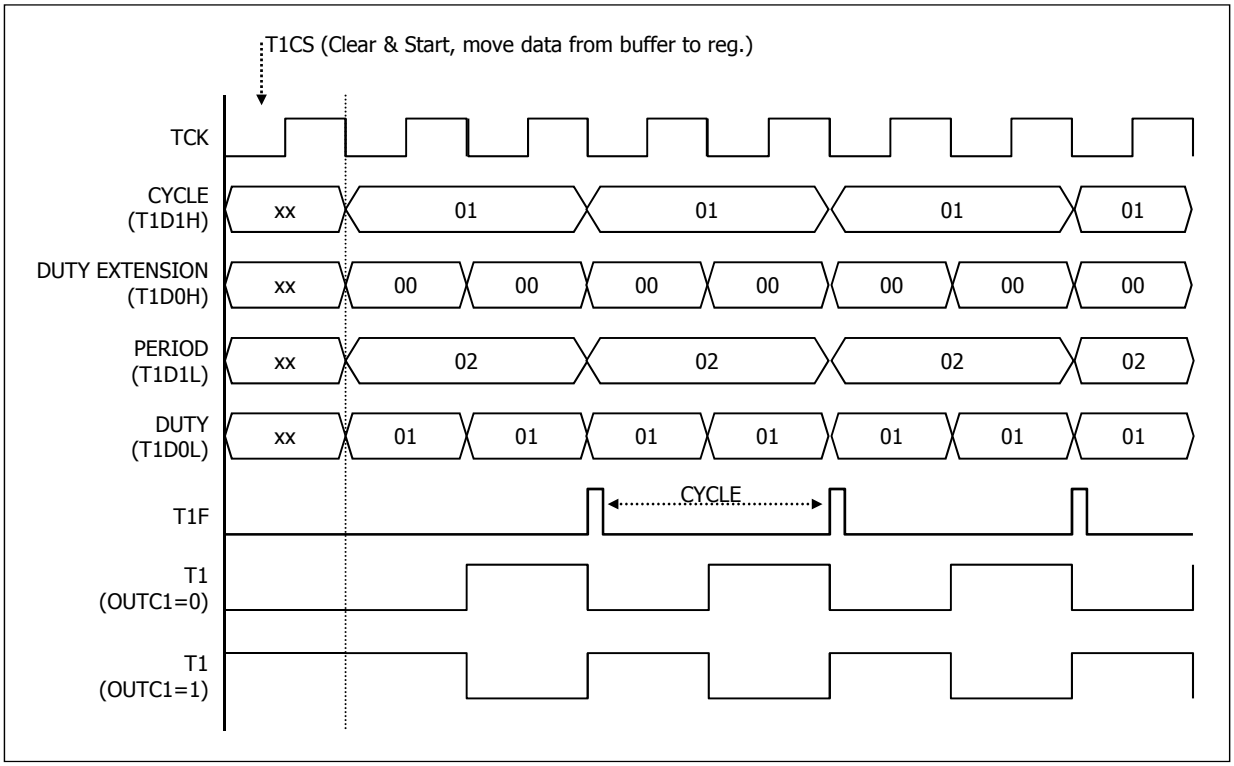
• PWM mode Timing Diagram : (T1EG=1)



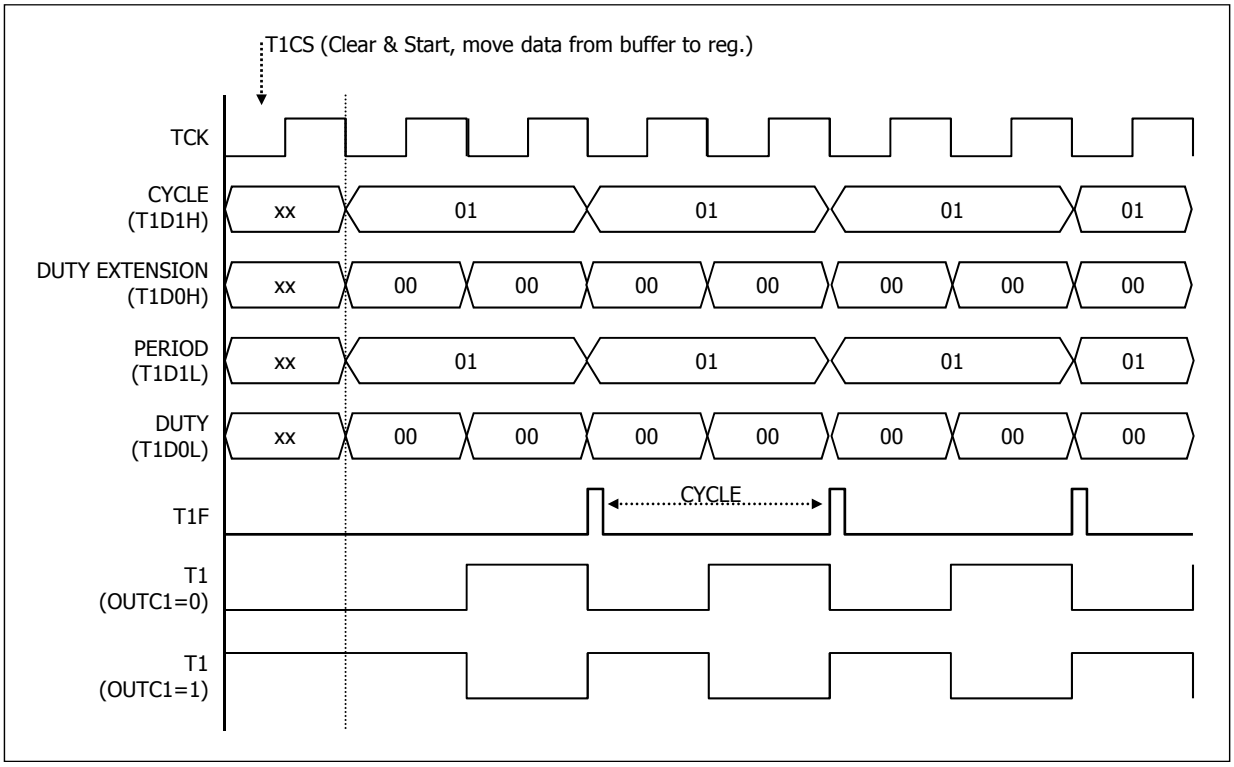
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• PWM mode Timing Diagram : (T1EG=0, DUTY EXTENSION=0)



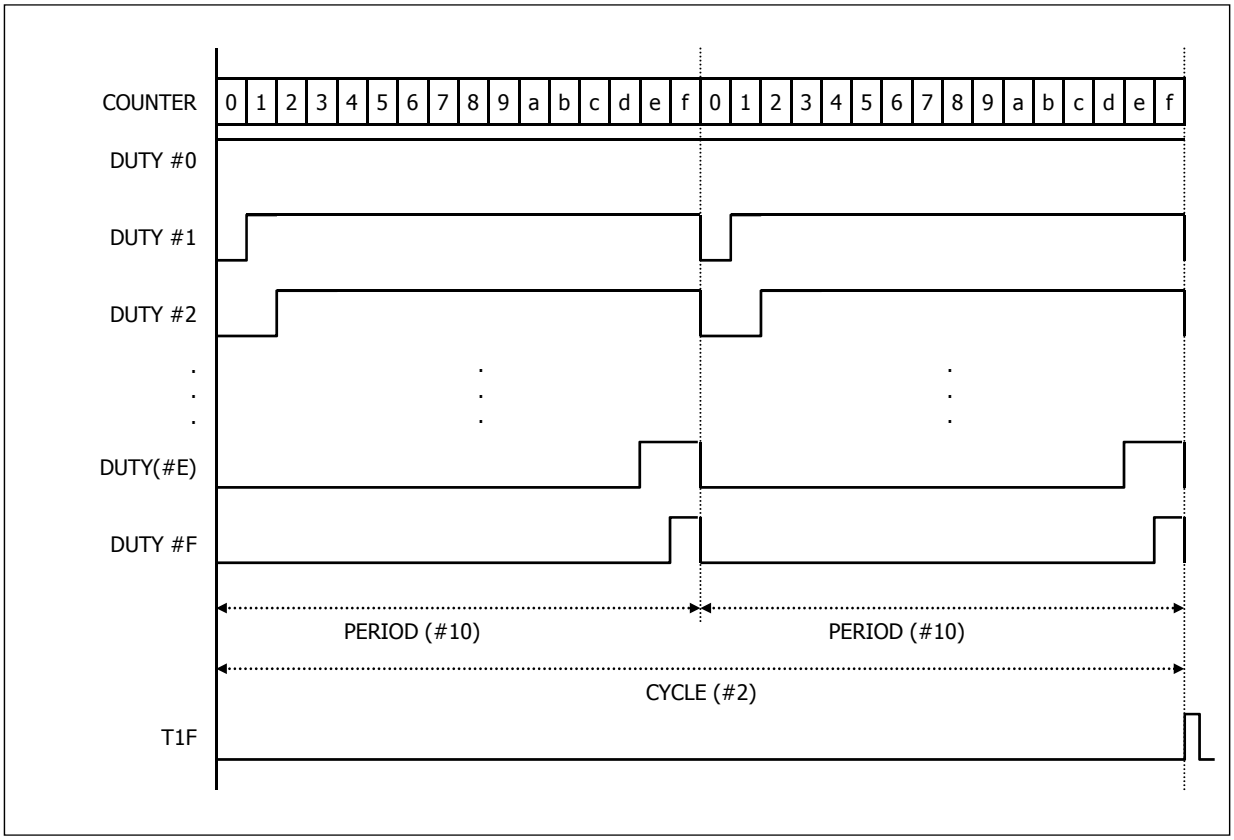
• PWM mode Timing Diagram : (T1EG=1, DUTY EXTENSION=0)



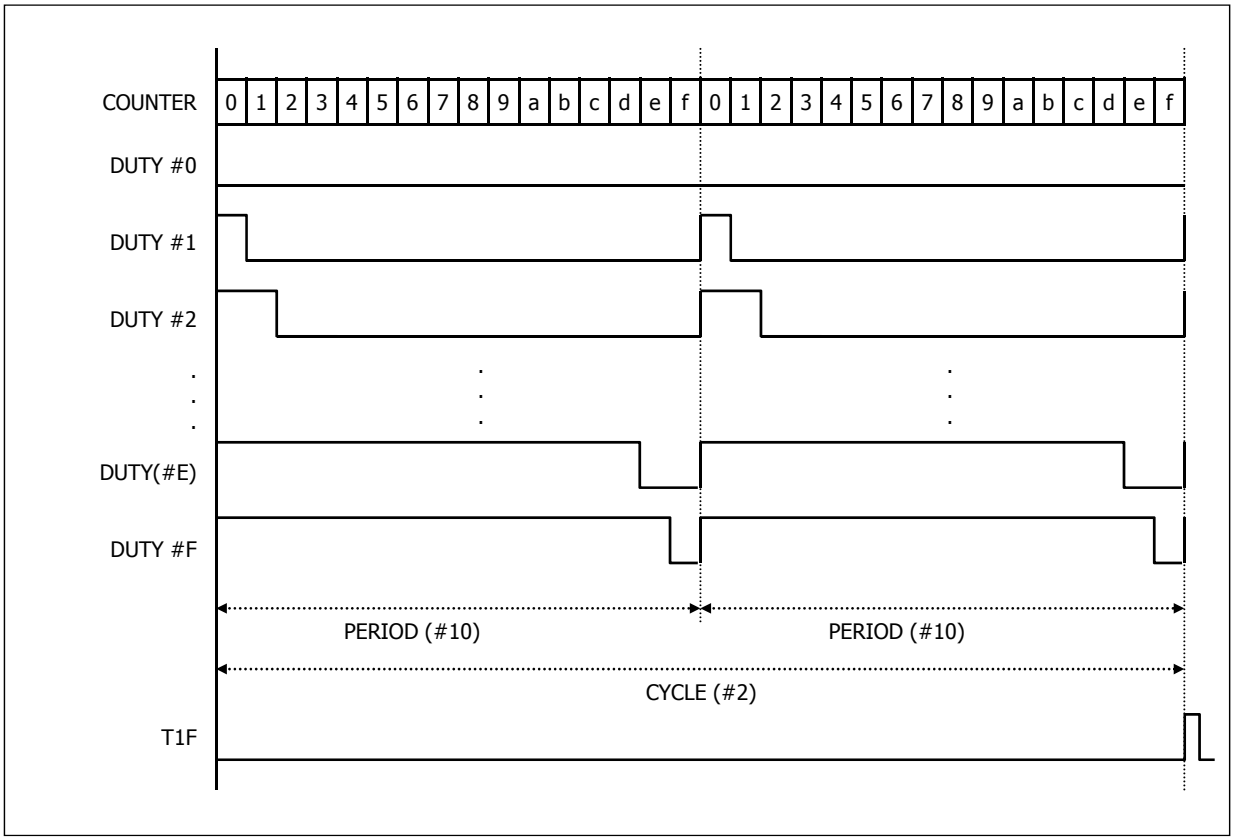
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

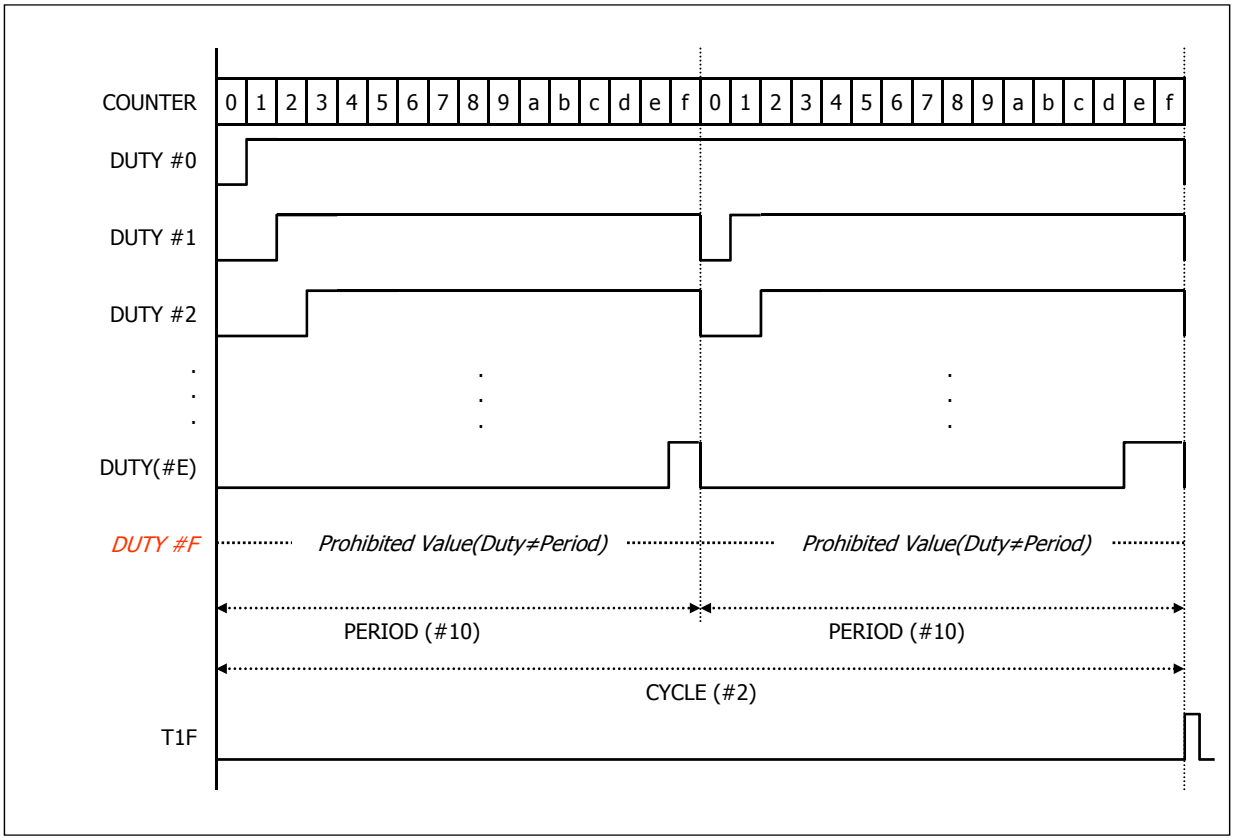
• T1 OUTPUT (PWM mode) Timing Diagram : (OUTC1=0, T1EG=0, DUTY EXTENSION=0)



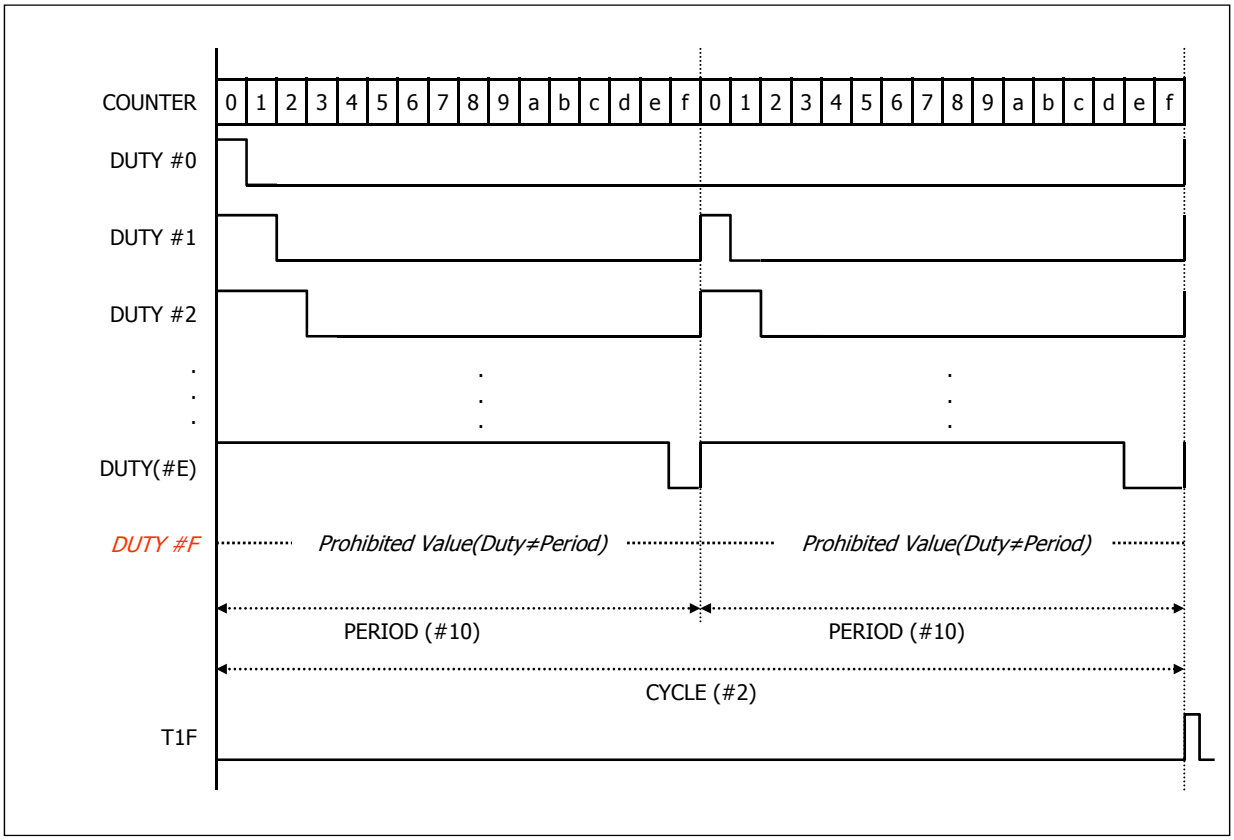
• T1 OUTPUT (PWM mode) Timing Diagram : (OUTC1=1, T1EG=0, DUTY EXTENSION=0)



• T1 OUTPUT (PWM mode) Timing Diagram : (OUTC1=0, T1EG=0, DUTY EXTENSION=1)

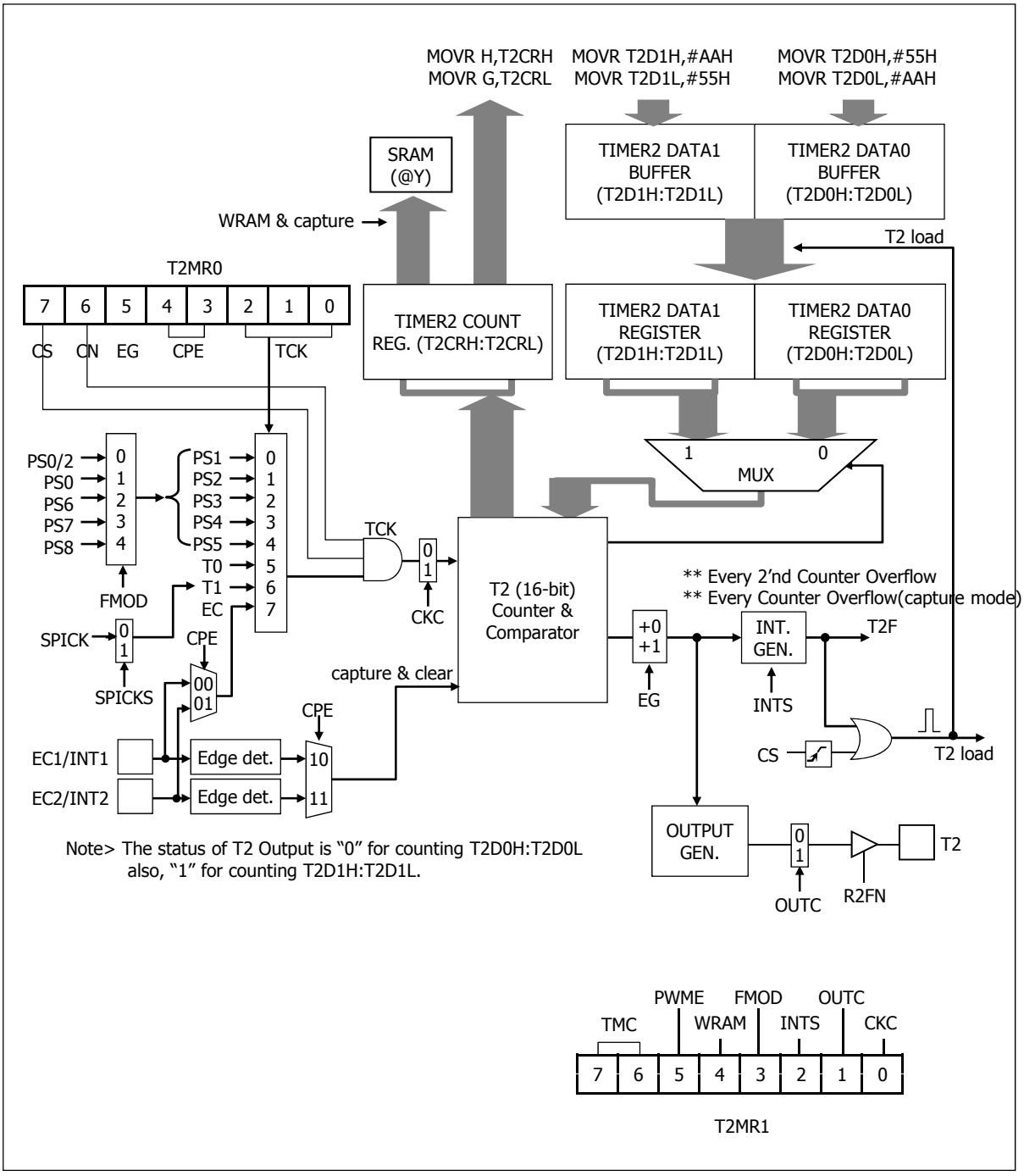


• T1 OUTPUT (PWM mode) Timing Diagram : (OUTC1=1, T1EG=0, DUTY EXTENSION=1)



6.4. Timer2

6.4.1. Timer2(T2) Block Diagram



6.4.2. Timer2 Control Register

• Timer2 Mode Register 0 (T2MR0)

	7	6	5	4	3	2	1	0	
T2MR0	T2CS	T2CN	T2EG	T2CPE1	T2CPE0	T2CK2	T2CK1	T2CK0	5dh
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T2MR0 (f_{OSC} = 4MHz)

Bit Name			Selection Mode		Remarks
T2CS	Timer2 Clear / start Control	0	Timer2 Stop		
		1	Timer2 Clear and Start		
T2CN	Timer2 Pause / Continue Control	0	Timer2 Pause		
		1	Timer2 continue		
T2EG	Timer2 Count Control	0	Timer2 Count		
		1	Timer2 Count + 1		
T2CPE1 T2CPE0	Input capture & Event Count selection	00	EC1		
		01	EC2		
		10	Capture 0 (INT1)		
		11	Capture 1 (INT2)		
T2CK2 T2CK1 T2CK0	Input clock selection	000	PS1 (0.5us)	*PS0/2	*FMODE
		001	PS2 (1us)	*PS0 (0.25us)	
		010	PS3 (2us)	*PS6 (16us)	
		011	PS4 (4us)	*PS7 (32us)	
		100	PS5 (8us)	*PS8 (64us)	
		101	T0		
		110	T1 SPICK (@SPICKS=1)		
		111	EC (EC1 or EC2)		

• Timer2 Mode Register 1 (T2MR1)

	7	6	5	4	3	2	1	0	
T2MR1	T2MC2	T2MC1	PWME2	WRAM2	FMOD2	INTS2	OUTC2	CKC2	5eh
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T2MR1

Bit Name			Selection Mode	Remarks
T2MC2 T2MC1	mPWM Control	00	Logical 'AND' of Timer1 output and Timer2 output	
		01	Logical 'OR' of Timer1 output and Timer2 output	
		10	Logical 'NAND' of Timer1 output and Timer2 output	
		11	Logical 'NOR' of Timer1 output and Timer2 output	
PWME2	Timer/PWM Mode Selection	0	Timer2 Normal Mode	
		1	Timer2 PWM Mode	
WRAM2	Automatically Save Capture data to RAM	0	Disable	
		1	Timer2 Automatically Save Capture data to RAM	
FMOD2	Fast Mode Selection	0	Timer2 Normal Mode	
		1	Timer2 Fast Mode	
INTS2	Timer2 Interrupt Overflow Control	0	Timer2 Interrupt Every 2nd Overflow	
		1	Timer2 Interrupt Every Overflow	
OUTC2	Timer2 Output Control	0	Timer2 Output Normal	
		1	Timer2 Output Reverse	
CKC2	Timer2 Input Clock Control	0	Timer2 Input Clock Normal	
		1	Timer2 Input Clock Reverse	

Note: 16bit Timer : Save 2bytes capture data to RAM (2cycle) - addressed by @Y++.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T2CRL	T2CRH	T2CRL	T2CRH	T2CRL	T2CRH	T2CRL	T2CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

• Timer2 Data0 Register Low (T2D0L) = PWM2 DUTY

	7	6	5	4	3	2	1	0	
T2D0L	T2D0L7	T2D0L6	T2D0L5	T2D0L4	T2D0L3	T2D0L2	T2D0L1	T2D0L0	5fh
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer2 Count Register Low (T2CRL)

	7	6	5	4	3	2	1	0	
T2CRL	T2CRL7	T2CRL6	T2CRL5	T2CRL4	T2CRL3	T2CRL2	T2CRL1	T2CRL0	5fh
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

Note: At 16bit counter value read, Must be read T2CRL first.

• Timer2 Data1 Register Low (T2D1L) = PWM2 PERIOD

	7	6	5	4	3	2	1	0	
T2D1L	T2D1L7	T2D1L6	T2D1L5	T2D1L4	T2D1L3	T2D1L2	T2D1L1	T2D1L0	60h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer2 Data0 Register High (T2D0H) = PWM2 DUTY EXTENSION

	7	6	5	4	3	2	1	0	
T2D0H	T2D0H7	T2D0H6	T2D0H5	T2D0H4	T2D0H3	T2D0H2	T2D0H1	T2D0H0	61h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• Timer2 Count Register High (T2CRH)

	7	6	5	4	3	2	1	0	
T2CRH	T2CRH7	T2CRH6	T2CRH5	T2CRH4	T2CRH3	T2CRH2	T2CRH1	T2CRH0	61h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

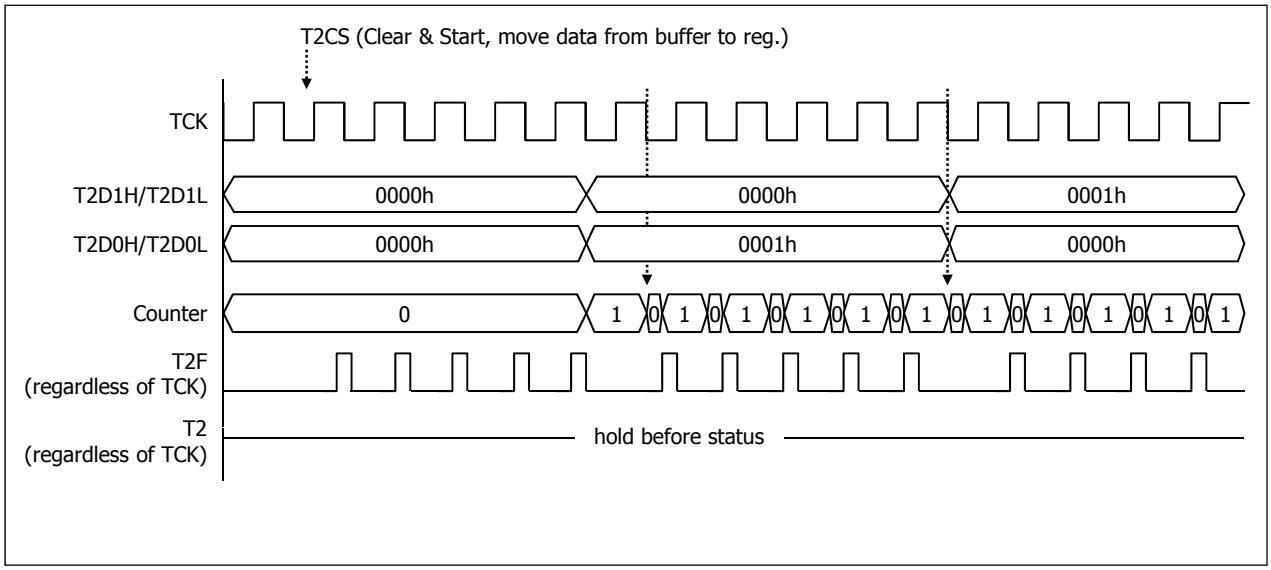
Note: At 16bit counter value read, Must be read T2CRL first.

• Timer2 Data1 Register High (T2D1H) = PWM2 CYCLE

	7	6	5	4	3	2	1	0	
T2D1H	T2D1H7	T2D1H6	T2D1H5	T2D1H4	T2D1H3	T2D1H2	T2D1H1	T2D1H0	62h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

6.4.3. Timer2 Caution

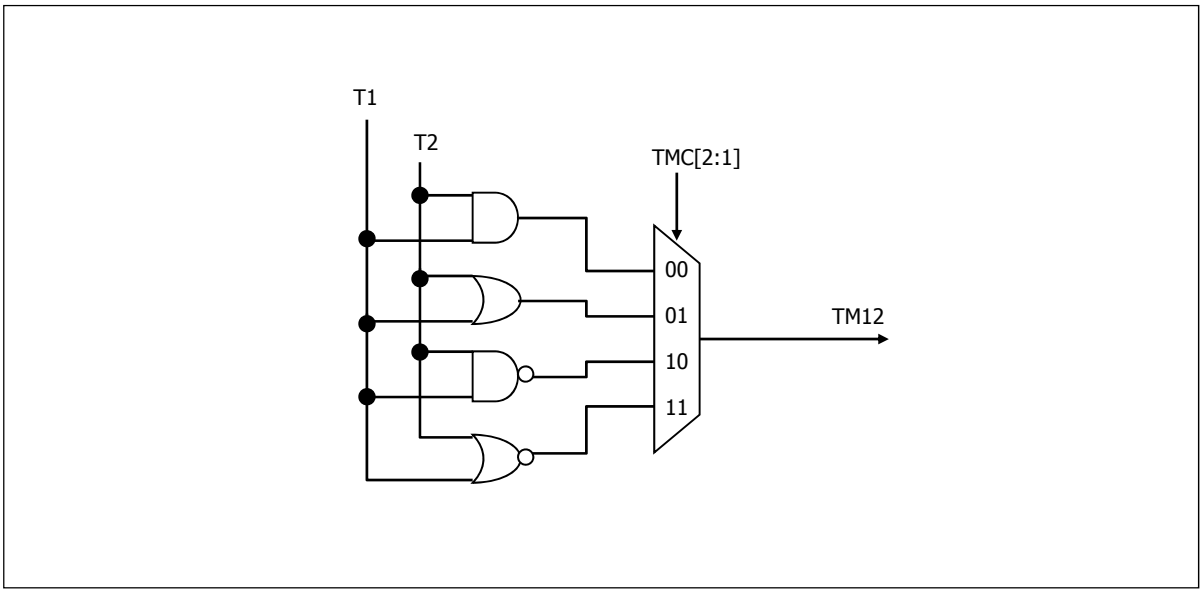
Caution : In the case of T2EG is "0",



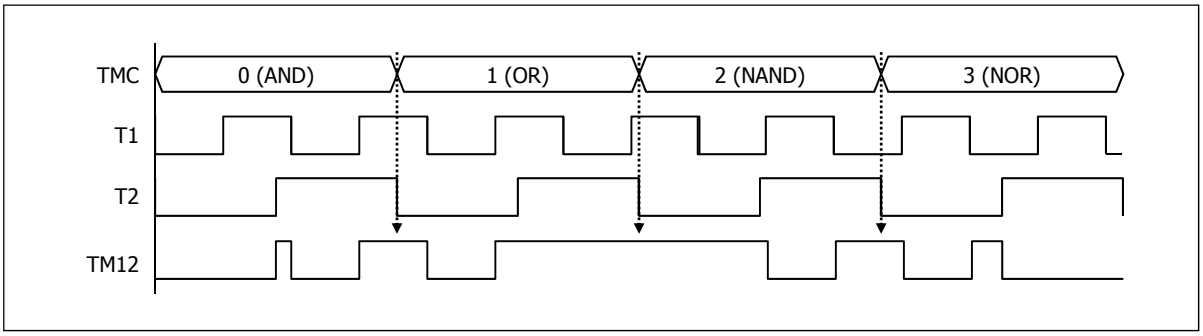
Want to count "0", set T2EG=1

6.4.4. TM12 Mode

* TM12 Logical Output Control

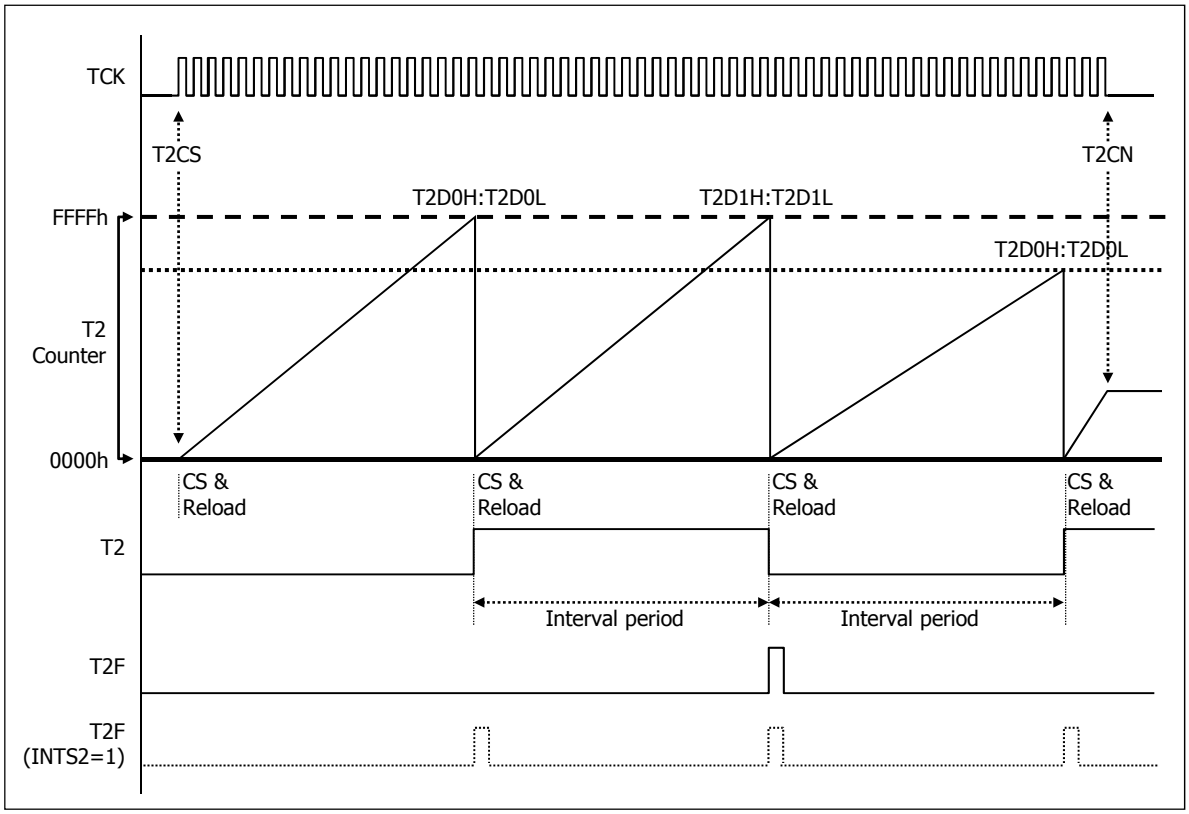


* TM12 mode Timing Diagram



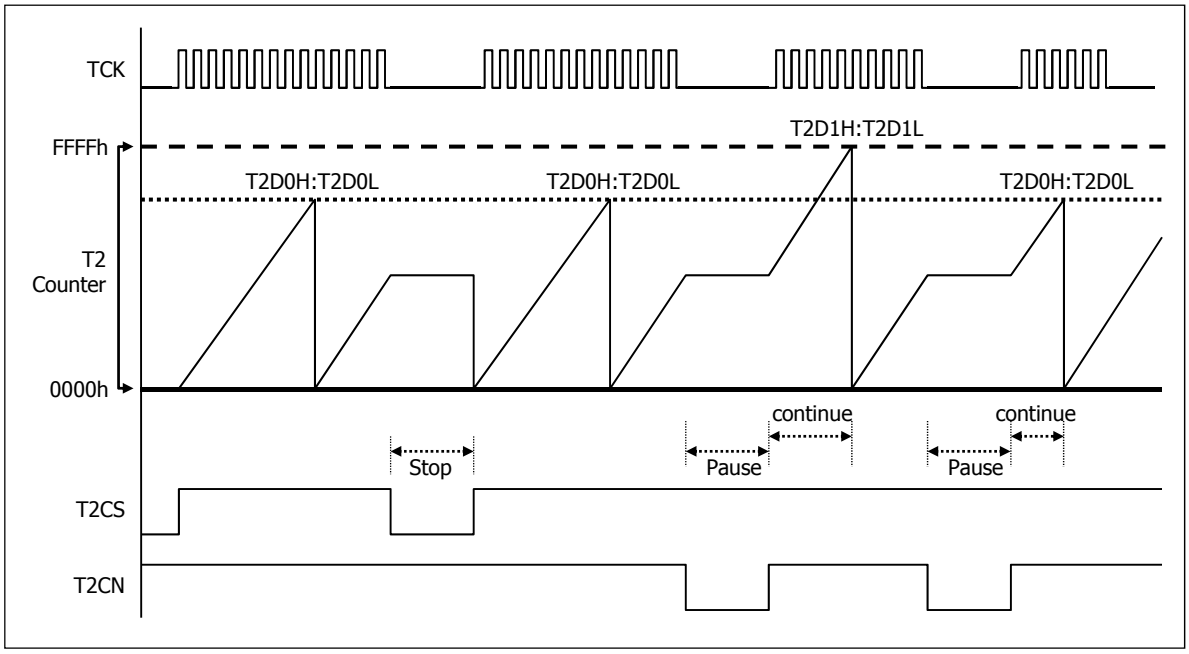
6.4.5. Timer2 Timing Diagram

* 16-bit Timer/Counter mode Timing Diagram

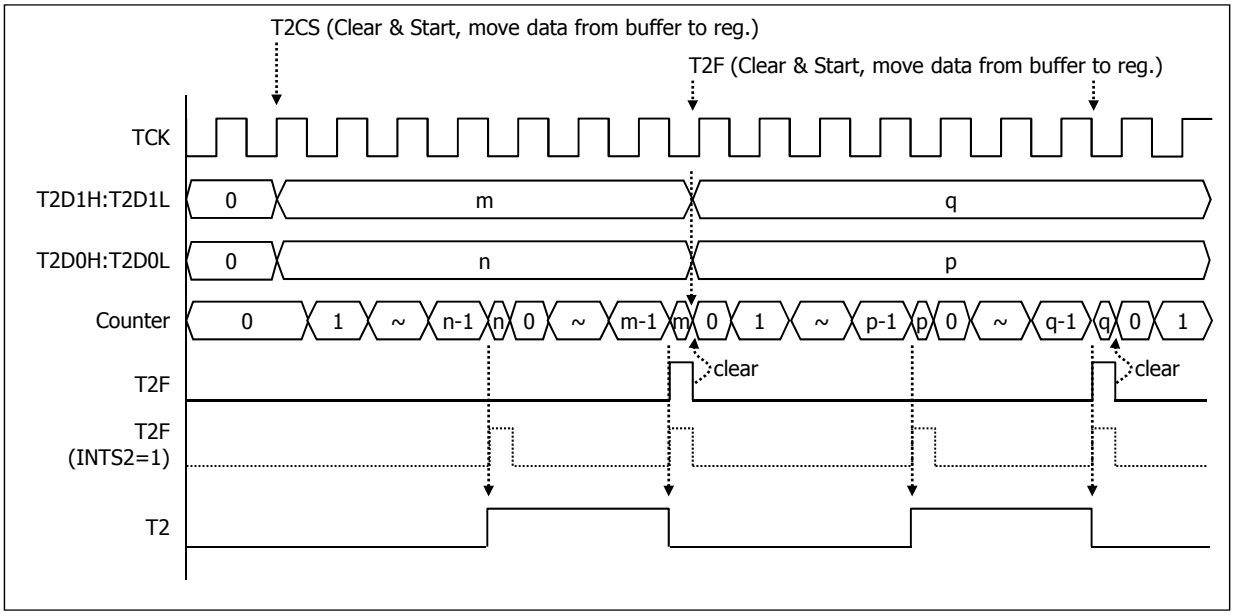


Note > CS : Timer2 Counter Clear & Start.
Reload : Timer2 Data move from Data buffer to Data register.

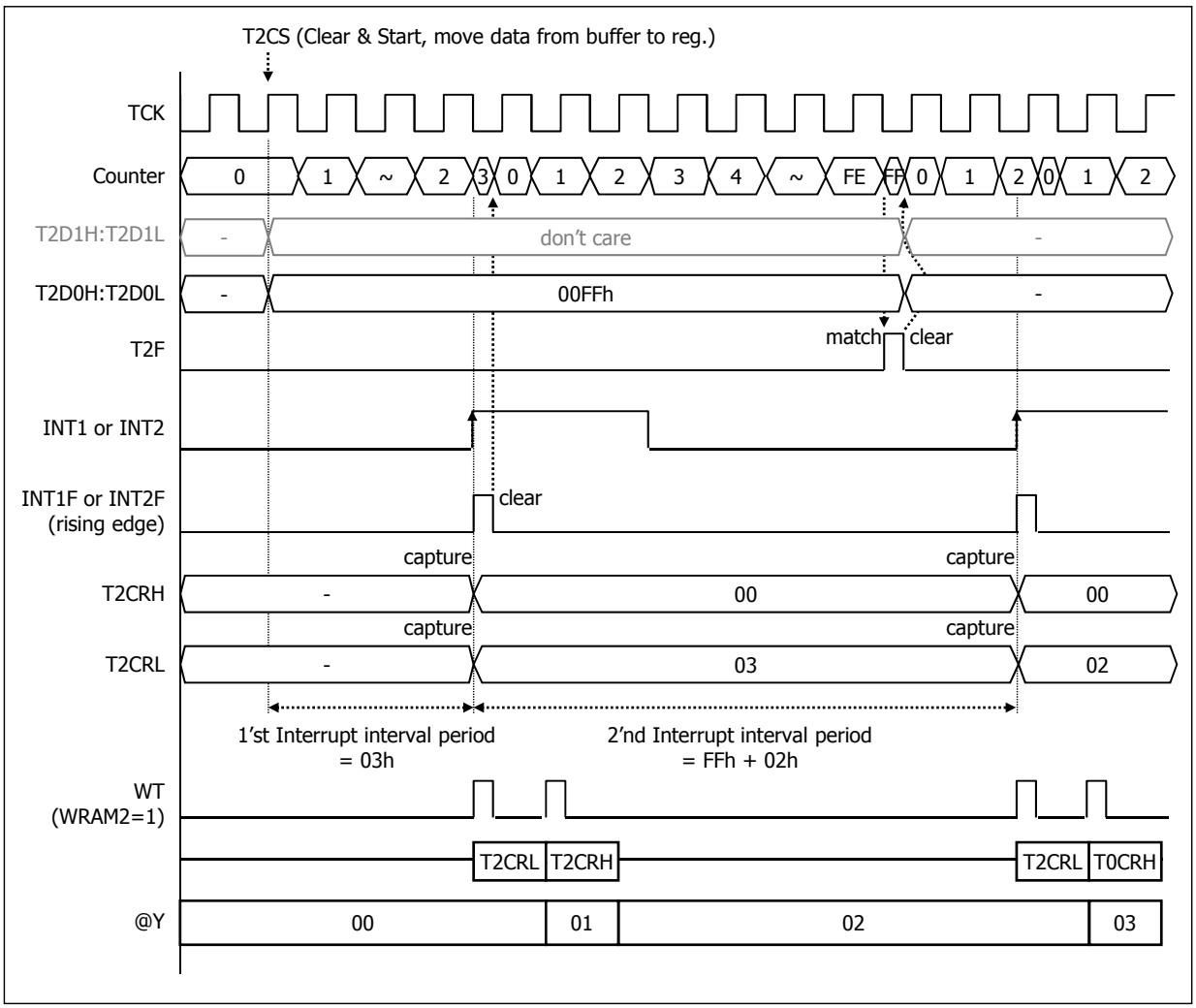
* Start / Stop operation



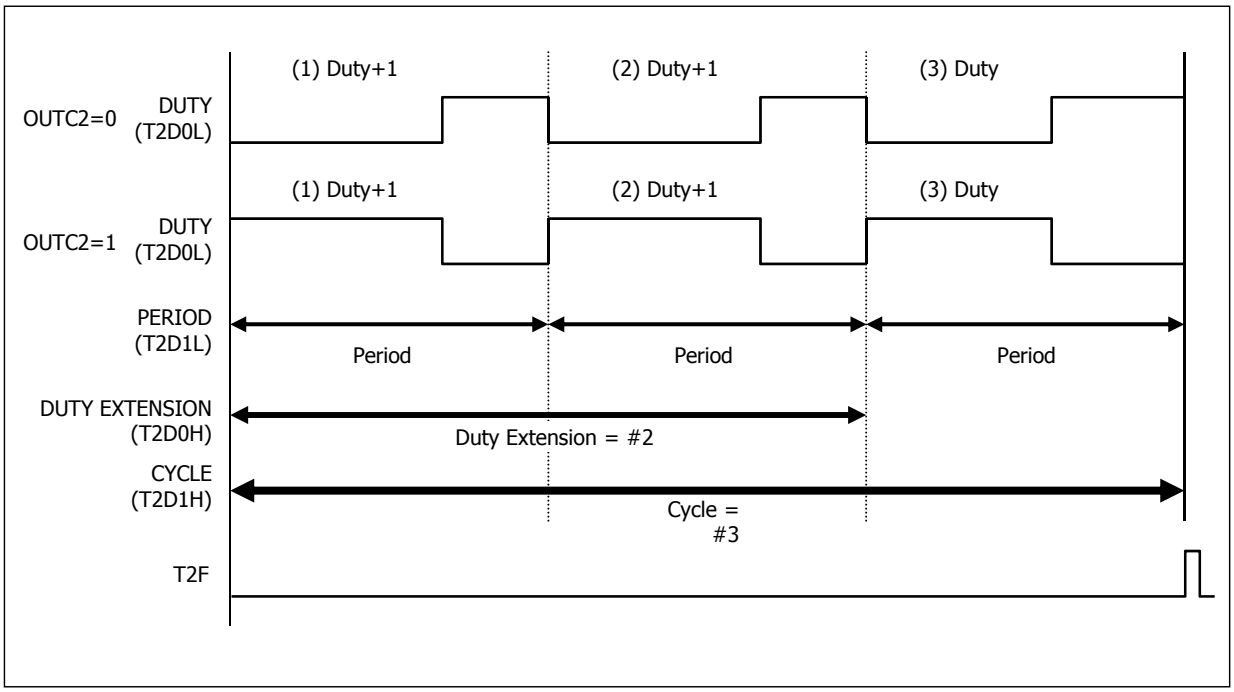
* 16-bit Timer/Counter mode Timing Diagram



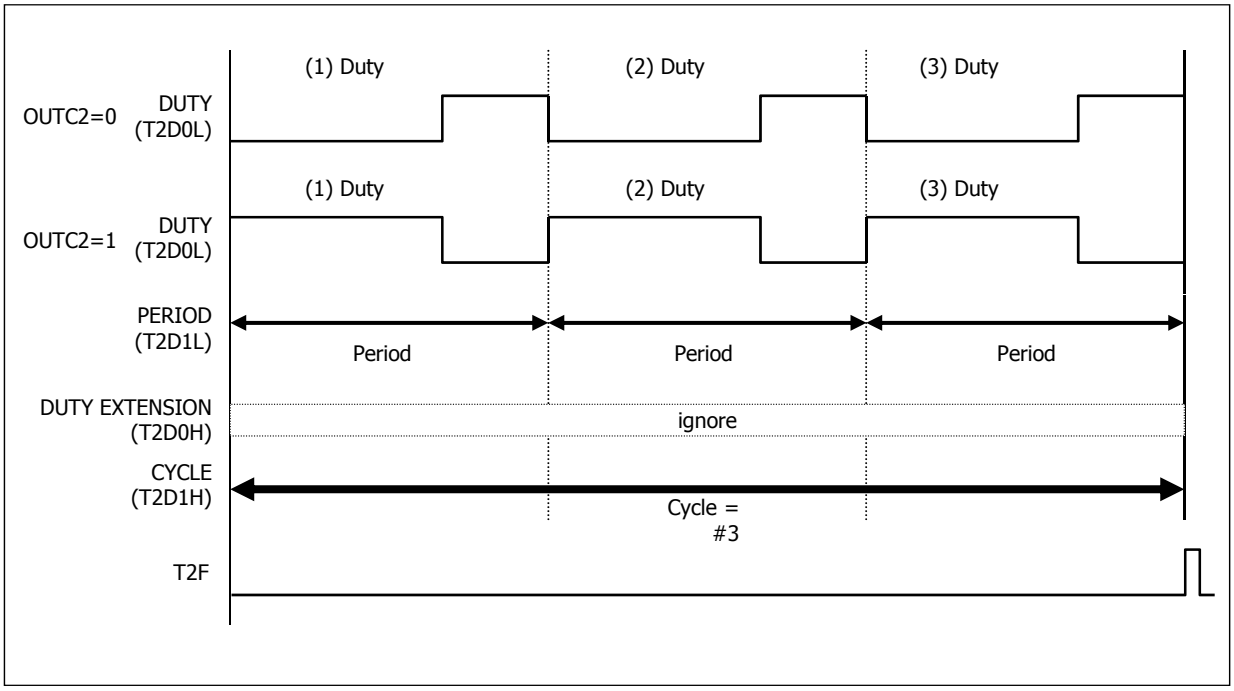
* 16-bit Capture mode Timing Diagram



• PWM mode Timing Diagram : (T2EG=0)



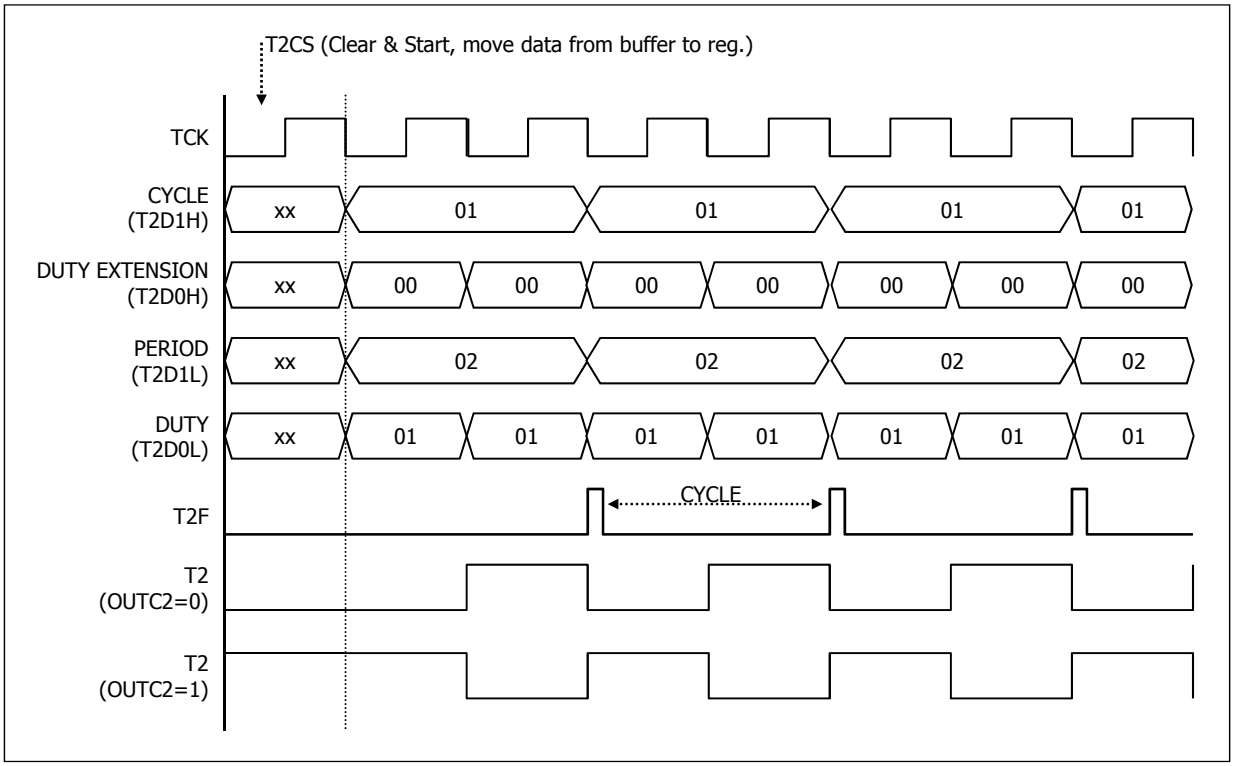
• PWM mode Timing Diagram : (T2EG=1)



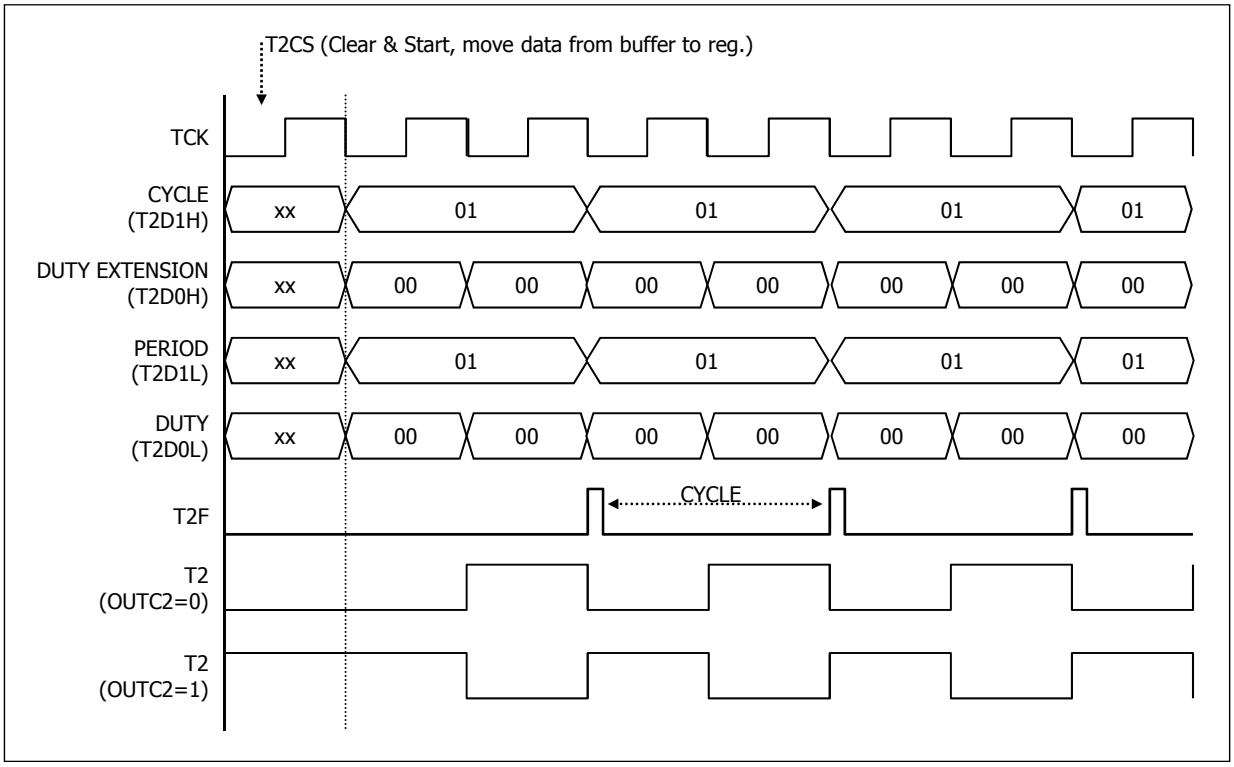
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• PWM mode Timing Diagram : (T2EG=0, DUTY EXTENSION=0)



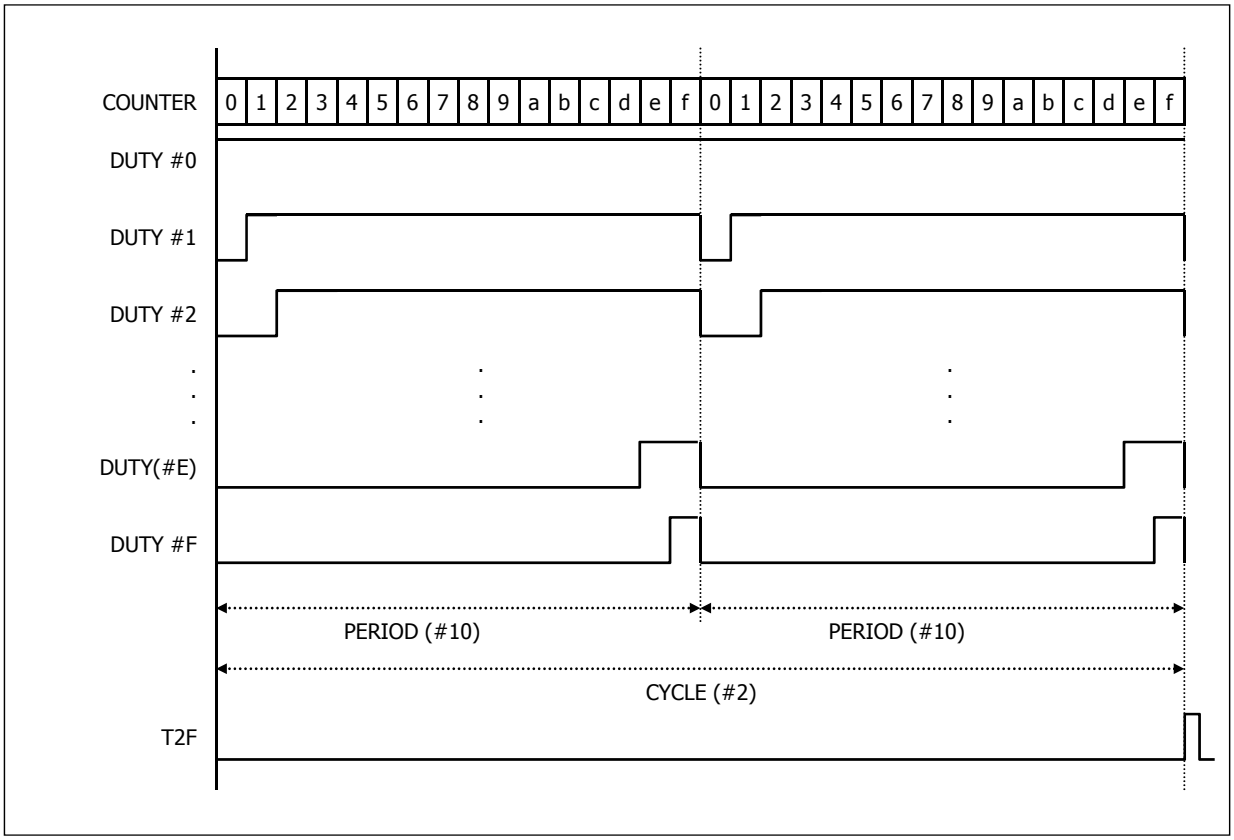
• PWM mode Timing Diagram : (T2EG=1, DUTY EXTENSION=0)



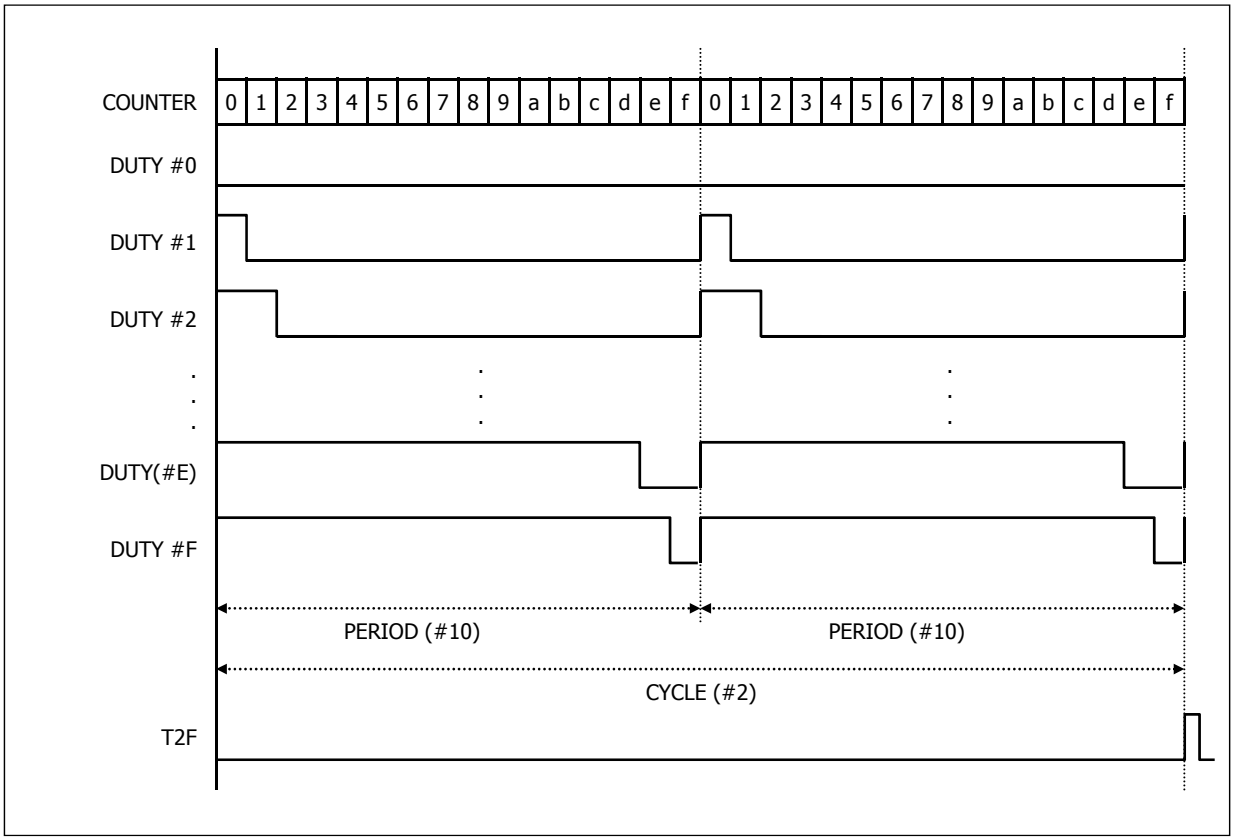
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

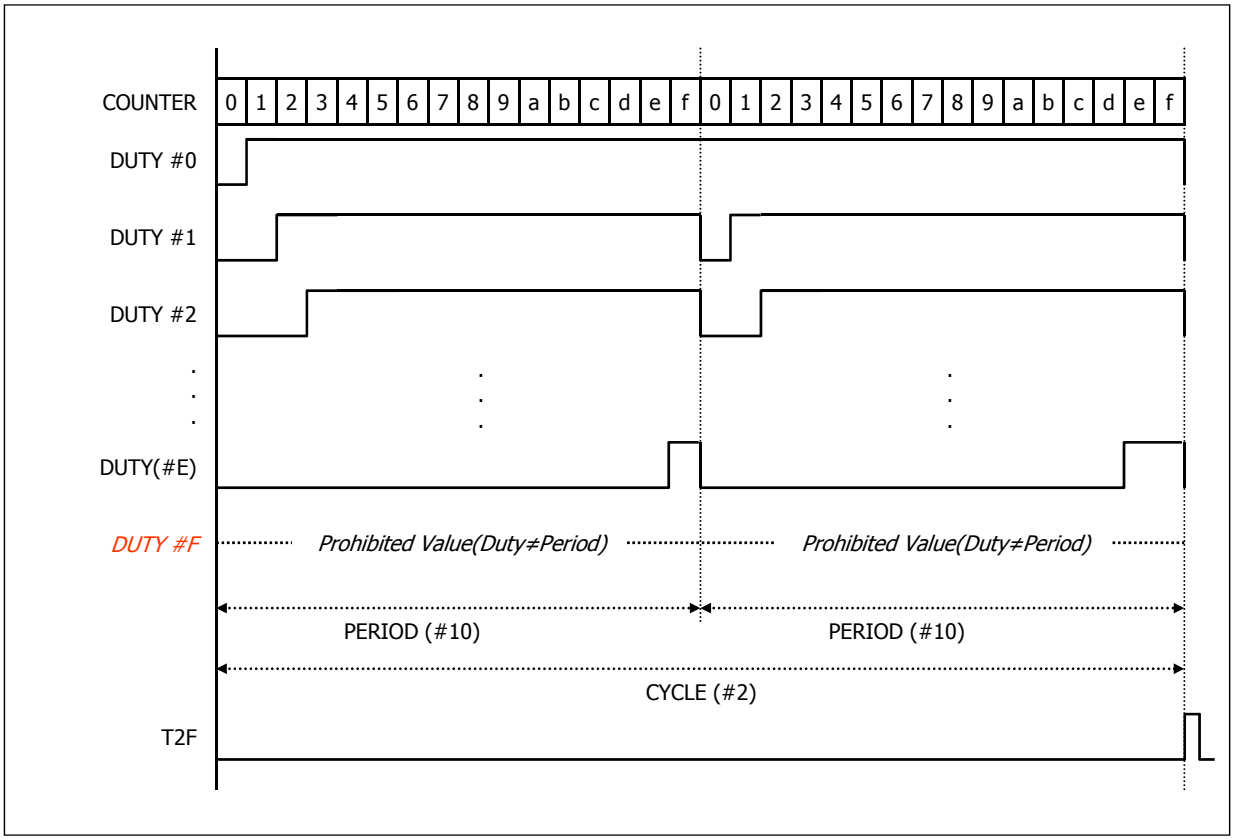
• T2 OUTPUT (PWM mode) Timing Diagram : (OUTC2=0, T2EG=0, DUTY EXTENSION=0)



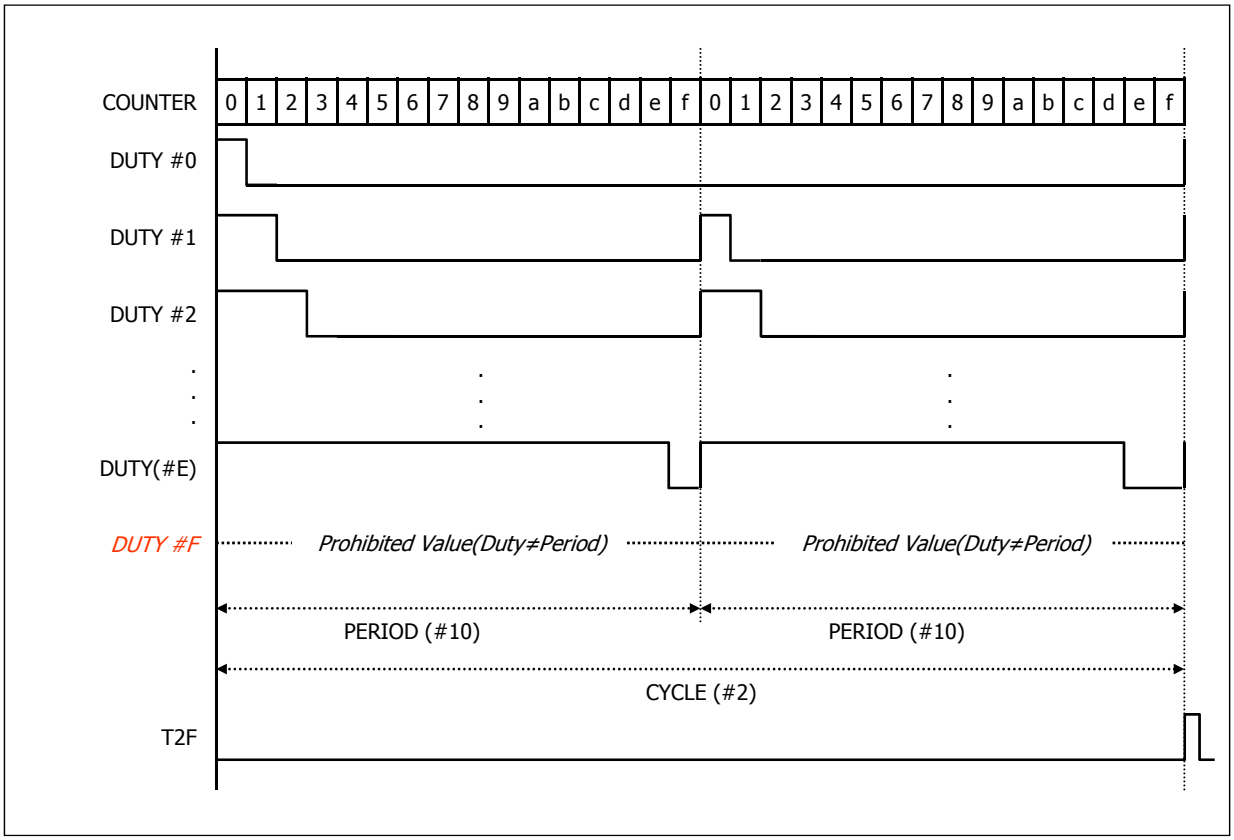
• T2 OUTPUT (PWM mode) Timing Diagram : (OUTC2=1, T2EG=0, DUTY EXTENSION=0)



• T2 OUTPUT (PWM mode) Timing Diagram : (OUTC2=0, T2EG=0, DUTY EXTENSION=1)



• T2 OUTPUT (PWM mode) Timing Diagram : (OUTC2=1, T2EG=0, DUTY EXTENSION=1)

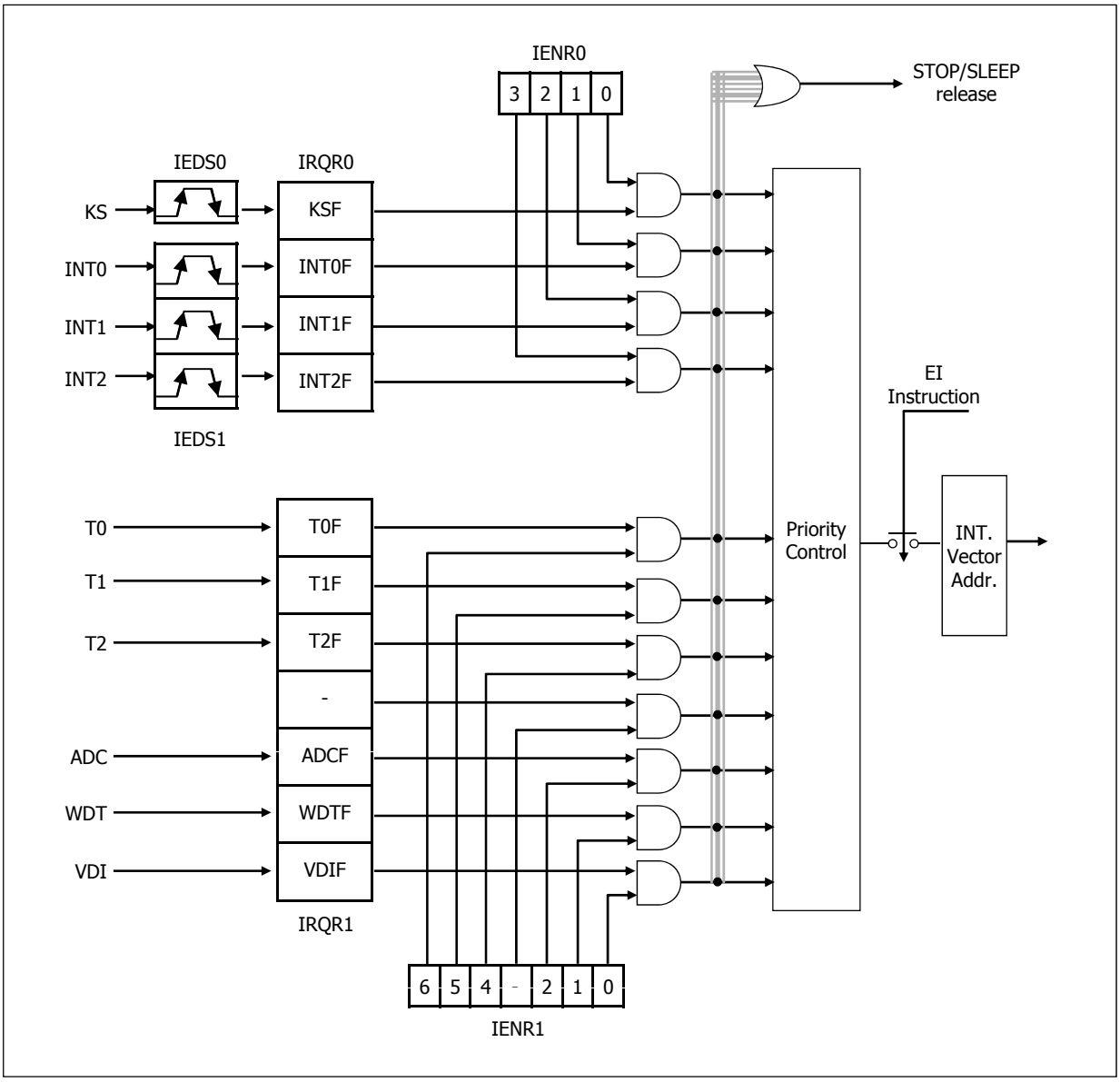


The ADAM81 contains 10 interrupt sources; 4 externals and 6 internals.
Nested interrupt services with priority control is also possible.

- 10 interrupt source (KS, INT0, INT1, INT2, T0, T1, T2, ADC, WDT, VDI)
- 10 interrupt vector
- 8 level nested interrupt control is possible.
- Read of interrupt request flag are possible.
- In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR0, IENR1), Interrupt Request Register (IRQR0, IRQR1) and priority circuit.
Interrupt function block diagram is shown in Fig. 5.1

Fig. Interrupt Source



7.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

After internal reset is released, RESET vector Address is 0000h thus program start point should be defined as follows (also interrupt):

Example :

```
                ORG     0000h
vRESET:         MOVPG   #0H
                BR      !PGM_START
vKS:            MOVPG   #0H
                BR      !INT_KS
vINT0:          MOVPG   #0H
                BR      !INT_INT0
vINT1:          MOVPG   #0H
                BR      !INT_INT1
vINT2:          MOVPG   #0H
                BR      !!INT_INT2

vT0:            MOVPG   #0H
                BR      !INT_T0
vT1:            MOVPG   #0H
                BR      !INT_T1
vT2:            MOVPG   #0H
                BR      !INT_T2

vADC:           MOVPG   #0H
                BR      !INT_ADC
vWDT:           MOVPG   #0H
                BR      !INT_WDT
vVDI:           MOVPG   #0H
                BR      !INT_VDI
```

```
                ORG     INT_ADDR
INT_KS:         JOB_TO_WORK
                RETI
INT_INT0:       JOB_TO_WORK
                RETI
INT_INT1:       JOB_TO_WORK
                RETI
INT_INT2:       JOB_TO_WORK
                RETI

INT_T0:         JOB_TO_WORK
                RETI
INT_T1:         JOB_TO_WORK
                RETI
INT_T2:         JOB_TO_WORK
                RETI

INT_ADC:        JOB_TO_WORK
                RETI
INT_WDT:        JOB_TO_WORK
                RETI
INT_VDI:        JOB_TO_WORK
                RETI
```

Table. Interrupt Source

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	0	RESET	0000h
	maskable	1	KS	0002h
		2	INT0 (External Interrupt 0)	0004h
		3	INT1 (External Interrupt 1)	0006h
		4	INT2 (External Interrupt 2)	0008h
		5	-	000Ah
		6	T0 (Timer0)	000Ch
		7	T1 (Timer1)	000Eh
		8	T2 (Timer2)	0010h
		9	-	0012h
		10	ADC (Analog Digital Converter)	0014h
		11	WDT (Watch-Dog Timer)	0016h
		12	VDI (Voltage Detection Indicator)	0018h
		13	-	-
		14	-	-
		15	-	-

7.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag.
When I flag = "0", all interrupts become disable.
When I flag = "1", interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR0, IENR1).
When interrupt is occurred, interrupt request flag is set,and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process.
The interrupt request flag maintains "1" until the interrupt is accepted or is cleared in program.
In reset state, interrupt request flag register (IRQR0, IRQR1) is cleared to "0".
It is possible to read the state of interrupt register and to manipulate the contents of register.

• External Interrupt Edge selection Register (IEDS0)

	7	6	5	4	3	2	1	0	
IEDS0	-	-	-	-	-	-	IEDK		40h
initial value	-	-	-	-	-	-	0	0	
R/W	-	-	-	-	-	-	W	W	

Selection Mode of IEDS0

Bit Name	Selection Mode		Remarks
IEDK	00	-	KS
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	

• External Interrupt Edge selection Register (IEDS1)

	7	6	5	4	3	2	1	0	
IEDS1	-		IED2		IED1		IED0		41h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	W	W	W	W	W	W	

Selection Mode of IEDS1

Bit Name	Selection Mode		Remarks
-	00	-	-
	01	-	
	10	-	
	11	-	
IED2	00	-	INT2
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	
IED1	00	-	INT1
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	
IED0	00	-	INT0
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	

• Interrupt Enable Register (IENR0)

	7	6	5	4	3	2	1	0	
IENR0	-	-	-	-	INT2E	INT1E	INT0E	KSE	42h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	R/W	R/W	R/W	R/W	

Selection Mode of IENR0

Bit Name	Selection Mode		Remarks
INT2E	1	External Interrupt 2 enable	
INT1E	1	External Interrupt 1 enable	
INT0E	1	External Interrupt 0 enable	
KSE	1	Key Scan Interrupt enable	

• Interrupt Request Flag Register (IRQR0)

	7	6	5	4	3	2	1	0	
IRQR0	-	-	-	-	INT2F	INT1F	INT0F	KSF	43h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	-	R/W	R/W	R/W	R/W	

Selection Mode of IRQR0

Bit Name	Selection Mode		Remarks
INT2F	1	External Interrupt 2 Request enable	
INT1F	1	External Interrupt 1 Request enable	
INT0F	1	External Interrupt 0 Request enable	
KSF	1	Key Scan Interrupt Request enable	

• Interrupt Enable Register (IENR1)

	7	6	5	4	3	2	1	0	
IENR1	-	VDIE	WDTE	ADCE	-	T2E	T1E	T0E	44h
initial value	0	0	0	0	0	0	0	0	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR1

Bit Name	Selection Mode		Remarks
VDI	1	VDI Interrupt enable	
WDT	1	WDT Interrupt enable	
ADC	1	ADC Interrupt enable	
-	-	-	
T2E	1	Timer 2 Interrupt enable	
T1E	1	Timer 1 Interrupt enable	
T0E	1	Timer 0 Interrupt enable	

• Interrupt Request Flag Register (IRQR1)

	7	6	5	4	3	2	1	0	
IRQR1	-	VDIF	WDTF	ADCF	-	T2F	T1F	T0F	45h
initial value	0	0	0	0	0	0	0	0	
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR1

Bit Name	Selection Mode		Remarks
VDIF	1	VDI Interrupt Request enable	
WDTF	1	WDT Interrupt Request enable	
ADCF	1	ADC Interrupt Request enable	
-	-	-	
T2F	1	Timer 2 Interrupt Request enable	
T1F	1	Timer 1 Interrupt Request enable	
T0F	1	Timer 0 Interrupt Request enable	

7.3. Interrupt Timing

Interrupt Request Sampling Time :
-. Maximum 2 machine cycle (2 machine cycle Instructions)

Interrupt preprocess step is 1 machine cycle

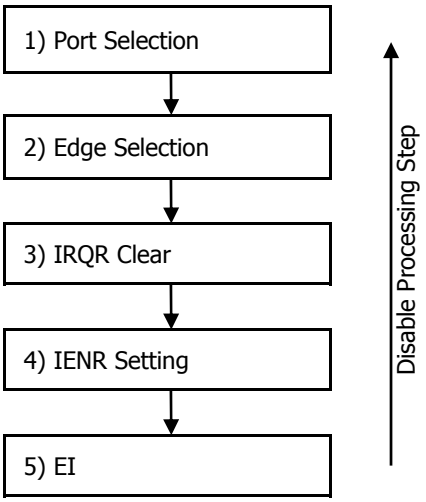
7.4. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

7.5. Multiple Interrupt

If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes "1", and each enable bit can accept interrupt request.
When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

Key-Scan or External Interrupt Enable Processing Step



7.6. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.
As soon as an interrupt is accepted, the content of the program counter is saved in the stack register which is 16 level stack area, and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 8 level stack area.
At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table corresponding to each interrupt.

Interrupt Processing Step

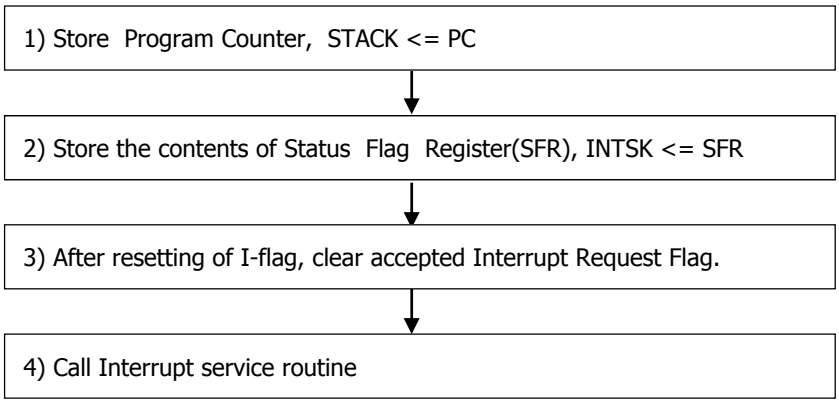
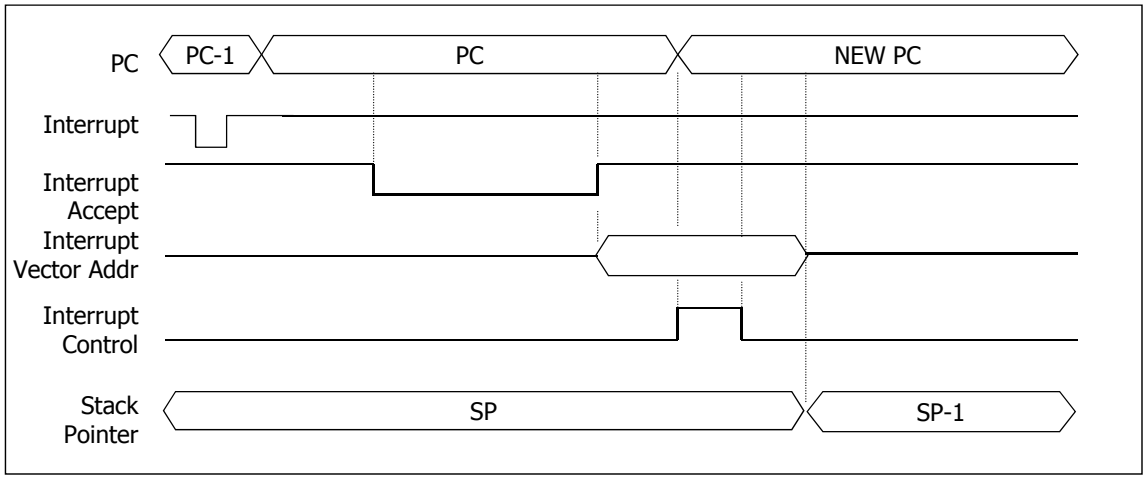


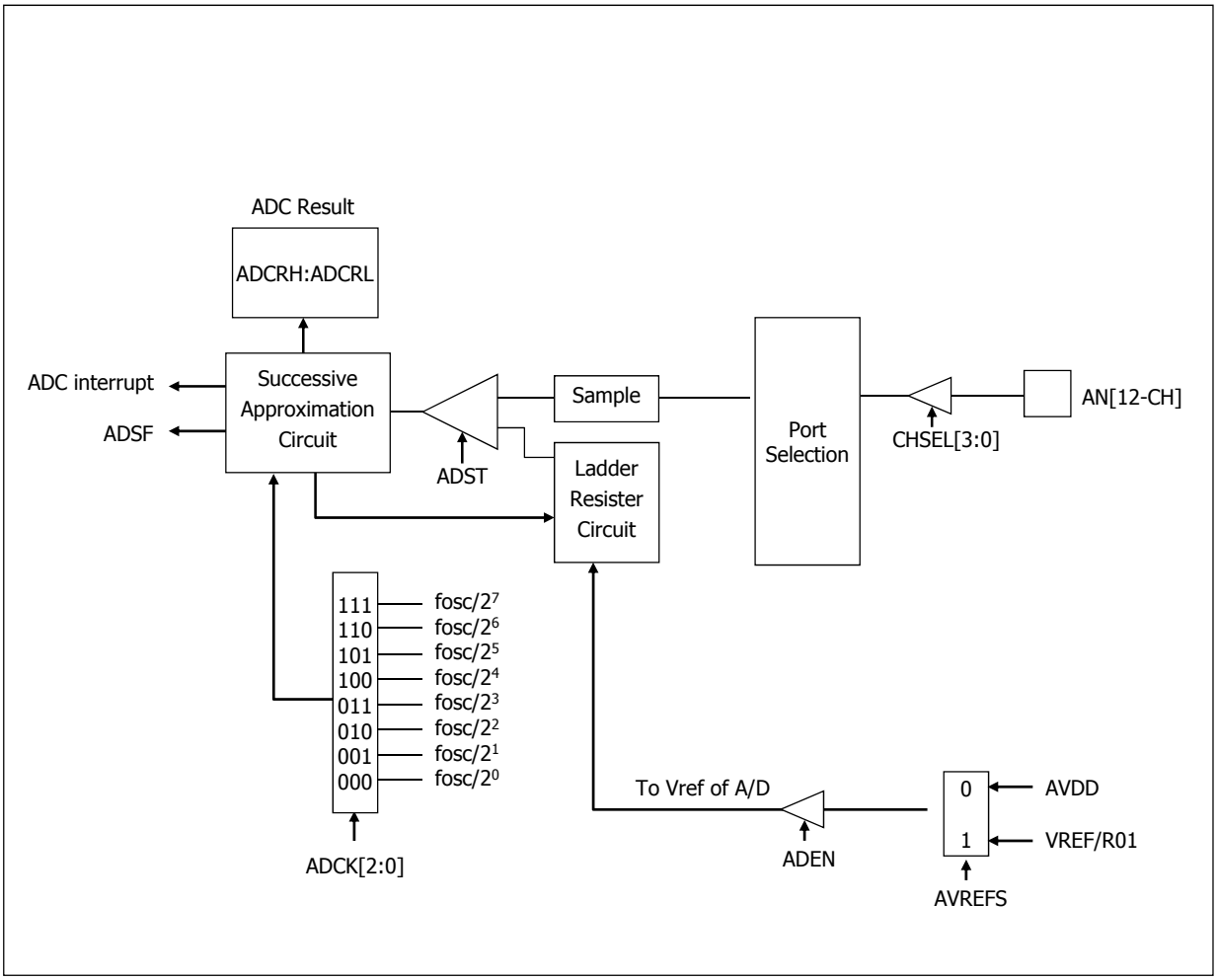
Fig. Interrupt Processing Step Timing



The analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding digital number.The A/D module has 16 selectable analog inputs.
The output of sample is the input into converter , which generates the result via successive approximation.

The A/D module has four register. These registers are
- A/D CONTROL MODE REG 0.(ADCM0)
- A/D CONTROL MODE REG 1.(ADCM1)
- A/D CONVERTER DATA REG LOW.(ADCRL)
- A/D CONVERTER DATA REG HIGH.(ADCRH)

Fig. A/D Converter Block Diagram



8.1. A/D Converter Control Registers

• A/D Converter Mode Register (ADCM0)

	7	6	5	4	3	2	1	0	
ADCM0	-	-	-	-	-	ADEN	ADST	ADSF	65h
initial value	0	0	0	0	0	0	0	1	
R/W	-	-	-	-	-	R/W	R/W	R	

Selection Mode of ADCM0

Bit Name	Selection Mode		Remarks
ADEN	0	ADC Disable	if (STOP) ADEN go to "L"
	1	ADC Enable	
ADST	0	A/D Conversion is Stop	
	1	A/D Conversion is Start. and cleared to "L" after 1 cycle	
ADSF	0	A/D Conversion is Processing	
	1	A/D Conversion is Completed	

• A/D Converter Mode Register (ADCM1)

	7	6	5	4	3	2	1	0	
ADCM1	CHSEL3	CHSEL2	CHSEL1	CHSEL0	ADCK2	ADCK1	ADCK0	AVREFS	67h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of ADCM1

(f_{OSC} = 4MHz)

Bit Name	Selection Mode		Remarks
CHSEL[3:0]	0000	Channel 0 Selection	if analog port selected
	0001	Channel 1 Selection	
	0010	Channel 2 Selection	
	0011	Channel 3 Selection	
	0100	Channel 4 Selection	
	0101	Channel 5 Selection	
	0110	Channel 6 Selection	
	0111	Channel 7 Selection	
	1000	Channel 8 Selection	
	1001	Channel 9 Selection	
	1010	Channel 10 Selection	
	1011	Channel 11 Selection	
	1100	Channel 12 Selection	
	1101	Channel 13 Selection	
	1110	Channel 14 Selection	
	1111	Channel 15 Selection	
ADCK[2:0]	000	PS0 (0.25us)	
	001	PS1 (0.5us)	
	010	PS2 (1us)	
	011	PS3 (2us)	
	100	PS4 (4us)	
	101	PS5 (8us)	
	110	PS6 (16us)	
	111	PS7 (32us)	
AVREFS	0	AVDD for ADC power	
	1	VREF for ADC power	

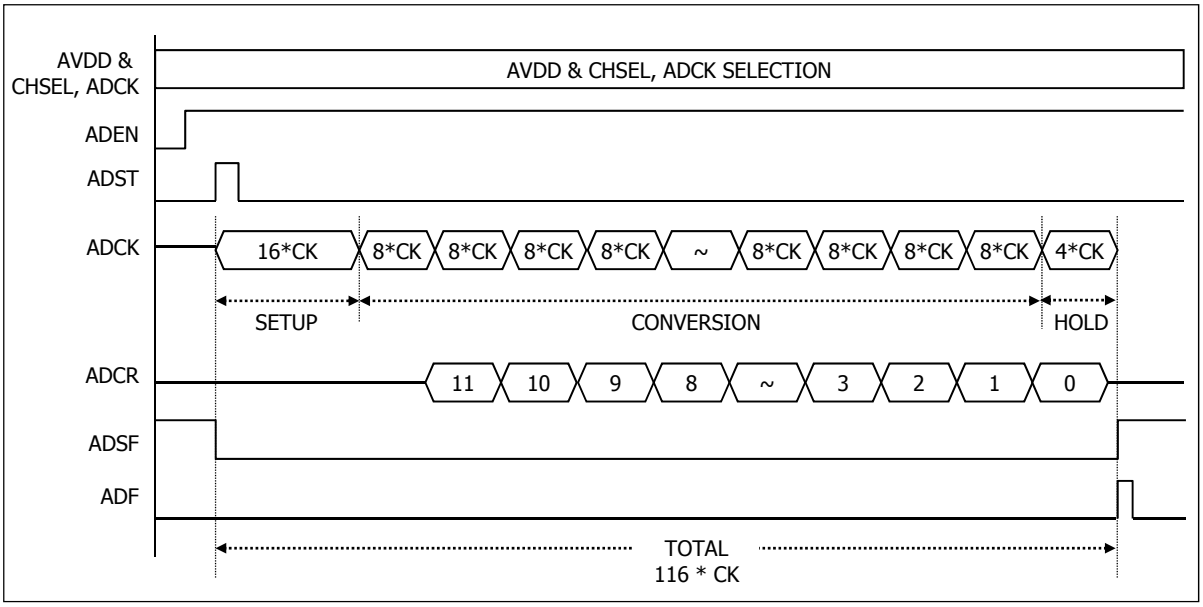
• A/D Converter Data Register Low (ADCRL)

	7	6	5	4	3	2	1	0	
ADCRL	ADCRL7	ADCRL6	ADCRL5	ADCRL4	ADCRL3	ADCRL2	ADCRL1	ADCRL0	66h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

• A/D Converter Data Register High (ADCRH)

	7	6	5	4	3	2	1	0	
ADCRH	-	-	-	-	ADCRH3	ADCRH2	ADCRH1	ADCRH0	67h
initial value	-	-	-	-	-	-	-	-	
R/W	-	-	-	-	R	R	R	R	

ADC Timing Diagram



• Total Conversion Time is

(16 + 8*12 + 4) * ADCK

freq = 4MHz

Bit Name	Selection Mode			Remarks
ADCK	000	Conversion Source Clock ($1/f_{OSC}$)	116 * 250ns = 29us	
	010	Conversion Source Clock ($2^2/f_{OSC}$)	116 * 1us = 116us	

8.2. A/D Converter Caution

8.2.1. Noise Countermeasures of AN[15:0]

It is recommend that a capacitor be connected externally as shown Fig. in order to reduce noise.

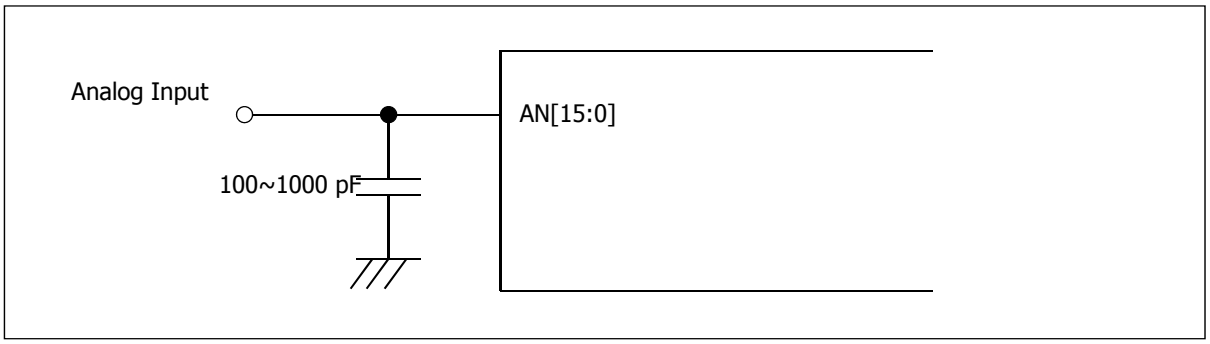


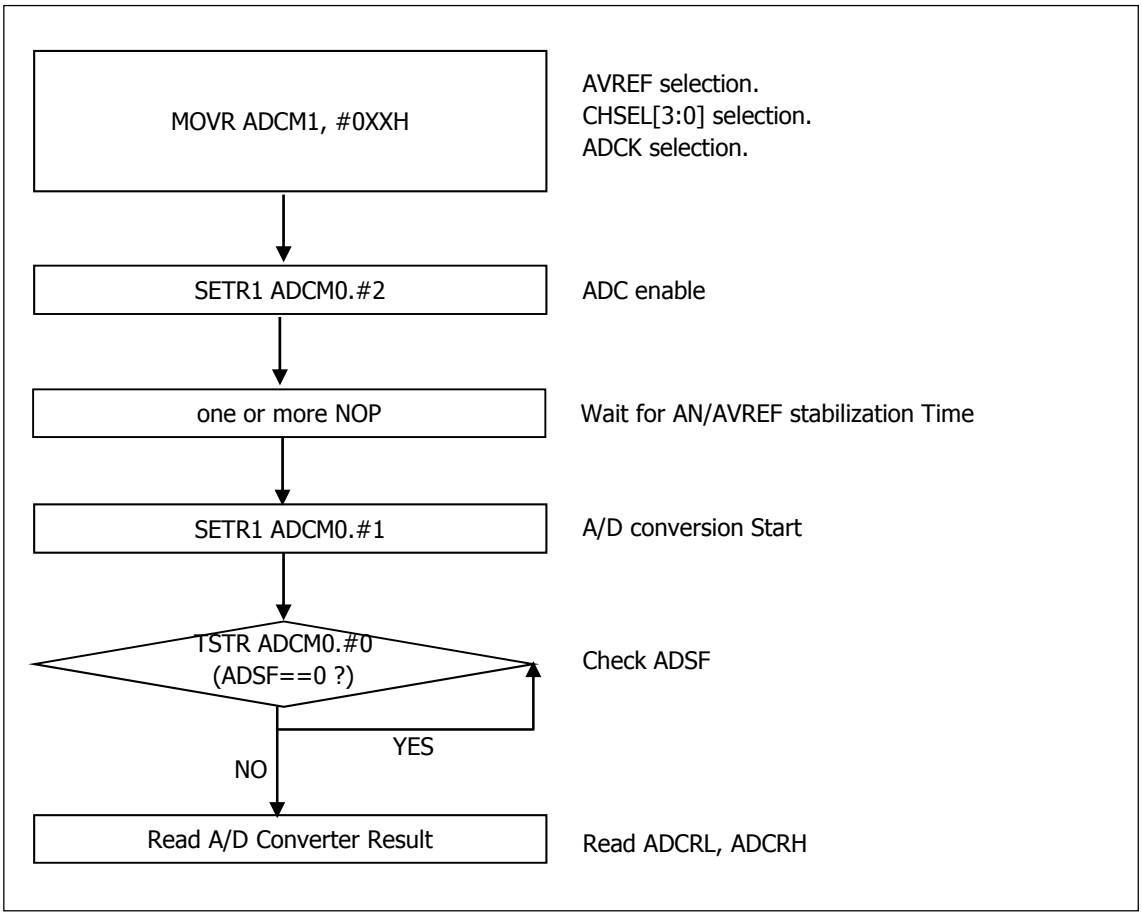
Fig. Analog input pin Connecting capacitor

8.2.2. AVDD pin input impedance

A series resistor string of approximately 100kΩ~150kΩ is connected between AVDD pin and VSS.

If the output impedance of AVDD is high, it will result in parallel connection to the series resistor between AVDD pin and AVSS, and there will be a large reference voltage error.

8.3. A/D Converter Operation Flow



9. STOP/SLEEP FUNCTION

9.1. Stop Mode

STOP mode can be entered by STOP instruction during program.
In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)     STOP        ;STOP instruction execution
        NOP         ;NOP instruction
```

Table. Operation State in Stop Mode

Internal circuit	STOP mode	REMARKS
Oscillator	Stop	
Internal CPU clock	Stop	
Register	Retained	
RAM	Retained	
I/O port , OUTPUT port	Retained	
Timer	Stop	
Watch dog Timer	Reset and restart at stop release	
Address Bus, Data Bus	Retained	

9.2. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port which is selected by KS Selection register for stop release is both edge , external interrupt and LVD, VDI mode release .
When there is a release signal of STOP mode, the instruction execution starts after stabilization oscillation time($2^{14} \times 4/f_{OSC}$ = 16.384ms at f_{OSC} = 4MHz)

Table. Stop Mode Release

Release Factor	Release Method	REMARKS
Power on reset	By Power on reset, Stop mode is release and system is initialized	
Key Input Port	Stop mode is released by low input of selected pin by KS Selection register	
External interrupt	Stop mode is release external interrupt input	
Release from LVD/VDI detection	Stop mode is release when release from LVD/VDI detection.	

9.3. Sleep Mode

Sleep mode can be entered by SLEEP instruction during program.
In SLEEP mode, oscillator and Peripheral source clock is running but system clock is stopped, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows SLEEP instruction for pre-charge time of Data Bus line.

```
ex)     SLEEP       ;SLEEP instruction execution
        NOP         ;NOP instruction
```

Table. Operation State in Sleep Mode

Internal circuit	SLEEP mode	REMARKS
Oscillator	Running	
Internal CPU clock	Stop	
Register	Retained	
RAM	Retained	
I/O port , OUTPUT port	Retained	
Timer	Operation	
Watch dog Timer	Reset and restart at sleep release	
Address Bus, Data Bus	Retained	

9.4. Sleep Mode Release

Release of SLEEP mode is executed by Power on reset , Key input Port which is selected by KS Selection register for sleep release is both edge , external interrupt, timer interrupt and Low LVD, VDI mode release .
When there is a release signal of SLEEP mode, the instruction execution starts after stabilization time($2^5 \times 4/f_{OSC}$ = 32us at f_{OSC} = 4MHz)

Table. Sleep Mode Release

Release Factor	Release Method	REMARKS
Power on reset	By Power on reset, Sleep mode is release and system is initialized	
Key Input Port	Sleep mode is released by low input of selected pin by KS Selection register	
External interrupt	Sleep mode is release external interrupt input	
Timer interrupt	Sleep mode is release Timer interrupt input	
Release from LVD/VDI detection	Sleep mode is release when release from LVD/VDI detection.	

10.1. Power On RESET

Power On Reset circuit automatically detects the rise of power voltage
(the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at "L" Level until oscillator is stable.
After power applies and starting of oscillation, this reset state is maintained for about oscillation cycle of fosc/4 $x2^{16}$ (about 65.536ms : at 4MHz).

Fig. Block Diagram of Power On Reset Circuit

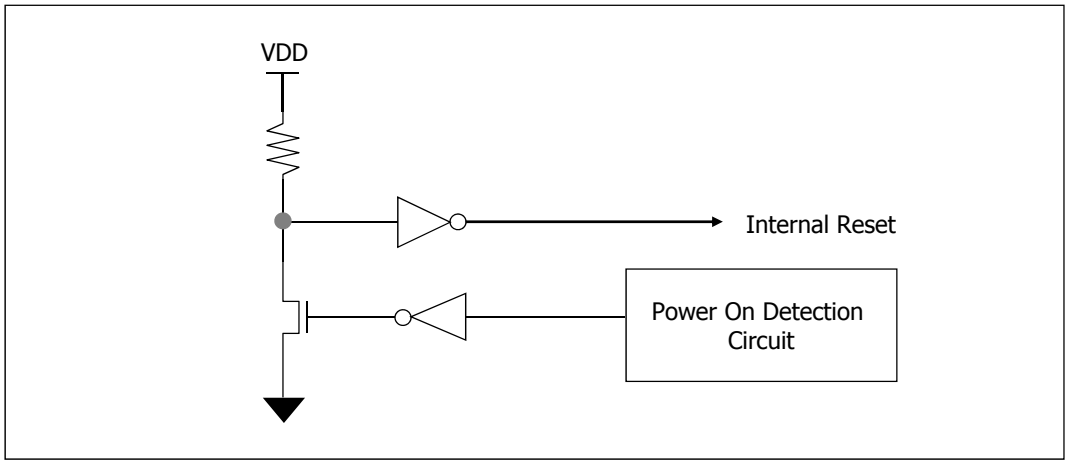
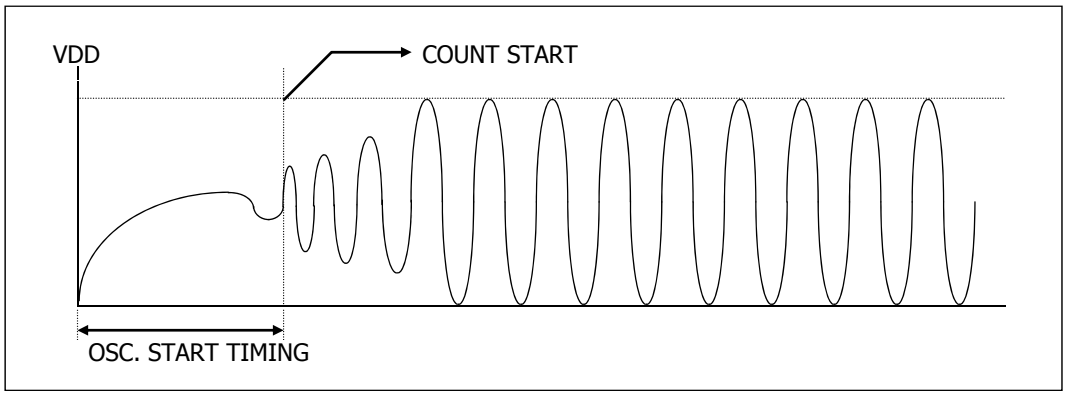


Fig. Oscillator stabilization diagram



Notice. When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

11.1. Low Voltage Detection Condition

An on board voltage comparator checks that V_{DD} is at the required level to ensure correct operation of the device.
If V_{DD} is below a certain level, Low voltage detector forces the device into low voltage detection mode.

11.2. Low Voltage Detection Mode

There is no power consumption except stop current.
1. STOP mode release function is disabled.
2. I/O port is configured as input mode.
3. Data memory is retained until voltage through external capacitor is worn out.
4. Interrupt disabled.
5. Oscillator is stop.

11.3. Release of Low Voltage Detection Mode

Reset signal result from new battery or any other power (normally 3V/5V) wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

11.4. Low Voltage Detection voltage selection (option)

User can select the voltage of Low Voltage detection voltage level.
One is high voltage version , another is low voltage version.

12. Voltage Detection Indicator Mode

12.1. Voltage Detection Indicator Register

It is useful to display the consumption of Batteries.
If V_{DD} power level is below a low voltage level which is higher than low voltage detection level (refer to Fig .) , The bit of VDIR register could be set according to the V_{DD} level sequentially.
The V_{DD} detection levels for Indication are three , that is , VDIER[2:0] of VDIER Register.
The V_{DD} detection flag for Indication are three , that is , VDIR[6:4], VDIR[2:0] of VDIR Register.
If detection is occurred, flag is set. After READ VDIR, flag VDIR[6:4] is cleared automatically.
The detection voltage level is in the DC Characteristics.

• Voltage Detection Indicator Enable Register (VDIER)

	7	6	5	4	3	2	1	0	
VDIER	-	-	-	ENST	VDIRST	VDIER2	VDIER1	VDIER0	7Eh
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	-	W	W	W	W	W	

Selection Mode of VDIER

Bit Name	Selection Mode		Remarks
ENST	0	Disable at STOP mode	
	1	Enable at STOP mode	
VDIRST	0	VDI Interrupt enable	if(VDIER[2:0] == enable)
	1	VDI RESET enable Must Set (ENST=1)	
VDIEN2	0	Disable	-
	1	Enable	*Indicator voltage : V_{VDIH} < 3.8V
VDIEN1	0	Disable	-
	1	Enable	*Indicator voltage : V_{VDIM} < 3.0V
VDIEN0	0	Disable	-
	1	Enable	*Indicator voltage : V_{VDIL} < 2.3V

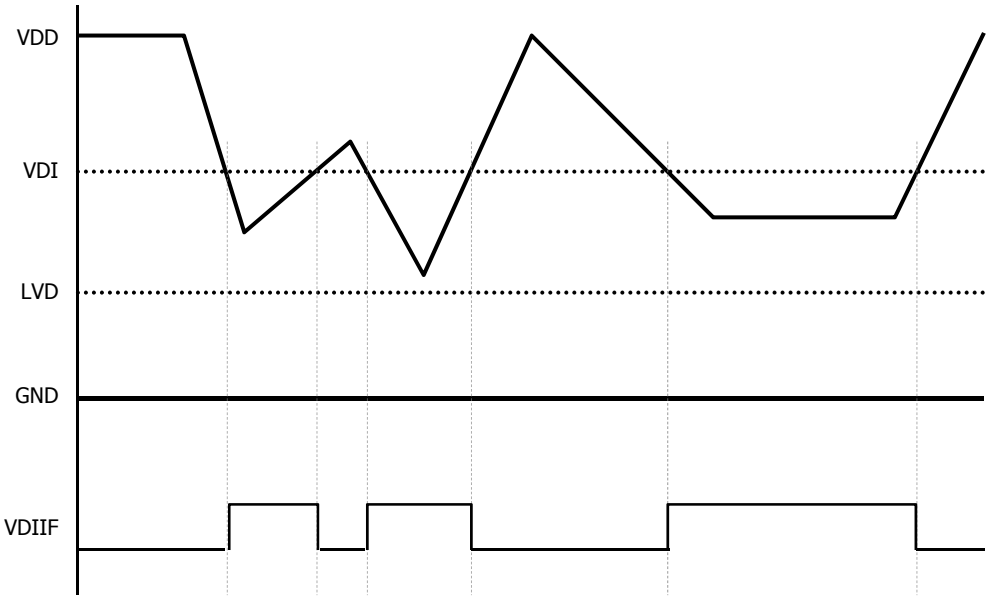
• Voltage Detection Indicator Data Register (VDIR)

	7	6	5	4	3	2	1	0	
VDIR	-	VDIR6	VDIR5	VDIR4	-	VDIR2	VDIR1	VDIR0	7Eh
initial value	0	0	0	0	0	0	0	0	
R/W	-	R	R	R	-	R	R	R	

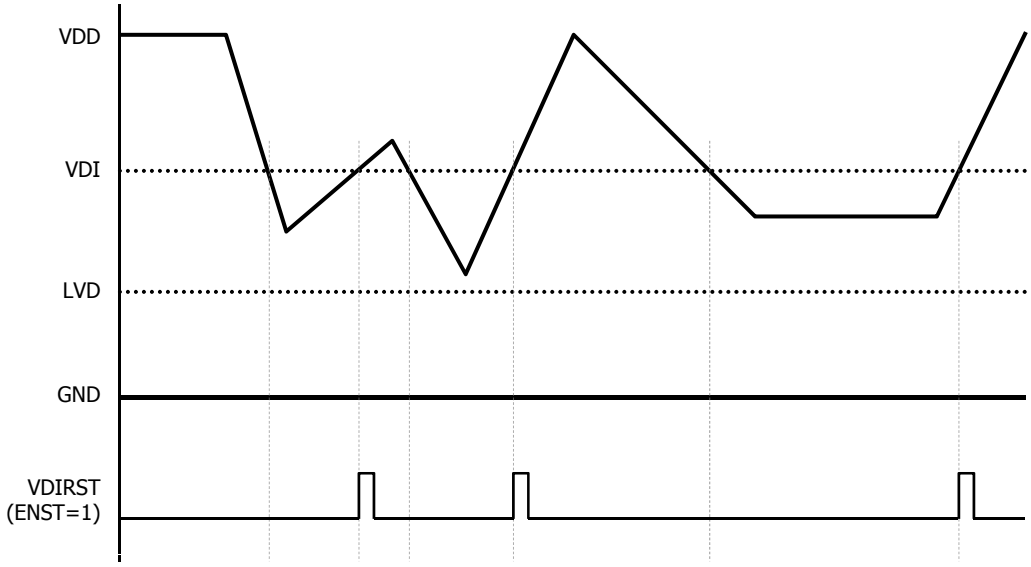
Selection Mode of VDIR

Bit Name	Selection Mode		Remarks
VDIR6	Set	if (VDIR2 == 1), flag is set.	if (V_{DD} > V_{VDIH}) after read, automatically cleared.
VDIR5	Set	if (VDIR1 == 1), flag is set.	if (V_{DD} > V_{VDIM}) after read, automatically cleared.
VDIR4	Set	if (VDIR0 == 1), flag is set.	if (V_{DD} > V_{VDIL}) after read, automatically cleared.
VDIR2	Set	*Indicator Status	always V_{DD} < V_{VDIH}
VDIR1	Set	*Indicator Status	always V_{DD} < V_{VDIM}
VDIR0	Set	*Indicator Status	always V_{DD} < V_{VDIL}

12.2. Timming Diagram (VDI Interrupt mode)

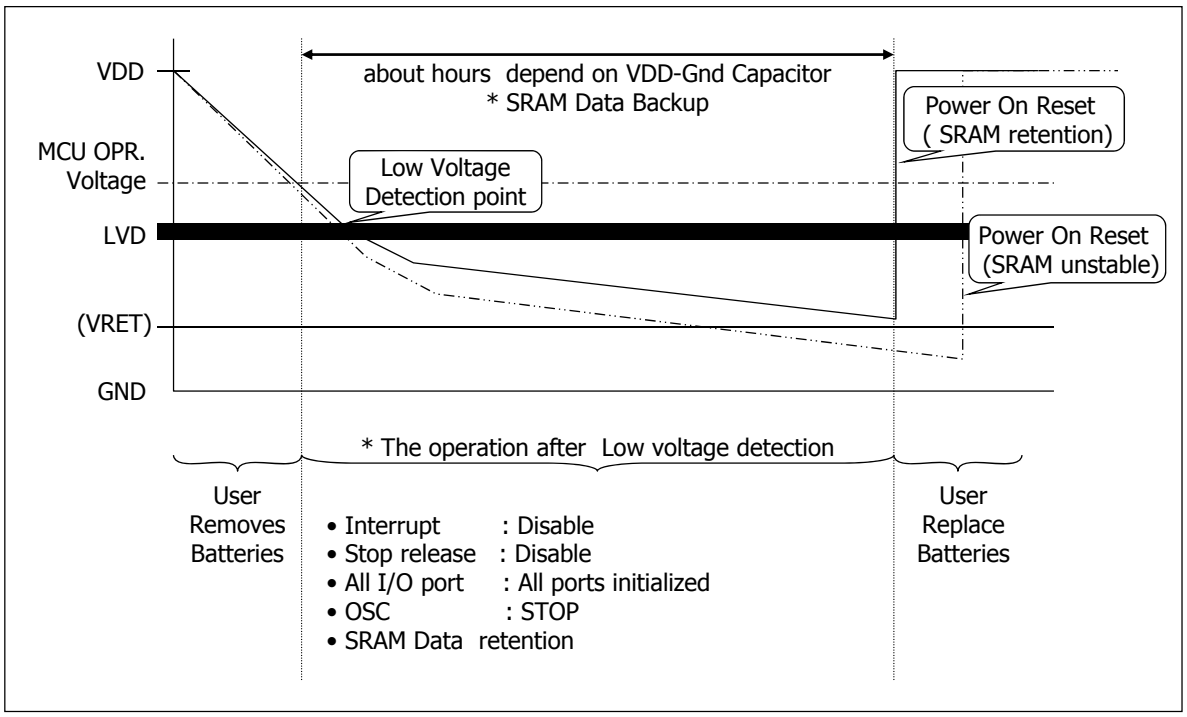


12.3. Timming Diagram (VDI RESET mode, Must set (ENST=1))



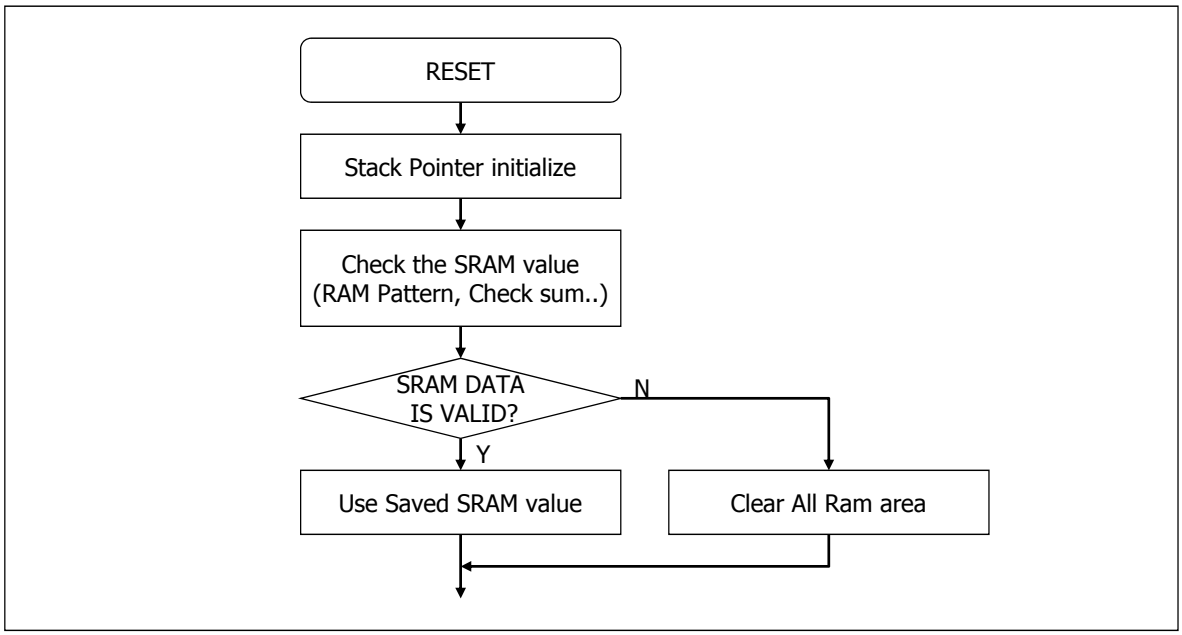
13.1 SRAM DATA BACK-UP after Low Voltage Detection

Fig. Low Voltage Detection and Protection



13.2. S/W flow chart example after Reset using SRAM DATA Back-up

Fig. S/W Flow Chart Example for SRAM Back-up



*. Code Options

Code Option Bit Mapping

☑ OPTION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTION	LOCK		prohibit bits		RSTS	XTS[2:0]			SXT	prohibit bits						
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Name	Code Option Description	Option Value	Remarks	
15	LOCK	LOCK Definition	Refer to Device Options		
14					
13:12	← *PROHIBIT BITS*				
11	RSTS	RESETB/R32 Selection	1	RESETB	
			0	R32	
10:8	XTS	Oscillator Type Selection	XTS[2:0]	R30/OSC1	R31/OSC2
		Internal RC 4MHz	111	R30(I/O)	R31(I/O)
		Internal RC 2MHz	110	R30(I/O)	R31(I/O)
		Internal RC 1MHz	101	R30(I/O)	R31(I/O)
		Internal RC 8MHz	100	R30(I/O)	R31(I/O)
		Internal RC 16MHz	011	R30(I/O)	R31(I/O)
		XT Oscillator	010	OSC1(I)	OSC2(O)
		External Clock Input	001	OSC1(I)	R31(I/O)
		External RC Oscillator	000	OSC1(I)	R31(I/O)
7	SXT	32.768KHz Oscillator enable	1	Disable	
			0	also, Selection XT[010] mode	
6:0	← *PROHIBIT BITS*				