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VSC8476
Datasheet

10 GbE/FC Serial Transceiver with XAUI and XGMII I/O

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FEATURES

- 10 GbE and 10 G Fibre Channel serial LAN transceiver
- Fully compliant with IEEE 802.3ae (10 GbE) and (10 G Fibre Channel) T11 Project-1413-D
- XFI compliant
- CML 10.3 Gbps to 10.5 Gbps high-speed front-end
- 4 × 3.125 Gbps to 3.1875 Gbps XAUI I/O
- XAUI lane programmability: lane swap, bit-order swap, invert, deskew, amplitude, emphasis, and equalization
- 8b/10b encoders/decoders
- XGMII I/O (1.5 V supply HSTL)
- Integrated gearbox function
- Support for data and control character 64B and 66B encoding and decoding
- Clock rate disparity compensation
- Multiple loopback modes
- Multiple test pattern generation and checking
- MDIO and two-wire serial interface management interfaces
- JTAG access port
- 1.2 V supply for low power consumption
- 1.5 V supply for XGMII operation
- Optional 1.5 V, 1.8 V, 2.5 V, or 3.3 V supply for TTL compatibility
- 1.2 W (typical) power in XAUI to XFI mode

GENERAL DESCRIPTION

The VSC8476 is a 10-gigabit Ethernet and 10-gigabit Fibre Channel serial transceiver, which provides a 10-gigabit attachment unit interface (XAUI) I/O, 8b/10b encoders/decoders, 10-gigabit media-independent interface (XGMII) I/O, 64b/66b encoding/decoding, gearbox function, 16:1 mux/demux, and high-speed I/O. With these functions, the VSC8476 implements the IEEE 802.3ae and T11 10 GFC XGMII extender sublayer (XGXS or PHY XS), physical coding sublayer (PCS), and physical medium attachment (PMA).

The VSC8476 supports the 10.3 Gbps and the 10.5 Gbps rates as defined by IEEE 802.3ae and T11 10 GFC. All specifications refer to the higher 10.5 Gbps rate for consistency; the lower 10 GbE rate is identified with parenthesis (10.3 Gbps). The device can operate using 1.2 V supply for optimal power and 1.5 V supply for the XGMII interface, dissipating a typical power of only 1.2 W. The VSC8476 is available in a 17 mm × 17 mm 252-ball package with 1 mm ball pitch.

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Figures

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Tables

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.0

Revision 4.0 of this datasheet was published on June 3, 2005. The following is a summary of the changes:

- The number of bits in the data field in the MDIO Frame Format figure was changed from 32 bits to 16 bits. For more information, see Figure 29, page 58.
- The GND and power locations in the top view of the power and ground pin location diagram were modified to match the pin diagram. For more information, see Figure 35, page 68.
- The maximum input high voltage was modified and footnotes were added to the input high voltage and the output high voltage parameters in the MDIO Electrical Interface Characteristics table. For more information, see Table 20, page 202.
- The descriptions of the E5, P4, and T3 pins were modified in the Pin Identifications table. For more information, see Table 35, page 216.
- The VSC8476 is available in two package types, including a lead-free package. For more information, see "Ordering Information," page 229.
- Thermal specifications were added for the lead-free package. For more information, see "Thermal Specifications," page 225.

Revision 2.2

Revision 2.2 of this datasheet was published on April 20, 2005. In revision 2.2 of the document, the AC characteristics for the XGMII driver were modified based on voltage.

Revision 2.1

Revision 2.1 of this datasheet was published on February 14, 2005. In revision 2.1 of the document, the label for the orientation of the pin diagram was corrected.

Revision 2.0

Revision 2.0 of this datasheet was published on February 4, 2005. This was the first publication of the document.

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1 Functional Descriptions

This section presents the functional description for the VSC8476 device. The VSC8476 is a 10-gigabit Ethernet and 10-gigabit Fibre Channel serial transceiver with a 10-gigabit attachment unit interface (XAUI) I/O, 8B and 10B encoders and decoders, 10-gigabit media-independent interface (XGMII) I/O, 64B and 66B encodeing and decoding, gearbox function, 16:1 mux/demux and high speed I/O.

With these functions, the VSC8476 implements the IEEE 802.3ae standard and T11 10 GFC XGMII extender sublayer (XGXS or PHY XS), physical coding sublayer (PCS), and physical medium attachment (PMA), as shown in Figure 1 in XAUI mode and Figure 2 in XGMII mode.

Figure 1. VSC8476 Functions in XAUI Mode

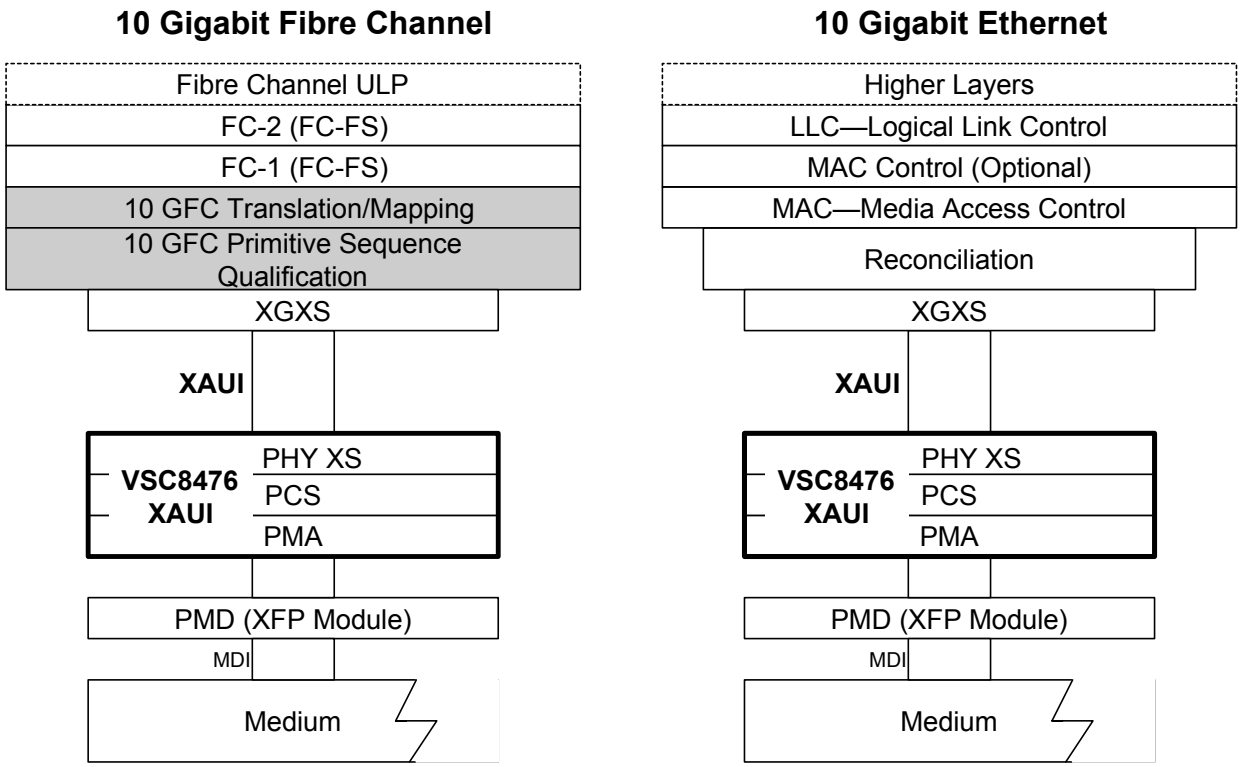

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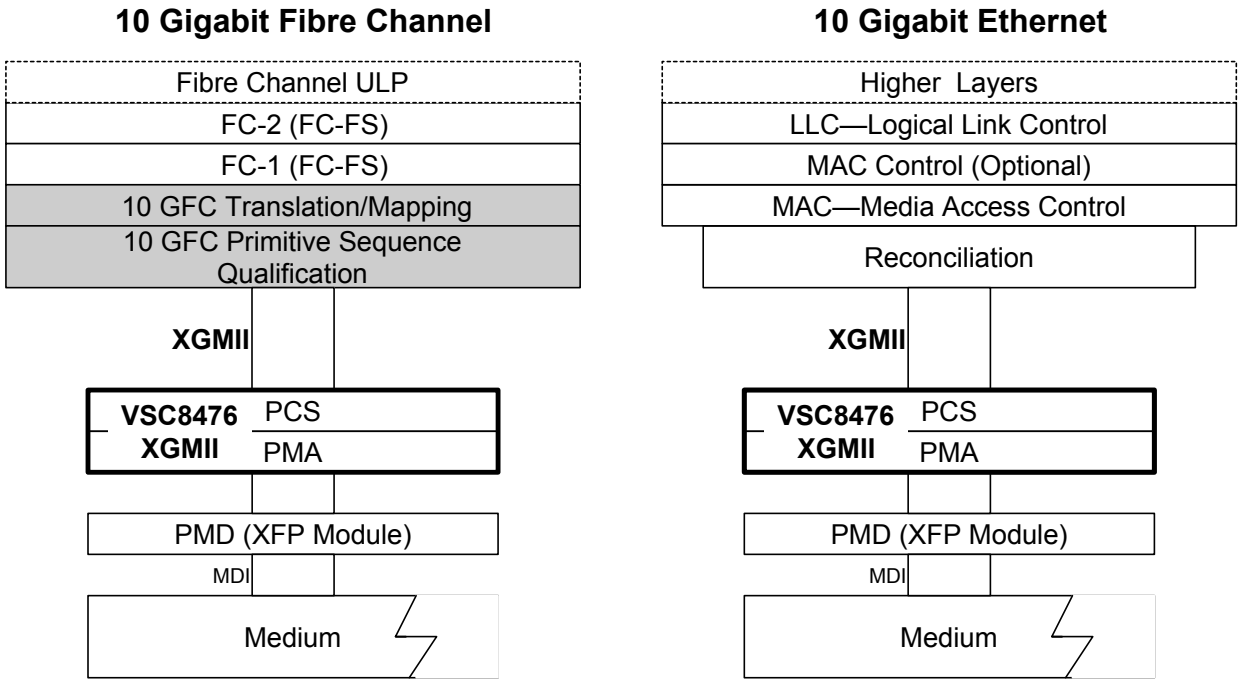
Figure 2. VSC8476 Functions in XGMII Mode



1.1 XAUI to XFI Mode

The transmit and receive operations are highlighted in the the XAUI to XFI mode and are illustrated in Figure 3.

To put the VSC8476 in the XAUI to XFI mode, set the IO mode select pin high (IOMODESEL=1). IOMODESEL sets the default value of bits 6 and 8 in the VS Control PCS register (see "Vendor-Specific Control PCS," page 116).

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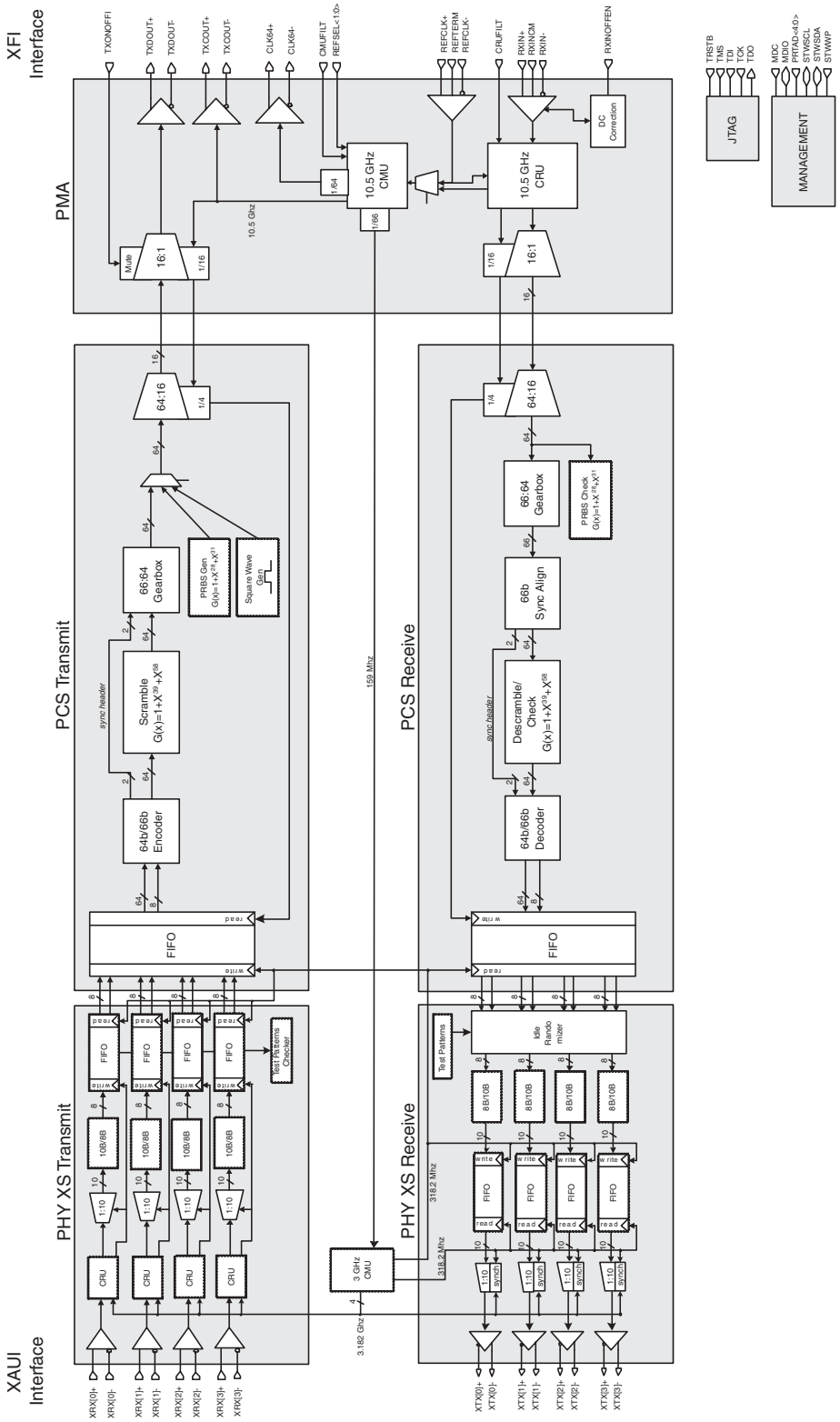
Figure 3. Functional Block Diagram - XAUI Mode



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1.1.1 Transmit Operation for XAUI to XFI Mode

The PHY XS block receives four 8b/10b encoded 3.1875 Gbps data lanes, XRX±[0:3] (XAUI interface). The clock is recovered and the data is deserialized on each of the four lanes. Synchronization is performed before the data is passed into the 10b/8b decoders. The decoded data and accompanying control bits are then presented to the FIFO. The FIFO deskews the four lanes and presents the aligned data to the PCS.

The FIFO within the PCS transfers path timing from the PHY XS recovered clock by adding or deleting idle characters during inter-packet gaps (IPG) as needed, as defined in Table 49-1 of IEEE 802.3ae-2002, to the integrated clock multiplier unit (CMU), which is driven by an external reference clock.

The eight data octets (8-bit characters) and eight control bits pass through the 64b/66b encoder, which maps XGMII data to a single 66-bit transmission block, as defined in Figure 49-7 of IEEE 802.3ae-2002. The first two bits of the 66-bit block contain the sync header, which is used to establish block boundaries for the synchronization process during the receive operation. The remaining 64 bits contain the payload.

The payload passes through the scrambler, which implements the polynomial G(x) = 1 + x39 + x58. The sync header bypasses the scrambler, and joins the scrambled payload at the 66:64 gearbox.

The gearbox adapts between the 66-bit width of the blocks and the 16-bit width of the PMA interface. The 64-bit block is demultiplexed to 16 bits and passed to the PMA, where it is serialized into the data stream. The 10.5-Gbps data stream and the divide by 64 (164.35 MHz) clock are provided on pins TXDOUT± and CLK64± respectively, for line transmission.

1.1.2 Receive Operation for XAUI to XFI Mode

High-speed NRZ serial data is received on pins RXIN± where it can be equalized for copper trace dispersion and presented to the CRU for clock recovery. The output of the CRU is then deserialized to a 16-bit bus and presented to the PCS. Within the PCS, data is further demultiplexed into 64 bits and presented to the 66:64 gearbox.

The 66-bit block is then aligned using the embedded two-bit sync header, which generates the 64-bit payload. The payload is descrambled using the polynomial G(x) = 1 + x39 + x58.

The descrambled payload and two-bit sync header pass through the 64b/66b decoder, where the block is mapped to valid XGMII data (eight octets) and control characters (eight bits).

The eight data octets and eight control bits are passed to the FIFO, where path timing is transferred from the divided (1/64) recovered clock to the divided (1/66) CMU clock. During IPG, idle characters are added or deleted as necessary to adapt between the two clock rates.

The eight data octets and eight control bits are then presented to the PHY XS block, where it is 8b/10b encoded and serialized. The serialized code words are then transmitted four at a time on the four XAUI outputs, XTX ±[0:3].

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1.2 XGMII to XFI Mode

The transmit and receive operations are highlighted in the the XGMII to XFI mode and are illustrated in Figure 4.

To set the VSC8476 into the XGMII to XFI mode, the IO mode select pin must be set low (IOMODESEL=0). IOMODESEL sets the default value of bits 6 and 8 in register VS Control PCS (see "Vendor-Specific Control PCS," page 116). VS Control PCS defaults to the appropriate value of 0x0140 after a reset is executed.

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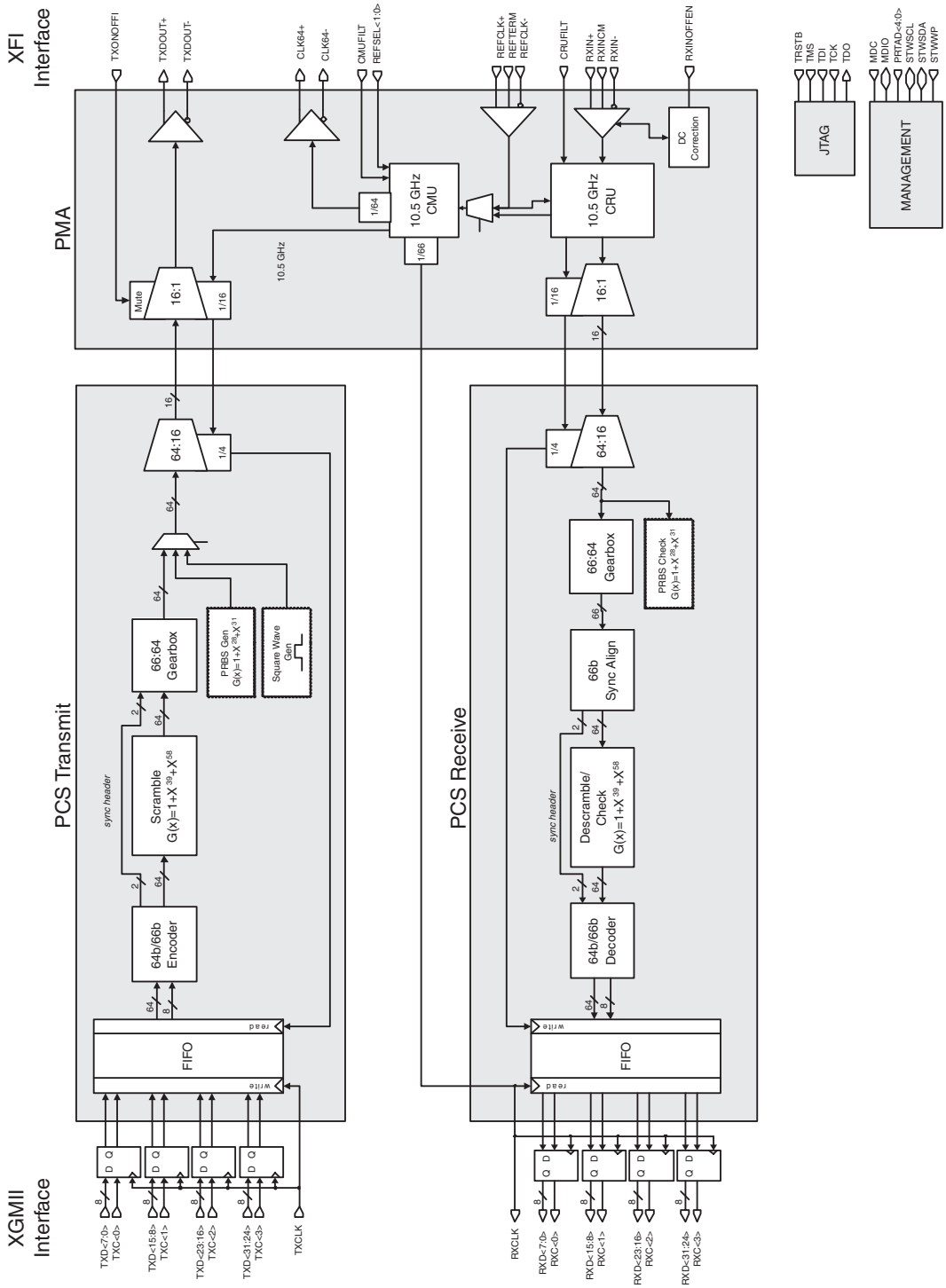
Figure 4. Functional Block Diagram - XGMII Mode



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1.2.1 Transmit Operation for XGMII to XFI Mode

Data and control signals are received on the XGMII Tx input pins TXD[31:0] and TXC[3:0] on each rising and falling edge of TXCLK. The data and accompanying control bits are then presented to the FIFO, which adds or deletes idle control characters during inter-packet gaps (IPG) as needed to adapt between the XGMII and PMA data rates as defined in Table 49-1 of IEEE 802.3ae.

Within the FIFO, path timing is transferred from the XGMII input clock to the integrated clock multiplier unit (CMU), which in turn is driven by an external reference clock.

The eight data octets (8-bit characters) and eight control bits pass through the 64b/66b encoder, which maps XGMII data to a single 66-bit transmission block, as defined in Figure 49-7 of IEEE 802.3ae standard. The first two bits of the 66-bit block contain the sync header, which is used to establish block boundaries for the synchronization process during the receive operation. The remaining 64 bits contain the payload.

The payload passes through the scrambler, which implements the polynomial G(x) = 1 + x39 + x58. The sync header bypasses the scrambler and joins the scrambled payload at the 66:64 gearbox.

The gearbox adapts between the 66-bit width of the blocks and the 16-bit width of the PMA interface. The 64-bit block is muxed down to 16 bits and passed to the PMA, where it is serialized into the high-speed data stream. The 10.5-Gbps data stream and divide by 64 (164.35 MHz) clock are provided on pins TXDOUT± and CLK64± respectively, for line transmission.

1.2.2 Receive Operation for XGMII to XFI Mode

High-speed NRZ serial data is received on pins RXIN± where it can be equalized for copper channel losses and presented to the CRU for clock recovery. The output of the CRU is then deserialized to a 16-bit bus and presented to the PCS. Within the PCS, data is further demultiplexed into 64 bits and presented to the 66:64 gearbox.

The 66-bit block is then aligned using the embedded two-bit sync header, generating the 64-bit payload. The payload is descrambled using the polynomial G(x) = 1 + x39 + x58.

The descrambled payload, and two-bit sync header pass through the 64b/66b decoder, where the block is mapped to valid XGMII data (eight octets) and control characters (eight bits).

The eight data octets and eight control bits are passed to the FIFO, where path timing is transferred from the divided (1/64) recovered clock to the divided (1/66) CMU clock. During IPG, idle characters are added or deleted as necessary to adapt between the two clock rates.

The eight data octets and eight control bits are then presented at the XMGII output interface on pins RXD[31:0] and RXC[3:0] in two consecutive transfers occurring on both rising and falling edges of output clock RXCLK.

When the VSC8478 detects a receive error (loss of lock) or an invalid sync header, a local fault is asserted on the XGMII Rx output interface (RXD[31:0] = 0100009c hex, and RXC[3:0] = "0001").

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1.3 XGMII to XAUI Mode

To set the VSC8476 into the XGMII to XAUI mode, do the following:

1. Set the IO mode select pin high (IOMODESEL=1).
2. Issue a reset to the device.
3. Write the value, 0x00C4, to VS Control PCS.

In this mode there are a few restrictions on the clock domains. The restrictions are as follows:

- REFCLK and TXCLK (XGMII input clock) must be derived from a common local source.
- RXCLK (XGMII output clock) is derived from REFCLK.
- Incoming XAUI data can be ±100 ppm from the REFCLK.

1.3.1 Transmit Operation for XGMII to XAUI Mode

Data and control signals are received on the XGMII Tx input pins TXD[31:0] and TXC[3:0] on each rising and falling edge of TXCLK. The eight data octets and eight control bits are then presented to the PHY XS block, where the data is 8b/10b encoded and serialized. The serialized code words are then transmitted four at a time on the four XAUI outputs, XTX±[0:3].

Note that the XGMII input clock (TXCLK) must be synchronous with the CMU reference clock (REFCLK±).

1.3.2 Receive Operation for XGMII to XAUI Mode

The PHY XS block receives four 8b/10b encoded 3.1875-Gbps data lanes, XRX±[0:3] (XAUI Interface). The clock is recovered and the data is deserialized on each of the four lanes. Synchronization is performed before the data is passed into the 10b/8b decoders. The decoded data and accompanying control bits are then presented to the FIFO. The FIFO deskews the four lanes transfers path timing from the PHY XS recovered clock to the integrated clock multiplier unit (CMU), which is locked to the external reference clock. The path timing is transferred by adding or deleting idle characters during inter-packet gaps (IPG) as needed, as defined in 48.2.4.2.3 of the IEEE standard 802.3ae.

The eight data octets and eight control bits are then presented at the XMGII output interface on pins RXD[31:0] and RXC[3:0] in two consecutive transfers occurring on both rising and falling edges of output clock RXCLK.

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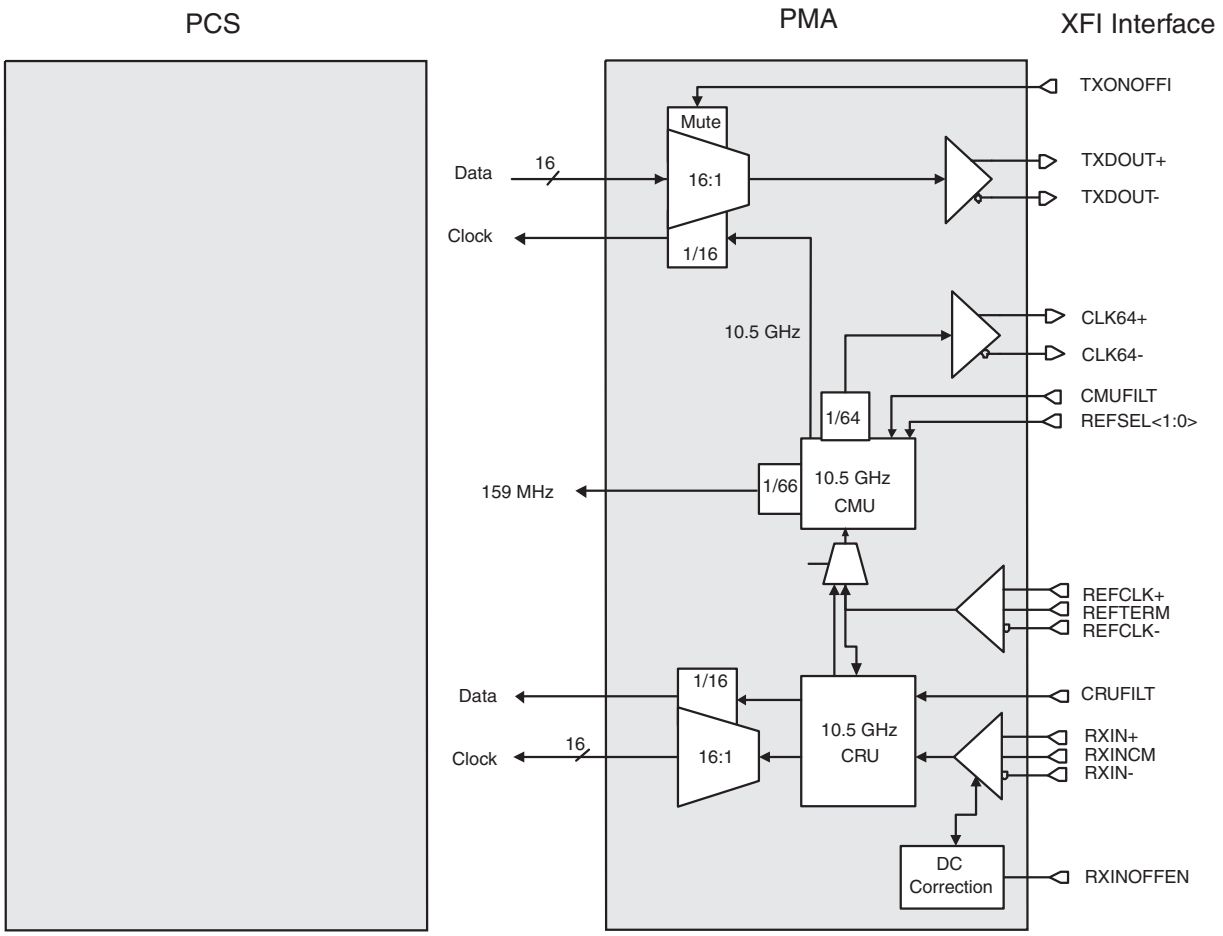
1.4 Physical Media Attachment (PMA)

The following block diagram (see Figure 5) shows the PMA.

Figure 5. PMA Block Diagram



1.4.1 Multiplexer Operation

The PMA transmitter includes a CMU and a 16-bit multiplexer that receives 16-bit data from the PCS block, which generates a 10.5-Gbps serial output on pins TXDOUT±. The CMU provides a divided down by 64 (164.35 MHz) clock output on pins CLK64± for optional use as a reference clock to an XFP module.

By default, the PMA transmits the LSB first. If desired, the MSB can be selected (using MDIO) as the first bit transmitted.

The high-speed output data (TXDOUT±) can be muted (continuous zeros) by setting TXONOFFI = '0'. The default is 1, which is set by an internal pull-up.

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1.4.2 Clock Multiplier Unit (CMU)

An on-chip PLL generates the high-speed transmit clock from the externally provided REFCLK± input. The on-chip PLL uses a low-phase noise reactance-based VCO. The reference clock should be of high quality since noise on the reference clock below the loop bandwidth of the PLL passes through the PLL and appears as jitter on the outputs (TXDOUT±, CLK64±).

The VSC8476 transfers reference clock noise in addition to its own intrinsic jitter during such conditions. Preconditioning the reference clock signal may be necessary to avoid passing reference clock noise. The reference clock must have a frequency accuracy of ±100 ppm.

1.4.2.1 Reference Clock Input

The VSC8476 accepts any of the following REFCLK frequency ranges for 10-GFC and 10-GbE data rates:

- 657.4 (644.53) MHz
- 164.35 (161.13) MHz
- 159.37 (156.25) MHz

Use the REFSEL[1:0] input pins to select the appropriate clock frequency multiplier. The following REFCLK Frequency Selection table lists the correspondence between the REFSEL[1:0] settings and selected REFCLK frequencies.

Table 1. REFCLK Frequency Selection

REFSEL[1:0]	REFCLK Frequency (MHz) 10 GFC (10 GbE)	REFCLK Multiplier
00	159.37 (156.25)	66
01	164.35 (161.13)	64
10	657.4 (644.53)	16
11	Reserved	

The incoming low-speed reference clock inputs are received by differential LVPECL inputs (REFCLK±) with DC levels shown in Table 29, “Reference Clock Specifications,” page 209. The reference clock input receiver diagram is shown in Figure 6.

The on-chip termination is 100 Ω equivalent between true and complement. An internal bias generator, nominally set at 0.67 * VDD12TX, is provided for AC-coupling. An internal termination tap, REFTERM, is provided to allow adjustment of the input common-mode voltage. It is recommended to add an external capacitor between REFTERM, and VDD or ground. Single-ended reference clock operation is possible, and when implemented, both inputs must have equivalent termination. However, the best jitter performance is obtained using a differential reference clock.

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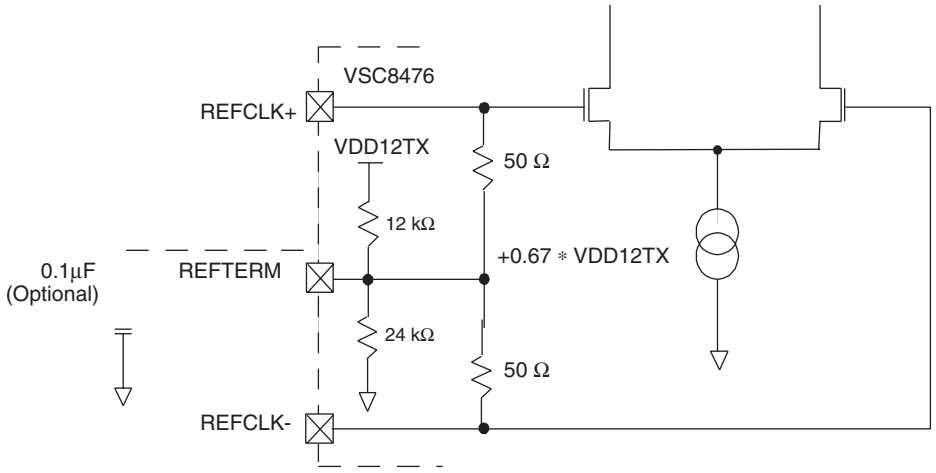
Figure 6. Reference Clock Input Receiver



1.4.3 External Capacitors

For loop filter control and to minimize the impact of common mode noise, especially power supply noise, the on-chip PLLs require external 1 µF capacitors that are connected between pins CMUFILT and GND for the CMU, and CRUFILT and GND for the CRU. These capacitors should be amultilayer ceramic dielectric or better with at least a 5-V working voltage rating. NPO is preferred over an X7R capacitor for temperature stability and to reduce power supply noise sensitivity.

1.4.4 Transmitter XFI Data CML Output

The CML high-speed data output driver consists of a differential pair designed to drive a 50 Ω transmission line. The output driver uses an on-chip source termination of 50 Ω to VDD12TX, minimizing any reflections as shown in Figure 7, "CML XFI Output Termination".

For single-ended operation at the transmitter, the unused TXDOUT+ or TXDOUT– signal must be terminated with a resistor to VSS having a value equal to the characteristic impedance of the copper transmission channel. The TXONOFFI control input, when LOW, causes TXDOUT± to maintain logic zero output.

1.4.5 Transmitter Data CML Output

The CML high-speed data output driver consists of a differential pair designed to drive a 50-Ω transmission line. The output driver uses an on-chip source termination of 50 Ω to VDD12TX, minimizing any reflections. See Figure 7.

For single-ended operation at the transmitter, the unused TXDOUT+ or TXDOUT– signal must be terminated with a resistor to VSS having a value equal to the characteristic impedance of the copper transmission channel.

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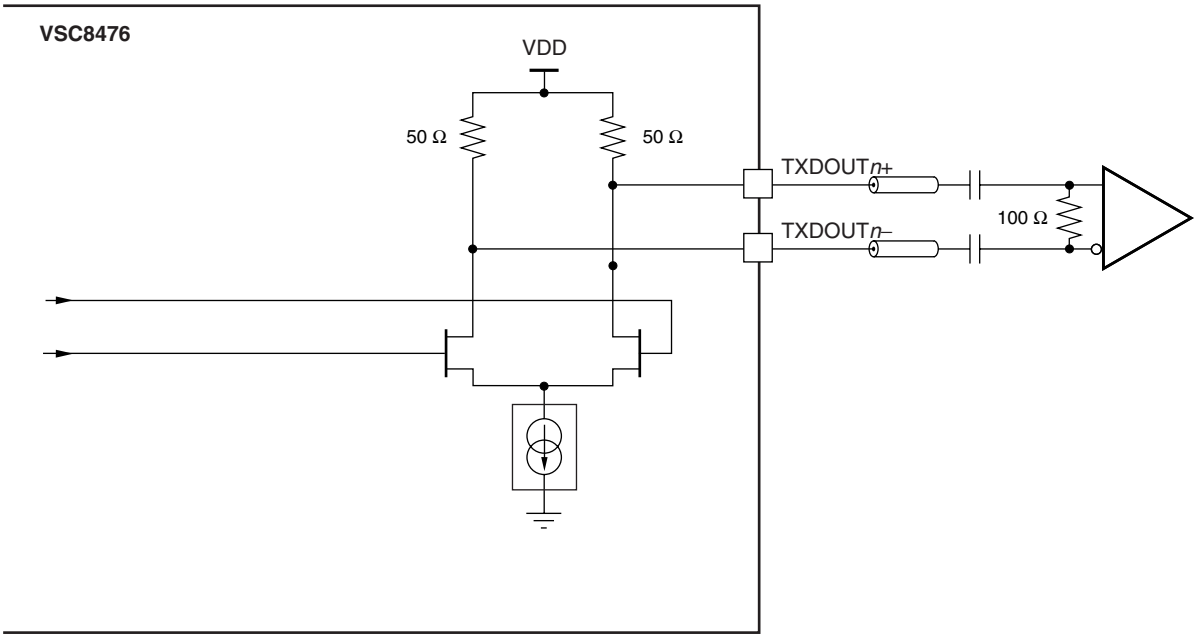
1.4.6 Transmitter Divide by 64 Clock Output

The divide by 64 clock output (CLK64±) is intended as a reference clock source for a XFP module. The divide by 64-clock output driver consists of a differential pair designed to drive a 50-Ω transmission line. The output driver is source terminated on the die (50 Ω to VDD12TX) similar to the high-speed clock output, minimizing any reflections. For more information about the CML XFI output termination diagram, see Figure 7.

For single-ended operation at the transmitter, the unused CLK64+ or CLK64– signal must be terminated similar to the signal trace in use.

Figure 7. CML XFI Output Termination



1.4.7 High-Speed Data Inputs

The incoming 10.3 Gbps or 10.5 Gbps data is received by high-speed connections (RXIN±). The VSC8476 incorporates a demultiplexer to convert the high-speed serial data (RXIN±) into 16 bits. The inputs are terminated internally with 50 Ω to RXINCM (see Figure 8, page 31). This forms a 100 Ω AC equivalent impedance across the differential inputs to absorb differential mode noise and a center-tapped virtual ground brought out as the RXINCM pin to absorb common mode noise. The transmission lines to the inputs comply with the XFI link requiring a nominal 100-Ω differential impedance (50-Ω single-ended impedance) for optimum signal transfer.

The inputs can be AC-coupled to allow for appropriate common mode voltage adjustments. The device may optionally be DC-coupled, which requires that proper common mode be provided. For more information about the AC and DC requirements for this interface, see "XFI Receiver Specifications for Serial Input Performance," page 203.

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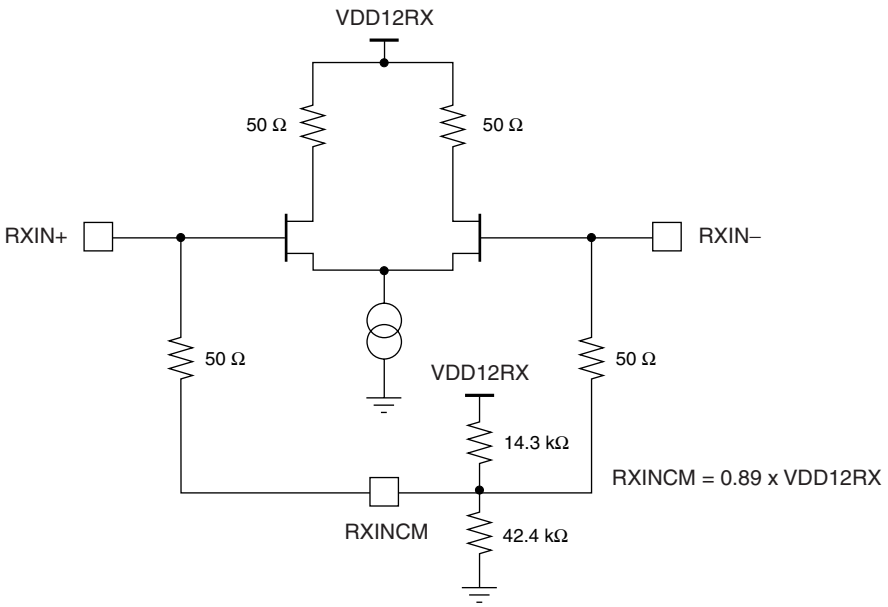
The VSC8476 is designed to operate with XFI signaling based on nominal 100-Ω differential impedance and AC coupling. The AC coupling capacitors on the high-speed serial data inputs (RXIN±) are expected to be in the module. The RXINCM pin should be AC-coupled to ground through a 0.1 µF capacitor to provide a proper return path for the 50-Ω termination. For more information, see Figure 9, page 32.

The VSC8476 can also operate in a single-ended mode. The RXINCM pin should be AC-coupled to ground through a 0.1 µF capacitor. The unused input should also be tied to a clean AC ground to prevent the RXIN+ signal from internally coupling through to RXIN- and degrading input sensitivity. Note that the total current through the 50-Ω resistor is limited to 25 mA and therefore, there is not more than a 1-V difference between RXIN+ and RXINCM, or RXIN– and RXINCM.

Figure 8. CML XFI Data Receiver



1.4.7.1 XFI Data Input Receiver Equalization

Incoming data on the RXIN± inputs may contain a substantial amount of inter-symbol interference (ISI) or deterministic jitter that reduces the ability of the receiver to recover data without errors. A programmable equalizer is provided in the receiver input buffer to compensate for this deterministic jitter. This circuit is designed to effectively reduce the ISI commonly found in the copper PCB traces of an XFI-compliant channel or backplane due to low frequencies being attenuated less than high frequencies as a result of the skin effect and dielectric losses. See the channel loss model as defined in the XFP multi-source agreement.

The XFI RXIN equalizer includes two-bit control for peaking and decay. Overall receiver equalization response is adjusted by setting the four internal register bits, as shown in Table 2.

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Table 2. Register 1x8002 Vendor-Specific RXIN Equalization Control

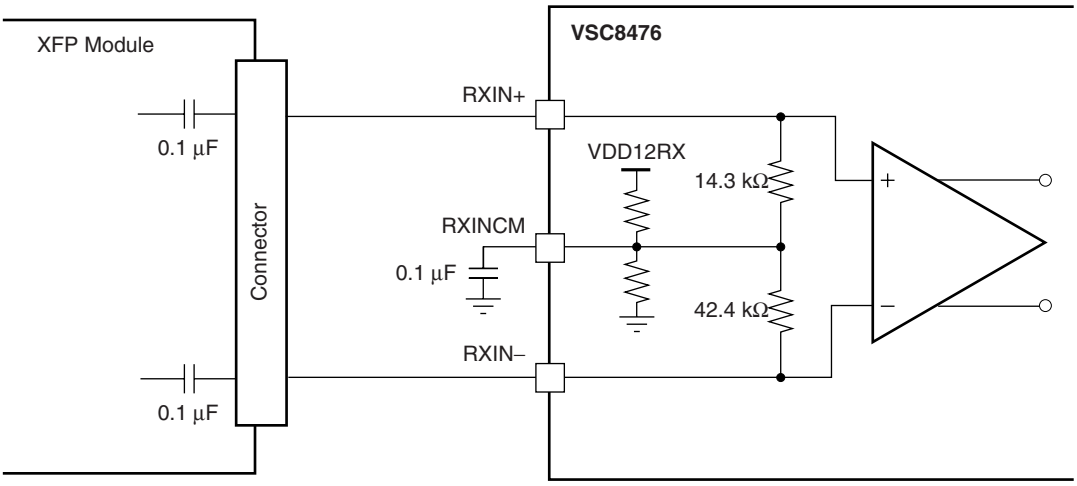
Peaking		Decay		Comment
Bit 14	Bit 13	Bit 12	Bit 11	
1	1	1	1	Default
1	1	0	0	XFI channel recommended[1]

1. Recommendations are based on characterization data. Some applications may have optimal settings that diverge from the recommendations.

1.4.7.2 Limiting Amplifier

The incoming XFI data inputs, RXIN±, are internally biased to accommodate AC-coupling from an optical receiver or transceiver module, as shown in Figure 9, "Differential Limiting Amplifier Input, AC-Coupled". In most situations, these inputs have high-transition density and little DC offset. All serial data and clock inputs have the same circuit topology with the reference voltage created by a resistor divider, as shown in Figure 8, page 31.

Figure 9. Differential Limiting Amplifier Input, AC-Coupled



1.4.7.3 Loss of Signal

There is a SONET-compliant CRU LOS detector that monitors the incoming high-speed data and detects if the signal has failed to transition from a 1 to 0, or from 0 to 1 within 2.3 µs to 100 µs. After detection of this condition, the CRU outputs an error to the MDIO and the PCS. The CRU automatically locks to the reference clock input, and the PCS presents local fault on the XGMII output interface (RXD[31:0] = 0100009c hex). Upon the restoration of data at the high-speed input, the CRU automatically switches from locking on the reference clock to locking back to the incoming data within 125 µs to 250 µs.

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1.5 Physical Coding Sublayer (PCS)

The physical coding sublayer (PCS) is defined in IEEE 802.3ae standard Clause 49. It is composed of the PCS transmit, PCS receive, block synchronization, and BER monitor processes. The PCS functions can be further broken down into encode or decode, scramble or descramble, and gearbox functions, as well as various test and loopback modes.

1.5.1 XGMII Tx and Rx FIFO

The PCS block transmits and receives eight data octets and eight control bits in two consecutive transfers of four data octets and four control bits at the XGMII interface. For either direction, the FIFO adds or deletes idle characters (/I/), or deletes sequence ordered_sets (/Q/), as required to perform clock rate disparity compensation between the XGMII and PMA data rates.

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1.6 Control Codes

The following table lists the control characters, notation, and control codes.

Table 3. Control Codes

Control Character	Notation	XGMII Control Code	10-G BASE-R Control Code	10-G BASE-R O Code	8b/10b Code[1]
Idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
Start	/S/	0xfb	Encoded by block type field		K27.7
Terminate	/T/	0xfd	Encoded by block type field		K29.7
Error	/E/	0xfe	0x1e		K30.7
Sequence ordered_set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
Reserved 0	/R/[2]	0x1c	0x2d		K28.0
Reserved 1		0x3c	0x33		K28.1
Reserved 2	/A/	0x7c	0x4b		K28.3
Reserved 3	/K/	0xbc	0x55		K28.5
Reserved 4		0xdc	0x66		K28.6
Reserved 5		0xf7	0x78		K23.7
Signal ordered _set[3]	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

1. For information only. The 8b/10b code is specified in Clause 36. Usage of the 8b/10b code for 10-Gbps operation is specified in Clause 4.

2. The codes for /A/, /K/ and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the PHY XS to send them on the XGMII.

3. Reserved for INCITS T11 - 10-G Fibre Channel µs.

1.6.1 64b/66b Encode and Decode

For the transmit path, the 64b/66b encoder maps the eight characters and eight control bits on the XGMII to a single 66-bit block. For the receive path, the reverse is performed. The first two bits (0 and 1) of this block contain the block synchronization header, which is used for block alignment on the receive path. These bits have the value of 01 when all eight XGMII characters are data or they have the value of ten if at least one XGMII character is a control character. The remaining 64 bits of the 66-bit block contain the payload (see Figure 10). VSC8476 supports the use of all control codes and ordered sets necessary for 10-GbE and 10-GFC operation. If an invalid block is encountered, all characters of the block are mapped to the error (/E/) character.

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Figure 10. 64b/66b Block Formats

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_0 C_1 C_2 C_3/O_4 D_5 D_6 D_7	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
C_0 C_1 C_2 C_3/S_4 D_5 D_6 D_7	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
O_0 D_1 D_2 D_3/S_4 D_5 D_6 D_7	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
O_0 D_1 D_2 D_3/O_4 D_5 D_6 D_7	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
O_0 D_1 D_2 D_3/C_4 C_5 C_6 C_7	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

1.6.2 Scrambler and Descrambler

For the transmit path, the 64-bit payload is scrambled using a self-synchronizing scrambler that implements the polynomial G(x) = 1 + x39 + x58. The sync header bypasses the scrambler. For the receive path, the data is passed through the same polynomial, resulting in restoration of the original payload data.

1.6.3 66:64 Gearbox

The PCS block also contains the gearbox function, which adapts between the 66-bit width of the encoded and scrambled data blocks and the 16-bit width of the PMA parallel interface.

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1.6.4 PCS Test Modes

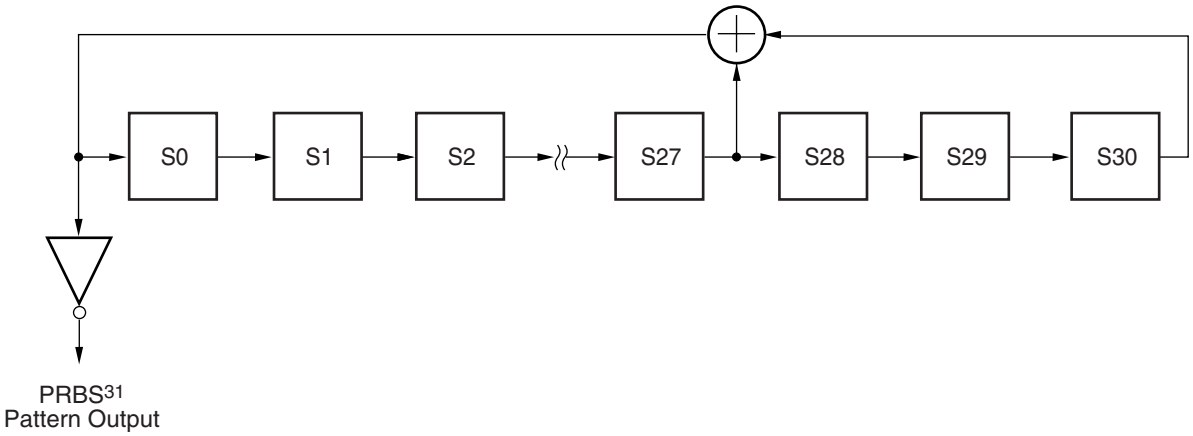
For more information about the bit settings for test mode settings for the MDIO Test Pattern Control register (3x002A), see Table 16, page 112.

For recommended test patterns, see IEEE 802.3ae-2002 Clause 52.9.

1.6.4.1 PRBS31 Test Pattern Generator and Checker

The PCS contains a 2^{31} –1 PRBS pattern generator and checker, which implements the inverted version of the generating and checking polynomial $G(x) = 1 + x^{28} + x^{31}$. When enabled, the generator sends PRBS31 data on the transmit path to TXDOUT± (see Figure 11).

Figure 11. PRBS31 Pattern Generator



The self-synchronizing PRBS31 test pattern checker in the receive path checks the incoming PRBS31 pattern for bit errors (see Figure 12). A 16-bit counter is implemented to record bit errors. This counter is accessed using MDIO register 10GBASE-R PCS Test Error Counter (see "10GBASE-R PCS Test Error Counter," page 113). This is a saturating counter (stops counting when full) that is cleared upon read and upon reset.

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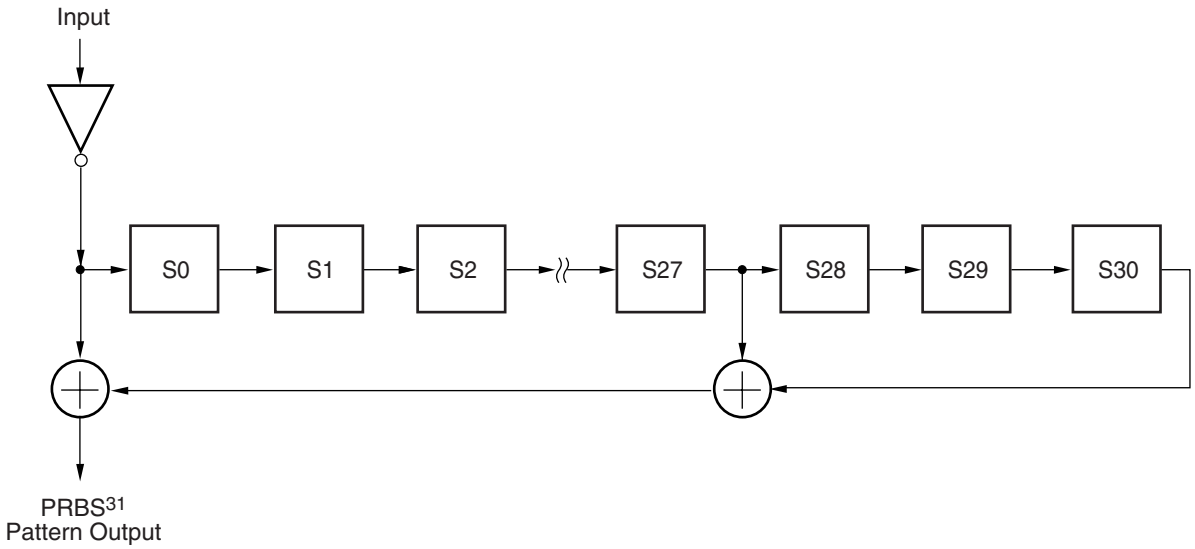
Figure 12. PRBS31 Pattern Checker



1.6.4.2 Pseudo-Random Test Pattern Generator and Checker

When the pseudo-random pattern is selected, the test pattern is generated by the scrambler using 58-bit seeds, which are loaded using the MDIO registers and the selected data patterns. The seeds are loaded in the following pattern:

- Seed A
- Seed A invert
- Seed B
- Seed B invert

Either 64 zeros or the 64-bit encoding for the two local fault ordered sets can be selected as the data pattern using the MDIO register (3x2A.0). Additionally, a user-defined 64-bit data pattern can be selected by loading MDIO registers (3x8000) through (3x8003) with the desired pattern (MSB at MDIO register (3x8003[15])), and setting MDIO register (3x8005[0])='1'.

The characteristics of the pseudo-random test pattern can be varied by varying the seed values and the data pattern.

When Pseudo-Random Test mode is selected for the receive path, the 16-bit counter MDIO register (3x2B) (same as PRBS31 counter) is used to record errored blocks. Note that for the PRBS31 mode, the counter records BIT errors, and for the Pseudo-Random mode, the counter records block errors.

During PRBS31 mode, a single bit error generates three error counts: one count after it is received and one for each tap of the checker shift register.

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1.6.4.3 Square-Wave Test Pattern Generator

Square-wave pattern generation is supported and is defined as the transmission of a repeating pattern of n ones followed by n zeros. The value of n can range from 4 to 11. This value is controlled using the MDIO register (3x8004.3[0]). For example, MDIO register (3x8004[3:0] = "1001" generates a repeating pattern of nine ones followed by nine zeros at TXDOUT±.

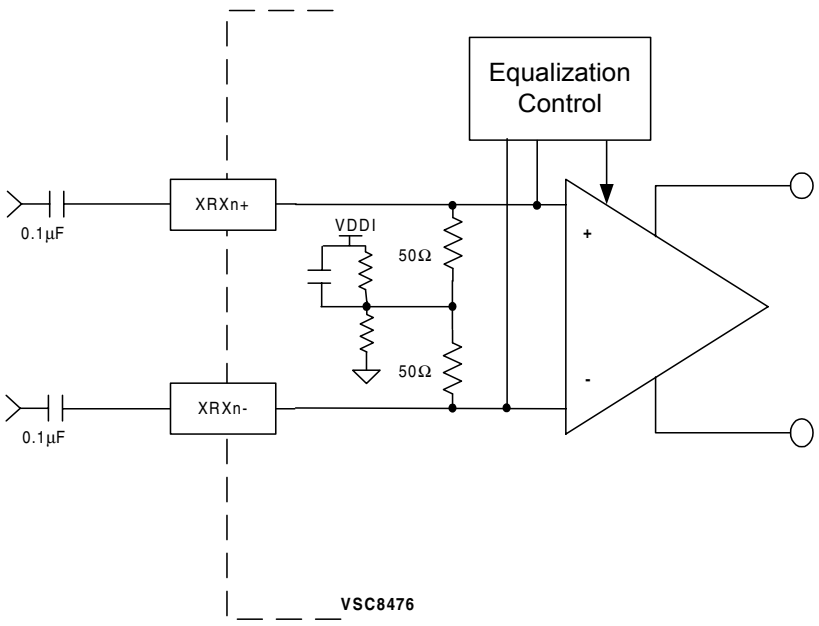
1.7 XGMII Extender Sublayer (PHY XS)

The PHY XS block interfaces from the four-lane 10-Gbps attachment unit interface (XAUI) to the PCS. Each AC coupled lane has 8b/10b encoded data running at 3.1875 Gbps.

1.7.1 XAUI Receiver

The XAUI interface features on-chip terminations of 100 Ω for all XAUI inputs, as shown in Figure 13:

Figure 13. XAUI Input - Simplified Schematic



1.7.2 XAUI Loss of Signal (LOS)

Each XRXn channel's input buffer has a loss of signal (LOS) detect that can be accessed through the MDIOVS IO 2 register. Each loss of signal level status is set low when the differential signal peak-to-peak swing exceeds a high-threshold level selected for each input, using the MDIO register interface. A high indicates that the signal amplitude is below the low-threshold level, which is also programmable using the MDIO management interface. The LOS detect status bits are considered undefined when the signal swing is between the high threshold and low threshold.

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The upper and lower threshold levels are shown in Table 4. For more information, see "Vendor-Specific XAUI Output Pre-Emphasis Control and LOS," page 147.

Table 4. XAUI Signal Detection Levels

MDIO Reg 4x8011 (3:2)	Lower Threshold	Upper Threshold	Unit	Notes
00	X	X	mV	Disabled, output set low
01	30	140	mV	Differential, p-p[1]
10	120	200	mV	Differential, p-p
11	190	300	mV	Differential, p-p

1. Peak-to-peak differential swing with each polarity driven with half the stated number.

1.7.3 XAUI Receiver Equalization

Incoming data on the XRXn inputs typically contains a substantial amount of intersymbol interference (ISI) or deterministic jitter, which reduces the ability of the receiver to recover data without errors. A programmable equalizer is included in each of the receiver's input buffers to compensate for this. This circuit is designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies being attenuated less than high frequencies as a result of the skin effect and dielectric losses. The equalizer boosts high-frequency edge response in 12 programmable levels of peaking ratio and decay time independently for each channel. The 12 programmable levels are intended to meet the equalization needs of commonly used trace lengths. Equalization level is selected or disabled on each channel independently by setting the appropriate internal register bits accessed through the MDIO management interface.

For more information about the optimal settings for most applications, see "Vendor-Specific XAUI Input Equalization Control," page 146.

1.7.4 XAUI Clock and Data Recovery

At the XAUI receiver, each channel contains an independent clock recovery unit (CRU) that accepts the selected serial input source, extracts the high-speed clock, and retimes the data. Each CRU automatically locks on data and if the data is not present, it automatically locks to the reference clock.

The clock recovery unit must perform bit synchronization, which occurs when the CRU locks onto and properly samples the incoming serial data, as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data from the decoder is invalid, resulting in numerous 8b/10b decoding errors or disparity errors. When the link is disturbed (that is, the cable is disconnected or the serial data source is switched), then the CRU requires 300 data edges to lock onto the data.

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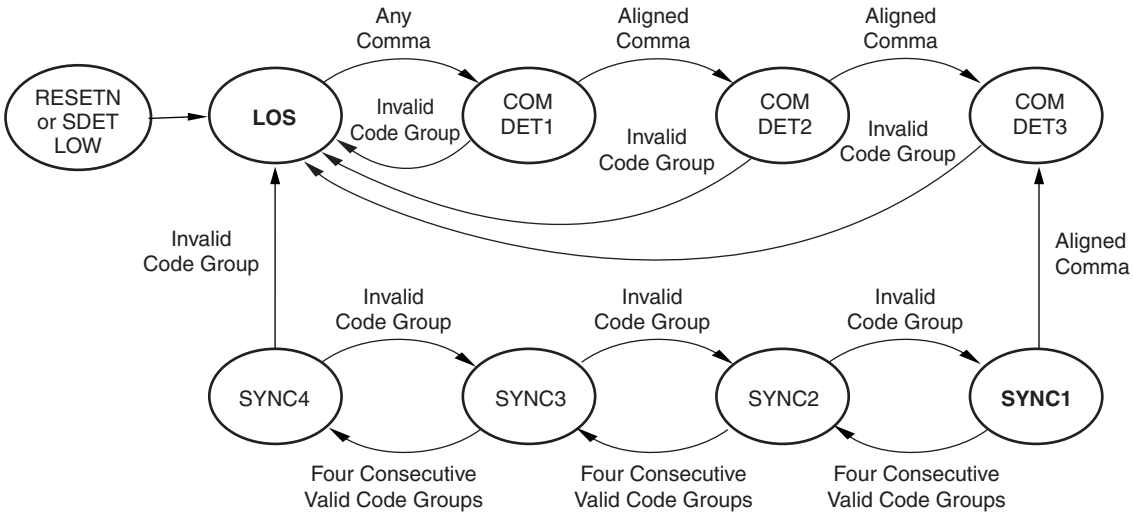
1.7.5 XAUI Code Group Synchronization

The retimed serial data stream is converted into 10-bit code groups by the deserializer. A special 7-bit comma pattern (0011111xxx or 1100000xxx where x is don't care) is recognized by the receiver and allows it to identify the 10-bit code group boundary.

Character, or code group, alignment occurs when the deserializer synchronizes the 10-bit code group boundary to a comma pattern in the incoming serial data stream. If the receiver identifies a comma pattern in the incoming data stream that is misaligned to the current framing boundary and the receiver is in LOS state, the receiver re-synchronizes the recovered data to align the data to the new comma pattern. Re-synchronization ensures that the comma character is output on the internal 10-bit bus so that bits 0 through 9 equal 0011111xxx or 1100000xxx. If the comma pattern is aligned with the current framing boundary, then the re-synchronization does not change the current alignment.

The detection of a series of consecutive 10-bit code group violations is the mechanism by which loss of synchronization (LOS) is declared by the XAUI receiver. The LOS condition is cleared by the detection of a series of comma characters that are properly aligned on code group boundaries. For additional information, see IEEE 802.3ae-2002 Clause 48, Figure 48-7 and the following Figure 14.

Figure 14. Loss of Synchronization (LOS) State Machine



Note that comma detection is enabled only when in the loss of synchronization (LOS) state rather than at all times. This is desirable to prevent incorrect character realignment due to the appearance of false commas, resulting from single-bit errors.

1.7.6 XAUI Lane Deskew

XAUI bit lane skew occurs due to skew between channels of a XAUI transmitter and skew accumulated across the transmission medium. The VSC8476 can deskew up to 63-bit periods of such inter-channel skew by using elastic buffers after each of the receiver inputs. For the XAUI interface to perform deskew or channel alignment, the receiver must receive a specific code group defined in IEEE 802.3ae standard Clause 48 as the alignment code group, ||A||.

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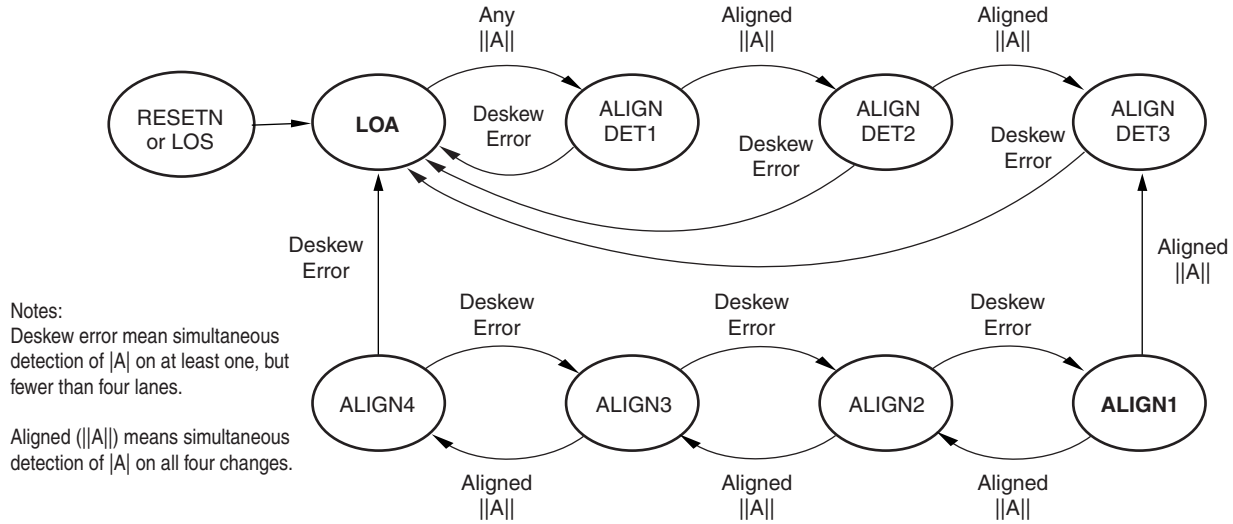
For inter-channel alignment to occur, the ||A|| ordered set consisting of four ||A|| code groups must appear, one ||A|| on each of the four XAUI inputs. This provides a unique synchronization point across the four serial data streams, which are used to align the received channels. Alignment status is governed by the reception of ||A|| code groups across the inputs, as shown in the loss of alignment (LOA) state machine in Figure 15.

Figure 15. Loss of Alignment (LOA) State Machine



Successive synchronization points must be separated by at least 170-bit periods in order for up to 63-bit periods of interchannel skew to be corrected unambiguously. An IEEE-compliant source of XAUI data provides a minimum spacing between sync points of 17 code groups, or 170-bit periods (at least 16 other IDLE code groups must occur between consecutive occurrences of ||A||). The alignment mechanism is always enabled when code group synchronization is attained on all four channels.

1.7.7 10b/8b Decoder

The 10-bit character from the deserializer is decoded in the 10b/8b decoder, which outputs the eight-bit data bytes plus control to the physical coding sublayer (PCS) section of the chip.

If the 10-bit code group does not match any valid value, a code-group error is generated that increments the code-group error counter. Similarly, if the running disparity of the code group does not match the expected value, a disparity error is generated.

1.7.8 8b/10b Encoder and Serializer

Each channel contains an 8b/10b encoder that translates 8-bit input data fed internally from the PCS block into a 10-bit code word. This data is then fed into a multiplexer that serializes the parallel data, using the synthesized transmit clock. The most significant bit of the 10-bit data is transmitted first. Each channel has a serial output port, XTXn, which consists of a differential XAUI output buffer operating at 3.1875 Gbps.

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1.7.9 XAUI Transmitter

On the transmit side, each polarity of the CML-type output driver is back-terminated with 50-Ω resistance to the supply, providing a 100-Ω differential output impedance.

1.7.9.1 XAUI Transmitter Pre-Emphasis

High-speed digital waveforms are subject to skin effect phenomena, such as velocity dispersion and frequency-dependent attenuation of their Fourier components. These effects cause the signal to become increasingly distorted with increasing propagation distance along a transmission medium. The situation is exacerbated with increasing frequency. Recognizing this, the device provides the capability of signal pre-distortion, or pre-emphasis, in its transmitter section.

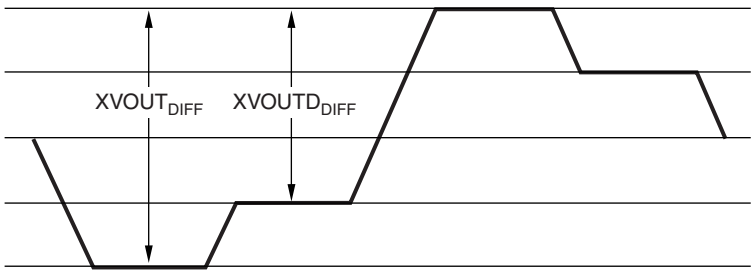
When used, transmit pre-emphasis causes the XAUI transmitter outputs to be distorted in a manner that is the inverse of skin effect distortion, as shown in Figure 16. When signal pre-emphasis is chosen, the effects of pre-distortion and skin effect distortion offset each other, and a high-quality waveform is seen at the receiving device. Several levels of signal pre-emphasis are available and are selected on an individual-channel-basis through the MDIO management interface.

For more information about the operation of the VS XAUI Output Pre-Emphasis Control and LOS register, see "Vendor-Specific XAUI Output Pre-Emphasis Control and LOS," page 147.

Note that the settings vary with trace length and loss characteristics of the transmission material. It is recommended to experiment with these settings to obtain optimum performance.

$$\text{Emphasis ratio} = \frac{\text{XVOUT}}{\text{XVOUTD}} \quad \textbf{(EQ 1)}$$

Figure 16. XAUI Output Differential Voltage with Emphasis



1.7.9.2 XAUI Transmitter Programable-Output Swing

Control of this function is provided on a global basis with the HI_SWING bit in the MDIO in the VS XAUI Output Pre-Emphasis Control and LOS register. When the HISWNG bit is set low, the corresponding channel operates in the normal mode. When HISWNG is set high, full output swing is increased by approximately 15%.

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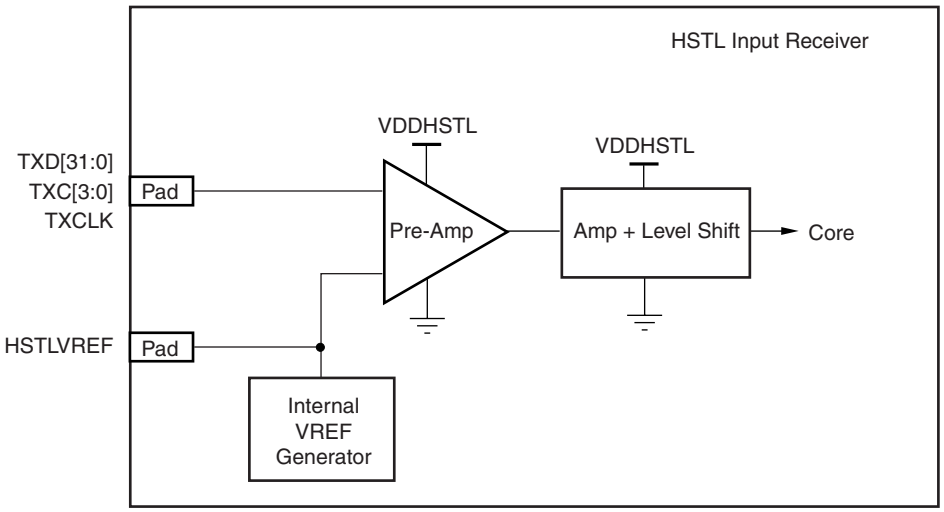
1.7.10 XGMII Tx Input Interface

The VSC8476 expects to receive a continuous stream of data and control characters from the MAC or 10-GFC equivalent at the XGMII input. The XGMII interface is organized into four groups of eight data bits (octet) and one control bit. Octets originating from a MAC device are received on TXD[31:0] in octet-striped fashion with the first octet appearing on TXD[7:0] (lane 0), the second on TXD[15:8] (lane 1), and so forth. Within the octets, bit ordering is set so that bit 0 of a serial bit stream appears on TXD0, bit 1 appears on TXD1, and so forth. Within each octet, the lowest-numbered bit (bit 0 in the first octet, bit 8 in the second octet, etc.) is considered the LSB and is transmitted first.

XGMII data is latched into the VSC8476 on both the rising and falling edges of TXCLK, which serves as a timing reference for the transfer of TXD[31:0] and TXC[3:0] across the XGMII interface. TXCLK is 159.37 (156.25) MHz clock, ± 100 ppm. The XGMII interface follows the high-speed transceiver logic (HSTL) electrical specifications for a 1.5-V supply voltage, as specified in EIA/JESD8-6 for Class I output buffers. The HSTL inputs are designed to function with or without termination. For the specifications and timing diagrams, see "Electrical Specifications," page 201. Simplified diagrams of the XGMII input and output structures are illustrated in Figure 17.

Figure 17. XGMII Input - Simplified Schematic



1.7.11 XGMII Rx Output Interface

The VSC8476 provides a continuous stream of data and control characters to the MAC or 10-GFC equivalent on its XGMII outputs. The XGMII interface is organized into four groups of eight data bits (octet) and one control bit. Octets originating from the PCS block are transmitted on RXD[31:0] in octet striped fashion, with the first octet appearing on RXD[7:0] (lane 0), the second on RXD[15:8] (lane 1), and so forth. Within the octets, bit ordering is such that bit 0 of a serial bit stream appears on RXD0, bit 1 appears on RXD1, and so forth. Within each octet, the lowest-numbered bit (bit 0 in the first octet, bit 8 in the second octet, and so forth.) is considered the LSB and is received first.

XGMII data is latched to the output of the VSC8476 on both rising and falling edges of RXCLK, which serves as a timing reference for the transfer of RXD[31:0] and RXC[3:0] across the XGMII interface.

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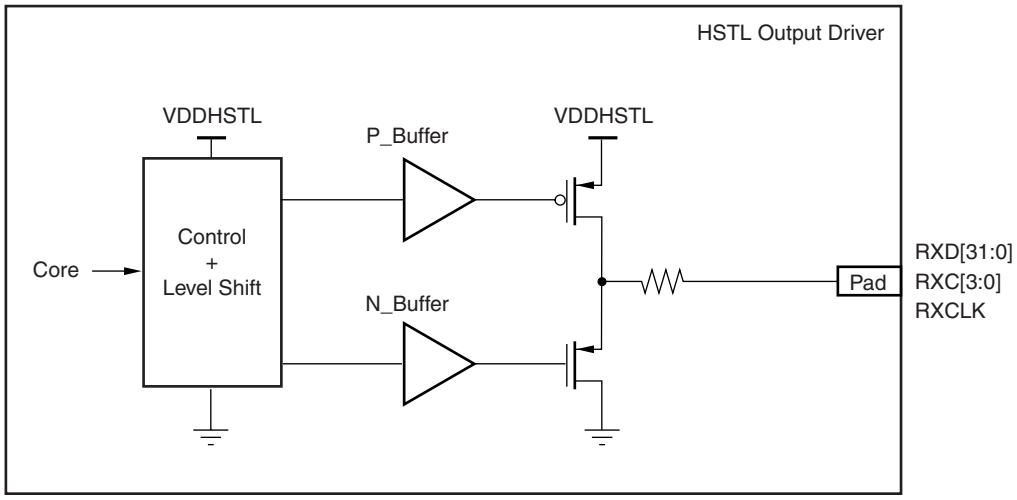
The RXCLK output is 159.37 MHz (156.25 MHz) ±100 ppm. The XGMII interface follows the high-speed transceiver logic (HSTL) electrical specifications for a 1.5-V supply voltage, as specified in the EIA/JESD8-6 for Class I output buffers. The HSTL outputs are designed to function with or without termination and swing from the ground rail to the power supply rail without termination. For more information about specifications and timing diagrams, see "XGMII Input Specifications," page 206. For more information about the simplified diagrams of the XGMII output structures, see Figure 18.

Figure 18. XGMII Output Structure and Termination



1.8 Loopback Operation

The VSC8476 LAN PHY has three major external data ports (XAUI, XFI, XGMII). There are several methods available to the user for routing traffic between the various ports. The purpose of this section is to outline the operation of several modes loosely termed loopbacks. These modes can be extremely useful for both test and debug purposes.

Seven loopback paths are provided, as illustrated in Figure 19. Two split loopback paths (that is, two loopback paths simultaneously switched on) are enabled with control pins SPLITLOOPN and LP_XAUI. All other data path routing and loopback controls must be enabled through the MDIO interface.

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Figure 19. VSC8476 Data Path Configuation

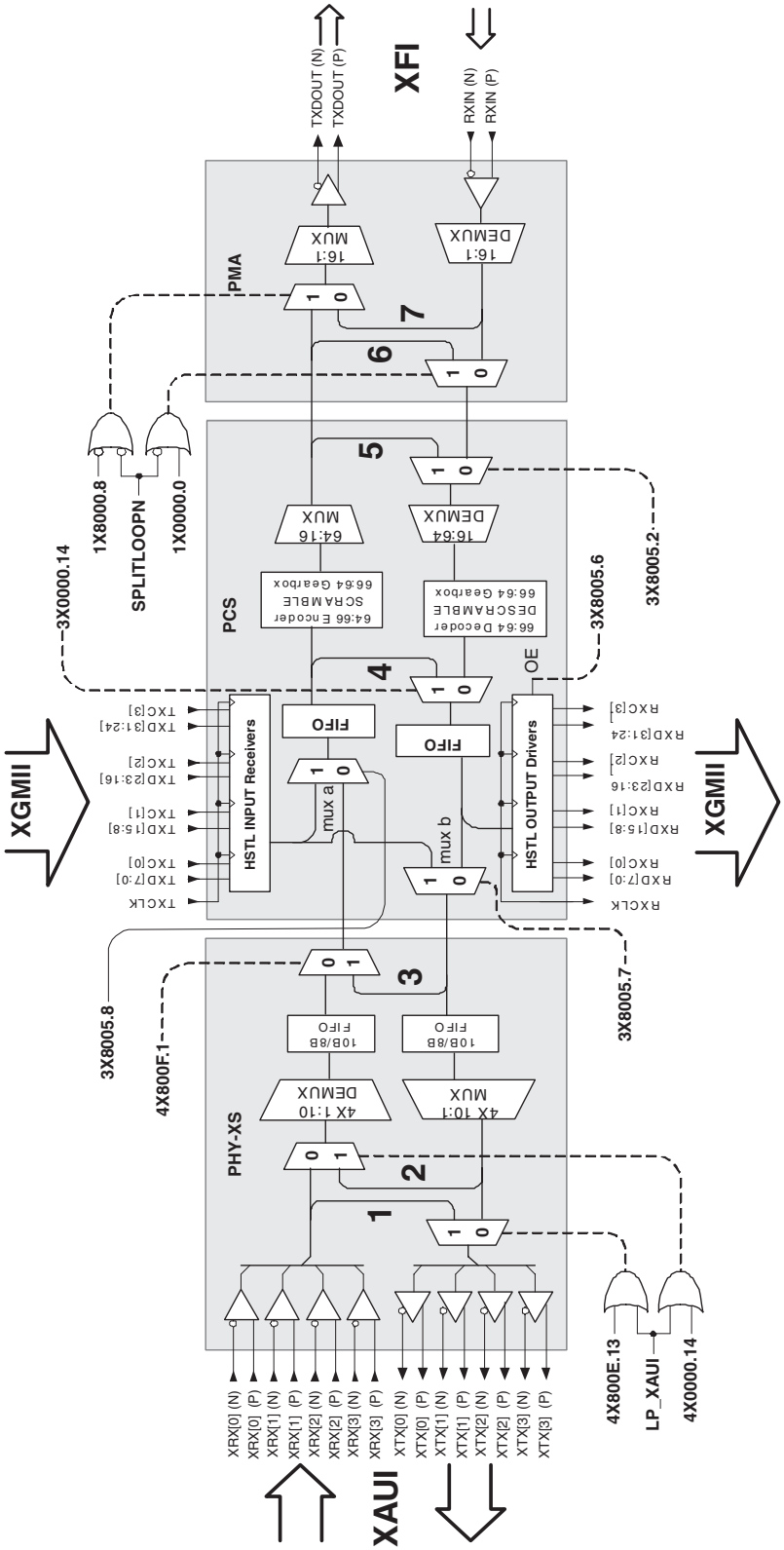

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Table 5 summarizes the register addresses and specific bits that control the loopback paths on the device.

PCS data path routing multiplexers a and b have different default controls after a power up reset, which depend on the state of the IOMODESEL pin. In general, if IOMODESEL = 1 at power on or reset, the VSC8476 is configured for a XAUI to XFI operation (mux a control = 0, mux b control = 0) and the XGMII outputs are held static. If IOMODESEL = 0 at power on or reset, the VSC8476 is configured for an XGMII to XFI operation (mux a control = 1, mux b control =1), and XGMII output drivers are enabled (OE =1). Mux a, mux b, and OE controls can also be configured after a reset, using the MDIO interface.

Table 5. Loopback Path Control Summary

Data Path	Control Hex	Clock Domain	Comments
1	4x800E[13]	No re-time	Phase delay only, no re-timing.
2	4x0000[14]	10 G recovered	
1 & 2	LP_XAUI (pin D15)	1: No XAUI re-time 2: 10 G recovered	On-chip pull-down disables loopback.
3	4x800F[1]	10 G recovered in Refclk timed out	Also enables XGMII Tx to Rx loop.
4	3x0000[14]	XAUI recovered in Refclk timed out	Also enables XGMII ingress to egress loop with XAUI mirror.
5	3x8005[2]	XAUI recovered in Refclk timed out	Also enables XGMII Tx to Rx loop through PCS
6	1x0000[0]	XAUI recovered in Refclk timed out	XAUI input also routes to XFI serial output.
7	1x8000[8]	10 G recovered	XSBI loop-line code independent.
6&7	SPLITLOOPN (pin E8)	6: XAUI recovered in Refclk timed out 7: 10 G recovered	On-chip pull-up disables loopback. 0: Enable 1: Disable

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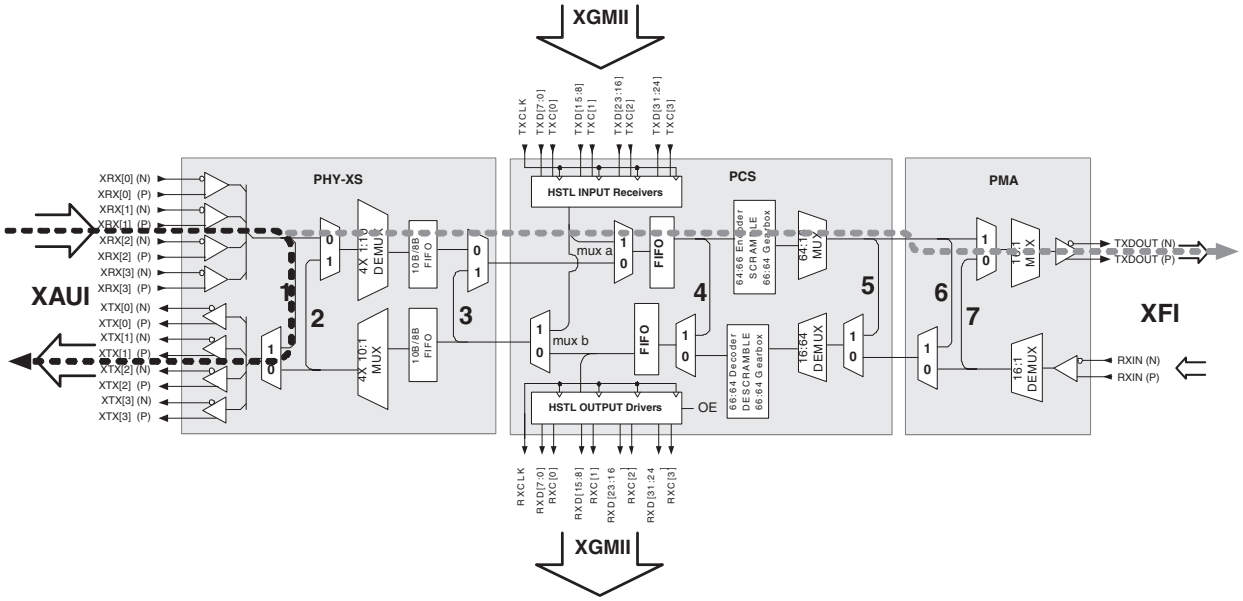
1.8.1 Loopback 1

Loopback data path 1 routes the incoming XAUI data directly from the XAUI input receivers to the XAUI output transmitters without retiming. The data does not pass through the XAUI CRU.

PHY-XS register 4x800E[13] must be set to 1 to enable this path. The default value of bit 13 is 0, loopback disabled. Figure 20 shows the data path when this loopback is enabled.

XAUI ingress data is also sent using the PCS and PMA to the XFI egress port, and does not require additional MDIO register commands if IOMODESEL = 1 at reset followed by loopback 1 enable, as described.

Figure 20. Loopback 1 Enabled



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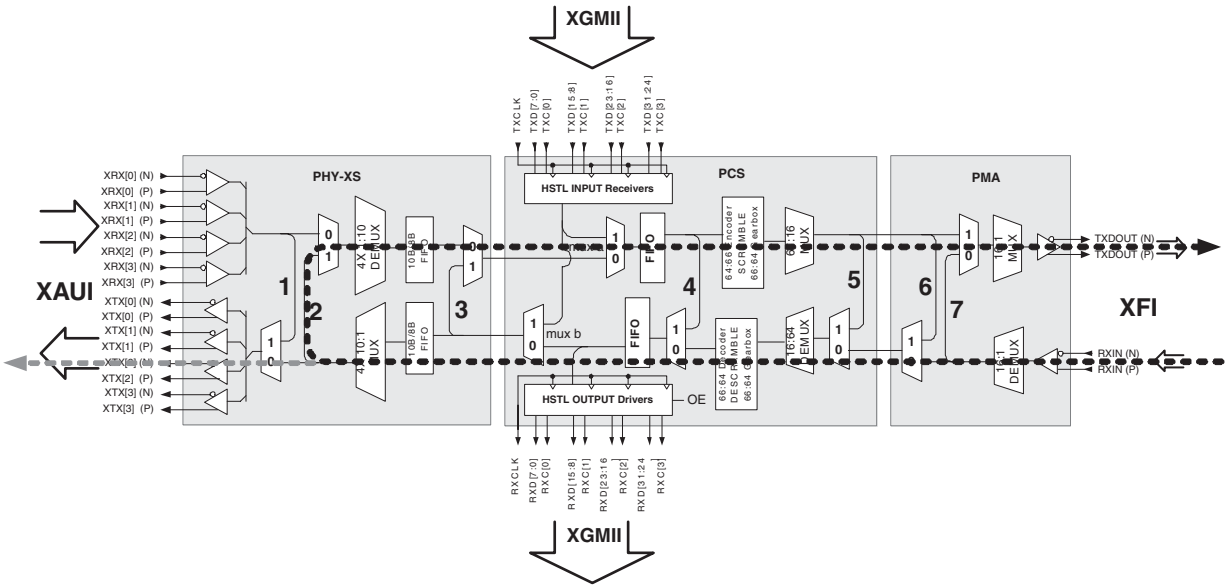
1.8.2 Loopback 2

Loopback data path 2 routes the incoming 10 G XFI data through the PCS to be looped around the PHY-XS and back out to the 10 G XFI output, as shown in Figure 21. Data is retimed with the 10-G recovered clock. Register 4x0000[14] must be set to 1 to enable the path. The default value of bit 14 is 0, loopback disabled. XFI ingress data is mirrored to the XAUI egress port simultaneously without further MDIO instructions.

Figure 21. Loopback 2 Enabled



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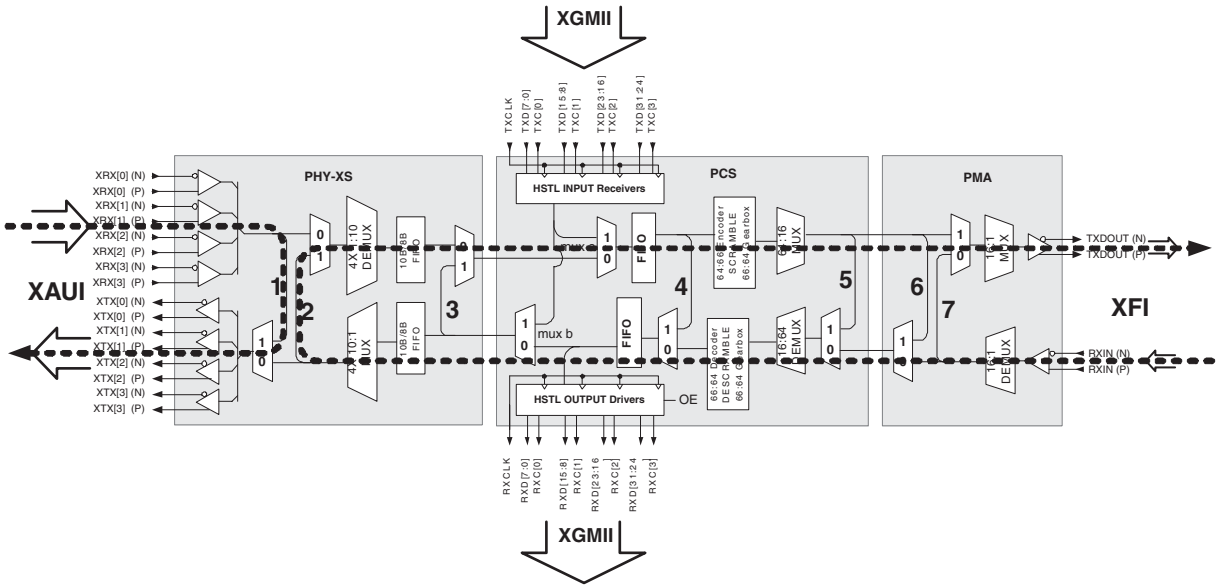
1.8.3 Loopback 1 and 2 LP_XAUI

Split loopback paths 1 and 2 are simultaneously enabled by setting LP_XAUI to 1 (pin D15), as shown in Figure 22. Loopback 1 is not retimed; loopback 2 is retimed by the 10-G recovered clock. If left unconnected, the LP_XAUI input is pulled down on-chip, disabling these loopback paths.

Figure 22. Split Loopback 1 and 2 Enabled (LP_XAUI = 1)



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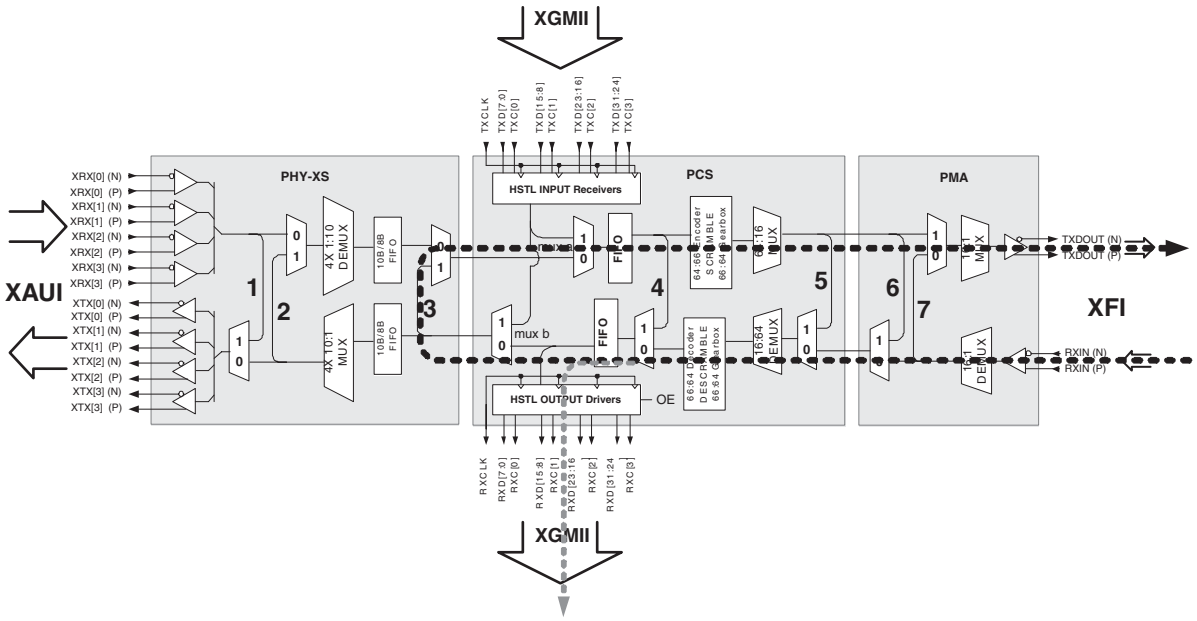
1.8.4 Loopback 3

Loopback data path 3 can route ingress XFI data through the PCS and simultaneously can route it to the egress XGMII port and back to the XFI egress port, depending on the IOMODESEL pin state at reset, as shown in Figure 23. XFI ingress data is routed to the XGMII egress port when IOMODESEL = 1 (pin M16) at reset and register 4x800F[1] is set to 1. The default value of bit 1 is 0, loopback 3 disabled. XFI ingress data is routed to XGMII egress port when IOMODESEL = 0 at reset.

XFI ingress data can be mirrored to the XGMII and XFI egress ports simultaneously. To configure this port mirror operation, set IOMODESEL to 1 at reset, set register 4x800F[1] to 1, and set register 3x8005[6] to 1 (HSTL output enable).

Figure 23. Loopback 3 Enabled



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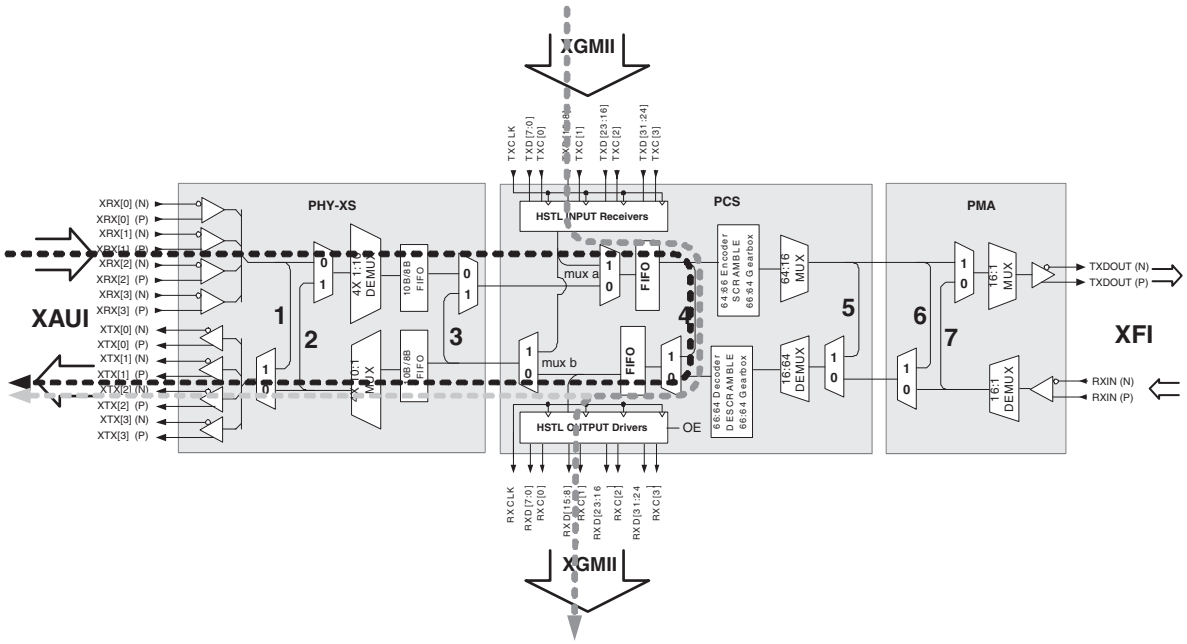
1.8.5 Loopback 4

Loopback data path 4 can route ingress XAUI or XGMII data simultaneously to the egress XAUI and XGMII ports, depending on the IOMODESEL pin state at reset, as shown in Figure 24. XAUI ingress data is routed to the XAUI egress port when IOMODESEL = 1 (pin M16) at reset and register 3x0000[14] is set to 1. The default value of bit 14 is 0, loopback 4 disabled. XGMII ingress data is routed to XGMII egress port when IOMODESEL = 0 at reset and 3x0000[14] is set to 1.

XGMII ingress data can be mirrored to the XGMII and XAUI egress ports simultaneously. To configure this port mirror operation, set IOMODESEL to 1 at reset, set register 3x8005[8] to 1 (mux a control), set register 3x0000[14] to 1, and set register 3x8005[6] to 1 (HSTL output enable).

Figure 24. Loopback 4 Enabled



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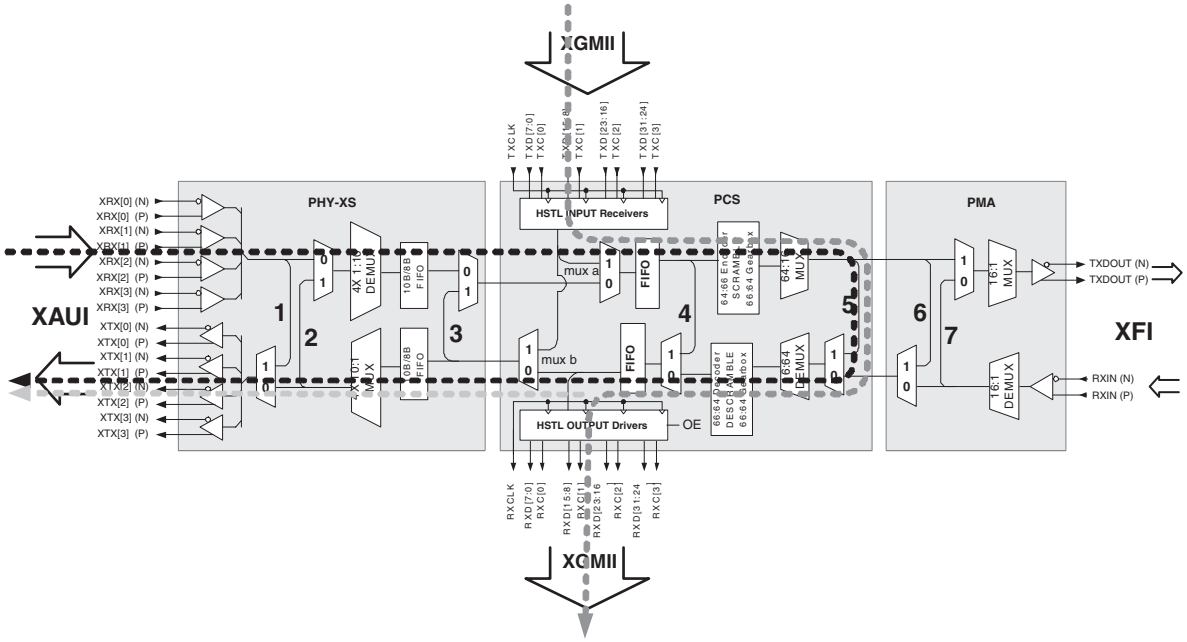
1.8.6 Loopback 5

Loopback data path 5 can route ingress XAUI or XGMII data through the PCS, and can simultaneously route it to the egress XAUI and XGMII ports, depending on the IOMODESEL pin state at reset, as shown in Figure 25. XAUI ingress data is routed through the PCS and then to the XAUI egress port when IOMODESEL = 1 (pin M16) at reset and 3x8005[2] is set to 1. The default value of bit 2 is 0, loopback 5 disabled. XGMII ingress data is routed through the PCS and then to XGMII egress port when IOMODESEL = 0 at reset and 3x8005[2] is set to 1.

XGMII ingress data can be routed through the PCS and then mirrored to the XGMII and XAUI egress ports simultaneously. To configure this port mirror operation, set IOMODESEL to 1 at reset, set register 3x8005[8] to 1 (mux a control), set register 3x 8005[2] to 1, and set register 3x8005[6] to 1 (HSTL output enable).

Figure 25. Loopback 5 Enabled



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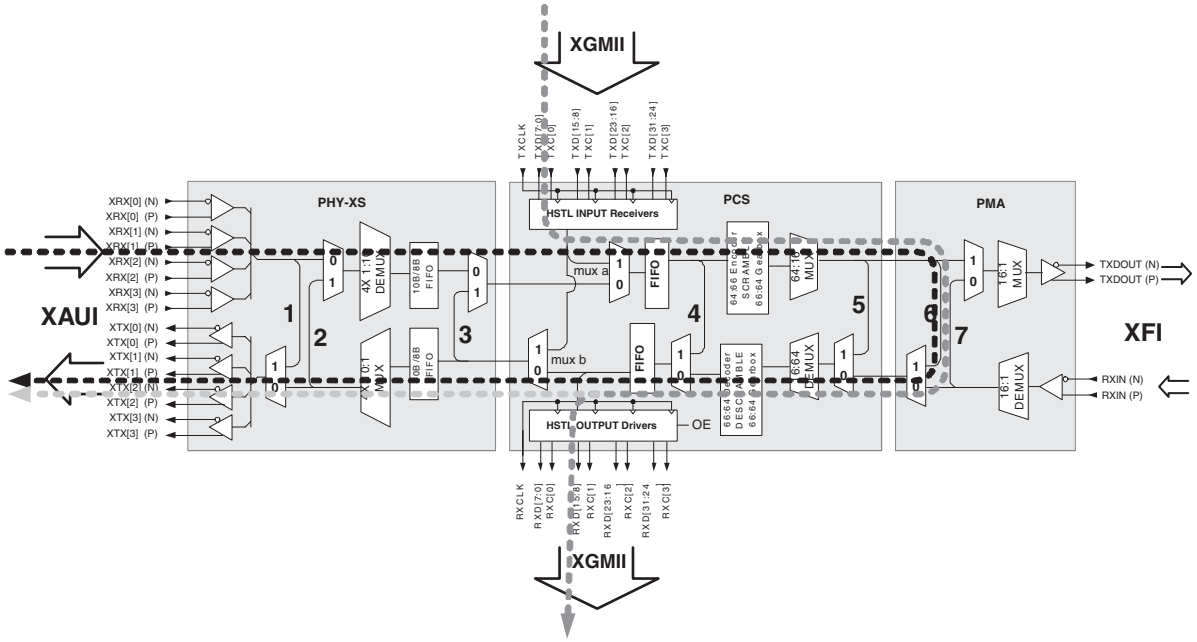
1.8.7 Loopback 6

Loopback data path 6 can route ingress XAUI or XGMII data through the PCS and PMA, and can simultaneously route it to the egress XAUI and XGMII ports, depending on the IOMODESEL pin state at reset, as shown in Figure 26. XAUI ingress data is routed through the PCS and the PMA and then to the XAUI egress port when IOMODESEL = 1 (pin M16) at reset and 1x0000[0] is set to 1. The default value of bit 0 is 0, loopback 6 disabled. XGMII ingress data is routed through the PCS and PMA, and then to XGMII egress port when IOMODESEL = 0 at reset and 1x0000[0] is set to 1.

XGMII ingress data can be routed through the PCS and the PMA and then mirrored to the XGMII and XAUI egress ports simultaneously. To configure this port mirror operation, set IOMODESEL to 1 at reset, set register 3x8005[8] to 1 (mux a control), set register 1x0000[0] to 1, and set register 3x8005[6] to 1 (HSTL output enable).

Figure 26. Loopback 6 Enabled



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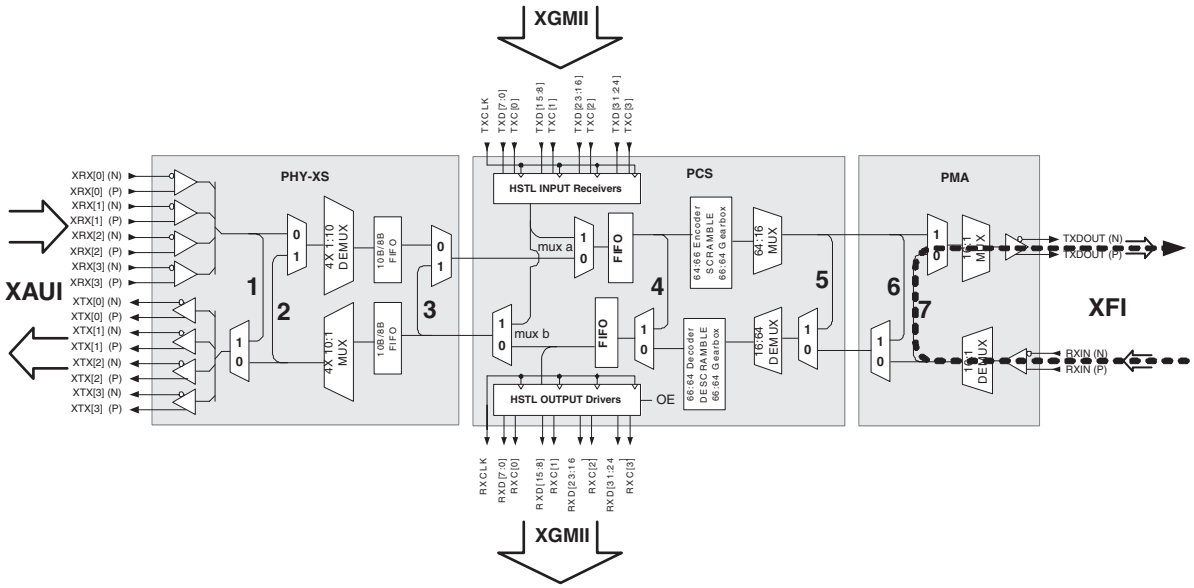
1.8.8 Loopback 7

Loopback data path 7 routes the incoming 10G XFI data through the XSBI 16 bit interface and back to the 10-G XFI output, as shown in Figure 27. Loopback 7 is protocol agnostic. Data is retimed with the 10-G recovered clock. Register 1x8000[8] is set to 0 to enable this loopback path. The default value of bit 8 is 1, loopback 7 disabled.

Figure 27. Loopback 7 Enabled



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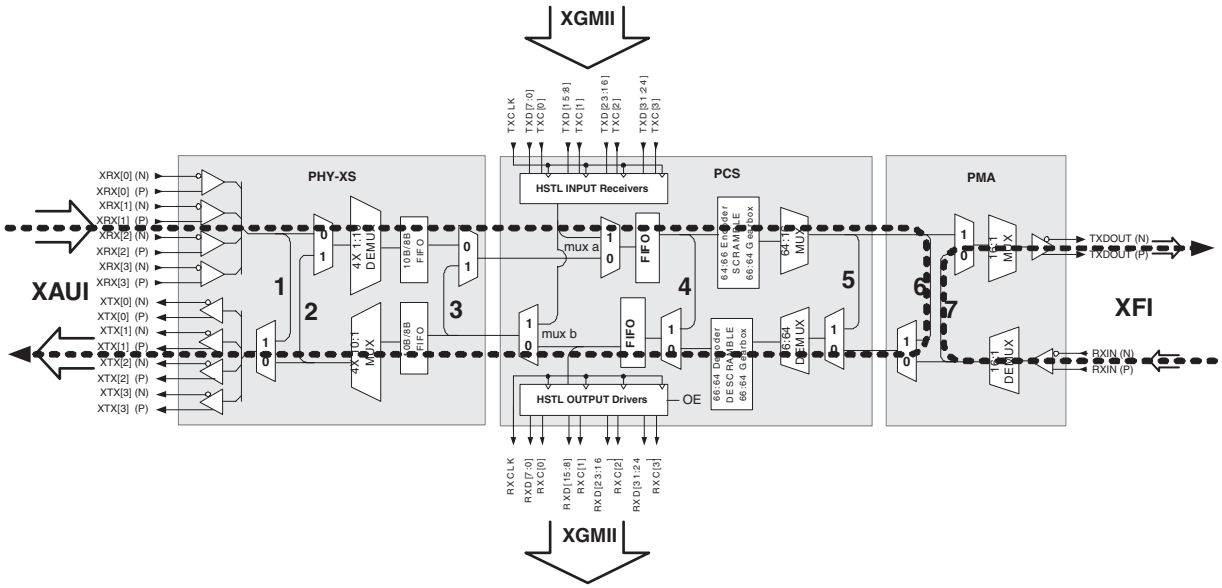
1.8.9 Loopback 6 and 7 SPLITLOOPN

Split loopback paths 6 and 7 are simultaneously enabled by setting SPLITLOOPN to 0 (pin E8), as shown in Figure 28. Loopback 6 recovers the clock from the XAUI ingress data, passes through a rate compensation FIFO, and is timed out by the refclk. Loopback 7 is retimed by the 10-G recovered clock. If left unconnected, the SPLITLOOPN input is pulled up on-chip, disabling these loopback paths.

Figure 28. Loopback 6 and 7 Enabled (SPLITLOOPN = 0)



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1.9 JTAG Access Port

A JTAG access port is provided on the VSC8476 transceiver to facilitate device-level and board-level testing. Most pins can be accessed or controlled through this port and all TTL outputs can be tri-stated. This port is compliant with IEEE Standard 1149.1-1990 (subsequently referred to as the JTAG specification) with the five TTL signals listed in Table 6.

Table 6. JTAG TTL Signals

Signal	Description
TCK	Test clock input
TMS	Test mode select input
TDI	Test data input
TDO	Test data output
TRSTB	Test reset input

To ensure reliability, a TRSTB input (instead of a power-on reset circuit) is provided to initialize the JTAG logic. This input, TRST* in the JTAG specification, is asserted when in the low (logic 0) state. The TRSTB, TDI, and TMS input pins have an on-chip, high-impedance, pull-up resistor connected to the VDDTTL supply so that an undriven input behaves as though a logic 1 were applied.

1.10 MDIO Serial Interface

The VSC8476 contains a management data input/output (MDIO) interface, as specified in IEEE 802.3ae standard Clause 22 and amended by Clause 45. This section provides an overview of the operation of the MDIO interface. For more information, see IEEE 802.3ae-2002 Clause 22 and Clause 45.

1.10.1 MDIO Interface Operation

The VSC8476 implements a management data input/output (MDIO) interface in accordance with the requirements of IEEE 802.3ae standard Clause 45. The several operational sublayers within the device are individually known as MDIO-manageable devices (MMD). Using the PRTAD[4:0] pins, the station management entity (STA) can access up to 32 PHYs. Using the 5-bit DEVAD field within the management frame format, up to 32 MMDs can be addressed in each PHY. The MDIO-manageable device addresses are shown in Table 7.

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Table 7. MDIO-Manageable Device Addresses

Device Address	MMD Name
0	Reserved
1	PMA
2	WIS (not implemented)
3	PCS
4	PHY XS
5	DTE XS (not implemented)
6:29	Reserved
30	Vendor-specific name for two-wire serial CPU interface
31	Vendor specific name

When referring to registers in this text, the following format is used [device address] × [hex value], where device address is shown in the previous table. For example, 1x00F is the decimal value address 15 in the PMA.

The management frame format supports indirect addressing to provide more accessible register space within each MMD (see Figure 29, page 58). The management frame field structure is shown in Table 8.

Table 8. Management Frame Format for Indirect Register Access

Management Frame Fields								
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**Address/Data**	**Idle**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read increment	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

A 16-bit address register stores the address of the register to be accessed by data transaction frames. The address register is overwritten by address frames. Upon device-reset, the contents of the address register is set to zero. At power up, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames access the register whose address is stored in the address register. Write and read frames do not modify the contents of the address register.

After receiving a post-read-increment-address frame and completing the read operation, the address register is incremented by one. When the register contains 65,535, the address register is not incremented.

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The idle condition is a high-impedance state. All tri-state drivers are disabled, and the pull-up resistor pulls the MDIO line to a one.

At the beginning of each transaction, the station management entity (STA) sends a preamble (PRE) sequence of 32 continuous one-bits on MDIO during 32 corresponding cycles on the management data clock (MDC), providing a pattern that the MMD uses to establish synchronization. All MMDs observe the 32 continuous one-bits before responding to any transaction.

Figure 29. MDIO Frame Format

The MDIO frame format consists of the eight segments, shown above. Definitions for the segments are shown in the following table.

PRE 32	32 bits of 1 supplied by the STA.
ST	2 bits of 0, which indicates the start of frame.
OP	2 bits of Op-Code as described in IEEE 802.3ae, Chapter 45.
PA 5	5 bits of port address, which provides up to 32 ports to a physical bus.
DA 5	5 bits of destination MMD address, which provides up to 32 MMDs to a port.
TA	2 bits of turnaround time to change the bus ownership from the STA to MMD if required.
D 16	16 bits for address/data driven on the bus by the current master of the bus, the STA for write operation, and the MMD for a read or read-address-increment operation.
Z	Idle time, bus three-stated.

The start of frame (ST) is indicated by the [00] pattern. Frames, containing the ST = [01] pattern that is defined in IEEE 802.3ae Clause 22, are ignored.

The operation code (OP) indicates the type of transaction being performed by the frame. A [00] pattern indicates that the frame payload contains the address of the register to access. A [01] pattern indicates that the frame payload contains data to be written to the register whose address is provided in the previous address frame. A [11] pattern indicates that the frame is a read operation. A [10] pattern indicates that the frame is a post-read-increment-address operation.

The port address (PRTAD) consists of five bits. The first bit to be transmitted and received is the MSB. The device address (DEVAD) also consists of five bits. The first bit transmitted and received is the MSB.

Turnaround (TA) is a two-bit time spacing between the DEVAD field and data field of a frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, the STA and MMD remain in a high-impedance state for the first-bit time of the turnaround. The MMD drives a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA drives a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround.

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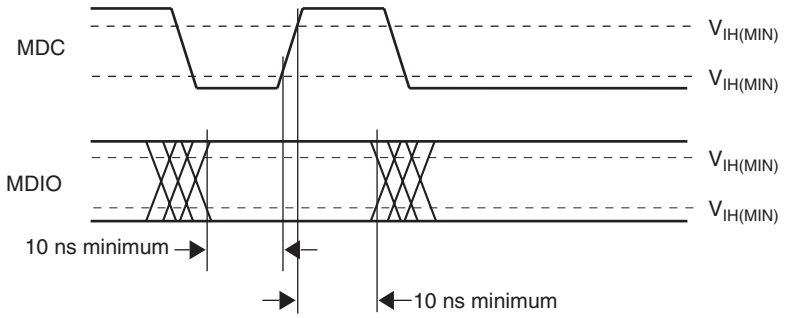
The address or data field consists of 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, and increment read cycles, the field contains the data for the register. The first bit transmitted and received is bit 15.

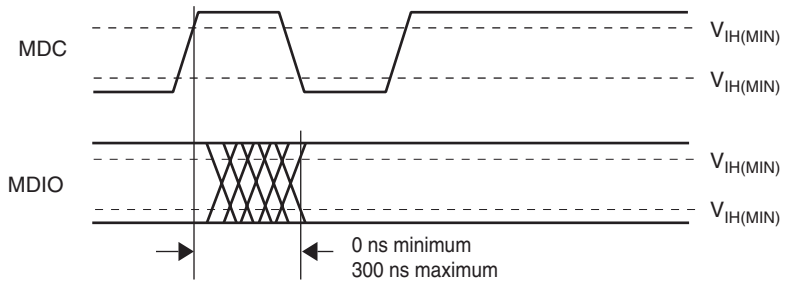
MDIO is a bidirectional signal that can be sourced by STA or the MMD. When STA sources the MDIO signal, a minimum of 10 ns of setup time and 10 ns of hold time with reference to the rising edge of MDC is provided, as shown in Figure 30.

Figure 30. Timing When MDIO Is Sourced by STA



When MDIO is sourced by the MMD, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock-to-output delay from the MMD, as measured at STA, is a minimum of 0 ns and a maximum of 300 ns, as shown in Figure 31.

Figure 31. Timing When MDIO Is Sourced by MMD



For more information about the MDIO register definitions, see "Registers," page 73.

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1.10.2 Two-Wire Serial Interface

The VSC8476 also contains a two-wire serial management interface that provides a communications bus to digital optical monitors. The two-wire serial bus interfaces with MDIO registers and is controlled by the MDIO interface. For a block diagram illustrating the MDIO to two-wire serial interface relationship, see Figure 32.

The industry-standard, two-wire serial interface bus is a master-only controller and supports three modes: Standard (100 kbps), Fast (400 kbps) and High-Speed (3.2 Mbps), including both 7-bit and 10-bit addressing.

Writing to the MDIO register (0x8000) initiates activity on the two-wire serial interface. There are two modes of operation: Automatic and Manual. In Automatic mode, up to 256 bytes are automatically copied from an external CMOS EEPROM, as defined for the ATMEL AT24C01A/02/04 family of components, to the internal two-wire serial interface registers. In Manual mode, you can communicate with other devices connected to the two-wire serial interface bus through the MDIO interface. In this mode, any instruction written to the STW Instruction register (0x8000) initiates execution of the instruction.

The two-wire serial interface controller module integrated into the VSC8476 is intended to facilitate serial communication within a XENPAK module or with an XFP-compliant device. The two-wire serial interface module is controlled by the VSC8476 MDIO interface through internal registers. The module consists of a register file and a two-wire serial interface bus controller. The two-wire serial interface bus controller is a master-only controller, which supports all three two-wire serial interface modes (Standard, Fast, and High-Speed modes).

The two-wire serial interface controller supports both 7-bit and 10-bit addressing. The VSC8476 two-wire serial interface interface complies with the *Phillips Semiconductor I^2C-bus Specification, Version 2.1*. For more information about the detailed descriptions of the two-wire serial interface operating modes and addressing, see the *Phillips Semiconductor I^2C-bus Specification, Version 2.1*. Figure 32 shows the four MDIO-manageable devices in the VSC8476 SerDes.

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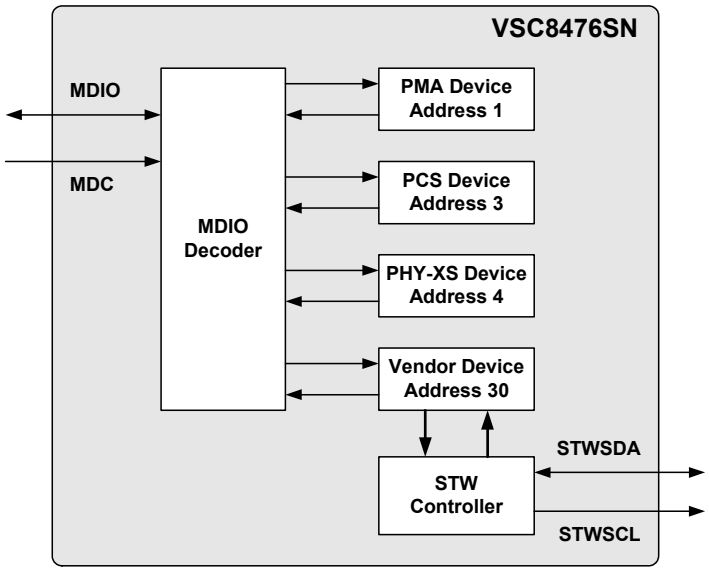
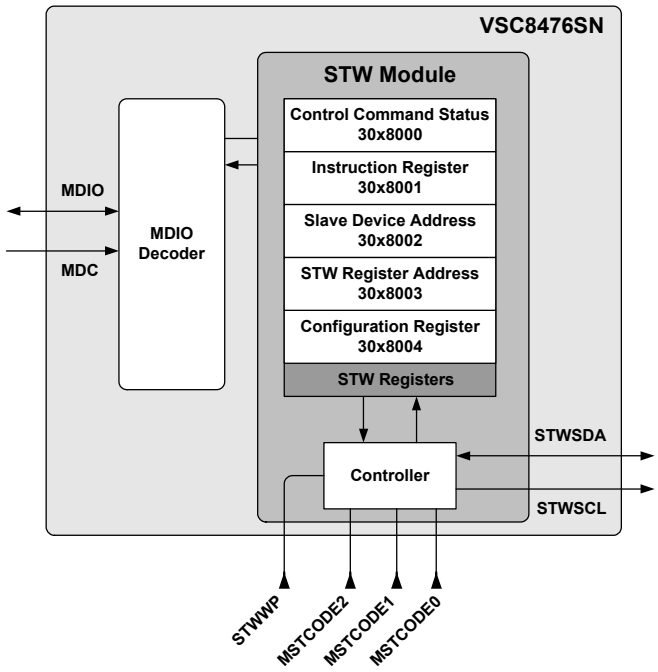
Figure 32. VSC8476 MDIO-Manageable Devices (MMDs) On-Chip



1.10.2.1 Two-Wire Serial Interface Controller Operating Modes

The VSC8476 two-wire serial interface controller has two working modes: Automatic and Manual. The structure of the two-wire serial interface module and its relationship to the VSC8476 MDIO module is shown in Figure 33.

Figure 33. VSC8476SN Serial Management Interface



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MSTCODE[2:0] are the last three bits of the eight-bit master code (00001XXX) for two-wire serial interface data transfer in High-Speed mode only. The two-wire serial interfaceWP input, when set to 1, inhibits two-wire serial interface write activity. Both the MDIO decoder and two-wire serial interface controller have access to the two-wire serial interface registers. A write transaction to the Vendor-Specific NVR Control Command Status register through the MDIO interface initiates a read/write action for the two-wire serial interface controller. The MDIO decoder loses access to the two-wire serial interface registers until the two-wire serial interface controller finishes reading or writing to the two-wire serial interface bus (STWSDA and STWSCL).

A write action writes the content of the register whose address is stored in STW Register Address register (30x8003) to the external two-wire serial interface device whose address is stored in the Slave Device Address register (30x8002). A read action, where data is read from an external device to internal registers, is the opposite of a write action. The two-wire serial interface controller has two operational modes (Automatic and Manual), which are discussed in the following section.

1.10.3 Two-Wire Serial Interface Module Register Descriptions

The two-wire serial interface module registers are described in this section.

1.10.3.1 Vendor-Specific NVR Control Command Status Register (30x8000)

The Vendor-Specific NVR Control Status register (30x8000) is the same as the NVR Control/Status register x8000 defined in *XENPAK MSA Revision 3.0* with one exception. In addition to the XENPAK-defined structure, the VSC8476 uses bit 8 of this register to set the Two-Wire Serial Interface Operational mode. The MDIO decoder activates the two-wire serial interface module by writing to this register. Writes to this register through MDIO during a two-wire serial interface action are ignored.

For more information about the Vendor-Specific NVR Control Status register (30x8000), see "Vendor-Specific NVR Control Command Status," page 149.

1.10.3.2 STW Instruction Register (30x8001)

The STW Instruction register (30x8001) is only active when Manual mode is selected. One instruction written to this register using MDIO causes the two-wire serial interface controller to read or write one data byte to or from the two-wire serial interface bus. Writes to this register through MDIO during execution of an instruction are ignored.

For more information about the STW Instruction register (30x8001), see "STW Instruction," page 151.

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1.10.3.3 Slave Device Address Register (30x8002)

The Slave Device Address register stores the two-wire serial interface slave device address that is read or written. The two-wire serial interface controller does not directly use the contents of this register to address the slave device; instead it uses its internal slave address register. Setting bit 9 of register 30x8001 to one synchronizes these two registers, which allows register 30x8002 to be updated while the two-wire serial interface controller is active. All XFP modules use the same seven-bit address, which is A0 (hexadecimal).

For more information about the Slave Device Address register (30x8002), see "Slave Device Address," page 152.

1.10.3.4 STW Register Address Register (30x8003)

The STW Register Address register is used to store the address of the two-wire serial interface register, which is used to store the data read from or written to the slave device. Similar to register 30x8002, this register is not directly used by the two-wire serial interface controller. Setting bit 8 of register 30x8001 to one synchronizes the two-wire serial interface controller internal register with register 30x8003.

For more information about the TW Register Address register (30x8003), see "STW Register Address," page 152.

1.10.3.5 Configuration Register (30x8004)

The Configuration register 30x8004 is used to configure the desired operating mode for the two-wire serial interface module. Bits 11:9 configure the two-wire serial interface master bus controller operating characteristics, bus signaling speed, and addressing mode. Bit 12 sets the two-wire serial interface controller to make block reads or writes in accordance with the XENPAK or XFP register maps. The XFP and XENPAK modes are different only when the Two-Wire Serial Interface Automatic mode is selected (using bit 8 of register 30x8000). In Manual mode, the XENPAK and XFP modes are same.

In Automatic mode, the XFP or XENPAK register contents are mapped into 256 eight-bit registers beginning at internal address 8007'h and ending with 8106'h.

For more information about the Configuration register (30x8004), see "Configuration," page 152.

1.10.4 Functional Description

The two-wire serial interface read or write action is initiated by writing to the Vendor-Specific NVR Control Command Status register (30x8000). After the write transaction finishes, the two-wire serial interface controller reads the register and sets the command status bits 3:2 to 10 (command in progress). In this condition, the MDIO decoder cannot read or write to the two-wire serial interface registers. After the two-wire serial interface controller completes the data read or write, it sets the command status bits to 01 if the operation is completed successfully or to 11 if the operation failed. The MDIO decoder then regains access to the two-wire serial interface module registers. For more information, see Figure 34.

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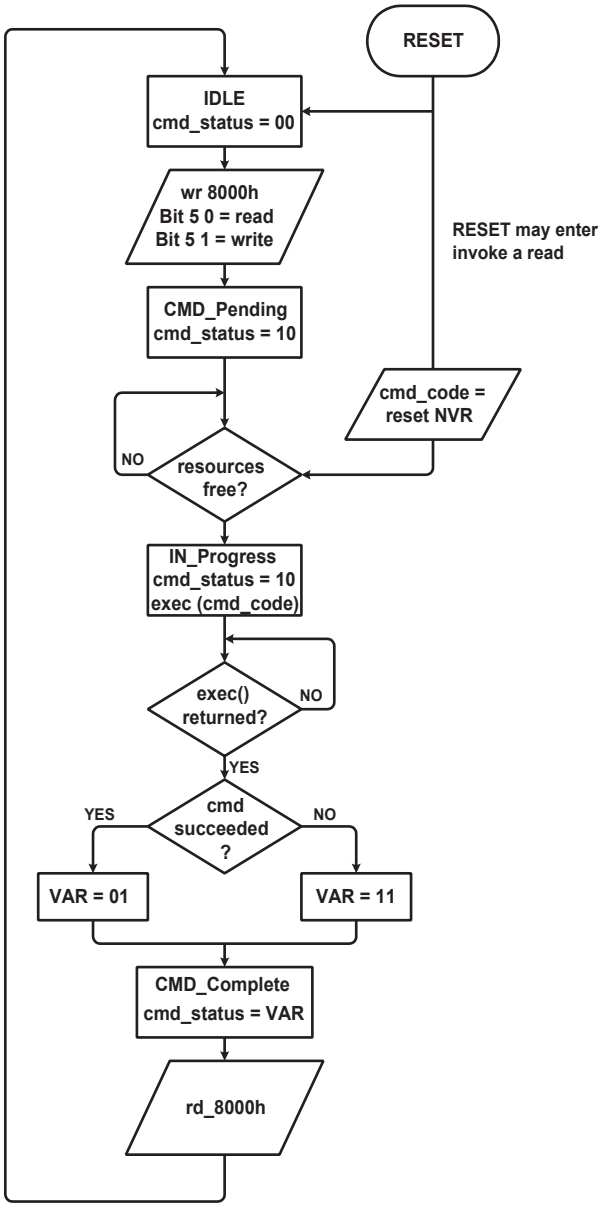
Figure 34. Two-Wire Serial Interface Module Access State Diagram



A zero written to bit 8 sets the two-wire serial interface module to Automatic mode. A one written to bit 8 sets the two-wire serial interface module to Manual mode

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1.10.4.1 Automatic Mode

Automatic mode provides easy access to non-volatile registers (NVR), such as EEPROM, used in XENPAK and XFP modules. In Automatic mode, the two-wire serial interface controller performs reads or writes to different sections of non-volatile memory according to the value of the Extended Command bits (bits 1 and 0) in the Vendor-Specific NVR Control Command Status register, as defined in "Vendor-Specific NVR Control Command Status," page 149. A value of 11 (binary) reads and writes all NVR contents, which is compliant with *XENPAK MSA Revision 3.0,* Section 10.10. Bit 5 determines whether the operation is read or write (where 0: Read, 1: Write).

In Automatic mode, the two-wire serial interface maps internal registers 30x8007 through 30x8106 to external NVR address 0 to 255. To perform an automatic read, first write external NVR address to Slave Device Address register (30x8002); then write to the Vendor-Specific NVR Control Command Status register (30x8000) using the proper settings. The two-wire serial interface controller reads the data stored in a certain section of NVR, which is defined by command bits (bits 1 and 0) of the Vendor-Specific NVR Control Command Status register, and saves data to the corresponding section of internal registers. For example, if the data written to Vendor-Specific NVR Control Command Status register (30x8000) is 0000h, the two-wire serial interface controller reads XFP EEPROM bytes 2-57, and stores data into internal registers from 30x8009 to 30x8040. The automatic write operation is similar, except for using the opposite direction.

The auto read/write operation is compatible with the ATMEL AT24Cxx series two-wire serial EEPROM. For the detailed description of the read/write operation, see the *ATMEL AT24Cxx Series Two-Wire Serial EEPROM Specification*. After the read/write operation is complete, the two-wire serial interface controller writes to Vendor-Specific NVR Control Command Status register and sets the command status bit 3 and bit 2 to 10 (binary) if the operation completes successfully, or sets the bits to 11 (binary) if the operation fails.

1.10.4.2 Manual Mode

A value of 1 in bit 8 of Vendor-Specific NVR Control Command Status register (30x8000) sets the two-wire serial interface module to Manual mode. This mode may be used to achieve communication with any other two-wire serial interface compliant devices connected to the two-wire serial interface bus through the MDIO interface, or to read or write particular words to or from the non-volatile registers. In this mode, any instruction written to the STW Instruction register (30x8001) initiates setting the connection to other devices, or to read/write byte data from or to other devices. The instruction set is shown in Table 9.

Table 9. Two-Wire Serial Interface Instruction Set for the STW Instruction Register (30x8001)

Instruction	Description
0301H	Read registers 30x8002 and 30x8003 to controller, start or re-start with slave transmitter
0201H	Read register 30x8003 to controller, start or re-start with slave transmitter
0101H	Read register 30x8002 to controller, start or re-start with slave transmitter
0001H	Start or restart with slave transmitter

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Table 9. Two-Wire Serial Interface Instruction Set for the STW Instruction Register (30x8001)

Instruction	Description
0309H	Read registers 30x8002 and 30x8003 to controller, start or re-start with slave receiver
0209H	Read register 30x8003 to controller, start or re-start with slave receiver
0109H	Read register 30x8002 to controller, start or re-start with slave receiver
0009H	Set connection with the slave receiver
0204H	Read 30x8003 to controller, Read data from slave transmitter, save data to register addressed 30x8003
0004H	Read data from slave transmitter, save data to the register whose address is stored in controller
0202H	Read 30x8003 to controller, Read data from slave transmitter, save data to register addressed by 30x8003, then terminate the transfer and disconnects with slave transmitter
0002H	Read data from slave transmitter, save data to the register whose address is stored in controller, then terminate the transfer and disconnects with slave transmitter
0208H	Read 30x8003 to controller, write the data stored in the register addressed by 30x8003 to slave receiver.
0008H	Write content of the register whose address is stored in controller to slave receiver
020AH	Read 30x8003 to controller, Write the data stored in the register addressed 30x8003 to slave receiver, then terminates the transfer and disconnects with slave receiver
000AH	Write the content of the register whose address is stored in controller to slave receiver, then terminates the transfer and disconnects with slave receiver
0020H	Soft reset transceiver.

Following a write transaction to STW Instruction register 30x8001, the two-wire serial interface module reads the contents of that register and sets the bits 7 and 6 (instruct status) to instruction in progress (10 binary).

- If the instruction executes successfully, the two-wire serial interface module writes to the 30x8001 register, sets the instruction status bits to 01 binary (instruction complete successfully), and is then ready to take the next instruction. Successful execution of instructions 0002H and 000AH makes the command completion successful.
- If the instruction execution fails, 11 (binary) for instruction failed is written to STW Instruction register 30x8001. Execution failure of an instruction also leads to command failure, and 11 (binary) is written to the Vendor-Specific NVR Control Command Status register 30x8000 bits 3 and 2.

1.10.4.3 Two-Wire Serial Interface Command Sequence Examples

The first two examples describe the command sequence for a single-byte read or write from a slave device connected to the two-wire serial interface bus in Two-Wire Serial Interface Manual mode. The third example shows the MDIO command sequence that executes a block read of the XFP module alarm and warning threshold data contained in the lower memory map byte address 2 to 57 (decimal).

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Example #1:

Use the following procedure to perform manual read operation:

1. Write to the Configuration register (30x8004) (Two-Wire Serial Interface mode).
2. Write the address of a slave internal register to a two-wire serial interface register with an address higher than 30x8007.
3. Write to Vendor-Specific NVR Control Status register (30x8000) set bit 8 to 1 (Manual mode).
4. Write address of the slave device to the Slave Device Address register (30x8002) (50'h for XFP modules).
5. Write the address of a two-wire serial interface register that stores the address of a slave internal register to the STW Register Address register (30x8003).
6. Write 0309H to the STW Instruction register (30x8001).
7. Write 0008H to the STW Instruction register (30x8001).
8. Write the address of the internal register that stores data read from slave to the STW Register Address register (30x8003).
9. Write 0001H to the STW Instruction register (30x8001).
10. Write 0202H to the STW Instruction register (30x8001), to read data and to end operation.

Example #2:

Use the following procedure to perform a manual write operation:

1. Write to the Configuration register (30x8004) (Two-Wire Serial Interface mode).
2. Write the address of a slave internal register to a two-wire serial interface register with an address higher than 30x8007.
3. Write to Vendor-Specific NVR Control Status register (30x8000) set bit 8 to 1 (Manual mode).
4. Write address of the slave device to the Slave Device Address register (30x8002) (50'h for XFP modules).
5. Write the address of an two-wire serial interface register that stores the address of a slave internal register to the STW Register Address register (30x8003).
6. Write 0309H to the STW Instruction register (30x8001).
7. Write 0008H to the STW Instruction register (30x8001).
8. Write the address of the internal register that contains the data to be written to the slave to the STW Register Address register (30x8003).
9. Write 020AH to the STW Instruction register (30x8001) to write data and to end operation.

Example #3:

Use the following procedure to perform an automatic block read operation:

1. Write the address of the slave device to the Slave Device Address register (30x8002) (50'h for XFP modules).
2. Write to the Configuration register (30x8004) bit 12 = 1 (XFP module).
3. Write 0000H to the Vendor-Specific NVR Control Command Status register (30x8000) (XFP bytes 2 through 57, auto read).

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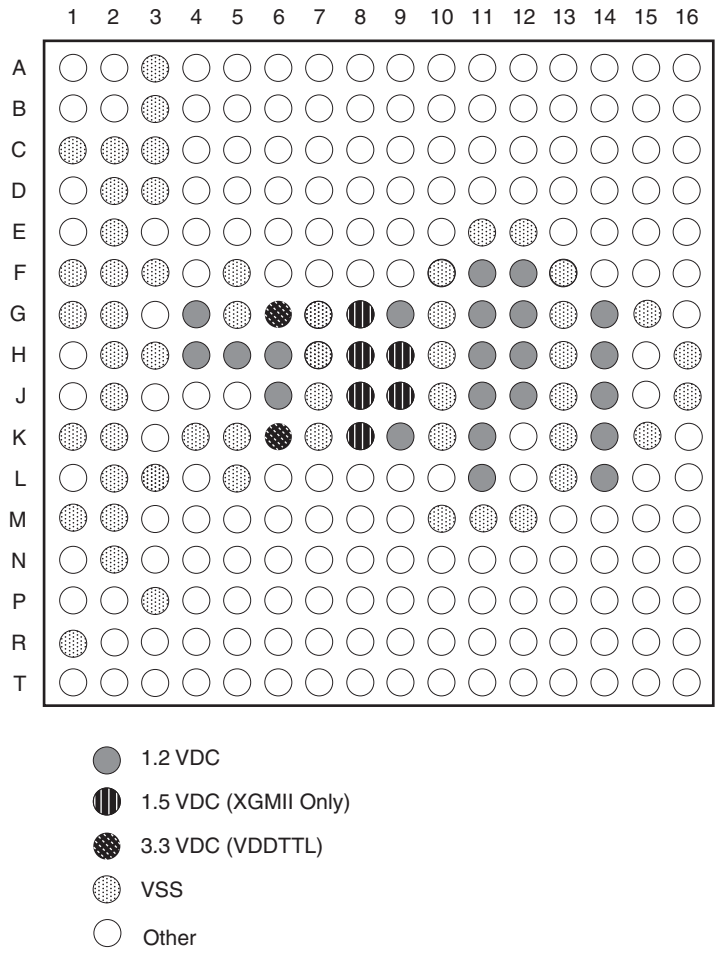
1.11 Power Supplies

In XAUI mode, the VSC8476 operates from a single 1.2 V power supply. If XGMII is used, a 1.5 V power supply is required. A 3.3 V power supply can be used to interface to other system devices on the low-speed LVTTL I/O. Figure 35 shows a top view of the VSC8476 power supply and VSS pin locations.

Figure 35. Top View of VSC8476 Showing Power and Ground Pin Locations



Current spikes, resulting from the rising and falling edges of the outputs, can couple to power lines and planes. A bypass or decoupling capacitor stores electrical charge and releases it onto the power lines and planes whenever one of these spikes occurs.

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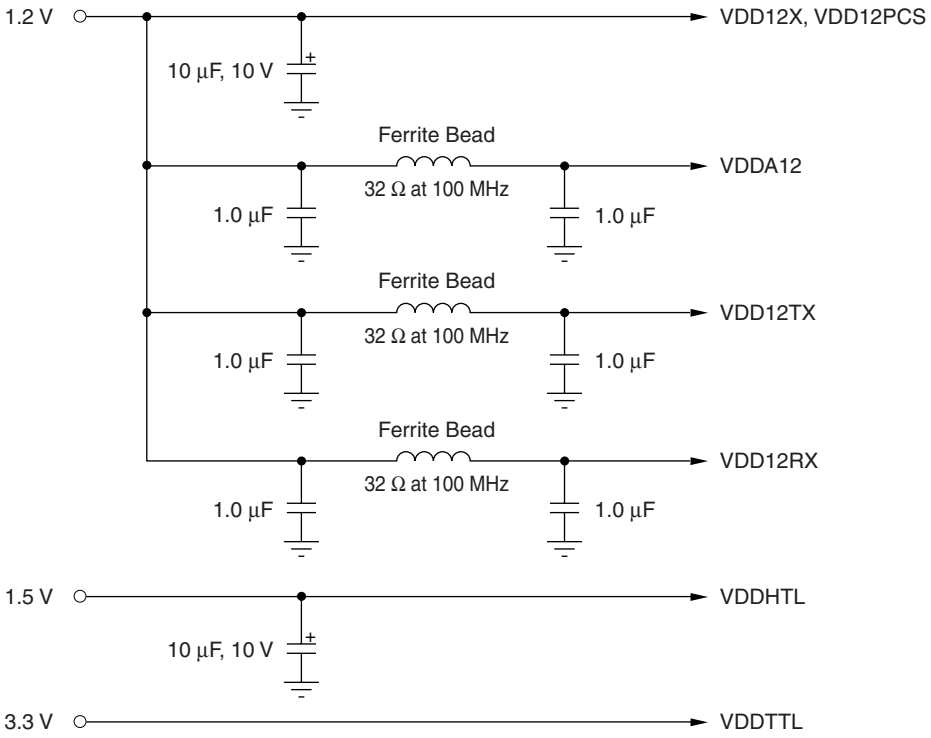
The recommended filter structures for the VSC8476 transceiver are illustrated in Figure 36.

Figure 36. Recommended Filter Structures for the VSC8476 Transceiver



Most of the VDD pins for the VSC8476 are +1.2 V. However, for optimum performance, there are some considerations for grouping these pins and treating them separately. It is recommended to isolate and separate the +1.2 V power supplies into four different areas of the device, as illustrated in Figure 37.

The digital regions of the device are supplied from the pins labeled VDD12X/VDD12PCS; these can be connected directly to the +1.2 V power supply. The analog supply for the XAUI is labeled VDDA12. The high-speed transmitter pins are labeled VDD12TX, and the high-speed receiver pins are labeled VDD12RX. These supplies should be isolated from the main supply using a low-pass filter structure. The series ferrite element provides isolation between the power groups on the device and should provide at least 32 ohms at 100 MHz. If possible, a local 10 µF, 10 V tantalum capacitor should be placed close to the device for the digital supply of +1.2 V (VDDX) and the supply of +1.5 V(VDDHTL) for XGMII.

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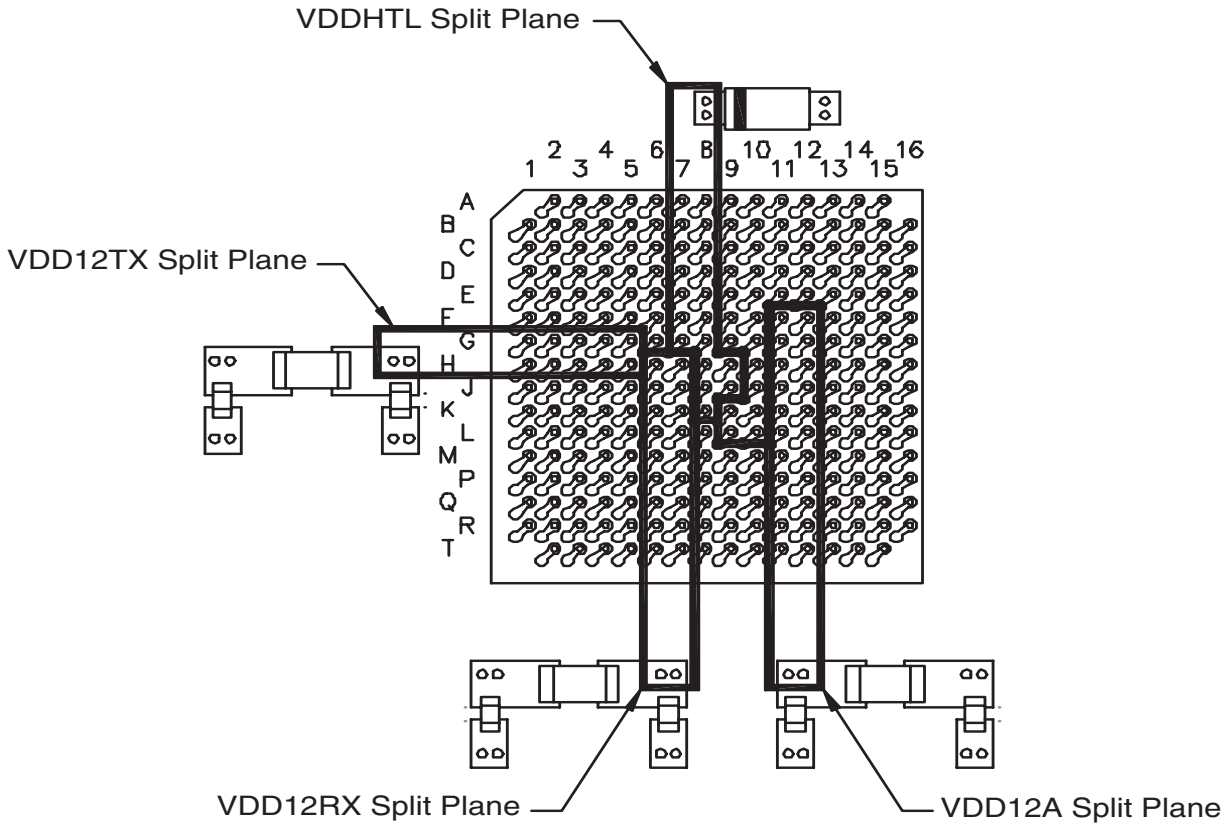
Figure 37. VSC8476 with the 1.2 V Power Supply Split into Four Separate Areas



Physical location is very important for a bypass capacitor to work properly. Consider a device driving a line from a low state to a high state. For the device to change state properly, an output current is needed instantaneously. This current needs to be provided to the device in a period less than or equal to the rise time of the output of the device. The bypass capacitor must charge and discharge in the same period; otherwise, a voltage drop occurs. Distance also becomes an important issue because the inductance due to line length reduces the effectiveness of the capacitance.

Local decoupling of each of these power supplies is critical in maintaining the proper operation of the part. It is recommended to decouple each power supply pin using a size 0402 0.1 µF X7R ceramic capacitor. Locating the capacitor as close as possible to the supply pin is the most effective way to address lead inductance and switching noise. If possible, do this directly below the device in the BGA field that connects the capacitor to the applicable power supply and an adjacent return.

Providing a low inductance current path is critical to electronics that switch at very high speeds. For more information about recommended decoupling schemes that provide power with maximum stability, see Figure 38.

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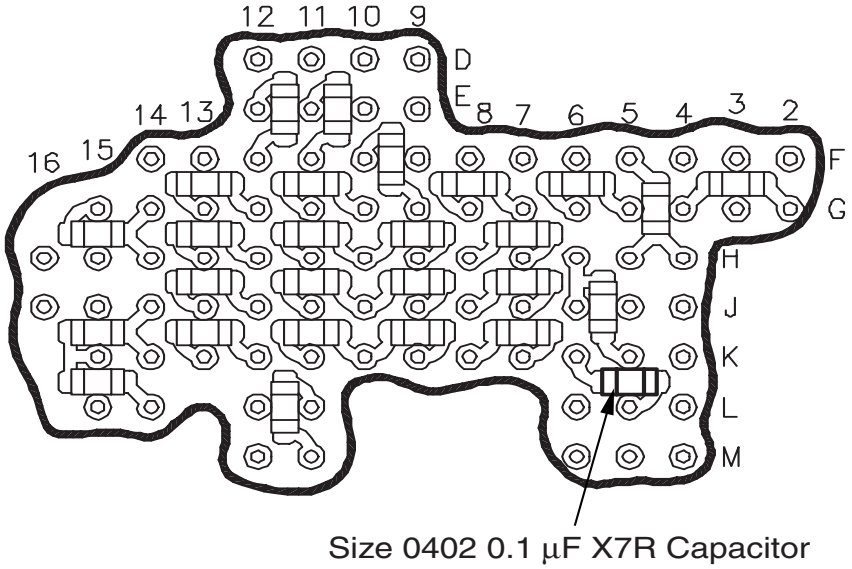
Figure 38. Power Supply Decoupling Layout Pattern Example



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2 Registers

This section describes the registers for the VSC8476 device.

2.1 Register Description

The following MDIO-Managable Device Addresses table shows the map for the MMD (MDIO-manageable devices) addresses that are accessible to the host using the MDIO interface. All the registers contained within each MMD are shown in "PMA Registers MMD1," page 74 and "PCS Registers MMD3," page 75. When writing to registers that contain reserved bits, the reserved bits should be programmed to zero to promote upward compatibility with future hardware revisions. Read requests of reserved bits or to reserved address locations return zero for this hardware revision. The software should ignore the values of reserved bits to promote upward compatibility.

Table 10. MDIO-Manageable Device MMD Addresses

Device Address	MMD Name
0	Reserved
1	PMA
2	WIS (not implemented)
3	PCS
4	PHY XS
5	DTE XS (not implemented)
6 - 29	Reserved
30	Vendor-Specific for the two-wire serial interface
31	(Not implemented)

Register bits can be read and write accessible; this is denoted by the R and W keywords in the register's access field. Additionally, some status registers and counters are cleared when read. These are denoted by the COR keyword in the access field. Finally, other registers are self-clearing, which is indicated by RWSC. For register tables with one row representing multiple bits, the reset values are given in hexadecimal and are indicated by 0x preceeding the value.

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Table 11. Access Types

Access Type	Description
RO	Read only—Writes are ignored.
RW	Read/write.
RO/LL	Read only/latch low—Defaults high. Latches and hold a low on designated event. Sets to high on read.
RO/LH	Read only/latch high—Defaults low. Latches and hold a high on designated event. Sets to low on read.
COR	Clear on read—Used for counter registers.
RWSC	Read/write self-clearing—Reset registers.
RWDV	Read/write default value—Test bits. The bits must be written to the default value for normal operation.

Table 12. PMA Registers MMD1

Register Address	Register Name	Details (Cross-Reference)
1x0000	PMA Control 1	See "PMA Control 1," page 83.
1x0001	PMA Status 1	See "PMA Status 1," page 85.
1x0002	PMA Device Identifier 1	See "PMA Device Identifier 1 and 2," page 86.
1x0003	PMA Device Identifier 2	See "PMA Device Identifier 1 and 2," page 86.
1x0004	PMA Speed Ability	See "PMA Speed Ability," page 86.
1x0005	PMA Devices in Package 1	See "PMA Devices in Package 1," page 87.
1x0006	PMA Devices in Package 2	See "PMA Devices in Package 2," page 88.
1x0007	PMA Control 2	See "PMA Control 2," page 89.
1x0008	PMA Status 2	See "PMA Status 2," page 89.
1x000E - 1x000F	PMA Package Identifier	See "PMA Package Identifier," page 93.
1x8000	Vendor-Specific Control PMA	See "Vendor-Specific Control PMA," page 94.
1x8002	Vendor-Specific RXIN Equalization Control	See "Vendor-Specific RXIN Equalization Control," page 96.

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Table 13. PCS Registers MMD3

Register Address	Register Name	Details (Cross-Reference)
3x0000	PCS Control 1	See "PCS Control 1," page 97.
3x0001	PCS Status 1	See "PCS Status 1," page 98.
3x0002 - 3x0003	PCS Device Identifier	See "PCS Device Identifier," page 99.
3x0004	PCS Speed Ability	See "PCS Speed Ability," page 100.
3x0005	PCS Device in Package 1	See "PCS Devices in Package 1," page 101.
3x0006	PCS Device in Package 2	See "PCS Devices in Package 2," page 102.
3x0007	PCS Control 2	See "PCS Control 2," page 103.
3x0008	PCS Status 2	See "PCS Status 2," page 104.
3x000E - 3x000F	PCS Package Identifier	See "PCS Package Identifier Registers," page 106.
3x0018	10GBASE-X PCS Status	See "10GBASE-X PCS Status," page 106.
3x0019	10GBASE-X PCS Control	See "10GBASE-X PCS Control," page 106.
3x0020	10GBASE-R PCS Status 1	See "10GBASE-R PCS Status 1," page 107.
3x0021	10GBASE-R PCS Status 2	See "10GBASE-R PCS Status 2," page 108.
3x0025	10GBASE-R PCS Test Pattern Seed A	See "10GBASE-R PCS Test Pattern Seed A," page 109.
3x0026 - 3x0029	10GBASE-R PCS Test Pattern Seed B	See "10GBASE-R PCS Test Pattern Seed B," page 111.
3x002A	10GBASE-R PCS Test Pattern Control	See "10GBASE-R PCS Test Pattern Control," page 112.
3x002B	10GBASE-R PCS Test Pattern Error Counter	See "10GBASE-R PCS Test Error Counter," page 113.
3x8000	Vendor-Specific USR Test 0	See "Vendor-Specific USR Test," page 114.
3x8001	Vendor-Specific USR Test1	See "Vendor-Specific USR Test," page 114.
3x8002	Vendor-Specific USR Test 2	See "Vendor-Specific USR Test," page 114.
3x8003	Vendor-Specific USR Test 3	See "Vendor-Specific USR Test," page 114.
3x8004	Vendor-Specific Square Wave Pulse Width	See "Vendor-Specific Square Wave Pulse Width," page 115.
3x8005	Vendor-Specific Control PCS	See "Vendor-Specific Control PCS," page 116.

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Table 13. PCS Registers MMD3 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
3x8007 - 3x8008	Vendor-Specific Test Error Counter	See "Vendor-Specific Test Error Counter," page 117.
3x8009	Vendor-Specific PCS FIFO Status	See "Vendor-Specific PCS FIFO Status," page 118.
3x800C	Vendor-Specific Tx FIFO Idle Add Count	See "Vendor-Specific Tx FIFO Idle Add Count," page 119.
3x800D	Vendor-Specific Tx FIFO Idle Drop Count	See "Vendor-Specific Tx FIFO Idle Drop Count," page 119.
3x800E	Vendor-Specific Rx FIFO Idle Add Count	See "Vendor-Specific Rx FIFO Idle Add Count," page 119.
3x800F	Vendor-Specific Rx FIFO Idle Drop Count	See "Vendor-Specific Rx FIFO Idle Drop Count," page 120.
3x8010	Vendor-Specific PCS Tx Sequencing Error Count	See "Vendor-Specific PCS Tx Sequencing Error Count," page 120.
3x8011	Vendor-Specific PCS Rx Sequencing Error Count	See "Vendor-Specific PCS Rx Sequencing Error Count," page 120.
3x8012	Vendor-Specific PCS Tx Block Encode Error Count	See "Vendor-Specific PCS Tx Block Encode Error Count," page 121.
3x8013	Vendor-Specific PCS Rx Block Decode Error Count	See "Vendor-Specific PCS Rx Block Decode Error Count," page 121.
3x8014	Vendor-Specific PCS Tx Character Encode Error Count	See "Vendor-Specific PCS Tx Character Encode Error Count," page 121.
3x8015	Vendor-Specific PCS Rx Character Decode Error Count	See "Vendor-Specific PCS Rx Character Decode Error Count," page 122.

Table 14. PHY XS Registers MMD4

Register Address	Register Name	Details (Cross-Reference)
4x0000	PHY XS Control	See "PHY XS Control," page 123.
4x0001	PHY XS Status 1	See "PHY XS Status 1," page 124.
4x0002	PHY XS Identifier 1	See "PHY XS Identifier," page 125.
4x0003	PHY XS Identifier 2	See "PHY XS Identifier," page 125.
4x0004	PHY XS Speed Ability	See "PHY XS Speed Ability," page 126.
4x0005	PHY XS Devices in Package 1	See "PHY XS Devices in Package 1," page 127.
4x0006	PHY XS Devices in Package 2	See "PHY XS Devices in Package 2," page 128.

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Table 14. PHY XS Registers MMD4 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
4x0008	PHY XS Status 2	See "PHY XS Status 2," page 128.
4x000E	PHY XS Package ID 1	See "PHY XS Package ID 1," page 129.
4x000F	PHY XS Package ID 2	See "PHY XS Package ID 2," page 129.
4x0018	10G PHY XGXS Lane Status	See "10G PHY XGXS Lane Status," page 130.
4x0019	10G PHY XGXS Test Control	See "10G PHY XS Test Control," page 132.
4x8000	Vendor-Specific Test Control	See "Vendor-Specific Test Control," page 133.
4x8001	Vendor-Specific Test Pattern Check Status	See "Vendor-Specific Test Pattern Check Status," page 134.
4x8002	Vendor-Specific Code Group Error Counter Control	See "Vendor-Specific Code Group Error Counter Control," page 135.
4x8003 - 4x8004	Vendor-Specific Code Group Error Counter	See "Vendor-Specific Code Group Error Counter," page 136.
4x8005	Vendor-Specific Running Disparity Error Counter Control	See "Vendor-Specific Running Disparity Error Counter Control," page 137.
4x8006 - 4x8007	Vendor-Specific Running Disparity Error Counter	See "Vendor-Specific Running Disparity Error Counter," page 138.
4x8008	Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter Control	See "Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter Control," page 139.
4x8009 - 4x800A	Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter	See "Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter," page 140.
4x800B	Vendor-Specific Test Pattern Mismatch Error Counter Control	See "Vendor-Specific Test Pattern Mismatch Error Counter Control," page 141.
4x800C - 4x800D	Vendor-Specific Test Pattern Mismatch Error Counter	See "Vendor-Specific Test Pattern Mismatch Error Counter," page 142.
4x800E	Vendor-Specific SerDes	See "Vendor-Specific SerDes," page 143.
4x800F	Vendor-Specific Loopback Control	See "Vendor-Specific Loopback Control," page 144.
4x8010	Vendor-Specific XAUI Input Equalization Control	See "Vendor-Specific XAUI Input Equalization Control," page 146.
4x8011	Vendor-Specific XAUI Output Pre-Emphasis Control and LOS	See "Vendor-Specific XAUI Output Pre-Emphasis Control and LOS," page 147.
4x8012	Vendor-Specific I/O 2	See "Vendor-Specific I/O 2," page 148.

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Table 15. Vendor-Specific Registers MMD30

Register Address	Register Name	Details (Cross-Reference)
30x8000	Vendor-Specific XENPAK NVR Control Command Status	See "Vendor-Specific NVR Control Command Status," page 149.
30x8001	STW Instruction	See "STW Instruction," page 151.
30x8002	Slave Device Address	See "Slave Device Address," page 152.
30x8003	STW Register Address	See "STW Register Address," page 152.
30x8004	Configuration	See "Configuration," page 152.
30x8005-30x8006	Optical Module Data Memory	See "Optical Module Data Memory Registers," page 153.
30x8007	Optical Module Data Version Number	See "Optical Module Data Version Number," page 153.
30x8008-30x8009	Non-Volatile Register Size	See "Non-Volatile Register Size," page 153.
30x800A-30x800B	Memory Used	See "Memory Used," page 153.
30x800C	Vendor-Specific Basic Address	See "Vendor-Specific Basic Address," page 154.
30x800D	Vendor-Specific Customer Address	See "Vendor-Specific Customer Address," page 154.
30x800E	Vendor Address	See "Vendor Address," page 154.
30x800F-30x8010	Extended Vendor Address	See "Extended Vendor Address," page 154.
30x8012	Transceiver Type	See "Transceiver Type," page 155.
30x8013	Connector Type	See "Connector Type," page 155.
30x8014	Bit Encoding	See "Bit Encoding," page 155.
30x8015-30x8016	Bit Rate	See "Bit Rate," page 156.
30x8017	Protocol Type	See "Protocol Type," page 157.
30x8018-30x8021 and 30x8024-30x8025	Standards Compliance Codes	See "Standard Compliance Codes," page 157.
30x8022-30x8023	Range	See "Range," page 161.
30x8026-30x8028	Wavelength Channel 0	See "Wavelength Channel 0," page 162.
30x8029-30x802B	Wavelength Channel 1	See "Wavelength Channel 1," page 163.
30x802C-30x802E	Wavelength Channel 2	See "Wavelength Channel 2," page 165.
30x802F-30x8031	Wavelength Channel 3	See "Wavelength Channel 3," page 166.
30x8032-30x8035	Package Idnetifier OUI	See "Package Identifier OUI," page 168.

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Table 15. Vendor-Specific Registers MMD30 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
30x8036-30x8039	Transceiver Vendor OUI	See "Transceiver Vendor OUI," page 170.
30x803A-30x8049	Vendor Name	See "Vendor Name," page 171.
30x804A-30x8059	Vendor PN	See "Vendor PN," page 172.
30x805A-30x805B	Vendor Revision	See "Vendor Revision," page 172.
30x805C-30x806B	Vendor Serial Number	See "Vendor Serial Number," page 172.
30x806C-30x8075	Vendor-Specific Date Code	See "Vendor-Specific Date Code," page 173.
30x8076	5 V Stressed Environment Reference 100% = 1A	See "5 V Stressed Environment Reference," page 173.
30x8077	3.3 V Stressed Environment Reference 100% = 2A	See "3.3 V Stressed Environment Reference," page 174.
30x8078	APS Stressed Environment Reference 100% = 2A	See "APS Stressed Environment Reference," page 174.
30x8079	Nominal APS Voltage	See "Nominal APS Voltage," page 175.
30x807A	DOM Capability	See "DOM Capability," page 175.
30x807B	Low-Power Startup Mode Capability	See "Low-Power Startup Mode Capability," page 176.
30x807C	Reserved	See "Reserved," page 176.
30x807D	Basic Checksum	See "Basic Checksum," page 176.
30x807E-30x80AD	Customer Space Area	See "Customer Space Area," page 176.
30x80AE-30x8106	Vendor-Specific Area	See "Vendor-Specific Area," page 177.
30x9000	Rx_ALARM Control	See "Rx_Alarm Control," page 177.
30x9001	Tx_ALARM Control	See "Tx_Alarm Control," page 178.
30x9002	LASI Control	See "LASI Control," page 178.
30x9003	Rx_ALARM Status	See "Rx_ALARM Status," page 179.
30x9004	Tx_ALARM Status	See "Tx_ALARM Status," page 179.
30x9005	LASI Status	See "LASI Status," page 180.
30x9006	Tx Flag Control	See "Tx Flag Control," page 180.
30x9007	Rx Flag Control	See "Rx Flag Control," page 181.
30xA000	Transceiver Temperature High Alarm (MSB)	See "Transceiver Temperature High Alarm (MSB)," page 182.
30xA001	Transceiver Temperature High Alarm (LSB)	See "Transceiver Temperature High Alarm (LSB)," page 182.
30xA002	Transceiver Temperature Low Alarm (MSB)	See "Transceiver Temperature Low Alarm (MSB)," page 182.

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Table 15. Vendor-Specific Registers MMD30 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
30xA003	Transceiver Temperature Low Alarm (LSB)	See "Transceiver Temperature Low Alarm (LSB)," page 183.
30xA004	Transceiver Temperature High Warning (MSB)	See "Transceiver Temperature High Warning (MSB)," page 183.
30xA005	Transceiver Temperature High Warning (LSB)	See "Transceiver Temperature High Warning (LSB)," page 183.
30xA006	Transceiver Temperature Low Warning (MSB)	See "Transceiver Temperature Low Warning (MSB)," page 184.
30xA007	Transceiver Temperature Low Warning (LSB)	See "Transceiver Temperature Low Warning (LSB)," page 184.
30xA008-30xA00F	Reserved	See "Reserved," page 184.
30xA010	Laser Bias Current High Alarm (MSB)	See "Laser Bias Current High Alarm (MSB)," page 184.
30xA011	Laser Bias Current High Alarm (LSB)	See "Laser Bias Current High Alarm (LSB)," page 185.
30xA012	Laser Bias Current Low Alarm (MSB)	See "Laser Bias Current Low Alarm (MSB)," page 185.
30xA013	Laser Bias Current Low Alarm (LSB)	See "Laser Bias Current Low Alarm (LSB)," page 185.
30xA014	Laser Bias Current High Warning (MSB)	See "Laser Bias Current High Warning (MSB)," page 186.
30xA015	Laser Bias Current High Warning (LSB)	See "Laser Bias Current High Warning (LSB)," page 186.
30xA016	Laser Bias Current Low Warning (MSB)	See "Laser Bias Current Low Warning (MSB)," page 186.
30xA017	Laser Bias Current Low Warning (LSB)	See "Laser Bias Current Low Warning (LSB)," page 187.
30xA018	Laser Output Power High Alarm (MSB)	See "Laser Output Power High Alarm (MSB)," page 187.
30xA019	Laser Output Power High Alarm (LSB)	See "Laser Output Power High Alarm (LSB)," page 187.
30xA01A	Laser Output Power Low Alarm (MSB)	See "Laser Output Power Low Alarm (MSB)," page 188.
30xA01B	Laser Output Power Low Alarm (LSB)	See "Laser Output Power Low Alarm (LSB)," page 188.
30xA01C	Laser Output Power High Warning (MSB)	See "Laser Output Power High Warning (MSB)," page 188.
30xA01D	Laser Output Power High Warning (LSB)	See "Laser Output Power High Warning (LSB)," page 189.
30xA01E	Laser Output Power Low Warning (MSB)	See "Laser Output Power Low Warning (MSB)," page 189.
30xA01F	Laser Output Power Low Warning (LSB)	See "Laser Output Power Low Warning (LSB)," page 189.

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Table 15. Vendor-Specific Registers MMD30 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
30xA020	Receiver Optical Power High Alarm (MSB)	See "Receiver Optical Power High Alarm (MSB)," page 190.
30xA021	Receiver Optical Power High Alarm (LSB)	See "Receiver Optical Power High Alarm (LSB)," page 190.
30xA022	Receiver Optical Power Low Alarm (MSB)	See "Receiver Optical Power Low Alarm (MSB)," page 190.
30xA023	Receiver Optical Power Low Alarm (LSB)	See "Receiver Optical Power Low Alarm (LSB)," page 191.
30xA024	Receiver Optical Power High Warning (MSB)	See "Receiver Optical Power High Warning (MSB)," page 191.
30xA025	Receiver Optical Power High Warning (LSB)	See "Receiver Optical Power High Warning (LSB)," page 191.
30xA026	Receiver Optical Power Low Warning (MSB)	See "Receiver Optical Power Low Warning (MSB)," page 192.
30xA027	Receiver Optical Power Low Warning (LSB)	See "Receiver Optical Power Low Warning (LSB)," page 192.
30xA060	Transceiver Temperature (MSB)	See "Transceiver Temperature (MSB)," page 194.
30xA061	Transceiver Temperature (LSB)	See "Transceiver Temperature (LSB)," page 194.
30xA062-30xA063	Reserved	See "Reserved," page 194.
30xA064	Laser Bias Current (MSB)	See "Laser Bias Current (MSB)," page 195.
30xA065	Laser Bias Current (LSB)	See "Laser Bias Current (LSB)," page 195.
30xA066	Laser Output Power (MSB)	See "Laser Output Power (MSB)," page 195.
30xA067	Laser Output Power (LSB)	See "Laser Output Power (LSB)," page 195.
30xA068	Receiver Optical Power (MSB)	See "Receiver Optical Power (MSB)," page 196.
30xA069	Receiver Optical Power (LSB)	See "Receiver Optical Power (LSB)," page 196.
30xA06A-30xA06D	Reserved	See "Reserved," page 196.
30xA07A	Digital Optical Monitoring Capability	See "Digital Optical Monitoring Capability," page 197.
30xA06E	Optical Status Bits	See "Optional Status Bits," page 197.
30xA06F	Digital Optical Monitoring Capability Extended	See "Digital Optical Monitoring Capability Extended," page 198.
30xA070	Tx Alarm Flags	See "Tx Alarm Flags," page 198.
30xA071	Rx Alarm Flags	See "Rx Alarm Flags," page 199.
30xA072-30xA073	Reserved	See "Reserved," page 199.
30xA074	Tx Warning Flags	See "Tx Warning Flags," page 199.

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Table 15. Vendor-Specific Registers MMD30 *(continued)*

Register Address	Register Name	Details (Cross-Reference)
30xA075	Rx Warning Flags	See "Rx Warning Flags," page 200.
30xA076-30xA077	Reserved	See "Reserved," page 200.

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2.2 PMA Registers

2.2.1 PMA Control 1

The following register contains the PMA control. The default value for each bit of the PMA Control 1 register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: PMA Control 1
Address: 1x0000

Bit	Name	Access	Description	Reset Value
15	Soft_Reset	RWSC	This bit is self-clearing. 0: Normal operation. 1: VSC8476 soft reset. Resets all MMDs.	0
14	Reserved	RO	Reserved.	0
13	Speed_Selection	RO	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
12	Reserved	RO	Reserved.	0
11	Low_Power	RW	Low power. 0: Normal. 1: Low power.	0
10:7	Reserved	RO	Reserved.	0x0
6	Speed_Selection	RW	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
5:2	Speed_Selection	RO	Speed selection. 5 4 3 2 1 x x x: Reserved. x 1 x x: Reserved. x x 1 x: Reserved. 0 0 0 1: Reserved. 0 0 0 0: 10 Gbps.	0x0
1	Reserved	RO	Reserved.	0
0	PMA_Parallel_Loopback	RW	PMA parallel loopback. See Figure 26, page 53. 0: Disable PMA loopback mode. 1: Enable PMA loopback mode. Note: This path can also be controlled in the hardware using the SPLITLOOPN package ball.	0

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2.2.1.1 Soft_Reset

Resetting the VSC8476 is accomplished by setting bit 15 to a value of one. This action sets all registers and state machines to their default states. As a consequence, this action may change the internal state of the PMA and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same chip. This bit is self-clearing and returns a value of one in bit 15 when a reset is in progress and a value of zero otherwise. A PMA is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process completes within 0.5 seconds from the setting of bit 15. During a reset, the PMA responds to reads from the PMA Control Register bit 15 and from the PMA Status 2 register bits 5 and 14.

2.2.1.2 Speed_Selection

Speed selection bits 13 and 6 are both set to one. Any attempt to change the bits to an invalid setting is ignored. The speed of the PMA may be selected using bits 5 through 2. The speed abilities of the PMA are identified in bits 15 through 0 of the PMA speed ability register. The PMA ignores writes to the PMA speed selection bits that select speeds not identified in the PMA speed ability register. The PMA speed selection defaults to 10 Gbps and above operation.

2.2.1.3 Low_Power

A PMA/PMD may be placed into a Low Power mode by setting bit 11 to a value of one. This action may also initiate a Low Power mode in any other MMDs that are instantiated in the same package. The low power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low power mode is implementation specific and any interface signals should not be relied upon. While in the Low Power mode, the device shall, as a minimum, respond to management transactions necessary to exit the Low Power mode. The default value of bit 11 is zero.

Note: This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at an optimum error rate after exiting from reset or Low Power mode.

2.2.1.4 PMA_Parallel_Loopback

The PMA is placed in Loopback mode 6 when bit 0 is set to one. The default value of bit 0 is set to zero for normal operation. For more information about loopback operation, see "Loopback Operation," page 44.

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2.2.2 PMA Status 1

The following register contains the PMA status. This register is read only; a write to this register has no effect.

Name: PMA Status 1
Address: 1x0001

Bit	Name	Access	Description	Reset Value
15:8	Reserved	RO	Reserved.	0x0
7	Fault	RO	Fault. 0: Fault condition is not detected. 1: Fault condition is detected.	0
6:3	Reserved	RO	Reserved	0x0
2	Receive_Link_Status	RO/LL	Receive link status. Latch low clears on read. 0: PMA receive link is down. 1: PMA receive link is up.	1
1	Low_Power_Ability	RO	Low power ability. 0: PMA does not support Low Power mode. 1: PMA supports Low Power mode.	1
0	Reserved	RO	Reserved.	0

2.2.2.1 Fault

Fault is a global PMA variable. When read as a one, bit 7 indicates that the PMA detects a fault condition on either the transmit or receive paths. When read as a zero, bit 7 indicates that the PMA does not detect a fault condition. This bit is set by a logical OR of receiver LOS, receiver LOL, and transmitter LOL. For 10-Gbps operation, bit 7 is set to a one when either of the fault bits 11 and 10 located in register 1x0008 are set to one.

2.2.2.2 Receive_Link_Status

When read as a one, bit 2 indicates the receive link is up. When read as a zero, bit 2 indicates the receive link is down. This bit is implemented with latch low behavior.

2.2.2.3 Low_Power_Ability

Bit 1 indicates that the PMA does support Low Power mode.

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2.2.3 PMA Device Identifier 1 and 2

The following registers provide a 32-bit value that constitutes a unique identifier for the PMA.

Name: PMA Device Identifier
Address: 1x0002
1x0003

Bit	Name	Access	Description	Reset Value
15:0	PMA_Device_Identifier	RO	32-bit value that is a unique identifier for the PMA bits 15:0	0x0007
15:0	PMA_Device_Identifier	RO	32-bit value that is a unique identifier for the PMA bits 31:16	0x0400

2.2.3.1 PMA_Device_Identifier

Address 1x0002 contains the lower word of the unique identifier of the PMA, and address 1x0003 contains the upper word of the unique identifier of the PMA.

2.2.4 PMA Speed Ability

The following register contains PMA speed assignment.

Name: PMA Speed Ability
Address: 1x0004

Bit	Name	Access	Description	Reset Value
15:1	Reserved	RO	Reserved.	0x0
0	10G_Capable	RO	10 G capable. 0: PMA is incapable of operating at 10 Gbps. 1: PMA is capable of operating at 10 Gbps.	1

2.2.4.1 10G_Capable

Bit 0 indicates that the PMA is able to operate at a data rate of 10 Gbps.

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2.2.5 PMA Devices in Package 1

The assignment of bits in the Devices in Package 1 register is shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD is instantiated within the same package as the other MMDs whose associated bits are set to a one within the Devices in Package registers.

Name: PMA Devices in Package 1
Address: 1x0005

Bit	Name	Access	Description	Reset Value
15:6	Reserved	RO	Reserved.	0x0
5	DTE_XS_Present	RO	DTE XS present. 0: DTE XS not present in package. 1: DTE XS present in package.	0
4	PHY_XS_Present	RO	PHY XS present. 0: PHY XS not present in package. 1: PHY XS present in package.	1
3	PCS_Present	RO	PCS present. 0: PCS not present in package. 1: PCS present in package.	1
2	WIS_Present	RO	WIS present. 0: WIS not present in package. 1: WIS present in package.	0
1	PMA_Present	RO	PMA present. 0: PMA not present in package. 1: PMA present in package.	1
0	Clause22_Register_Present	RO	Clause 22 register present 0: Not present. 1: Present	0

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2.2.6 PMA Devices in Package 2

The assignment of bits in the Devices in Package 2 register is shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD is instantiated within the same package as other MMDs whose associated bits are set to one in the Devices in Package registers.

Name: PMA Devices in Package 2
Address: 1x0006

Bit	Name	Access	Description	Reset Value
15	VS_Device2_Present	RO	Vendor-specific device 2 present. 1: Vendor-specific device 2 is present in the package. 0: Vendor-specific device 2 is not present in the package.	0
14	VS_Device1_Present	RO	Vendor-specific device 1 present. 0: Vendor-specific device 1 is not present in the package. 1: Vendor-specific device 1 is present in the package.	0
13:0	Reserved	RO	Reserved.	0x0

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2.2.7 PMA Control 2

The assignment of bits in the PMA Control 2 register is shown in the following table:

Name: PMA Control 2
Address: 1x0007

Bit	Name	Access	Description	Reset Value
15:3	VS_Device2_Present	RO	Reserved.	0x0
2:0	VS_Device1_Present	RW	PMA type selection. 2 1 0 1 1 1: 10GBASE-SR PMA type 1 1 0 : 10GBASE-LR PMA type 1 0 1: 10GBASE-ER PMA type 1 0 0: 10GBASE-LX4 PMA type 0 1 1: 10GBASE-SW PMA type 0 1 0: 10GBASE-LW PMA type 0 0 1: 10GBASE-EW PMA type 0 0 0: Reserved	0x111

2.2.7.1 PMA_Type_Selection

The PMA type of the 10-Gbps PMA may be selected using bits 2 through 0. The PMA type abilities of the 10-G PMA are advertised in bits 7 through 0 of the PMA Status 2 register. The PMA type selection defaults to a supported ability.

2.2.8 PMA Status 2

The assignment of bits in the PMA Status 2 register is shown in the following table. All the bits in this register are read only; a write to this register has no effect.

Name: PMA Status 2
Address: 1x0008

Bit	Name	Access	Description	Reset Value
15:14	Device_Present	RO	Device present 15 14 1 0: Device is responding at this address. 1 1: No device is responding at this address. 0 1: No device is responding at this address. 0 0: No device is responding at this address..	0x10
13	Transmit_Fault_Ability	RO	Transmit fault ability 0: PMA does not have the ability to detect a fault condition on the transmit path. 1: PMA has the ability to detect a fault condition on the transmit path.	1

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Bit	Name	Access	Description	Reset Value
12	Receive_Fault_Ability	RO	Receive fault ability 0: PMA does not have the ability to detect a fault condition on the receive path. 1: PMA has the ability to detect a fault condition on the receive path.	1
11	Transmit_Fault	RO/LH	Transmit fault 0: No fault condition on transmit path. 1: Fault condition on transmit path.	0
10	Receive_Fault	RO/LH	Receive fault 0: No fault condition on receive path. 1: Fault condition on receive path.	0
9	PMD_Loopback_Ability	RO	PMD loopback ability 0: PMD does not have the ability to perform a loopback function. 1: PMD has the ability to perform a loopback function.	0
8	PMD_Transmit_Disable_Ability	RO	PMD transmit disable ability 0: PMD does not have the ability to disable the transmit path. 1: PMD has the ability to disable the transmit path.	0
7	10GBASE-SR_Ability	RO	10GBASE-SR ability 0: PMA is not able to perform 10GBASE-SR. 1: PMA is able to perform 10GBASE-SR.	1
6	10GBASE-LR_Ability	RO	10GBASE-LR ability 0: PMA is not able to perform 10GBASE-LR. 1: PMA is able to perform 10GBASE-LR.	1
5	10GBASE-ER_Ability	RO	10GBASE-ER ability 0: PMA is not able to perform 10GBASE-ER. 1: PMA is able to perform 10GBASE-ER.	1
4	10GBASE-LX4_Ability	RO	10GBASE-LX4 ability 0: PMA is not able to perform 10GBASE-LX4. 1: PMA is able to perform 10GBASE-LX4.	0
3	10GBASE-SW_Ability	RO	10GBASE-SW ability 1: PMA is able to perform 10GBASE-SW. 0: PMA is not able to perform 10GBASE-SW.	0
2	10GBASE-LW_Ability	RO	10GBASE-LW ability 1: PMA is able to perform 10GBASE-LW. 0: PMA is not able to perform 10GBASE-LW.	0
1	10GBASE-EW_Ability	RO	10GBASE-EW ability 0: PMA is not able to perform 10GBASE-EW. 1: PMA is able to perform 10GBASE-EW.	0
0	PMA_Loopback_Ability	RO	PMA loopback ability 0: PMA does not have the ability to perform a loopback function. 1: PMA has the ability to perform a loopback function.	1

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2.2.8.1 Devices_Present

Read as 10, bits 15 and 14 indicate that the device is present and responding at this register address.

2.2.8.2 Transmit_Fault_Ability

Bit 13 indicates that the PMA has the ability to detect a fault condition on the transmit path.

2.2.8.3 Receive_Fault_Ability

Bit 12 indicates that the PMA has the ability to detect a fault condition on the receive path.

2.2.8.4 Transmit_Fault

When read as a one, bit 11 indicates that the PMA has detected a fault condition on the transmit path. When read as a zero, bit 11 indicates that the PMA transmit path is operating normally. This bit is set when a transmitter LOL fault occurred. The transmit fault bit is implemented with a latching function, such that the occurrence of a fault condition on the transmit path will cause the transmit fault bit to become set to a one and remain set until it is cleared. The transmit fault bit is cleared each time this register is read using the management interface, and by a PMA reset. If the transmit fault condition exists at the time the register is read using the management interface then the transmit fault bit is not cleared to a zero by the read operation.

2.2.8.5 Receive_Fault

When read as a one, bit 10 indicates that the PMA has detected a fault condition on the receive path. When read as a zero, bit 10 indicates that the PMA receive path is operating normally. This bit is set when a receiver LOL or receiver LOS fault has occurred. The receive fault bit is implemented with a latching function, such that the occurrence of a fault condition on the receive path will cause the receive fault bit to become set to a one and remain set until it is cleared. The receive fault bit is cleared each time this register is read using the management interface and by a PMA reset. If the receive fault condition exists at the time the register is read using the management interface then the receive fault bit is not be cleared to a zero by the read operation.

2.2.8.6 PMD_Loopback_Ability

Bit 9 indicates that the PMD is able to perform the loopback function. The PMD loopback function is controlled using the PMD loopback bit in the PMA Control 1 register.

2.2.8.7 PMD_Transmit_Disable_Ability

Bit 8 indicates that the PMD is not able to perform the transmit disable function.

2.2.8.8 10GBASE-SR_Ability

Bit 7 indicates that the PMA is able to support a 10GBASE-SR PMA type.

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2.2.8.9 10GBASE-LR_Ability

Bit 6 indicates that the PMA is able to support a 10GBASE-LR PMA type.

2.2.8.10 10GBASE-ER_Ability

Bit 5 indicates that the PMA is able to support a 10GBASE-ER PMA type.

2.2.8.11 10GBASE-LX4_Ability

Bit 4 indicates that the PMA is not able to support a 10GBASE-LX4 PMA type.

2.2.8.12 10GBASE-SW_Ability

Bit 3 indicates that the PMA is not able to support a 10GBASE-SW PMA type.

2.2.8.13 10GBASE-LW_Ability

Bit 2 indicates that the PMA is not able to support a 10GBASE-LW PMA type.

2.2.8.14 10GBASE-EW_Ability

Bit 1 indicates that the PMA is not able to support a 10GBASE-EW PMA type.

2.2.8.15 PMA_Loopback_Ability

Bit 0 indicates that the PMA is able to perform a loopback function. The loopback function is controlled using the PMA loopback bit in the PMA Control 1 register.

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2.2.9 PMA Package Identifier

The two PMA Package Identifier registers provide a 32-bit value, which constitute a unique identifier for the type of package that the PMA is instantiated within. The identifier is composed of bit 3 through bit 24 of the organizationally unique identifier (OUI) assigned to the package manufacturer by IEEE, plus a six-bit model number and a four-bit revision number.

Name: PMA Package Identifier
Address: 1x000E
1x000F

Bit	Name	Access	Description	Reset Value
15:0	PMA_Package_Identifier	RO	PMA package identifier bits 15:0	0x0000
15:0	PMA_Package_Identifier	RO	PMA package identifier bits 31:16	0x0000

2.2.9.1 PMA_Package_Identifier

Bits 15:0 of address 1x000E contain the lower word of the unique identifier of the PMA package, and bits 15:0 of address 1x000F contain the upper word of the unique identifier of the PMA package.

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2.3 Vendor-Specific Registers for PMA

The following sections describe the vendor-specific registers for PMA.

2.3.1 Vendor-Specific Control PMA

The assignment of bits in the Vendor-Specific Control register are shown in the following table. The default value for each bit of the Vendor-Specific Control register is chosen so that the initial state of the device upon completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Control PMA
Address: 1x8000

Bit	Name	Access	Description	Reset Value
15	Reserved	RWDV	Reserved.	1
14	Reserved	RWDV	Reserved.	0
13	Reserved	RWDV	Reserved.	1
12	Reserved	RWDV	Reserved.	1
11	TXCOUTMUTEB	RWDV	TXCOUTMUTEB. 0: TXCOUT output is disabled. 1: TXCOUT output enabled.	0
10	TXFIFORESB	RWDV	TXFIFORESB. 0: Reset MUX FIFO. 1: Normal operation.	1
9	TXFIFOARB	RWDV	TXFIFOARB. 0: Automatic reset MUX FIFO on overflow or underflow. This is the default. 1: Manual reset mode (for bit 10).	0
8	PMA_Serial_Loopback	RWDV	PMA serial loopback. See Figure 27, page 54. 0: Enable PMA loopback 7. 1: Disable PMA loopback 7. Note that this path can also be controlled in the hardware using the SPLITLOOPN package ball.	1
7	TXDATAINV	RWDV	TXDATAINV. 0: All data is inverted. 1: Normal operation.	1
6	TXMSBSELB	RWDV	TXMSBSELB. 0: No bit swapping enabled (MSB first). 1: Bit swapping enabled (LSB first).	1
5	Test_Bit	RWDV	Test bit only. Only write the default value.	0
4	Test_Bit	RWDV	Test bit only. Only write the default value.	1
3	RXLOSDATASQB	RWDV	RXLOSDATASQB. 0: Enable automatic data squelch mode. 1: Manual data squelch mode.	1

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Bit	Name	Access	Description	Reset Value
2	RXLCKREFB	RWDV	RXLCKREFB. 0: Lock to Refclk (squelch data). 1: Normal operation.	1
1	RXDATAINV	RWDV	RXDATAINV. 0: XFI receive data invert. 1: Normal operation.	1
0	RXMSBSELB	RWDV	RXMSBSELB. 0: No bit swapped enabled (MSB of XSBI sent first). 1: MSB/LSB swap at 16-bit interface (LSB of XSBI sent first).	1

2.3.1.1 TXCOUTMUTEB

Tx High-speed Clock Output Mute Bar is set to zero by default to disable the high-speed clock output. Set to one to enable TXCOUT.

2.3.1.2 TXFIFORESB

The MUX FIFO asynchronous reset.

2.3.1.3 TXFIFOARB

MUX FIFO automatically resets on overflow/underflow error indication by default. When disabled, the MUX FIFO requires a manual reset.

2.3.1.4 PMA_Serial_Loopback

The PMA is placed in a loopback 7 when bit 8 is set to one. The default value of bit 8 is set to zero for normal operation. For more information about loopback operation, see "Loopback Operation," page 44.

2.3.1.5 TXDATAINV

Transmit side data invert.

2.3.1.6 TXMSBSELB

Transmit side bit order swap.

2.3.1.7 RXLOSDATASQB

DMUX CRU loss of signal automatic squelch mode. RxLOSB=0 directs CRU to squelch (set to 0) output data and switch to lock-to-refclk. RxLOSB=1 for normal mode

2.3.1.8 RXLCKREFB

DMUX CRU lock to reference clock mode. When set to zero, the CRU ignores the status of RxLOSDATSQB and RxLOSB.

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2.3.1.9 RXDATAINV

Receive side data invert.

2.3.1.10 RXMSBSELB

Receive side bit order swap.

2.3.2 Vendor-Specific RXIN Equalization Control

The following registers contains the vendor-specific control of the 10 Gbps receiver equalization.

Name: Vendor-Specific RXIN Equalization Control
Address: 1x8002

Bit	Name	Access	Description	Reset Value
15:11	RXIN_Equalization_Control	RW	Amount of equalization applied to the data coming into the 10 Gbps receiver. For more information, see "XFI Data Input Receiver Equalization," page 31.	0x11111
10:0	Reserved	RWDV	Test bits. Always write to a default value.	0x10101010101

2.3.2.1 RXIN_Equalization_Control

This register sets the amount of equalization is applied to the data coming into the 10 Gbps receiver (RXIN). Setting bits to 1 increases equalization.

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2.4 PCS Registers

2.4.1 PCS Control 1

The assignment of bits in the PCS Control 1 register is shown in the following table. The default value for each bit of the PCS Control 1 register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: PCS Control 1
Address: 3x0000

Bit	Name	Access	Description	Reset Value
15	Reset	RWSC	Resets all MMDs. This bit is self-clearing. 0: Normal operation. 1: VSC8476 soft reset.	0
14	PCS_Parallel_Loopback	RW	PCS parallel loopback (Loopback 4). 0: Disable loopback mode. 1: Enable loopback mode.	0
13	Speed_Selection	RO	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
12	Reserved	RO	Reserved. Note that low-power mode for the PCS is enabled using register 1x0000, bit 14.	0
11	Reserved	RW	Reserved.	0
10:7	Reserved	RW	Reserved.	0x0
6	Speed_Selection	RO	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
5:2	Speed_Selection	RO	Speed selection. 5 4 3 2 1 x x x: Reserved x 1 x x: Reserved x x 1 x: Reserved 0 0 0 1: Reserved 0 0 0 0: 10 Gbps	0x0000
1:0	Reserved	RO	Reserved.	0x0

2.4.1.1 Reset

Resetting the VSC8476 is accomplished by setting bit 15 to a one. This action sets all registers and state machines to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This bit is self-clearing and returns a value of one in bit 15 when a reset is in progress and a value of zero otherwise. It is not recommended to write to any of the PCS registers during the reset process. The reset process is completed within 0.5 seconds after setting bit 15. During a reset, the PCS responds to reads from PCS Control 1 register bit 15 and from the PCS Status 2 register bits 15 and 14.

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2.4.1.2 PCS_Parallel_Loopback

The PCS is placed in the parallel loopback mode 1 when bit 14 is set to a one. The default value is zero. For more information, see "Loopback Operation," page 44.

2.4.1.3 Speed_Selection

Speed selection bits 13 and 6 should both be written as a one. Any attempt to change the bits to an invalid setting is ignored. The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are indicated in bits 15 through 0 of the PCS speed ability register. The PCS ignores writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. The PCS speed selection defaults to the supported ability.

2.4.2 PCS Status 1

The following register contains the PCS status. This register is read only; a write to this register has no effect.

Name: PCS Status 1
Address: 3x0001

Bit	Name	Access	Description	Reset Value
15:8	Reserved	RO	Reserved.	0x0
7	Fault	RO	Fault. 0: Fault condition not detected. 1: Fault condition detected.	0
6:3	Reserved	RO	Reserved.	0x0
2	PCS_Receive_Link_Status	RO/LL	PCS receive link status. 0: PCS receive link is down. 1: PCS receive link is up.	0
1	Low_Power_Ability	RO	Low power ability. Indirectly controlled by register 1x0000, bit 11. 0: PCS does not support low-power mode. 1: PCS supports low-power mode.	1
0	Reserved	RO	Reserved.	0

2.4.2.1 Fault

When read as a one, bit 7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 7 indicates that the PCS has not detected a fault condition. For 10 Gbps operation, bit 7 is set to a one when either of the fault bits 11 or 10 located in register 3x0008 are set to a one.

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2.4.2.2 PCS_Receive_Link_Status

When read as a one, bit 2 indicates that the PCS receive link is up. When read as a zero, bit 2 indicates that the PCS receive link is down. When a 10GBASE-R mode of operation is selected for the PCS using the PCS type selection field, this bit is a latching low version of bit 12 register 3x0020. The receive link status bit is implemented with a latching function, such that the failure of a link causes the receive link status bit to become cleared to a zero and remain cleared until it is read using the management interface. If the link is down at the time the register is read using the management interface, then the PCS link status bit is not set to a one by the read operation.

2.4.2.3 Low_Power_Ability

This feature is controlled by register 1x0000[11].

2.4.3 PCS Device Identifier

Registers 3x0002 and 3x0003 provide a 32-bit value, which constitutes an unique identifier for this PCS.

Name: PCS Identifier
Address: 3x0002
3x0003

Bit	Name	Access	Description	Reset Value
15:0	PCS_Identifier	RO	PCS identifier for bits 15:0	0x0007
15:0	PCS_Identifier	RO	PCS identifier for bits 31:16	0x0400

2.4.3.1 PCS_Identifier

Address 3x0002 contains the low-order word of the unique identifier for the PCS, and address 3x0003 contains the high-order word of the unique identifier for the PCS.

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2.4.4 PCS Speed Ability

The following register contains PCS speed assignment.

Name: PCS Speed Ability
Address: 3x0004

Bit	Name	Access	Description	Reset Value
15:1	Reserved	RO	Reserved.	0x0
0	10G_Capable	RO	10 G capable. 0: PCS is not capable of operating at 10 Gbps. 1: PCS is capable of operating at 10 Gbps.	1

2.4.4.1 10 G Capable

Bit 0 indicates that the PCS is able to operate at a data rate of 10 Gbps.

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2.4.5 PCS Devices in Package 1

The assignment of bits in the Devices in Package registers are shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD was instantiated within the same package as other MMDs whose associated bits were set to a one within the Devices in Package registers.

Name: PCS Devices in Package 1
Address: 3x0005

Bit	Name	Access	Description	Reset Value
15:6	Reserved	RO	Reserved.	0x0
5	DTE_XS_Present	RO	DTE XS present. 0: DTE XS is not present in the package. 1: DTE XS is present in the package.	0
4	PHY_XS_Present	RO	PHY XS present. 0: PHY XS is not present in the package. 1: PHY XS is present in the package. **Note**: The reset value of this bit is mode-dependent. The reset value is 1 for XFI to XAUI mode and for XAUI to XGMII mode. The reset value is 0 for XFI to XGMII mode.	0: for XFI to XGMII 1: for XFI to XAUI and XAUI to XGMII
3	PCS_Present	RO	PCS present. 0: PCS is not present in the package. 1: PCS is present in the package.	1
2	WIS_Present	RO	WIS present. 0: WIS is not present in the package. 1: WIS is present in the package.	0
1	PMA_Present	RO	PMA present. 0: PMA is not present in the package. 1: PMA is present in the package.	1
0	Clause_22_Registers_Present	RO	Clause 22 registers present. 0: Clause 22 registers are not present in the package. 1: Clause 22 registers are present in the package.	0

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2.4.6 PCS Devices in Package 2

The assignment of bits in the Devices in Package registers are shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD was instantiated within the same package as other MMDs whose associated bits were set to a one within the Devices in Package registers.

Name: PCS Devices in Package 2
Address: 3x0006

Bit	Name	Access	Description	Reset Value
15	VS_Device2_Present	RO	Vendor-specific device 2 present. 0: Vendor-specific device 2 is not present in the package. 1: Vendor-specific device 2 is present in the package.	0
14	VS_Device1_Present	RO	Vendor-specific device 1 present. 0: Vendor-specific device 1 is not present in the package. 1: Vendor-specific device 1 is present in the package.	0
13:0	Reserved	RO	Reserved.	0x0

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2.4.7 PCS Control 2

The assignment of bits in the PCS Control 2 register is shown in the following table:

Name: PCS Control 2
Address: 3x0007

Bit	Name	Access	Description	Reset Value
15:2	Reserved	RO	Reserved	0x0
1:0	PCS_Type_Selection	RO	PCS type selection. 1 0 1 1: Reserved 1 0: 10GBASE-W PCS type 0 1: 10GBASE-X PCS type 0 0: 10GBASE-R PCS type	0x00

2.4.7.1 PCS_Type_Selection

The device supports 10GBASE-R PCS.

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2.4.8 PCS Status 2

The assignment of bits in the PCS Status 2 register is shown in the following table. All the bits in this register are read only; a write to this register has no effect.

Name: PCS Status 2
Address: 3x0008

Bit	Name	Access	Description	Reset Value
15:14	Device_Present	RO	Device present. 15 14 1 0: Device is responding at this address. 1 1: No device is responding at this address. 0 1: No device is responding at this address. 0 0: No device is responding at this address.	0x10
13:12	Reserved	RO	Reserved.	0x0
11	Transmit_Fault	RO/LH	Transmit fault (path to PMA). 0: Fault condition on the transmit path. 1: No fault condition on the transmit path.	0
10	Receive_Fault	RO/LH	Receive fault (path from PMA). 0: Fault condition on the receive path. 1: No fault condition on the receive path.	0
9:3	Reserved	RO	Reserved.	0x0
2	10GBASE-W_Capable	RO	10GBASE-W capable. 0: PCS is not able to support 10GBASE-W. 1: PCS is able to support 10GBASE-W.	0
1	10GBASE-X_Capable	RO	10GBASE-X capable. 0: PCS is not able to support 10GBASE-X. 1: PCS is able to support 10GBASE-X.	0
0	10GBASE-R_Capable	RO	10GBASE-R capable. 0: PCS is not able to support 10GBASE-R. 1: PCS is able to support 10GBASE-R.	1

2.4.8.1 Devices_Present

Read as 10, bits 15 and 14 indicate that a device is present and responding at this register address.

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2.4.8.2 Transmit_Fault

When read as a one, bit 11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit is implemented with a latching function, such that the occurrence of a fault condition on the transmit path causes the transmit fault bit to become set to a one and remain set until it is cleared. The transmit fault bit is cleared each time this register is read using the management interface and a PCS reset. If the transmit fault condition exists at the time the register is read using the management interface, then the transmit fault bit is not cleared to a zero by the read operation.

2.4.8.3 Receive_Fault

When read as a one, bit 10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit is implemented with a latching function, such that the occurrence of a fault condition on the receive path causes the receive fault bit to become set to a one and remain set until it is cleared. The receive fault bit is cleared each time this register is read using the management interface and by a PCS reset. If the receive fault condition exists at the time the register is read using the management interface, then the receive fault bit is not cleared to a zero by the read operation.

2.4.8.4 10GBASE-W_Capable

Bit 2 indicates that the 64b/66b PCS is not able to support the 10GBASE-W PCS type.

Note: Since the VSC8476 does not support 10GBASE-W, this description is for information only.

2.4.8.5 10GBASE-X_Capable

Bit 1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

Note: Since the VSC8476 does not support 10GBASE-X, this description is for information only.

2.4.8.6 10GBASE-R_Capable

Bit 0 indicates that the PCS is able to support the 10GBASE-R PCS type.

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2.4.9 PCS Package Identifier Registers

The following registers provide a 32-bit value, which constitute a unique identifier for the type of package that the PCS is instantiated within. The identifier composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by IEEE, plus a six-bit model number and a four-bit revision number.

Name: PCS Package Identifier
Address: 3x000E
3x000F

Bit	Name	Access	Description	Reset Value
15:0	PCS_Package_Identifier	RO	PCS package identifier bits 15:0	0x0000
15:0	PCS_Package_Identifier	RO	PCS package identifier bits 31:16	0x0000

2.4.9.1 PCS_Package_Identifier

Bits 15:0 of address 1x000E contain the lower word of the unique identifier of the PCS package, and bits 15:0 of address 1x000F contain the upper word of the unique identifier of the PCS package.

2.4.10 10GBASE-X PCS Status

10GBASE-X PCS is not implemented.

Name: 10GBASE-X PCS Status
Address: 3x0018

Bit	Name	Access	Description	Reset Value
15:0	Reserved	RO	Reserved	0x0

2.4.11 10GBASE-X PCS Control

10GBASE-X PCS is not implemented.

Name: 10GBASE-X PCS Control
Address: 3x0019

Bit	Name	Access	Description	Reset Value
15:0	Reserved	RO	Reserved	0x0

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2.4.12 10GBASE-R PCS Status 1

The assignment of bits in the 10GBASE-R PCS Status 1 register is shown in the following table. All the bits in this register are read only; a write to this register has no effect.

Name: 10GBASE-R PCS Status 1
Address: 3x0020

Bit	Name	Access	Description	Reset Value
15:13	Reserved	RO	Reserved.	0x0
12	10GBASE-R_RX_Link_Status	RO	10GBASE-R receive link status. 0: 10GBASE-R PCS receive links are not up. 1: 10GBASE-R PCS receive links are up. **Note**: This does not apply in Pattern Generation and Checking mode.	0
11:3	Reserved	RO	Reserved.	0x0
2	PRBS31_Pattern_Testing_Ability	RO	PRBS31 pattern testing ability. 0: PCS does not support PRBS31 pattern testing. 1: PCS is able to support PRBS31 pattern testing.	1
1	10GBASE-R_PCS_High_BER	RO	10GBASE-R PCS high BER ($\geq 10^{-4}$). 0: 10GBASE-R PCS not reporting a high BER. 1: 10GBASE-R PCS reporting a high BER. **Note**: This does not apply in Pattern Generation and Checking mode.	0
0	10GBASE-R_PCS_Block_Lock	RO	10GBASE-R PCS block lock. 0: 10GBASE-R PCS is not locked to received blocks. 1: 10GBASE-R PCS is locked to received blocks. **Note**: This does not apply in Pattern Generation and Checking mode.	0

2.4.12.1 10GBASE-R_RX_Link_Status

When read as a one, bit 12 indicates that the 10GBASE-R PCS has BLOCK_LOCK = TRUE and HI_BER = FALSE. When read as a zero, bit 12 indicates that either BLOCK_LOCK = FALSE or HI_BER = TRUE.

2.4.12.2 PRBS31_Pattern_Testing_Ability

Bit 2 indicates that the PCS is able to support PRBS31 pattern testing. The pattern generation and checking is controlled by using bits 5 and 4 of register 3x002A.

2.4.12.3 10GBASE-R_PCS_High_BER

When read as a one, bit 1 indicates that the 64b/66b receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 1 indicates that the 64b/66b receiver is detecting a BER of $< 10^{-4}$.

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2.4.12.4 10GBASE-R_PCS_Block_Lock

When read as a one, bit 0 indicates that the 64b/66b receiver has block lock. When read as a zero, bit 0 indicates that the 64b/66b receiver does not have block lock.

2.4.13 10GBASE-R PCS Status 2

The assignment of bits in the 10GBASE-R PCS Status 2 register is shown in the following table. All the bits in this register are read only; a write to this register has no effect. The contents of this register are undefined when the 10GBASE-R PCS is operating in Jitter Test mode.

Name: 10GBASE-R PCS Status 2
Address: 3x0021

Bit	Name	Access	Description	Reset Value
15	Latched_Block_Lock	RO/LL	Latched block lock. 0: 10GBASE-R PCS does not have block lock. 1: 10GBASE-R PCS has block lock. **Note**: This does not apply in PCS pattern testing generator modes.	1
14	Latched_High_BER	RO/LH	Latched high BER. 0: 10GBASE-R PCS has not reported a high BER. 1: 10GBASE-R PCS has reported a high BER. **Note**: This does not apply in PCS pattern testing generator modes.	0
13:8	BER_Counter	RO	BER counter. Non-rollover (saturation counter). **Note**: This does not apply in PCS pattern testing generator modes.	0x0
7:0	Error_Block_Counter	RO	Error block counter. Non-rollover (saturation counter). **Note**: This does not apply in PCS pattern testing generator modes.	0x0

2.4.13.1 Latched_Block_Lock

When read as a one, bit 15 indicates that the 10GBASE-R PCS has achieved block lock. When read as a zero, bit 15 indicates that the 10GBASE-R PCS lost the block lock. The block lock bit is implemented with a latching function so that a loss of block lock causes the latched block lock bit to become cleared to a zero and remain cleared until it is read using the management interface. If the PCS does not have block lock at the time the register is read using the management interface, then the latched block lock bit is not set to a one by the read operation.

This bit is a latching low version of the 10GBASE-R PCS block lock status bit.

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2.4.13.2 Latched_High_BER

When read as a one, bit 14 indicates that the 10GBASE-R PCS has detected a high BER. When read as a zero, bit 14 indicates that the 10GBASE-R PCS did not detect a high BER. The latched high BER bit is implemented with a latching function so that the occurrence of a high BER causes the latched high BER condition exists at the time the register is read using the management interface, then the high BER bit is not cleared to a zero by the read operation.

This bit is a latching low version of the 10GBASE-R PCS high BER status bit.

2.4.13.3 BER_Counter

The BER counter contains a six-bit count of the number of times that the bad_ber_sh state was entered since the register was last accessed using MDIO. The BER counter is implemented as a non-rollover counter so that when the counter reaches 63 counts, it does not roll to 0 when the bad_ber_sh state is subsequently entered. The BER counter clears to zero when read.

2.4.13.4 Error_Blocks_Counter

The error blocks counter contains an eight-bit count of the number of error blocks that occurred since the register was last accessed using MDIO. The error blocks counter is implemented as a non-rollover counter so that when the counter reaches 255, it does not roll to 0 when further error blocks are detected. The error blocks counter is cleared to zero when read.

2.4.14 10GBASE-R PCS Test Pattern Seed A

The assignment of bits in the 10GBASE-R PCS Test Pattern Seed A registers (3x0022 to 3x0025) is shown in the following tables.

Name: 10GBASE-R PCS Pattern Seed A
Address: 3x0025

Bit	Name	Access	Description	Reset Value
15:10	Reserved	RO	Reserved	0x0
9:0	Test_SeedA	RW	Test seed A3 for bits 57:48	0x0

Name: 10GBASE-R PCS Pattern Seed A
Address: 3x0024

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedA	RW	Test seed A2 for bits 47:32	0x0

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Name: 10GBASE-R PCS Pattern Seed A
Address: 3x0023

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedA	RW	Test seed A1 for bits 31:16	0x0

Name: 10GBASE-R PCS Pattern Seed A
Address: 3x0022

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedA	RW	Test seed A0 for bits 15:0	0x0

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2.4.15 10GBASE-R PCS Test Pattern Seed B

The assignment of bits in the 10GBASE-R PCS Test Pattern Seed B register is shown in the following tables.

Name: 10GBASE-R PCS Pattern Seed B
Address: 3x0029

Bit	Name	Access	Description	Reset Value
15:10	Reserved	RO	Reserved	0x0
9:0	Test_SeedB	RW	Test seed B3 for bits 57:48	0x0

Name: 10GBASE-R PCS Pattern Seed B
Address: 3x0028

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedB	RW	Test seed B2 for bits 47:32	0x0

Name: 10GBASE-R PCS Pattern Seed B
Address: 3x0027

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedB	RW	Test seed B1 for bits 31:16	0x0

Name: 10GBASE-R PCS Pattern Seed B
Address: 3x0026

Bit	Name	Access	Description	Reset Value
15:0	Test_SeedB	RW	Test seed B0 for bits 15:0	0x0

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2.4.16 10GBASE-R PCS Test Pattern Control

The assignment of bits in the 10GBASE-R PCS Test Pattern Control register is shown in the following table.

Name: 10GBASE-R PCS Test Pattern Control
Address: 3x002A

Bit	Name	Access	Description	Reset Value
15:6	Reserved	RO	Reserved.	0x0
5:1	PCS Test Mode Selection	RW	PCS Test mode selection. For information about mode selection, see Table 16.	0x0
0	Data_Pattern_Select	RW	Data pattern select. 0: Local fault (LF) data pattern. 1: Zeros data pattern.	0

Table 16. MDIO Test Pattern Control Register 3 × 2A Bit Settings

Test Mode	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRBS31 Generator	x	1	0	x	x	x
Pseudo-Random Generator	x	x	1	x	0	x
Square-Wave Generator	x	x	1	x	1	x
PRBS31 Checker	1	x	x	0	x	x
Pseudo-Random Checker	0	x	x	1	x	x

2.4.16.1 Test_Pattern_Select

Default register contents (all zeros) must be written prior to issuing each test mode command.

2.4.16.2 Data_Pattern_Select

When bit 0 is set to a one, the zeros data pattern is used for testing. When bit 0 is set to a zero, the LF data pattern is used for testing.

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2.4.17 10GBASE-R PCS Test Error Counter

The assignment of bits in the 10GBASE-R PCS Test Error Counter register is shown in the following table. The test error counter is a 16-bit counter that contains the number of errors received during a test. The counter is reset to zero when read using the MDIO and saturates at 65535. The 32-bit versions of this counter (in registers 3x8007 and 3x8008) also clear upon read of the register. For more information, see "PCS Test Modes," page 36.

Name: 10GBASE-R PCS Test Pattern Control
Address: 3x002B

Bit	Name	Access	Description	Reset Value
15:0	Test_Pattern_Error_Counter	R	Test pattern error counter	0x0000

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2.5 Vendor-Specific Registers for PCS

2.5.1 Vendor-Specific USR Test

The assignment of bits in the four Vendor-Specific USR Test registers (3x8000 to 3x8003) are shown in the following tables. The default value for each bit of the vendor-specific registers are chosen so that the initial state of the device upon completion of reset is a normal operational state without requiring management intervention.

The user-defined test pattern is scrambled and transmitted during Pseudo-Random Test mode. This is an optional pattern used instead of an LF or zeros pattern during Pseudo-Random Test mode.

Name: Vendor-Specific USR Test (0, 1, 2, and 3)
Address: 3x8000
3x8001
3x8002
3x8003

Bit	Name	Access	Description	Reset Value
15:0	User_Data_Pattern	RW	User data pattern. Address 3x8000: bits [15:0] Address 3x8001: bits [31:16] Address 3x8002: bits [47:32] Address 3x8003: bits [63:48]	0x0

2.5.1.1 User_Data_Pattern

User-programable test pattern used in pseudo-random test mode.

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2.5.2 Vendor-Specific Square Wave Pulse Width

The assignment of bits in the Vendor-Specific Square Wave Pulse Width register is shown in the following table. The default value for each bit of the vendor-specific registers are chosen so that the initial state of the device upon completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Square Wave Pulse Width
Address: 3x8004

Bit	Name	Access	Description	Reset Value
15:4	Reserved	RO	Reserved.	0x0
3:0	Square_Wave_Pulse_Width	RW	Square wave pulse width bits [3:0]. Vendor-specific transmit square wave test pattern length.	0x0000

2.5.2.1 Square_Wave_Pulse_Width

When square-wave pattern generation is enabled, the transmission of a repeating pattern of n ones is followed by n zeros. The value of n can be in the range from 4 to 11, inclusive, and is set by this register. Register values ≤4 sets n = 4. Register values ≥ 11 sets n = 11.

For more information, see "Square-Wave Test Pattern Generator," page 38.

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2.5.3 Vendor-Specific Control PCS

The assignment of bits in the Vendor-Specific Control register is shown in the following table. The default value for each bit of the Vendor-Specific Control register is chosen so that the initial state of the device upon completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Control PCS
Address: 3x8005

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RO	Reserved.	0x0
10	Disable_Descramble	RW	Disable descrambler.	0
9	Disable_Scrambler	RW	Disable scrambler.	0
8	PCS_XGMII_Data_Source	RW	PCS XGMII data source.	0: XAUI to XFI 1: XGMII to XFI
7	PHY_XS_XGMII_Source	RW	PHY XS XGMII data source.	0
6	Enable_XGMII_Output	RW	Enable XGMII output (XGMII Rx).	0: XAUI to XFI 1: XGMII to XFI
5	Disable_RX_Block_Seq_Check	RW	Disable Rx block sequence checking.	0
4	Disable_TX_Block_Seq_Check	RW	Disable Tx block sequence checking.	0
3	Reserved	RO	Reserved.	0
2	PCS_Parallel_Loopback	RW	PCS parallel loopback. 0: Disable loopback 5. 1: Enable loopback 5.	0
1	Reserved	RW	Reserved.	0
0	User_Test_Pattern_Enable	RW	User test pattern enable.	0

2.5.3.1 Disable_Descramble

Setting bit 10 to 1 disables the scrambler in the Rx path.

2.5.3.2 Disable_Scrambler

Setting bit 9 to 1 disables the scrambler in the Tx path.

2.5.3.3 PCS_XGMII_Data_Source

When bit 8 is set to 1, PCS receives Tx XGMII from the IOMODESEL pin. When set to 0, PCS receives Tx XGMII from PHY XS. Upon reset, this bit defaults to 0 when in XAUI to XFI mode, and 1 when in XGMII to XFI mode.

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2.5.3.4 PHY_XS_XGMII_Source

When bit 7 is set to 1, PHY XS receives external Tx XGMII data. When set to 0, PHY XS receives PCS Rx XGMII data.0

2.5.3.5 Enable_XGMII_Output

When bit 6 is set to 1, Rx XGMII is sent to external pins. When set to 0. Rx XGMII external pins are quiet. Upon reset, this bit defaults to 0 when IOMODESEL=1 in the XAUI to XFI mode, and 1 when IOMODESEL = 1 in the XGMII to XFI mode.

2.5.3.6 Disable_RX_Block_Seq_Check

When bit 5 is set to 1, block sequence checking is disabled in PCS Rx path. In this mode, block errors are not generated when an invalid block sequence is encountered in the Rx path.

2.5.3.7 Disable_TX_Block_Seq_Check

When bit 4 is set to 1, block sequence checking is disabled in the PCS Tx path. In this mode, block errors are not generated when an invalid block sequence is encountered in the Tx path.

2.5.3.8 PCS_Parallel_Loopback

When bit 2 is set to 1, XAUI input data or Tx XGMII data is looped back at internal XSBI. For more information, see "Loopback 5," page 52.

2.5.3.9 User_Test_Pattern_Enable

Enables the user test pattern when using pseudo-random test mode.

2.5.4 Vendor-Specific Test Error Counter

The assignment of bits in the Vendor-Specific Test Error Counter registers 3x8007 and 3x8008 is shown in the following table.

Name: Vendor-Specific Test Error Counter 1 and 2
Address: 3x8007
3x8008

Bit	Name	Access	Description	Reset Value
15:0	Test_Error_Counter	RO	Test error counter bits. Vendor-specific test error counter bits. Address 3x8007: Test error counter bits [15:0]. Address 3x8008: Test error counter bits [31:16].	0x0

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2.5.5 Vendor-Specific PCS FIFO Status

The assignment of bits in the Vendor-Specific PCS FIFO Status register is shown in the following table:

Name: Vendor-Specific PCS FIFO Status
Address: 3x8009

Bit	Name	Access	Description	Reset Value
15:4	Reserved	RO/LH	Reserved	0x0
3	FIFO_RX_Overflow	RO/LH	FIFO Rx overflow	0
2	FIFO_RX_Underflow	RO/LH	FIFO Rx underflow	0
1	FIFO_TX_Overflow	RO/LH	FIFO Tx overflow	0
0	FIFO_TX_Underflow	RO/LH	FIFO Tx underflow	0

2.5.5.1 FIFO_RX_Overflow

Rx FIFO overflow alarm that is set to one when an overflow occurs and is cleared when the register is read.

2.5.5.2 FIFO_RX_Underflow

Rx FIFO underflow alarm that is set to one when an underflow occurs and is cleared when the register is read.

2.5.5.3 FIFO_TX_Overflow

Tx FIFO overflow alarm that is set to one when an overflow occurs and is cleared when the register is read.

2.5.5.4 FIFO_TX_Underflow

Tx FIFO underflow alarm that is set to one when an underflow occurs and is cleared when the register is read.

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2.5.6 Vendor-Specific Tx FIFO Idle Add Count

The assignment of bits in the Vendor-Specific Tx FIFO Idle Add Count register is shown in the following table. The counter is incremented once for each idle group that is added to the Tx path for clock rate disparity compensation.

Name: Vendor-Specific TX FIFO Idle Add Count
Address: 3x800C

Bit	Name	Access	Description	Reset Value
15:0	FIFO_TX _Idle_Add_Count	COR	FIFO Tx idle group (||I||) add count	0x0

2.5.7 Vendor-Specific Tx FIFO Idle Drop Count

The assignment of bits in the Vendor-Specific Tx FIFO Idle Drop Count register is shown in the following table. The counter is incremented once for each idle group that is dropped in the Tx path for clock rate disparity compensation.

Name: Vendor-Specific Tx FIFO Idle Drop Count
Address: 3x800D

Bit	Name	Access	Description	Reset Value
15:0	FIFO_TX _Idle_Drop_Count	COR	FIFO Tx idle group (||I||) drop count.	0x0

2.5.8 Vendor-Specific Rx FIFO Idle Add Count

The assignment of bits in the Vendor-Specific Rx FIFO Idle Add Count register is shown in the following table. The counter is incremented once for each idle group that is added to the Rx path for clock rate disparity compensation.

Name: Vendor-Specific Rx FIFO Idle Add Count
Address: 3x800E

Bit	Name	Access	Description	Reset Value
15:0	FIFO_RX _Idle_Add_Count	COR	FIFO Rx idle group (||I||) add count.	0x0

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2.5.9 Vendor-Specific Rx FIFO Idle Drop Count

The assignment of bits in the Vendor-Specific Rx FIFO Idle Drop Count register is shown in the following table. The counter is incremented once for each idle group that is dropped in the Rx path for clock rate disparity compensation.

Name: Vendor-Specific Rx FIFO Idle Drop Count
Address: 3x800F

Bit	Name	Access	Description	Reset Value
15:0	FIFO_RX _Idle_Drop_Count	COR	FIFO Rx idle group (||I||) drop count.	0x0

2.5.10 Vendor-Specific PCS Tx Sequencing Error Count

The assignment of bits in the Vendor-Specific PCS Tx Sequencing Error Count register is shown in the following table. The counter is incremented once for each block sequence error encountered in the Tx path.

Name: Vendor-Specific PCS Tx Sequencing Error Count
Address: 3x8010

Bit	Name	Access	Description	Reset Value
15:0	TX_Sequencing_Error_Count	COR	Tx sequencing error count.	0x0

2.5.11 Vendor-Specific PCS Rx Sequencing Error Count

The assignment of bits in the Vendor-Specific PCS Rx Sequencing Error Count register is shown in the following table. The counter is incremented once for each block sequence error encountered in the Rx path.

Name: Vendor-Specific PCS Rx Sequencing Error Count
Address: 3x8011

Bit	Name	Access	Description	Reset Value
15:0	RX_Sequencing_Error_Count	COR	Rx sequencing error count.	0x0

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2.5.12 Vendor-Specific PCS Tx Block Encode Error Count

The assignment of bits in the Vendor-Specific PCS Tx Block Error Count register is shown in the following table. The counter is incremented once for each block encoding error encountered in the Tx path.

Name: Vendor-Specific PCS Tx Block Encode Error Count
Address: 3x8012

Bit	Name	Access	Description	Reset Value
15:0	TX_Block_Encode_Error_Count	COR	Tx block encode error count.	0x0

2.5.13 Vendor-Specific PCS Rx Block Decode Error Count

The assignment of bits in the Vendor-Specific PCS Rx Block Decode Error Count register is shown in the following table. The counter is incremented once for each block encoding error encountered in the Rx path.

Name: Vendor-Specific PCS Rx Block Decode Error Count
Address: 3x8013

Bit	Name	Access	Description	Reset Value
15:0	RX_Block_Decode_Error_Count	COR	Rx block decode error count.	0x0

2.5.14 Vendor-Specific PCS Tx Character Encode Error Count

The assignment of bits in the Vendor-Specific PCS Tx Character Encode Error Count register is shown in the following table. The counter is incremented once for each character encoding error encountered in the Tx path.

Name: Vendor-Specific PCS Tx Character Encode Error Count
Address: 3x8014

Bit	Name	Access	Description	Reset Value
15:0	TX_Char_Encode_Error_Count	COR	Tx character encode error count.	0x0

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2.5.15 Vendor-Specific PCS Rx Character Decode Error Count

The assignment of bits in the Vendor-Specific PCS Rx Character Decode Error Count register is shown in the following table. The counter is incremented once for each character encoding error encountered in the Rx path.

Name: Vendor-Specific PCS Rx Character Decode Error Count
Address: 3x8015

Bit	Name	Access	Description	Reset Value
15:0	RX_Char_Decode_Error_Count	COR	Rx character decode error count.	0x0

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2.6 PHY XS Registers

2.6.1 PHY XS Control

The assignment of bits in the PHY XS Control register is shown in the following table. The default value for each bit of the PHY XS Control register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: PHY XS Control
Address: 4x0000

Bit	Name	Access	Description	Reset Value
15	Reset	RWSC	Reset. This bit is self-clearing. 0: Normal operation. 1: Soft reset. Resets all MMDs.	0
14	XFI_Equipment_Loopback	RW	XFI equipment loopback—Loopback 2. 0: Disable loopback. 1: Enable loopback.	0
13	Speed_Selection	RO	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
12	Reserved	RO	Reserved.	0
11	Low_Power	RW	Low power. 0: Normal operation. 1: Low Power mode.	0
10:7	Reserved	RO	Reserved.	0x0
6	Speed_Selection	RO	Speed selection. 0: Unspecified. 1: Operation at 10 Gbps and above.	1
5:2	Speed_Selection	RO	Speed selection. 5 4 3 2 1 x x x: Reserved. x 1 x x: Reserved. x x 1 x: Reserved. 0 0 0 1: Reserved. 0 0 0 0: 10 Gbps.	0x0000
1:0	Reserved	RO	Reserved.	0x0

2.6.1.1 Reset

Resetting the VSC8476 can be accomplished by setting bit 15 to a one. This action sets all registers and state machines to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This bit is self-clearing and returns a value of one in bit 15 when a reset is in progress and returns a value of zero otherwise.

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It is not recommended to write to any of the PCS registers during the reset process. The reset process is completed within 0.5 seconds after setting bit 15. During a reset, a PCS responds to reads from the PCS Control 1 register bit 15 and from the PCS Status 2 register bits 15 and 14.

Note: This operation may interrupt data communication.

2.6.1.2 XFI_Equipment_Loopback

The PHY XS is placed in a loopback mode of operation when bit 14 is set to a one. When bit 14 is set to a one, the PHY XS accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other loopbacks. When bit 14 is set to a zero, the loopback function is disabled. For more information, see "Loopback 2," page 48.

2.6.1.3 Low_Power

When this bit is set to one, the PHY XS goes into low-power mode.

2.6.1.4 Speed_Selection

Speed selection bits 13 and 6 both be written as a one. Any attempt to change the bits to an invalid setting is ignored. The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in bits 15 through 0 of the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. The PHY XS speed selection defaults to a supported ability.

2.6.2 PHY XS Status 1

The following register contains the PHY XS Status. This register is read only; a write to this register has no effect.

Name: PHY XS Status 1
Address: 4x0001

Bit	Name	Access	Description	Reset Value
15:8	Reserved	RO	Reserved.	0x0
7	Fault	RO	Fault. 0: Fault condition is not detected. 1: Fault condition is detected.	0
6:3	Reserved	RO	Reserved.	0x0
2	PHY_XS_Transmit_Link_Status	RO/LL	PHY XS transmit link status. 0: PHY XS transmit link is down. 1: PHY XS transmit link is up.	1
1	Low_Power_Ability	RO	Low power ability. 0: PHY XS does not support low-power mode. 1: PHY XS supports low-power mode.	1
0	Reserved	RO	Reserved.	0

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2.6.2.1 Fault

When read as a one, bit 7 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 7 indicates that the PHY XS has not detected a fault condition. For 10 Gbps operation, bit 7 is set to a one when either of the fault bits 11 or 10 located in register 4x0008 are set to one.

2.6.2.2 PHY_XS_Transmit_Link_Status

When read as 1, bit 2 indicates that the PHY XS link is aligned. When read as zero, bit 2 indicates that the PHY XS transmit link is not aligned.

2.6.2.3 Low_Power_Ability

The PHY XS supports the low-power feature.

2.6.3 PHY XS Identifier

The following two registers provide a 32-bit value, which constitute an unique identifier for a particular type of PHY XS. A PHY XS may return a value of zero in each of the 32 bits of the device identifier.

The following registers contain a unique identifier for a particular type of PHY XS.

Name: PHY XS Identifier 1
Address: 4x0002

Bit	Name	Access	Description	Reset Value
15:0	PHY_XS_Identifier.	RO	PHY XS identifier	0x0007

Name: PHY XS Identifier 2
Address: 4x0003

Bit	Name	Access	Description	Reset Value
15:0	PHY_XS_Identifier.	RO	PHY XS identifier	0x0400

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2.6.4 PHY XS Speed Ability

The following register contains PHY XS speed assignment.

Name: PHY XS Speed Ability
Address: 4x0004

Bit	Name	Access	Description	Reset Value
15:1	Reserved.	RO	Reserved.	0x0
0	10G_Capable	RO	10 Gbps capable. 1: PHY XS is capable of operating at 10 Gbps. 0: PHY XS is incapable of operating at 10 Gbps.	1

2.6.4.1 10G_Capable

Bit 0 indicates that the PHY XS is able to operate at a data rate of 10 Gbps.

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2.6.5 PHY XS Devices in Package 1

The assignment of bits in the Devices in Package registers are shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD was instantiated within the same package as other MMDs whose associated bits were set to one within the Devices in Package registers. The Clause 22 Registers Present bit is used to indicate that Clause 22 functionality was implemented within a Clause 45 electrical interface device. The definition of the term package is vendor-specific and could be a device, module, or other similar entity.

Name: PHY XS Devices in Package 1
Address: 4x0005

Bit	Name	Access	Description	Reset Value
15:6	Reserved	RO	Reserved.	0x0
5	DTE_XS_Present	RO	DTE XS present. 0: DTE XS not present in the package. 1: DTE XS present in the package.	0
4	PHY_XS_Present	RO	PHY XS present. 0: PHY XS not present in the package. 1: PHY XS is present in the package.	1: XFI to XAUI mode 0: Other modes
3	PCS_Present	RO	PCS present. 0: PCS not present in the package. 1: PCS is present in the package.	1
2	WIS_Present	RO	WIS present. 0: WIS not present in the package. 1: WIS is present in the package.	0
1	PMA_Present	RO	PMA present. 0: PMA not present in the package. 1: PMA is present in the package.	1
0	Clause_22_Registers_Present	RO	Clause 22 registers present 1: Clause 22 registers are present in the package 0: Clause 22 registers are not present in the package	0

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2.6.6 PHY XS Devices in Package 2

The assignment of bits in the Devices in Package registers are shown in the following table. When read as a one, a bit in the Devices in Package registers indicates that the associated MMD was instantiated within the same package as other MMDs whose associated bits are set to one in the Devices in Package registers.

Name: PHY XS Devices in Package 2
Address: 4x0006

Bit	Name	Access	Description	Reset Value
15	VS_Device2_Present	RO	Vendor-specific device 2 present. 0: Vendor-specific device 2 is not present in the package 1: Vendor-specific device 2 is present in the package	0
14	VS_Device1_Present	RO	Vendor-specific device 1 present. 0: Vendor-specific device 1 is not present in package 1: Vendor-specific device 1 is present in package	0
13:0	Reserved	RO	Reserved.	0x0

2.6.7 PHY XS Status 2

The assignment of bits in the PHY XS Status 2 register is shown in the following table. All the bits in this register are read only; a write to this register has no effect.

Name: PHY XS Status 2
Address: 4x0008

Bit	Name	Access	Description	Reset Value
15:14	Devices_Present	RO	Devices present. 15 14 1 0: Device is responding at this address. 1 1: No device is responding at this address. 0 1: No device is responding at this address. 0 0: No device is responding at this address.	0x0
13:12	Reserved	RO	Reserved.	0x0
11	Transmit_Fault	RO/LH	Transmit fault (path to PCS). 0: No fault condition is on the transmit path. 1: Fault condition is on the transmit path.	0
10	Receive_Fault	RO/LH	Receive fault (path from PCS). 0: No fault condition is on the receive path. 1: Fault condition is on the receive path.	0
9:0	Reserved	RO	Reserved.	0x0

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2.6.7.1 Devices_Present

When read as 10, bits 15 and 14 indicate that a device is present and responding at this register address. When read as anything other than 10, bits 15 and 14 indicate that no device is present at this register address or that the device is not functioning properly.

2.6.7.2 Transmit_Fault

When read as a one, bit 11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit is implemented with a latching function so that the occurrence of a fault condition on the transmit path causes the transmit fault bit to become set to a one and remain set until it is cleared. The transmit fault bit is cleared each time this register is read using the management interface and by a PHY XS reset. If the transmit fault condition exists at the time the register is read using the management interface, then the transmit fault bit not be cleared to a zero by the read operation.

2.6.7.3 Receive_Fault

When read as a one, bit 10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit is implemented with a latching function so that the occurrence of a fault condition on the receive path causes the receive fault bit to become set to a one and remain set until it is cleared. The receive fault bit is cleared each time this register is read using the management interface and a PHY XS reset. If the receive fault condition exists at the time the register is read using the management interface, then the receive fault bit is not cleared to zero by the read operation.

2.6.8 PHY XS Package ID 1

The assignment of bits for the PHY XS Package ID 1 register is shown in the following table:

Name: PHY XS Package ID 1
Address: 4x000E

Bit	Name	Access	Description	Reset Value
15:0	PHY_XS_PackageID	RO	PHY XS package ID (bits 15:0).	0x0

2.6.9 PHY XS Package ID 2

The assignment of bits for the PHY XS Package ID 2 register is shown in the following table:

Name: PHY XS Package ID 2
Address: 4x000F

Bit	Name	Access	Description	Reset Value
15:0	PHY_XS_PackageID	RO	PHY XS package ID (bits 31:16).	0x0

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2.6.10 10G PHY XGXS Lane Status

The assignment of bits in the 10G PHY XGXS Lane Status register is shown in the following table. All the bits in this register are read only; a write to this register has no effect.

Name: 10G PHY XGXS Lane Status
Address: 4x0018

Bit	Name	Access	Description	Reset Value
15:13	Reserved	RO	Reserved.	0X0
12	XGXS_Lane_Alignment_Status	RO	PHY XGXS lane alignment status. 0: PHY XS transmit lanes are not aligned. 1: PHY XS transmit lanes are aligned.	0
11	PHY_ XGXS_Pattern_Test_Ability	RO	PHY XS pattern testing ability. 0: PHY XS is not able to generate test patterns. 1: PHY XS is able to generate test patterns.	1
10	PHY_XGXS_Loopback_Ability	RO	PHY XS loopback ability. 0: PHY XS does not have the ability to perform loopback. 1: PHY XS has the ability to perform loopback .	1
9:4	Reserved	RO	Reserved.	0X0
3	XGXS_Lane3_Synch_Status.	RO	XGXS lane 3 synchronization status. 0: Lane 3 is not synchronized. 1: Lane 3 is synchronized. **Note**: When regisrer address 4x800F bit 10 is set to 1 (XAUI Rx lane swap), the synchronization status is for lane 0.	0
2	XGXS_Lane2_Synch_Status	RO	XGXS lane 2 synchronization status. 0: Lane 2 is not synchronized. 1: Lane 2 is synchronized.	0
1	XGXS_Lane1_Synch_Status	RO	XGXS lane 1 synchronization status. 0: Lane 1 is not synchronized. 1: Lane 1 is synchronized.	0
0	XGXS_Lane0_Synch_Status	RO	XGXS lane 0 synchronization status. 0: Lane 0 is not synchronized. 1: Lane 0 is synchronized.	0

2.6.10.1 PHY_XS_Lane_Alignment_Status

When read as a one, bit 12 indicates that the PHY XS has synchronized and aligned all four transmit lanes. When read as a zero, bit 12 indicates that the PHY XS has not synchronized and aligned all four transmit lanes.

2.6.10.2 PHY_XS_Pattern Test_Ability

The PHY XS is able to generate test patterns. The test pattern controls are located in register 4x0019.

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2.6.10.3 PHY_XS_Loopback_Ability

The PHY XS is able to perform a loopback function. The loopback control bit is located in the PHY XS Control 1 register.

2.6.10.4 XGXS_Lane3_Sync_Status

When read as a one, bit 3 indicates that the 10 G PHY XGXS receive lane 3 is synchronized. When read as a zero, bit 3 indicates that the 10 G PHY XGXS receive lane 3 is not synchronized.

2.6.10.5 XGXS_Lane2_Sync_Status

When read as a one, bit 2 indicates that the 10 G PHY XGXS receive lane 2 is synchronized. When read as a zero, bit 2 indicates that the 10 G PHY XGXS receive lane 2 is not synchronized.

2.6.10.6 XGXS_Lane1_Sync_Status

When read as a one, bit 1 indicates that the 10 G PHY XGXS receive lane 1 is synchronized. When read as a zero, bit 1 indicates that the 10 G PHY XGXS receive lane 1 is not synchronized.

2.6.10.7 XGXS_Lane0_Sync_Status

When read as a one, bit 0 indicates that the 10 G PHY XGXS receive lane 0 is synchronized. When read as a zero, bit 0 indicates that the 10 G PHY XGXS receive lane 0 is not synchronized.

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2.6.11 10G PHY XS Test Control

The assignment of bits in the 10G PHY XS Test Control register is shown in the following table. The default value for each bit in this register is chosen so that the initial state of the device at power up or reset is a normal operational state without requiring management intervention.

Name: 10G PHY XS Test Control
Address: 4x0019

Bit	Name	Access	Description	Reset Value
15:3	Reserved	RO	Reserved.	0x0
2	Test_Pattern_Check_Enable	RW	Test pattern check enable. 0: Receive test pattern checking is not enabled. 1: Receive test pattern checking is enabled.	0
1:0	Test_Pattern_Select	RW	Test pattern select. When register 4x8000, bit 3 = 0, then 1 0 1 1: Reserved 1 0: Mixed frequency test pattern 0 1: Low frequency test pattern 0 0: High frequency test pattern When register 4x8000, bit 3 = 1, then 1 0 1 1: Reserved 1 0: Fibre Channel CJPAT 0 1: Continuous jitter test pattern (CJPAT) 0 0: Continuous random test pattern (CRPAT)	0x0

2.6.11.1 Test_Pattern_Check_Enable

When set to one, test pattern checking is enabled on the receive path. When set to zero, test pattern checking is disabled.

2.6.11.2 Test_Pattern_Select

The test pattern to be used when pattern testing is enabled is selected by using bits 1 and 0 in conjunction with register 4x8000 bit 3. When bit 3 of register 4x8000 is zero, the mixed frequency test pattern, low frequency test pattern, and high-frequency test pattern are selected by setting the Test_Pattern_Select bits to 10, 01, and 00 respectively. When bit 3 of register 4x8000 is one, the Fibre Channel CJPAT, CJPAT, and CRPAT are selected by setting the Test_Pattern_Select bits to 10, 01, and 00 respectively.

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2.7 Vendor-Specific Registers for PHY XS

2.7.1 Vendor-Specific Test Control

The assignment of bits in the Vendor-Specific Test Control register is shown in the following table. The default value for each bit of the vendor-specific register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention

Name: Vendor-Specific Test Control
Address: 4x8000

Bit	Name	Access	Description	Reset Value
15:4	Reserved	RW	Reserved.	0x0
3	Test_Pattern_Check_Select	RW	Test pattern check select. Use with register 4x0019 bits 1:0.	0
2:0	Test_Pattern_Generator	RW	Test pattern generator. 2 1 0 1 1 1: Reserved 1 1 0: Fibre channel CJPAT 1 0 1: Continuous jitter test pattern 1 0 0: Continuous random test pattern 0 1 1: Disable pattern generation 0 1 0: Mixed frequency test pattern 0 0 1: Low-frequency test pattern 0 0 0: High-frequency test pattern	0x011

2.7.1.1 Test_Pattern_Check_Select

This bit when set to one enable the test pattern check function. This bit is used with register 4x0019 bit 1 and bit 0 to select the test pattern used by the test pattern checker. For more information, see "Test_Pattern_Select," page 132.

2.7.1.2 Test_Pattern_Generation

These bits select the test pattern being generated for testing.

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2.7.2 Vendor-Specific Test Pattern Check Status

The assignment of bits in the Vendor-Specific Test Pattern Check Status register is shown in the following table:

Name: Vendor-Specific Test Pattern Check Status
Address: 4x8001

Bit	Name	Access	Description	Reset Value
15:4	Reserved	RW	Reserved.	0x0
3	Check_Status_Lane3	RO	Lane 3 check status. 0: Lane 3 pattern check fail. 1: Lane 3 pattern check pass.	0
2	Check_Status_Lane2	RO	Lane 2 check status. 0: Lane 2 pattern check fail. 1: Lane 2 pattern check pass.	0
1	Check_Status_Lane1	RO	Lane 1 check status. 0: Lane 1 pattern check fail. 1: Lane 1 pattern check pass.	0
0	Check_Status_Lane0	RO	Lane 0 check status. 0: Lane 0 pattern check fail. 1: Lane 0 pattern check pass.	0

2.7.2.1 Check_Status_Lane

Status of test pattern check pass or failure for lanes 0 through 3.

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2.7.3 Vendor-Specific Code Group Error Counter Control

The assignment of bits in the Vendor-Specific Code Group Error Counter Control register is shown in the following table. The default value for each bit of the Vendor-Specific Code Group Error Control register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Test Pattern Check
Address: 4x8002

Bit	Name	Access	Description	Reset Value
15:5	Reserved	RW	Reserved.	0x0
4	Error_Counter_Clear	RW	Clear code group error counter. 0: Normal operation 1: Clear counter	0
3	Error_Counter_Enable	RW	Code group error counter enable. 0: Error counter disabled 1: Error counter enabled	1
2:0	Code_Group_Error_Count_Select	RW	Code group error count select. 2 1 0 1 1 1: Reserved 1 1 0: Reserved 1 0 1: Reserved 1 0 0: Cumulative error count on all lanes 0 1 1: Error count on lane 3 0 1 0: Error count on lane 2 0 0 1: Error count on lane 1 0 0 0: Error count on lane 0	0x100

2.7.3.1 Error_Counter_Clear

When set to one clear invalid code group error counter.

2.7.3.2 Error_Counter_Enable

When set to one enable invalid code group error counter.

2.7.3.3 Code_Group_Error_Count_Select

Select invalid code group error counter.

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2.7.4 Vendor-Specific Code Group Error Counter

The assignment of bits in the Vendor-Specific Code Group Error Counter registers (4x8003 to 4x8004) is shown in the following table:

Name: Vendor-Specific Test Pattern Check
Address: 4x8003
4x8004

Bit	Name	Access	Description	Reset Value
15:0	Code_Group_Error_Counter	RW	Code group error counter. Address 4x8003: Bits 15:0 Address 4x8004: Bits 31:16	0x0

2.7.4.1 Code_Group_Error_Counter

This is a 32-bit binary counter that counts code group errors and reports them through the MDIO using two 16-bit registers.

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2.7.5 Vendor-Specific Running Disparity Error Counter Control

The assignment of bits in the Vendor-Specific Running Disparity Error Counter Control register is shown in the following table. The default value for each bit of the Vendor-Specific Running Disparity Error Counter Control register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Running Disparity Error Counter Control
Address: 4x8005

Bit	Name	Access	Description	Reset Value
15:5	Reserved	RW	Reserved	0x0
4	Error_Counter_Clear	RW	Running disparity error counter clear. 0: Normal operation 1: Clear counter	0
3	Error_Counter_Enable	RW	Running disparity error counter enable 0: Error counter is disabled. 1: Error counter is enabled.	1
2:0	Error_Count_Select	RW	Running disparity error count select 2 1 0 1 1 1: Reserved 1 1 0: Reserved 1 0 1: Reserved 1 0 0: Cumulative error count on all lanes 0 1 1: Error count on lane 3 0 1 0: Error count on lane 2 0 0 1: Error count on lane 1 0 0 0: Error count on lane 0	0x100

2.7.5.1 Error_Counter_Clear

When set to one clear code group running disparity error counter.

2.7.5.2 Error_Counter_Enable

When set to one enable code group running disparity error counter.

2.7.5.3 Error_Count_Select

These bits select the code group running the disparity error count.

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2.7.6 Vendor-Specific Running Disparity Error Counter

The assignment of bits in the Vendor-Specific Running Disparity Error Counter registers (4x8006 to 4x8007) is shown in the following table:

Name: Vendor-Specific Running Disparity Error Counter
Address: 4x8006
4x8007

Bit	Name	Access	Description	Reset Value
15:0	Running_Disparity_Error_Counter	RW	Running disparity error counter. Address 4x8006: Bits 15:0 Address 4x8007: Bits 31:16	0x0

2.7.6.1 Running_Disparity_Error_Counter

This is a 32-bit binary counter that counts running disparity errors and reports them through the MDIO using two 16-bit registers.

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2.7.7 Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter Control

The assignment of bits in the Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter Control register is shown in the following table. The default value for each bit of this register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific PHY XGXS Elastic FIFO Over/Under Error Counter Control
Address: 4x8008

Bit	Name	Access	Description	Reset Value
15:5	Reserved	RW	Reserved.	0x0
4	Error_Counter_Clear	RW	PHY XGXS elastic FIFO over and under error counter clear. 0: Normal operation. 1: Clear counter.	0
3	Error_Counter_Enable	RW	FIFO over and under error counter enable. 0: Error counter is disabled. 1: Error counter is enabled.	1
2:0	Error_Count_Select	RW	FIFO over and under error count select. 2 1 0 1 1 1: Reserved 1 1 0: Reserved 1 0 1: Reserved 1 0 0: Cumulative error count on all lanes 0 1 1: Error count on lane 3 0 1 0: Error count on lane 2 0 0 1: Error count on lane 1 0 0 0: Error count on lane 0	0x100

2.7.7.1 Error_Counter_Clear

When set to one, this clears the PHY XGXS elastic FIFO over and under error counter.

2.7.7.2 Error_Counter_Enable

When set to one, this enables the PHY XGXS elastic FIFO over and under error counter.

2.7.7.3 Error_Count_Select

These bits select the PHY XGXS elastic FIFO over and under error count.

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2.7.8 Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter

The assignment of bits in the Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter registers (4x8009 to 4x800A) is shown in the following table.

Name: Vendor-Specific PHY XGXS Elastic FIFO Over and Under Error Counter
Address: 4x8009
4x800A

Bit	Name	Access	Description	Reset Value
15:0	FIFO_Over_Under_Error_Counter	RW	PHY XGXS elastic FIFO over and under error counter. Address 4x8009: Bits 15:0 Address 4x800A: Bits 31:16	0x0

2.7.8.1 FIFO_Over_Under_Error_Counter

This is a 32-bit binary counter that counts the PHY XS elastic errors and reports them through the MDIO using two 16-bit registers.

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2.7.9 Vendor-Specific Test Pattern Mismatch Error Counter Control

The assignment of bits in the Vendor-Specific Test Pattern Mismatch Error Counter Control register is shown in the following table. The default value for each bit of the Vendor-Specific Test Pattern Mismatch Error Counter Control register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Test Pattern Mismatch Error Counter Control
Address: 4x800B

Bit	Name	Access	Description	Reset Value
15:5	Reserved	RW	Reserved.	0x0
4	Error_Counter_Clear	RW	Test pattern mismatch error counter clear. 0: Normal operation. 1: Clear counter.	0
3	Error_Counter_Enable	RW	Test pattern mismatcherror counter enable. 0: Error counter is disabled. 1: Error counter is enabled.	1
2:0	Error_Count_Select	RW	Test pattern mismatch error count select. 2 1 0 1 1 1: Reserved 1 1 0: Reserved 1 0 1: Reserved 1 0 0: Cumulative error count on all lanes 0 1 1: Error count on lane 3 0 1 0: Error count on lane 2 0 0 1: Error count on lane 1 0 0 0: Error count on lane 0	0x100

2.7.9.1 Error_Counter_Clear

When set to one, this clears the test pattern mismatch error counter.

2.7.9.2 Error_Counter_Enable

When set to one, this enables test pattern mismatch error counter.

2.7.9.3 Error_Count_Select

These bits select select the test pattern mismatch error count.

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2.7.10 Vendor-Specific Test Pattern Mismatch Error Counter

The assignment of bits in the Vendor-Specific Test Pattern Mismatch Error Counter registers (4x800C to 4x800D) is shown in the following table.

Name: Vendor-Specific Test Pattern Mismatch Error Counter
Address: 4x800C
4x800D

Bit	Name	Access	Description	Reset Value
15:0	Test_Pattern_Mismatch_Error	RW	Test pattern mismatch errors. Address 4x800C: Bits 15:0 Address 4x800D: Bits 31:16	0x0

2.7.10.1 Test_Pattern_Mismatch_Error

This is a 32-bit binary counter that counts the test pattern mismatch errors and reports them through the MDIO using two 16-bit registers.

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2.7.11 Vendor-Specific SerDes

The assignment of bits in the Vendor-Specific Serializer Deserializer register is shown in the following table. The default value for each bit of the Vendor-Specific SerDes register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific SerDes
Address: 4x800E

Bit	Name	Access	Description	Reset Value
15:14	Reserved	RO	Reserved.	0x0
13	XAUI_Facility_Loopback	RW	XAUI facility loopback. Loopback 1. 0: Disable loopback. 1: Enable loopback.	0
12	FIFORSTN	RWCOR	FIFORSTN. 0: Normal operation. 1: Resets FIFOs in XAUI serializer.	1
11	Reserved	RW	Reserved.	1
10	Reserved	RW	Reserved.	0
9	Reserved	RW	Reserved.	0
8	Squelch_Data_Lane0	RW	Lane 0 data squelch. 0: Normal operation. 1: Force lane 0 data to zero.	0
7	Squelch_Data_Lane1	RW	Lane 1 data squelch. 0: Normal operation. 1: Force lane 1 data to zero.	0
6	Squelch_Data_Lane2	RW	Lane 2 data squelch. 0: Normal operation. 1: Force lane 2 data to zero.	0
5	Squelch_Data_Lane3	RW	Lane 3 data squelch. 0: Normal operation. 1: Force lane 3 data to zero.	0
4	Read_Write_Default_Value	RWDV	Read/write default value for normal operation.	0
3	Read_Write_Default_Value	RWDV	Read/write default value for normal operation.	0
2	Read_Write_Default_Value	RWDV	Read/write default value for normal operation.	0
1	Read_Write_Default_Value	RWDV	Read/write default value for normal operation.	0
0	Read_Write_Default_Value	RWDV	Read/write default value for normal operation.	0

2.7.11.1 XAUI_Facility_Loopback

This bit enables the XAUI input to XAUI output loopback when set to one.

2.7.11.2 FIFORSTN

This bit resets the FIFOs in the XAUI serializer when set to zero.

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2.7.11.3 Squelch_Data

This bit forces the XAUI data output to zero.

2.7.11.4 Read_Write_Default_Value

These bits contain the read/write default values for normal operation.

2.7.12 Vendor-Specific Loopback Control

The assignment of bits in the Vendor-Specific Loop register is shown in the following table. The default value for each bit of the Vendor-Specific Loop register has been chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific Loopback Control
Address: 4x800F

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RW	Reserved.	0x0
10	XAUI_RX_Lane_Swap	RW	XAUI Rx lane swap. 0: Enable 1: Disable	1
9	XAUI_TX_Lane_Swap	RW	XAUI Tx lane swap. 0: Enable 1: Disable	1
8	Reserved	RWDV	Reserved.	0
7	Reserved	RWDV	Reserved.	0
6	XAUI_RX_Data_Invert	RW	XAUI Rx data invert. 0: Enable 1: Disable	1
5	XAUI_TX_Data_Invert	RW	XAUI Tx data invert. 0: Enable 1: Disable	1
4:3	Reserved	RWDV	Reserved.	0x0
2	Reserved	RWDV	Reserved.	0
1	XGMII_Loopback_Enable	RW	XGMII interface loopback 3. 0: Disable 1: Enable	0
0	Reserved	RWDV	Reserved.	0

2.7.12.1 XAUI_RX_Lane_Swap

Swaps lane 0 with lane 3, and swaps lane 1 with lane 2.

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2.7.12.2 XAUI_TX_Lane_Swap

Swaps TXT ± [3] with TXT ± [0] and TXT ± [1] with TXT ± [2] .

2.7.12.3 XAUI_RX_Data_Invert

Inverts XRX + [0:3] with XRX – [0:3].

2.7.12.4 XAUI_TX_Data_Invert

Inverts TXT + [0:3] with TXT – [0:3].

2.7.12.5 XAUI_Loopback_Enable

Enable XGMII looback function.

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2.7.13 Vendor-Specific XAUI Input Equalization Control

The following table shows the equalization setting bits for each XAUI lane. The default value for each XAUI lane input equalization is disabled, which is the minimum setting. This default is chosen so that the initial value is for normal operation without requiring management intervention. The equalization settings for each XAUI input use 4 bits total. The two most significant bits set the receiver peaking ratio, and the two least significant bits set the decay time.

As a general guideline, minimum peaking and decay are recommended for the shortest (up to 4 inches) XAUI transmission lines, while maximum settings should be used for backplane applications where XAUI tracks may approach 1 meter or approximately 39 inches. Since the decay command 00 sets them to disabled, only 3 decay settings apply for each peaking setting: 01, 10, and 11. This limits the available overall equalization settings for each XAUI receiver to 12, excluding default disable. Peaking ratios are approximately 0 to approximately 6 dB, and the decay time range is approximately 0.1 to 1.9 UI.

Note that the settings vary with trace length and loss characteristics of the transmission material. It is recommended to experiment with these settings to obtain optimum performance.

Name: Vendor-Specific XAUI Input Equalization Control
Address: 4x8010

Bit	Name	Access	Description	Reset Value
15:12	Equalization_Control	RW	Set equalization for XAUI input of lane 0.	0x0
11:8	Equalization_Control	RW	Set equalization for XAUI input of lane 1.	0x0
7:4	Equalization_Control	RW	Set equalization for XAUI input of lane 2.	0x0
3:0	Equalization_Control	RW	Set equalization for XAUI input of lane 3.	0x0

2.7.13.1 Equalization_Control

These bits set the equalization for XAUI input for the specific lane. Equalization should be increased by writing a larger value per lane for longer trance lengths.

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2.7.14 Vendor-Specific XAUI Output Pre-Emphasis Control and LOS

The following table shows the pre-emphasis setting bits for each XAUI lane. The default value for each XAUI lane input equalization is pre-emphasis disabled. This default is chosen so that the initial value is normal operation without requiring management intervention. The most significant bit disables pre-emphasis, which is the default state. There are four available pre-emphasis settings.

As a general guideline, the shortest XAUI transmission lines (up to 3 inches) should use a minimum peaking setting (100) or none at all, while longer XAUI tracks may benefit from a maximum pre-emphasis setting (111). The peaking range is approximately 0 to 4 dB, and associated decay times range from approximately 0.1 to 1.7 UI.

Name: Vendor-Specific XAUI Output Pre-Emphasis Control
Address: 4x8011

Bit	Name	Access	Description	Reset Value
15:13	Pre-Emphasis_Lane0	RW	Set pre-emphasis for XAUI output of lane 0.	0x0
12:10	Pre-Emphasis_Lane1	RW	Set pre-emphasis for XAUI output of lane 1.	0x0
9:7	Pre-Emphasis_Lane2	RW	Set pre-emphasis for XAUI output of lane 2.	0x0
6:4	Pre-Emphasis_Lane3	RW	Set pre-emphasis for XAUI output of lane 3.	0x0
3:2	LOS_Threshold	RW	Set LOS threshold.	0x0
1	High_Swing	RW	Enable high swing mode.	0
0	Reserved	RW	Reserved.	0

2.7.14.1 Pre-Emphasis_Lane

These bits set the pre-emphasis level for the selected transmit lane.

2.7.14.2 LOS_Threshold

These bits set LOS threshold.

The following table provides the signal detection levels for the MDIO register bit 3 and bit 2:

Table 17. Signal Detection Levels

MDIO Register 4x8011 Bits 3:2	Lower Threshold	Upper Threshold	Unit	Comments
00	X	X	mV	Disabled, output set low
01	30	140	mV	Differential, p-p[1]
10	120	200	mV	Differential, p-p
11	190	300	mV	Differential, p-p

1. Peak-to-peak differential swing with each polarity driven with half the stated number.

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2.7.14.3 High_Swing

This bit is set to 1 to enable high swing mode on the XAUI output driver.

2.7.15 Vendor-Specific I/O 2

The assignment of bits in the Vendor-Specific I/O 2 register is shown in the following table. The default value for each bit of the Vendor-Specific I/O 2 register is chosen so that the initial state of the device at power up or completion of reset is a normal operational state without requiring management intervention.

Name: Vendor-Specific I/O 2
Address: 4x8012

Bit	Name	Access	Description	Reset Value
15:13	Reserved	RW	Reserved.	0x0
3	LOS	RO	Lane 3 XAUI input LOS status. 0: Signal present. 1: Loss of signal.	0
2	LOS	RO	Lane 2 XAUI input LOS status. 0: Signal present. 1: Loss of signal.	0
1	LOS	RO	Lane 1 XAUI input LOS status. 0: Signal present. 1: Loss of signal.	0
0	LOS	RO	Lane 0 XAUI input LOS status. 0: Signal present. 1: Loss of signal.	0

2.7.15.1 LOS

LOS status for each XAUI lane.

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2.8 Optical Module Data - NVR and DOM

The following registers are vendor-specific registers for the two-wire serial interface.

2.8.1 Vendor-Specific NVR Control Command Status

The Vendor-Specific NVR Control Command Status register provides facilities to read and write non-volatile memory for the XENPAK registers.

Name: Vendor-Specific NVR Control Command Status
Address: 30x8000

Bit	Name	Access	Description	Reset Value
15:9	Reserved	RW	Reserved.	0x0
8	Module_Working_Mode	RW	Two-wire serial interface module working mode. 0: Automatic mode. 1: Manual mode.	0
7:6	Reserved	RO	Reserved.	0x0
5	Command	RW	Command. 0: Read NVR. 1: Write NVR.	0
4	Reserved	RO	Reserved.	0
3:2	Command_Status	RO/LH	Command status. 00: Idle. 01: Command completed successfully. 10: Command in progress. 11: Command failed. **Note**: These bits clear on read, but if a condition persists, the bit does not clear.	0x0
1:0	Extended_Command	RW	Extended command. 00: Basic for XENPAK, bytes 2-57 for XFP. 01: Custom for XENPAK, bytes 72-111 for XFP. 10: Vendor for XENPAK, lower 128 bytes for XFP. 11: All NVR for XENPAK, upper 128 bytes for XFP.	0x0

2.8.1.1 Command

A zero written to this bit initiates an NVR read. A one written to this bit initiates an NVR write. The Extended Command bits determine the exact nature of the read/write operation. Inclusion of this function permits implementations that maintain non-volatile storage in an independent location. The read function pulls the NVR contents out of non-volatile storage and stores it in register addresses 30x8007 to 30x8106. Reads to this register after a command is completed reset the command status to 00 (idle). Read does not clear the command status. The write function commits the contents of the NVRs to the external non-volatile storage. Writes to this register are ignored while a command is in progress.

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2.8.1.2 Module_Working_Mode

This bit sets the two-wire serial interface operational mode.

2.8.1.3 Command_Status

Following a write command, bits 3 and 2 provide information on the status of the command. A value of 00 indicates an idle condition, 10 indicates that a command is in progress, 01 indicates that the command completed successfully, and 11 indicates that the command failed. The value of this bit is held until a command is exercised.

2.8.1.4 Extended_Command

Bits 1 and 0 supplement the basic read/write command (bit 5). A value of 11 reads and writes all NVR contents. The value of this bit is held until a command is exercised. All other values implement vendor-specific commands.

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2.8.2 STW Instruction

The assignment of bits in the STW Instruction register is shown in the following table.

Name: STW Instruction
Address: 30x8001

Bit	Name	Access	Description	Reset Value
15:10	Reserved	RW	Reserved.	0x0
8	Module_Working_Mode	RW	Read STW Slave Device Adress register (30x8002) to the controller's internal register. 0: Do not read register 30x8002. 1: Read register 30x8002. **Note**: Writes to this register are ignored during an instruction in progress. Read does not clear the instruction status.	0
7:6	Instruction_Status	RO/LH	Instruction status. Reads to this register after instruction complete resets the instruction status to 00 (idle). 00: Idle. 01: Instruction completed successfully. 10: Instruction in progress. 11: Instruction failed. **Note**: These bits clear on read. However, if a condition exists following a register read, the bit does not clear.	0x0
5	Soft_Reset_Slave_Transceiver	RW	Soft reset slave transceiver. 0: Normal mode. 1: Reset slave transceiver.	0
4	Reserved	RO	Reserved	0
3	Action	RW	Action. 0: Read. 1: Write.	0
2	Acknowledge	RW	Acknowledge. 0: Read/write without acknowledge. 1: Read/write with acknowledge.	0
1	Stop	RW	Stop. 0: Read/write without stop condition. 1: Read/write with stop condition.	0
0	Start	RW	Start. 0: Read/write without start condition. 1: Read/write with start condition.	0

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2.8.3 Slave Device Address

The assignment of bits in the Slave Device Address register is shown in the following table.

Name: Slave Device Address
Address: 30x8002

Bit	Name	Access	Description	Reset Value
15:0	STW_Slave_Address_Storage	RW	STW slave device address storage	0x0000

2.8.4 STW Register Address

The assignment of bits in the STW Register Address register is shown in the following table.

Name: STW Register Address
Address: 30x8003

Bit	Name	Access	Description	Reset Value
15:0	STW_Register_Address_Storage	RW	STW register address storage	0x0000

2.8.5 Configuration

The assignment of bits in the Configuration register is shown in the following table.

Name: Configuration
Address: 30x8004

Bit	Name	Access	Description	Reset Value
15:13	Reserved	RW	Reserved.	0x0
12	MSA_Compliance	RW	MSA-compliance. 0: XENPAK. 1: XFP.	0
11	STW_Addressing	RW	STW addressing. 0: Uses 7-bit address. 1: Uses 10-bit address	0
10:9	STW_Mode	RW	STW mode. 00: Standard mode. 01: Fast mode. 10: High-Speed mode. 11: Reserved.	0x0
8:0	Reserved	RW	Reserved.	0x0

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2.8.6 Optical Module Data Memory Registers

The following registers (30x8005 to 30x8006) are for the vendor-specific non-volatile memory area.

Name: Optical Module Data Memory
Address: 30x8005
30x8006

Bit	Name	Access	Description	Reset Value
15:0	Non_Volatile_Memory	RW	Vendor-specific non-volatile memory	0x0000

2.8.7 Optical Module Data Version Number

The following register contains optical module data version number.

Name: Optical Module Data Version Number
Address: 30x8007

Bit	Name	Access	Description	Reset Value
7:0	Version	RW	XENPAK NVR version number	0x0000

2.8.8 Non-Volatile Register Size

The following registers contain the total size of the non-volatile register, between 84766 and 2048 bytes.

Name: Non-Volatile Register Size
Address: 30x8008
30x8009

Bit	Name	Access	Description	Reset Value
7:0	NVR_Size	RW	Size of NVR	0x0000

2.8.9 Memory Used

The following registers contain the number of bytes used in the NVR including vendor-specific bytes. For the purposes of calculating this field it is assumed that all customer writable bytes are in use.

Name: Memory Used
Address: 30x800A
30x800B

Bit	Name	Access	Description	Reset Value
7:0	Memory_Used	RW	Memory used	0x0000

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2.8.10 Vendor-Specific Basic Address

The following register contains the Basic NVR starting address.

Name: Vendor-Specific Basic Address
Address: 30x800C

Bit	Name	Access	Description	Reset Value
7:0	Basic_Address	R	Basic address. Starting NVR address.	0x0000

2.8.11 Vendor-Specific Customer Address

The following register contains the Customer NVR starting address.

Name: Vendor-Specific Customer Address
Address: 30x800D

Bit	Name	Access	Description	Reset Value
7:0	Customer_Address	R	Customer address. Starting NVR address.	0x0000

2.8.12 Vendor Address

The following register contains the vendor-specific NVR starting address.

Name: Vendor-Specific Vendor Address
Address: 30x800E

Bit	Name	Access	Description	Reset Value
7:0	Vendor_Address	R	Vendor address. Starting NVR address.	0x0000

2.8.13 Extended Vendor Address

The following registers contain the Extended Vendor-Specific NVR starting address.

Name: Vendor-Specific Extended Vendor Address
Address: 30x800F
30x8010

Bit	Name	Access	Description	Reset Value
7:0	Extended_Vendor_Address	R	Extended vendor address. Starting NVR address.	0x0000

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2.8.14 Transceiver Type

The following register contains the transceiver type.

Name: Vendor-Specific Transceiver Type
Address: 30x8012

Bit	Name	Access	Description	Reset Value
7:1	Reserved	RW	Reserved.	0x0
0	Transceiver_Type	RW	Transceiver type. 0: Unspecified 1: XENPAK	0

2.8.15 Connector Type

The following register contains the connector type.

Name: Vendor-Specific Connector Type
Address: 30x8013

Bit	Name	Access	Description	Reset Value
7:6	Reserved	RW	Reserved.	0x0
5:0	Connector_Type	R	Connector type. 0x: Unspecified 1x: SC duplex 2x: LC 4x: MT-RJ 8x: MU 10x: FC/RC 20x: Pigtail	0x0

2.8.16 Bit Encoding

The following register contains the bit encoding method.

Name: Vendor-Specific Bit Encoding
Address: 30x8014

Bit	Name	Access	Description	Reset Value
7:2	Reserved	RW	Reserved.	0x0
1:0	Bit_Encoding	R	Bit encoding. 0: Unspecified 1: NRZ 2: FEC	0x0

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2.8.17 Bit Rate

The following registers (30x8015 and 30x8016) contain the nominal bit rate in multiples of 1 Mbps. A value of zero indicates that the value is unspecified.

Name: Vendor-Specific Bit Rate 1
Address: 30x8015

Bit	Name	Access	Description	Reset Value
7:0	Bit_Rate	RW	Bit rate. 80x: Bit 15 (MSB) 40x: Bit 14 20x: Bit 13 10x: Bit 12 8x: Bit 11 4x: Bit 10 2x: Bit 9 1x: Bit 8 0x: Unspecified	0x0

Name: Vendor-Specific Bit Rate 2
Address: 30x8016

Bit	Name	Access	Description	Reset Value
7:0	Bit_Rate	RW	Bit rate. 80x: Bit 7 40x: Bit 6 20x: Bit 5 10x: Bit 4 8x: Bit 3 4x: Bit 2 2x: Bit 1 1x: Bit 0 0x: Unspecified	0x0

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2.8.18 Protocol Type

The following register contains the protocol type. The protocol type may be indicated in this field or must be inferred from the Standards Compliance Codes.

Name: Vendor-Specific Protocol Type
Address: 30x8017

Bit	Name	Access	Description	Reset Value
7:5	Reserved	RW	Reserved.	0x0
4:0	Protocol_Type	R	Protocol type. 10x: SONET/SDH 8x: LSS 4x: WIS 2x: 10GFC 1x: 10GbE 0x: Unspecified	0x0

2.8.19 Standard Compliance Codes

The following registers (30x8018 to 30x8023) contain the standard compliance codes for recognized industry standards. If this field is left unspecified, the transceiver capability must be inferred from other information contained in the non-volatile RAM (NVR).

Name: Vendor-Specific Standard Compliance Code for 10 GbE (Byte 0)
Address: 30x8018

Bit	Name	Access	Description	Reset Value
7:0	10GbE_Code_Byte0	RW	10 GbE code byte 0. 80x: Reserved 40x: 10GBASE-EW 20x: 10GBASE-LW 10x: 10GBASE-SW 8x: 10GBASE-LX4 4x: 10GBASE-ER 2x: 10GBASE-LR 1x: 10GBASE-SR 0x: Unspecified	0x0

Name: Vendor-Specific Standard Compliance Code for 10 GbE (Byte 1)
Address: 30x8019

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved. 10 GbE code byte 1.	0x0

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2.8.19.1 10GbE_Code_Byte

This is reserved.

Name: Vendor-Specific Standard Compliance Code for SONET/SDH (Byte 0)
Address: 30x801A

Bit	Name	Access	Description	Reset Value
7:0	SONET_SDH_Code_Byte0	RW	SONET/SDH code byte 0. 80x: Reserved 40x: S-64.5b 20x: S-64.5a 10x: S-64.3b 8x: S-64.3a 4x: S-64.2b 2x: S-64.2a 1x: S-64.1 0x: Unspecified	0x0

Name: Vendor-Specific Standard Compliance Code for SONET/SDH (Byte 1)
Address: 30x801B

Bit	Name	Access	Description	Reset Value
7:0	SONET_SDH_Code_Byte1	RW	SONET/SDH code byte 1. 80x: Reserved 40x: Reserved 20x: I-64.5 10x: I-64.3 8x: I-64.2 4x: I-64.2r 2x: I-64.1 1x:I-64.1r 0x: Unspecified	0x0

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Name: Vendor-Specific Standard Compliance Code for SONET/SDH (Byte 2)
Address: 30x801C

Bit	Name	Access	Description	Reset Value
7:0	SONET_SDH_Code_Byte2	RW	SONET/SDH code byte 2. 80x: Reserved 40x: Reserved 20x: Reserved 10x: L-64.3 8x: L-64.2c 4x: L-64.2b 2x: L-64.2a 1x: L-64.1 0x: Unspecified	0x0

Name: Vendor-Specific Standard Compliance Code for SONET/SDH (Byte 3)
Address: 30x801D

Bit	Name	Access	Description	Reset Value
7:0	SONET_SDH_Code_Byte3	RW	SONET/SDH code byte 3. 80x: Reserved 40x: Reserved 20x: Reserved 10x: Reserved 8x: Reserved 4x: V-64.3 2x: V-64.2b 1x: V-64.2a 0x: Unspecified	0x0

Name: Vendor-Specific Standard Compliance Code for 10 GFC (Byte 0)
Address: 30x801E

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved. 10 GFC code byte 0.	0x0

Name: Vendor-Specific Standard Compliance Code for 10 GFC (Byte 1)
Address: 30x801F

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved. 10 GFC code byte 1.	0x0

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Name: Vendor-Specific Standard Compliance Code for 10 GFC (Byte 2)
Address: 30x8020

Bit	Name	Access	Description	Reset Value
70	Reserved	RW	Reserved. 10 GFC code byte 2.	0x0

Name: Vendor-Specific Standard Compliance Code for 10 GFC (Byte 3)
Address: 30x8021

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved. 10 GFC code byte 3.	0x0

Name: Vendor-Specific Standard Compliance Code for Fibre Type (Byte 0)
Address: 30x8024

Bit	Name	Access	Description	Reset Value
7:0	Fibre_Type_Byte0	RW	Fibre type byte 0. 80x: NZDSF only 40x: NDSF only 20x: SM, generic 10x: HPCF 8x: POF 4x: 62.5/125 only 2x: 50/125 only 1x: MM, generic 0x: Unspecified	0x0

Name: Vendor-Specific Standard Compliance Code for Fibre Type (Byte 1)
Address: 30x8025

Bit	Name	Access	Description	Reset Value
7:0	Fibre_Type_Byte1	RW	Fibre type byte 1. 80x: Reserved 40x: Reserved 20x: Reserved 10x: Reserved 8x: Reserved 4x: Reserved 2x: PMF only 1x: Large core only 0x: Unspecified	0x0

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2.8.20 Range

The following registers assign the bits for the Range registers. Range specifies the link length supported by the transceiver in multiples of 10 meters up to a maximum of 655.36 kilometers.

Name: Range (MSB)
Address: 30x8022

Bit	Name	Access	Description	Reset Value
7:0	Link_Length_MSB	RW	Link length supported by the transceiver (MSB)	0x0

Name: Range (LSB)
Address: 30x8023

Bit	Name	Access	Description	Reset Value
7:0	Link_Length_LSB	RW	Link length supported by the transceiver (LSB)	0x0

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2.8.21 Wavelength Channel 0

The following registers (30x8026 to 30x8028) contain the wavelength specification for channel 0. The wavelength is specified in multiples of 0.01 nm. This resolution allows for future dense-wave division multiplexing (DWDM) solutions.

Name: Vendor-Specific Wavelength Channel 0 (Bits 23:16)
Address: 30x8026

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength0_3	RW	Center wavelength for channel 0 bits 23:16. 80x: Bit 23 (MSB) 40x: Bit 22 20x: Bit 21 10x: Bit 20 8x: Bit 19 4x: Bit 18 2x: Bit 17 1x: Bit 16 0x: Unspecified	0x0

Name: Vendor-Specific Wavelength Channel 0 (Bits15:8)
Address: 30x8027

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength0_2	RW	Center wavelength for channel 0 bits 15:8. 80x: Bit 15 40x: Bit 14 20x: Bit 13 10x: Bit 12 8x: Bit 11 4x: Bit 10 2x: Bit 9 1x: Bit 8 0x: Unspecified	0x0

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Name: Vendor-Specific Wavelength Channel 0 (Bits 7:0)
Address: 30x8028

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength0_1	RW	Center wavelength for channel 0 bits 7:0. 80x: Bit 7 40x: Bit 6 20x: Bit 5 10x: Bit 4 8x: Bit 3 4x: Bit 2 2x: Bit 1 1x: Bit 0 0x: Unspecified	0x0

2.8.22 Wavelength Channel 1

The following registers (30x8029 to 30x802B) contain the wavelength specification for channel 1. The wavelength is specified in multiples of 0.01 nm. This resolution allows for future DWDM solutions.

Name: Vendor-Specific Wavelength Channel 1 (Bits 23:16)
Address: 30x8029

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength1_3	RW	Center wavelength for channel 1 bits 23:16. 80x: Bit 23 (MSB) 40x: Bit 22 20x: Bit 21 10x: Bit 20 8x: Bit 19 4x: Bit 18 2x: Bit 17 1x: Bit 16 0x: Unspecified	0x0

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Name: Vendor-Specific Wavelength Channel 1 (Bits 15:8)
Address: 30x802A

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength1_2	RW	Center wavelength for channel 1 bits 15:8. 80x: Bit 15 40x: Bit 14 20x: Bit 13 10x: Bit 12 8x: Bit 11 4x: Bit 10 2x: Bit 9 1x: Bit 8 0x: Unspecified	0x0

Name: Vendor-Specific Wavelength Channel 1 (Bits 7:0)
Address: 30x802B

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength1_1	RW	Center wavelength for channel 1 bits 7:0. 80x: Bit 7 40x: Bit 6 20x: Bit 5 10x: Bit 4 8x: Bit 3 4x: Bit 2 2x: Bit 1 1x: Bit 0 0x: Unspecified	0x0

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2.8.23 Wavelength Channel 2

The following registers (30x802C to 30x802E) contain the wavelength specification for channel 2. The wavelength is specified in multiples of 0.01 nm. This resolution allows for future DWDM solutions.

Name: Vendor-Specific Wavelength Channel 2 (Bits 23:16)
Address: 30x802C

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength2_3	RW	Center wavelength for channel 2 bits 23:16. 80x: Bit 23 (MSB) 40x: Bit 22 20x: Bit 21 10x: Bit 20 8x: Bit 19 4x: Bit 18 2x: Bit 17 1x: Bit 16 0x: Unspecified	0x0

Name: Vendor-Specific Wavelength Channel 2 (Bits 15:8)
Address: 30x802D

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength2_2	RW	Center wavelength for channel 2 bits 15:8. 80x: Bit 15 40x: Bit 14 20x: Bit 13 10x: Bit 12 8x: Bit 11 4x: Bit 10 2x: Bit 9 1x: Bit 8 0x: Unspecified	0x0

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Name: Vendor-Specific Wavelength Channel 2 (Bits 7:0)
Address: 30x802E

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength2_1	RW	Center wavelength for channel 2 bits 7:0. 80x: Bit 7 40x: Bit 6 20x: Bit 5 10x: Bit 4 8x: Bit 3 4x: Bit 2 2x: Bit 1 1x: Bit 0 0x: Unspecified	0x0

2.8.24 Wavelength Channel 3

The following registers (30x802F to 30x8031) contain the wavelength specification for channel 3. The wavelength is specified in multiples of 0.01 nm. This resolution allows for future DWDM solutions.

Name: Vendor-Specific Wavelength Channel 3 (Bits 23:16)
Address: 30x802F

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength3_3	RW	Center wavelength for channel 3 bits 23:16. 80x: Bit 23 (MSB) 40x: Bit 22 20x: Bit 21 10x: Bit 20 8x: Bit 19 4x: Bit 18 2x: Bit 17 1x: Bit 16 0x: Unspecified	0x0

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Name: Vendor-Specific Wavelength Channel 3 (Bits 15:8)
Address: 30x8030

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength3_2	RW	CCenter wavelength for channel 3 bits 15:8. 80x: Bit 15 40x: Bit 14 20x: Bit 13 10x: Bit 12 8x: Bit 11 4x: Bit 10 2x: Bit 9 1x: Bit 8 0x: Unspecified	0x0

Name: Vendor-Specific Wavelength Channel 3 (Bits 7:0)
Address: 30x8031

Bit	Name	Access	Description	Reset Value
7:0	Center_Wavelength3_1	RW	Center wavelength for channel 3 bits 7:0. 80x: Bit 7 40x: Bit 6 20x: Bit 5 10x: Bit 4 8x: Bit 3 4x: Bit 2 2x: Bit 1 1x: Bit 0 0x: Unspecified	0x0

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2.8.25 Package Identifier OUI

The package identifier OUI (organizationally unique identifier) is a 4-byte field (registers 30x8032 through 30x8035) that contains the XENPAK OUI bits. Bit order for the OUI follows the format of IEEE802.3 1998 Clause 22.2.4.3.1 and is therefore reversed in comparison to other non-volatile registers. The XENPAK OUI is 00-08-BE.

Name: Vendor-Specific Package Identifier OUI (Bits 10:3)
Address: 30x8032

Bit	Name	Access	Description	Reset Value
3:0	XENPAK_OUI	RW	XENPAK OUI. 80x: XENPAK OUI bit 3 40x: XENPAK OUI bit 4 20x: XENPAK OUI bit 5 10x: XENPAK OUI bit 6 8x: XENPAK OUI bit 7 4x: XENPAK OUI bit 8 2x: XENPAK OUI bit 9 1x: XENPAK OUI bit 10 0x: Unspecified	0x0

Name: Vendor-Specific Package Identifier OUI (Bits 18:11)
Address: 30x8033

Bit	Name	Access	Description	Reset Value
7:0	XENPAK_OUI	RW	XENPAK OUI. 80x: XENPAK OUI bit 11 40x: XENPAK OUI bit 12 20x: XENPAK OUI bit 13 10x: XENPAK OUI bit 14 8x: XENPAK OUI bit 15 4x: XENPAK OUI bit 15 2x: XENPAK OUI bit 17 1x: XENPAK OUI bit 18 0x: Unspecified	0x0

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Name: Vendor-Specific Package Identifier OUI (Bits 24:19 for OUI/Bits 4:3 for NVR)
Address: 30x8034

Bit	Name	Access	Description	Reset Value
7:0	XENPAK_OUI	RW	XENPAK OUI. 80x: XENPAK OUI bit 19 40x: XENPAK OUI bit 20 20x: XENPAK OUI bit 21 10x: XENPAK OUI bit 22 8x: XENPAK OUI bit 23 4x: XENPAK OUI bit 24 2x: NVR Div Addr bit 4 1x: NVR Dev Addr bit 3 0x: Unspecified	0x0

Name: Vendor-Specific Package Identifier OUI (Bits 2:0 for NVR/Bits 3:0 for Rev. No.)
Address: 30x8035

Bit	Name	Access	Description	Reset Value
3:0	XENPAK_OUI	RW	XENPAK OUI. 80x: NVR Dev Addr bit 2 40x: NVR Dev Addr bit 1 20x: NVR Dev Addr bit 0 10x: Revision No. bit 3 8x: Revision No. bit 2 4x: Revision No. bit 1 2x: Revision No. bit 0 1x: Reserved 0x: Unspecified	0x0

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2.8.26 Transceiver Vendor OUI

The transceiver vendor OUI is a three-byte field (registers 30x8036 to 30x8039) that contains the IEEE company identifier for the transceiver. Bit order for the OUI follows the format of IEEE802.3 1998 Clause 22.2.4.3.1 and is therefore reversed in comparison to other non-volatile registers. A value of all zeros in the 3-byte field indicates that the vendor OUI is unspecified.

Name: Transceiver Vendor OUI (Bits 10:3)
Address: 30x8036

Bit	Name	Access	Description	Reset Value
3:0	Vendor_OUI	RW	Vendor OUI. 80x: OUI bit 3 40x: OUI bit 4 20x: OUI bit 5 10x: OUI bit 6 8x: OUI bit 7 4x: OUI bit 8 2x: OUI bit 9 1x: OUI bit 10 0x: Unspecified	0x0

Name: Transceiver Vendor OUI (Bits 18:11)
Address: 30x8037

Bit	Name	Access	Description	Reset Value
7:0	Vendor_OUI	RW	Vendor OUI. 80x: OUI bit 11 40x: OUI bit 12 20x: OUI bit 13 10x: OUI bit 14 8x: OUI bit 15 4x: OUI bit 15 2x: OUI bit 17 1x: OUI bit 18 0x: Unspecified	0x0

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Name: Transceiver Vendor OUI (OUI Bits 24:19 and Model Bits 4:3)
Address: 30x8038

Bit	Name	Access	Description	Reset Value
7:0	Vendor_OUI	RW	Vendor OUI. 80x: OUI bit 19 40x: OUI bit 20 20x: OUI bit 21 10x: OUI bit 22 8x: OUI bit 23 4x: OUI bit 24 2x: Model No. bit 5 1x: Model No. bit 4 0x: Unspecified	0x0

Name: Transceiver Vendor OUI (Revision Bits 3:0 and Model Bits 2:0)
Address: 30x8039

Bit	Name	Access	Description	Reset Value
15:4	Reserved	RW	Reserved.	0x0
3:0	Vendor_OUI	RW	Vendor OUI. 80x: Model number bit 3 40x: Model number bit 2 20x: Model number bit 1 10x: Model number bit 0 8x: Revision number bit 3 4x: Revision number bit 2 2x: Revision number bit 1 1x: Revision number bit 0 0x: Unspecified	0x0

2.8.27 Vendor Name

The following registers (addresses: 30x803A to 30x8049) contain the transceiver vendor name in ASCII characters. It is left-aligned and padded on the right with ASCII spaces (20h).

Name: Vendor Name
Address: 30x803A through 30x8049

Bit	Name	Access	Description	Reset Value
7:0	Vendor_Name	RW	Vendor name in ASCII characters.	0x0

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2.8.28 Vendor PN

The following registers (30x804A to 30x8059) contain transceiver vendor part number in ASCII characters. It is left-aligned and padded on the right with ASCII space (20h). A value of all zeros in the field indicates that the vendor PN is unspecified.

Name: Vendor Part Number (PN)
Address: 30x804A through 30x8059

Bit	Name	Access	Description	Reset Value
7:0	Vendor_PN	RW	Vendor part number in ASCII	0x0

2.8.29 Vendor Revision

The following registers (30x805A and 30x805B) contain the vendor revision number in ASCII characters. It is left-aligned and padded on the right with ASCII spaces (20h). A value of all zeros in the field indicates that the vendor revision is unspecified.

Name: Vendor Revision
Address: 30x805A
30x805B

Bit	Name	Access	Description	Reset Value
7:0	Vendor_Revision_Number	RW	Vendor revision number in ASCII	0x0

2.8.30 Vendor Serial Number

The following registers (30x805C to 30x806B) contain transceiver vendor serial number (SN) in ASCII characters. It is left-aligned and padded on the right with ASCII space (20h). A value of all zeros in the field indicates that the vendor PN is unspecified.

Name: Vendor Serial Number (SN)
Address: 30x805C through 30x806B

Bit	Name	Access	Description	Reset Value
7:0	Vendor_SN	RW	Vendor serial number in ASCII	0x0

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2.8.31 Vendor-Specific Date Code

The following registers (30x806C to 30x8075) contain transceiver vendor date code in ASCII characters.

Name: Vendor Date Code
Address: 30x806C through 30x8075

Bit	Name	Access	Description	Reset Value
7:0	Vendor_Date_Code	RW	Vendor date code. 30x806C: Year in 1000s (bit 7: MSB, bit 0:LSB). 30x806D: Year in 100s (bit 7: MSB, bit 0:LSB). 30x806E: Year in 10s (bit 7: MSB, bit 0:LSB). 30x806F: Year units (bit 7: MSB, bit 0:LSB). 30x8070: Month in 10s (bit 7: MSB, bit 0:LSB). 30x8071: Month units (bit 7: MSB, bit 0:LSB). 30x8072: Day in 10s (bit 7: MSB, bit 0:LSB). 30x8073: Day units (bit 7: MSB, bit 0:LSB). 30x8073: Lot in 10s (bit 7: MSB, bit 0:LSB). 30x8073: Lot units (bit 7: MSB, bit 0:LSB).	0x0

2.8.32 5 V Stressed Environment Reference

The assignment of bits in the 5 Stressed Environment Reference register is shown in the following table.

Name: 5 V Stressed Environment Reference (100% of this register value is 1 A.)
Address: 30x8076

Bit	Name	Access	Description	Reset Value
7:0	5V_Stressed_Reference	RW	5 V stressed reference. 0x80: 90% – 99% used 0x40: 80% – 89% used 0x20: 70% – 79% used 0x10: 60% – 69% used 0x08: 50% – 59% used 0x04: 40% – 49% used 0x02: 30% – 39% used 0x01: 20% – 29% used 0x00: 5 V not used	0x0

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2.8.33 3.3 V Stressed Environment Reference

The assignment of bits in the 3.3 V Stressed Environment Reference register is shown in the following table.

Name: 3.3 V Stressed Environment Reference (100% of this register value is 2 A.)
Address: 30x8077

Bit	Name	Access	Description	Reset Value
7:0	3.3V_Stressed_Reference	RW	3.3 V stressed reference. 0x80: 90% – 99% used 0x40: 80% – 89% used 0x20: 70% – 79% used 0x10: 60% – 69% used 0x08: 50% – 59% used 0x04: 40% – 49% used 0x02: 30% – 39% used 0x01: 20% – 29% used 0x00: 3.3 V not used	0x0

2.8.34 APS Stressed Environment Reference

The assignment of bits in the APS Stressed Environment Reference register is shown in the following table.

Name: APS Stressed Environment Reference (100% of this register value is 2 A.)
Address: 30x8078

Bit	Name	Access	Description	Reset Value
7:0	APS_Stressed_Reference	RW	APS stressed reference. 0x80: 90% – 99% used 0x40: 80% – 89% used 0x20: 70% – 79% used 0x10: 60% – 69% used 0x08: 50% – 59% used 0x04: 40% – 49% used 0x02: 30% – 39% used 0x01: 20% – 29% used 0x00: APS not used	0x0

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2.8.35 Nominal APS Voltage

The assignment of bits in the Nominal APS Voltage register is shown in the following table.

Name: Nominal APS Voltage (100% of this register value is 2 A.)
Address: 30x8079

Bit	Name	Access	Description	Reset Value
7:0	Nominal_APS_Voltage	RW	Nominal APS voltage. 0x80: Reserved 0x40: C 0x20: 1.8 V 0x10: 1.5 V 0x08: 1.3 V 0x04: 1.2 V 0x02: 1.0 V 0x01: 0.9 V 0x00: Unspecified	0x0

2.8.36 DOM Capability

The assignment of bits in the DOM Capability register is shown in the following table.

Name: DOM Capability
Address: 30x807A

Bit	Name	Access	Description	Reset Value
7	DOM_Control_Status_Register	RO	DOM control status register implemented. 0: Not implemented. 1: Implemented.	0
6	DOM_Implementation	RO	Set when DOM implemented.	0
5	WDM_Lane_DOM_Capability	RO	WDM lane by lane DOM capability. Setting this bit indicates that registers A0C0 to A0FF are valid. Setting this bit does not override indications placed in register 30xA06F.	0
4	Laser_Bias_Scale_Factor	RO	Laser bias scale factor. 0: 2 µA 1: 10 µA	0
3	Reserved	RO	Reserved.	0
2:0	External_DOM_Address	RO	Address of external DOM device (if required).	0x0

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2.8.37 Low-Power Startup Mode Capability

The assignment of bits in the Low-Power Startup Mode Capability register is shown in the following table.

Name: Low-Power Startup Mode Capability
Address: 30x807B

Bit	Name	Access	Description	Reset Value
7:1	Reserved	RW	Reserved.	0x0
0	Low_Power_Startup_Capability	RW	Low-power startup capability. 1: LPS active. 0: LPS not active.	0

2.8.38 Reserved

The assignment of bits in the Reserved register is shown in the following table.

Name: Reserved
Address: 30x807C

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

2.8.39 Basic Checksum

The assignment of bits in the Basic Checksum register is shown in the following table.

Name: Basic Checksum
Address: 30x807D

Bit	Name	Access	Description	Reset Value
7:0	Basic_Field_Checksum	RW	Basic field checksum	0x0

2.8.40 Customer Space Area

The assignment of bits in the Customer Space Area register is shown in the following table.

Name: Customer Space Area
Address: 30x807E through 30x80AD

Bit	Name	Access	Description	Reset Value
7:0	Customer_Writable_Area	RW	Customer writable area	0x0

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2.8.41 Vendor-Specific Area

The assignment of bits in the Vendor-Specific Area register is shown in the following table.

Name: Vendor-Specific Area
Address: 30x80AE through 30x8106

Bit	Name	Access	Description	Reset Value
7:0	Vendor_Specific_Area	RW	Vendor-specific area	0x0

2.8.42 Rx_Alarm Control

The following register provides Rx_ALARM control settings. It may be programmed to assert only when a specific receive path fault condition is present. The Rx_ALARM signal is set when the same bit in both this register and register 30x9003 are set. For more information, see *XENPAK MSA Revision 3.0*.

Name: Rx_ALARM Control
Address: 30x9000

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RW	Reserved	0x0
10	Vendor_Specific	RW	Vendor-specific	0
9	WIS_Fault_Enable	RW	WIS fault enable	0
8:6	Vendor_Specific	RW	Vendor-specific	0x0
5	Laser_Output_Pwr_Fault_Enable	RW	Laser output power fault enable	0
4	PMA_PMD_RX_Fault_Enable	RW	PMA/PMD receiver fault enable	1
3	PCS_RX_Fault_Enable	RW	PCS receive fault enable	1
2	Vendor_Specific	RW	Vendor-specific	0
1	RX_Flag_Enable	RW	Receiver flag enable	0
0	PHY_XS_RX_Fault_Enable	RW	PHY XS receive fault enable	1

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2.8.43 Tx_Alarm Control

The following register provides Tx_ALARM control settings. It may be programmed to assert only when a specific receive path fault condition is present. The Tx_ALARM signal is set when the same bit in both this register and register 30x9004 are set. For more information, see *XENPAK MSA Revision 3.0*.

Name: Tx_ALARM Control
Address: 30x9001

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RW	Reserved	0x0
10	Vendor_Specific	RW	Vendor-specific	0
9	Laser_Bias_Current_Fault_Enable	RW	Laser bias current fault enable	0
8	Laser_Temperature_Fault_Enable	RW	Laser temperature fault enable	0
7	Laser_Output_Pwr_Fault_Enable	RW	Laser output power fault enable	0
6	TX_Fault_Enable	RW	Transmitter fault enable	0
5	Vendor_Specific	RW	Vendor-specific	0
4	PMA_PMD_TX_Fault_Enable	RW	PMA/PMD transmitter fault enable	1
3	PCS_TX_Fault_Enable	RW	PCS transmit fault enable	1
2	Vendor_Specific	RW	Vendor-specific	0
1	TX_Flag_Enable	RW	Tranceiver flag enable	0
0	PHY_XS_TX_Fault_Enable	RW	PHY XS transmit fault enable	1

2.8.44 LASI Control

The following register is a Link Alarm Status Interrupt (LASI) Control register that allows the global masking of the RX_ALARM, TX_ALARM, and LS_ALARM inputs. For more information, see *XENPAK MSA Revision 3.0*.

Name: LASI Control
Address: 30x9002

Bit	Name	Access	Description	Reset Value
15:8	Reserved	RO	Reserved	0x0
7:3	Vendor_Specific	RO	Vendor-specific	0x0
2	RX_ALARM_Enable	RW	RX_ALARM enable	0
1	TX_ALARM_Enable	RW	TX_ALARM enable	0
0	LS_ALARM_Enable	RW	LS_ALARM enable	0

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2.8.45 Rx_ALARM Status

Assertion of Rx_ALARM indicates that a fault occurred in the receive path of the XENPAK module. Bits in this register are cleared on read. For more information, see *XENPAK MSA Revision 3.0*.

Name: Rx_ALARM Status
Address: 30x9003

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RO	Reserved	0x0
10	Vendor_Specific	RO	Vendor-specific	0
9	WIS_Fault	RO	WIS fault	0
8:6	Vendor_Specific	RO	Vendor-specific	0x0
5	Laser_Output_Power_Fault	RO	Laser output power fault	0
4	PMA_PMD_RX_Fault	RO/LH	PMA/PMD receiver fault	0
3	PCS_RX_Fault	RO/LH	PCS receive fault	0
2	Vendor_Specific	RO	Vendor-specific	0
1	RX_Flag	RO/LH	Rx flag	0
0	PHY_XS_RX_Fault	RO/LH	PHY XS receive fault	0

2.8.46 Tx_ALARM Status

Assertion of Tx_ALARM indicates that a fault occurred in the transmit path of the XENPAK module. Bits in this register are cleared on read. For more information, see *XENPAK MSA Revision 3.0*.

Name: Tx_ALARM Status
Address: 30x9004

Bit	Name	Access	Description	Reset Value
15:11	Reserved	RO	Reserved	0x0
10	Vendor_Specific	RO	Vendor-specific	0
9	Laser_Bias_Current_Fault	RO	Laser bias current fault	0
8	Laser_Temperature_Fault	RO	Laser temperature fault	0
7	Laser_Output_Power_Fault	RO	Laser output power fault	0
6	TX_Fault	RO	Transmitter fault	0
5	Vendor_Specific	RO	Vendor-specific	0
4	PMA_PMD_TX_Fault	RO/LH	PMA/PMD transmitter fault	0
3	PCS_TX_Fault	RO/LH	PCS transmit fault	0
2	Vendor_Specific	RW	Vendor-specific	0
1	TX_Flag	RO/LH	Tx flag	0
0	PHY_XS_TX_Fault	RO/LH	PHY XS transmit fault	0

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2.8.47 LASI Status

The following register is a LASI status register that allows global masking of the Rx_ALARM, Tx_ALARM, and LS_ALARM inputs. For more information, see *XENPAK MSA Revision 3.0*.

Name: LASI Status
Address: 30x9005

Bit	Name	Access	Description	Reset Value
15:8	Reserved	RO	Reserved	0x0
7:3	Vendor_Specific	RW	Vendor-specific	0x0
2	RX_ALARM	RO	RX_ALARM	0
1	TX_ALARM	RO	TX_ALARM	0
0	LS_ALARM	RO/LH	LS_ALARM	0

2.8.48 Tx Flag Control

The assignment of the bits for the Tx Flag Control register is given in the following table. For more information, see *XENPAK MSA Revision 3.0*.

Name: Tx Flag Control
Address: 30x9006

Bit	Name	Access	Description	Reset Value
7	TX_Temp_High_ALarm_Enable	RW	Tranceiver temperature high alarm enable	0
6	TX_Temp_Low_ALarm_Enable	RW	Tranceiver temperature low alarm enable	0
5:4	Reserved	RW	Reserved	0x0
3	Laser_Current_High_Alarm_Enable	RW	Laser bias current high alarm enable	0
2	Laser_Current_Low_Alarm_Enable	RW	Laser bias current low alarm enable	0
1	Output_Power_High_Alarm_Enable	RW	Laser output power high alarm enable	0
0	Output_Power_Low_Alarm_Enable	RW	Laser output power low alarm enable	0

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2.8.49 Rx Flag Control

The assignment of the bits for the Rx Flag Control register is given in the following table. For more information, see *XENPAK MSA Revision 3.0*.

Name: Rx Flag Control
Address: 30x9007

Bit	Name	Access	Description	Reset Value
7	RX_Opt_Pwr_High_ALarm_Enable	RW	Receiver optical power high alarm enable	0
6	RX_Opt_Pwr_Low_ALarm_Enable	RW	Receiver optical power low alarm enable	0
5:4	Reserved	RW	Reserved	0x0

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2.9 Alarm and Warning Thresholds

The following registers (30xA000 to 30xA027) contain the alarm and warning thresholds.

2.9.1 Transceiver Temperature High Alarm (MSB)

The following register contains the MSB for the transceiver temperature high alarm.

Name: Transceiver Temperature High Alarm
Address: 30xA000

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_High_Alarm_MSB	RW	Most significant byte. Transceiver temperature high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

2.9.2 Transceiver Temperature High Alarm (LSB)

The following register contains the LSB for the transceiver temperature high alarm.

Name: Transceiver Temperature High Alarm
Address: 30xA001

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_High_Alarm_LSB	RW	Least significant byte. Transceiver temperature high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

2.9.3 Transceiver Temperature Low Alarm (MSB)

The following register contains the MSB for the transceiver temperature low alarm.

Name: Transceiver Temperature Low Alarm
Address: 30xA002

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_Low_Alarm_MSB	RW	Most significant byte. Transceiver temperature low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

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2.9.4 Transceiver Temperature Low Alarm (LSB)

The following register contains the LSB for the transceiver temperature low alarm.

Name: Transceiver Temperature Low Alarm
Address: 30xA003

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_Low_Alarm_LSB	RW	Least significant byte. Transceiver temperature low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.1	0x0

2.9.5 Transceiver Temperature High Warning (MSB)

The following register contains the MSB for the transceiver temperature high warning.

Name: Transceiver Temperature High Warning
Address: 30xA004

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_High_Warning_MSB	RW	Most significant byte. Transceiver temperature high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

2.9.6 Transceiver Temperature High Warning (LSB)

The following register contains the LSB for the transceiver temperature high warning.

Name: Transceiver Temperature High Warning
Address: 30xA005

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_High_Warning_LSB	RW	Least significant byte. Transceiver temperature high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

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2.9.7 Transceiver Temperature Low Warning (MSB)

The following register contains the MSB for the transceiver temperature low warning.

Name: Transceiver Temperature Low Warning
Address: 30xA006

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_Low_Warning_MSB	RW	Most significant byte. Transceiver temperature low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

2.9.8 Transceiver Temperature Low Warning (LSB)

The following register contains the LSB for the transceiver temperature low warning.

Name: Transceiver Temperature Low Warning
Address: 30xA007

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_Low_Warning_LSB	RW	Least significant byte. Transceiver temperature low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.1.	0x0

2.9.9 Reserved

The following register contains eight reserved bytes.

Name: Reserved
Address: 30xA008 to 30xA00F

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

2.9.10 Laser Bias Current High Alarm (MSB)

The following register contains the MSB for the laser bias current high alarm.

Name: Laser Bias Current High Alarm
Address: 30xA010

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_High_Alarm_MSB	RW	Most significant byte. Laser bias current high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.11 Laser Bias Current High Alarm (LSB)

The following register contains the LSB for the laser bias current high alarm.

Name: Laser Bias Current High Alarm
Address: 30xA011

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_High_Alarm_LSB	RW	Least significant byte. Laser bias current high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.12 Laser Bias Current Low Alarm (MSB)

The following register contains the MSB for the laser bias current low alarm.

Name: Laser Bias Current Low Alarm
Address: 30xA012

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Low_Alarm_MSB	RW	Most significant byte. Laser bias current low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.13 Laser Bias Current Low Alarm (LSB)

The following register contains the LSB for the laser bias current low alarm.

Name: Laser Bias Current Low Alarm
Address: 30xA013

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Low_Alarm_LSB	RW	Least significant byte. Laser bias current low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.14 Laser Bias Current High Warning (MSB)

The following register contains the MSB for the laser bias current high warning.

Name: Laser Bias Current High Warning
Address: 30xA014

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_High_Warning_MSB	RW	Most significant byte. Laser bias current high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.15 Laser Bias Current High Warning (LSB)

The following register contains the LSB for the laser bias current high warning.

Name: Laser Bias Current High Warning
Address: 30xA015

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_High_Warning_LSB	RW	Least significant byte. Laser bias current high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.16 Laser Bias Current Low Warning (MSB)

The following register contains the MSB for the laser bias current low warning.

Name: Laser Bias Current Low Warning
Address: 30xA016

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Low_Warning_MSB	RW	Most significant byte. Laser bias current low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.17 Laser Bias Current Low Warning (LSB)

The following register contains the LSB for the laser bias current low warning.

Name: Laser Bias Current Low Warning
Address: 30xA017

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Low_Warning_LSB	RW	Least significant byte. Laser bias current low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.18 Laser Output Power High Alarm (MSB)

The following register contains the MSB for the laser output power high alarm.

Name: Laser Output Power High Alarm
Address: 30xA018

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_High_Alarm_MSB	RW	Most significant byte. Laser output power high alarm. See *XENPAK MSA Revision 3.0,* Section 11.2.3.	0x0

2.9.19 Laser Output Power High Alarm (LSB)

The following register contains the LSB for the laser output power high alarm.

Name: Laser Output Power High Alarm
Address: 30xA019

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_High_Alarm_LSB	RW	Least significant byte. Laser output power high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.20 Laser Output Power Low Alarm (MSB)

The following register contains the MSB for the laser output power low alarm.

Name: Laser Output Power Low Alarm
Address: 30xA01A

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_Low_Alarm_MSB	RW	Most significant byte. Laser output power low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.21 Laser Output Power Low Alarm (LSB)

The following register contains the LSB for the laser output power low alarm.

Name: Laser Output Power Low Alarm
Address: 30xA01B

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_Low_Alarm_LSB	RW	Least significant byte. Laser output power low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.22 Laser Output Power High Warning (MSB)

The following register contains the MSB for the laser output power high warning.

Name: Laser Output Power High Warning
Address: 30xA01C

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_High_Warn_MSB	RW	Most significant byte. Laser output power high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.23 Laser Output Power High Warning (LSB)

The following register contains the LSB for the laser output power high warning.

Name: Laser Output Power High Warning
Address: 30xA01D

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_High_Warn_LSB	RW	Least significant byte. Laser output power high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.24 Laser Output Power Low Warning (MSB)

The following register contains the MSB for the laser output power low warning.

Name: Laser Output Power Low Warning
Address: 30xA01E

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_Low_Warn_MSB	RW	Most significant byte. Laser output power low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

2.9.25 Laser Output Power Low Warning (LSB)

The following register contains the LSB for the laser output power low warning.

Name: Laser Output Power Low Warning
Address: 30xA01F

Bit	Name	Access	Description	Reset Value
7:0	Laser_Out_Pwr_Low_Warn_LSB	RW	Least significant byte. Laser output power low warning, *XENPAK MSA Revision 3.0*, Section 11.2.3.	0x0

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2.9.26 Receiver Optical Power High Alarm (MSB)

The following register contains the MSB for the receiver optical power high alarm.

Name: Receiver Optical Power High Alarm
Address: 30xA020

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_High_Alarm_MSB	RW	Most significant byte. Receiver optical power high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

2.9.27 Receiver Optical Power High Alarm (LSB)

The following register contains the LSB for the receiver optical power high alarm.

Name: Receiver Optical Power High Alarm
Address: 30xA021

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_High_Alarm_LSB	RW	Least significant byte. Receiver optical power high alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

2.9.28 Receiver Optical Power Low Alarm (MSB)

The following register contains the MSB for the receiver optical power low alarm.

Name: Receiver Optical Power Low Alarm
Address: 30xA022

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_Low_Alarm_MSB	RW	Most significant byte. Receiver optical power low alarm. See XENPAK 3.0 Section 11.2.4.	0x0

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2.9.29 Receiver Optical Power Low Alarm (LSB)

The following register contains the LSB for the receiver optical power low alarm.

Name: Receiver Optical Power Low Alarm
Address: 30xA023

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_Low_Alarm_LSB	RW	Least significant byte. Receiver optical power low alarm. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

2.9.30 Receiver Optical Power High Warning (MSB)

The following register contains the MSB for the receiver optical power high warning.

Name: Receiver Optical Power High Warning
Address: 30xA024

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_High_Warn_MSB	RW	Most significant byte. Receiver optical power high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

2.9.31 Receiver Optical Power High Warning (LSB)

The following register contains the LSB for the receiver optical power high warning.

Name: Receiver Optical Power High Warning
Address: 30xA025

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_High_Warn_LSB	RW	Least significant byte. Receiver optical power high warning. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

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2.9.32 Receiver Optical Power Low Warning (MSB)

The following register contains the MSB for the receiver optical power low warning.

Name: Receiver Optical Power Low Warning
Address: 30xA026

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_Low_Warn_MSB	RW	Most significant byte. Receiver optical power low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

2.9.33 Receiver Optical Power Low Warning (LSB)

The following register contains the LSB for the receiver optical power low warning.

Name: Receiver Optical Power Low Warning
Address: 30xA027

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Pwr_Low_Warn_LSB	RW	Least significant byte. Receiver optical power low warning. See *XENPAK MSA Revision 3.0*, Section 11.2.4.	0x0

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2.10 Customer Area

The assignment of bits for the Customer Area registers is given in the following table.

Name: Customer Area

Address:

30xA048	30xA057
30xA049	30xA058
30xA050	30xA059
30xA051	30xA05A
30xA052	30xA05B
30xA053	30xA05C
30xA054	30xA05D
30xA055	30xA05E
30xA056	30xA05F

Bit	Name	Access	Description	Reset Value
7:0	Customer_Area	RW	Customer area.	0x0

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2.11 Registers Digital Optical Monitoring Interface

The following registers (30xA060 to 30xA077) are for the DOM interface.

2.11.1 Transceiver Temperature (MSB)

The following register contains the MSB for the transceiver temperature.

Name: Transceiver Temperature
Address: 30xA060

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_MSB	RW	Most significant byte. Transceiver temperature. See *XENPAK MSA Revision 3.0*, Table 23.	0x0

2.11.2 Transceiver Temperature (LSB)

The following register contains the LSB for the transceiver temperature.

Name: Transceiver Temperature
Address: 30xA061

Bit	Name	Access	Description	Reset Value
7:0	TX_Temp_LSB	RW	Least significant byte. Transceiver temperature. See *XENPAK MSA Revision 3.0*, Table 23.	0x0

2.11.3 Reserved

The following registers are reserved.

Name: Reserved
Address: 30xA062 to 30xA063

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

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2.11.4 Laser Bias Current (MSB)

The following register contains the MSB for the laser bias current.

Name: Laser Bias Current
Address: 30xA064

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Current_MSB	RW	Most significant byte. Laser bias current. See *XENPAK MSA Revision 3.0*, Table 24.	0x0

2.11.5 Laser Bias Current (LSB)

The following register contains the LSB for the laser bias current.

Name: Laser Bias Current
Address: 30xA065

Bit	Name	Access	Description	Reset Value
7:0	Laser_Bias_Current_LSB	RW	Least significant byte. Laser bias current. See *XENPAK MSA Revision 3.0*, Table 24.	0x0

2.11.6 Laser Output Power (MSB)

The following register contains the MSB for the laser output power.

Name: Laser Output Power
Address: 30xA066

Bit	Name	Access	Description	Reset Value
7:0	Laser_Output_Power_MSB	RW	Most significant byte. Laser output power. See *XENPAK MSA Revision 3.0*, Table 25.	0x0

2.11.7 Laser Output Power (LSB)

The following register contains the LSB for the laser output power.

Name: Laser Output Power
Address: 30xA067

Bit	Name	Access	Description	Reset Value
7:0	Laser_Output_Power_LSB	RW	Least significant byte. Laser output power. See *XENPAK MSA Revision 3.0*, Table 25.	0x0

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2.11.8 Receiver Optical Power (MSB)

The following register contains the MSB for the receiver optical power.

Name: Receiver Optical Power
Address: 30xA068

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Power_MSB	RW	Most significant byte. Receiver optical power. See *XENPAK MSA Revision 3.0*, Table 26.	0x0

2.11.9 Receiver Optical Power (LSB)

The following register contains the LSB for the receiver optical power.

Name: Receiver Optical Power
Address: 30xA069

Bit	Name	Access	Description	Reset Value
7:0	RX_Optical_Power_LSB	RW	Least significant byte. Receiver optical power. See *XENPAK MSA Revision 3.0*, Table 26.	0x0

2.11.10 Reserved

The following registers are reserved.

Name: Reserved
Address: 30xA06A to 30xA06D

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

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2.11.11 Digital Optical Monitoring Capability

The assignment of bits for the digital optical monitoring (DOM) capability register is shown in the following table.

Name: Digital Optical Monitoring Capability
Address: 30x807A

Bit	Name	Access	Description	Reset Value
7	DOM_Control_Status	RO	Digital optical monitoring control/status register implemented 0: Not Implemented 1: Implemented	0
6	DOM_Implementation	RO	Set when digital optical monitoring is implemented	0
5	WDM_Lane_DOM_Capability	RO	WDM lane-by-lane DOM capability: Setting this bit indicates that registers 30xA0C0 through 30xA0FF are valid. Setting this bit does not override indications placed in register 30xA06F (DOM capability)	0
4	Laser_Bias_Scale_Factor	RO	Laser bias scale factor 0: 2 µA 1: 10 µA	0
3	Served	RO	Reserved	0
2:0	DOM_Device_Address	RO	Address of external digital optical monitoring device (if required)	0x0

2.11.12 Optional Status Bits

The assignment of bits for the optional status bits register is shown in the following table.

Name: Optional Status Bits
Address: 30xA06E

Bit	Name	Access	Description	Reset Value
7:1	Reserved	RO	Reserved	0x0
0	Data_Ready_Bar	RO	Data ready bar. Optional bit is high during module power up and prior to the first valid A/D reading. After the first valid A/D reading occurs, the bit is set low until the device is powered down.	0

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2.11.13 Digital Optical Monitoring Capability Extended

The assignment of bits for the digital optical monitoring capability (extended) register is shown in the following table.

Name: Digital Optical Monitoring Capability Extended
Address: 30xA06F

Bit	Name	Access	Description	Reset Value
7	TX_Temp_Monitor	RO	Set to indicate transceiver termperature monitoring capable.	0
6	Laser_Bias_Current_Monitor	RO	Set to indicate laser bias current monitoring capable.	0
5	Laser_Optical_Pwr_Monitor	RO	Set to indicate laser optical power monitoring capable.	0
4	RX_Optical_Pwr_Monitor	RO	Set to indicate receive optical power monitoring capable.	0
3	Alarm_Flags_Implemented	RO	Set to indicate alarm flags implemented for monitored quantities.	0
2	Warning_Flags_Implemented	RO	Set to indicate warning flags implmented for monitored quantitiies.	0
1	LASI_Function_Input_Monitor	RO	Set to indicate monitored quantities are imputs to LASI function. If this bit is set, bit 3 must also be set (that is, the alarm flag support).	0
0	Reserved	RO	Reserved.	0

2.11.14 Tx Alarm Flags

The assignment of bits for the transceiver alarm flags register is shown in the following table.

Name: Tx Alarm Flags
Address: 30xA070

Bit	Name	Access	Description	Reset Value
7	TX_Temp_Monitor	RW	Transceiver temperature high alarm	0
6	Laser_Bias_Current_Monitor	RW	Transceiver temperature low alarm	0
5:4	Reserved	RW	Reserved	0x0
3	Laser_Bias_Current_High_Alarm	RW	Laser bias current high alarm	0
2	Laser_Bias_Current_Low_Alarm	RW	Laser bias current low alarm	0
1	Laser_Output_Pwr_High_Alarm	RW	Laser output power high alarm	0
0	Laser_Output_Pwr_Low_Alarm	RW	Laser output power low alarm	0

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2.11.15 Rx Alarm Flags

The assignment of bits for the transceiver alarm flags register is shown in the following table.

Name: Rx Alarm Flags
Address: 30xA071

Bit	Name	Access	Description	Reset Value
7	RX_Optical_Pwr_High_Alarm	RO	Receive optical power high alarm	0
6	RX_Optical_Pwr_Low_Alarm	RO	Receive optical power low alarm	0
5:0	Reserved	RO	Reserved	0x0

2.11.16 Reserved

The following two registers are reserved.

Name: Reserved
Address: 30xA072 to 30xA073

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

2.11.17 Tx Warning Flags

The assignment of bits for the transceiver warning flags register is shown in the following table.

Name: Tx Warning Flags
Address: 30xA074

Bit	Name	Access	Description	Reset Value
7	TX_Temp_Monitor	RW	Transceiver temperature high warning	0
6	Laser_Bias_Current_Monitor	RW	Transceiver temperature low warning	0
5:4	Reserved	RW	Reserved	0x0
3	Laser_Bias_Current_High_Warning	RW	Laser bias current high warning	0
2	Laser_Bias_Current_Low_Warning	RW	Laser bias current low warning	0
1	Laser_Output_Pwr_High_Warning	RW	Laser output power high warning	0
0	Laser_Output_Pwr_Low_Warning	RW	Laser output power low warning	0

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2.11.18 Rx Warning Flags

The assignment of bits for the receiver warning flags register is shown in the following table.

Name: Rx Warning Flags
Address: 30xA075

Bit	Name	Access	Description	Reset Value
7	RX_Optical_Pwr_High_Warning	RW	Receive optical power high warning	0
6	RX_Optical_Pwr_Low_Warning	RW	Receive optical power low warning	0
5:0	Reserved	RO	Reserved	0x0

2.11.19 Reserved

The following registers are reserved.

Name: Reserved
Address: 30xA076 to 30xA077

Bit	Name	Access	Description	Reset Value
7:0	Reserved	RW	Reserved	0x0

2.12 Digital Optical Monitoring for CWDM Registers

The registers (addresses 30xA0C0 to 20xA0FF) are not applicable for a serial line transceiver and are not defined here. However, this space is available for general-purpose use.

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3 Electrical Specifications

This section describes the electrical specifications, operating conditions, and stress ratings for the VSC8476 device.

3.1 DC Characteristics

The specifications listed in this section are guaranteed over the recommended operating conditions listed in Table 3.3, page 213.

Table 18. LVTTL I/O Specifications

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{OH}	Output high voltage	2.4 1.8 1.4 1.0	V_{DDTTL}	V	VDDTTL = 3.3 V I_{OH} = –4 mA VDDTTL = 2.5 V I_{OH} = –4 mA VDDTTL = 1.8 V I_{OH} = –2 mA VDDTTL = 1.5 V I_{OH} = –2 mA
V_{OL}	Output low voltage	0.0	0.5 0.5 0.4 0.2	V	VDDTTL = 3.3 V I_{OH} = –4 mA VDDTTL = 2.5 V I_{OH} = –4 mA VDDTTL = 1.8 V I_{OH} = –2 mA VDDTTL = 1.5 V I_{OH} = –2 mA
V_{IH}	Input high voltage	2.0 1.7 1.7 1.05	V_{DDTTL}	V	VDDTTL = 3.3 V VDDTTL = 2.5 V VDDTTL = 1.8 V VDDTTL = 1.5 V
V_{IL}	Input low voltage	0.0	0.8 0.8 0.6 0.45	V	VDDTTL = 3.3 V VDDTTL = 2.5 V VDDTTL = 1.8 V VDDTTL = 1.5 V
I_I	Input current	–50 (V_{IL} = 0 V)	500 (V_{IH} = V_{DDTTL})	µA	

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Table 19. Reference Clock Input (LVPECL) Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
ΔV_{REFCLK}	Input voltage	150		2000	mVp-p	Peak-to-peak both sides driven. Reference clock = 657.4 MHz.
		300		1000	mVp-p	Peak-to-peak single-ended driven. Reference clock = 657.4 MHz.
$V_{REFTERM}$	REFTERM voltage		0.67 * V_{DD12TX}		V	V_{DD12TX} = 1.2 V.
V_{IH}	Input high	$V_{REFTERM}$ + 75 mV			mV	V_{DD12TX} = 1.2 V.
V_{IL}	Input low			$V_{REFTERM}$ – 75 mV	mV	V_{DD12TX} = 1.2 V.

Table 20. MDIO Electrical Interface Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input high voltage[1]	0.84	V_{DDTTL}	V	
V_{IL}	Input low voltage	–0.3	0.36	V	
V_{OH}	Output high voltage[2]	1.0	1.5	V	I_{OH} = –100 µA
V_{OL}	Output low voltage	–0.3	0.2	V	I_{OL} = 100 µA
I_{OH}	Output high current		–4.0	mA	V_I = 1.0 V
I_{OL}	Output low current	4.0		mA	V_I = 0.2 V
C_{IN}	Input capacitance		10	pF	
C_L	Bus loading		470	pF	

1. Input is 3.3 V tolerant.

2. Output is open drain and can be pulled up to any VDDTTL from 1.2 V to 3.3 V (DC).

Table 21. Power Supply Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
P_{D_XGMII}	Total power dissipation, XFI to XGMII mode		1		W	V_{DD12X}, V_{DDA12}.
P_{D_XAUI}	Total power dissipation, XFI to XAUI mode		1.2		W	V_{DDHTL} = 0 V.
P_T	Total power dissipation		1		W	

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3.2 AC Characteristics

The specifications listed in this section are guaranteed over the recommended operating conditions listed in Table 3.3, page 213.

Table 22. XFI Receiver Specifications for Serial Input Performance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
ΔV_{SWING}	Data input swing	55		525	mV	Peak-to-peak each side (both sides driven)
ΔV_{SWING_DIFF}	Data differential input swing	110		1050	mV	Peak-to-peak both sides driven with no offset applied
ΔV_{SWING_SE}	Data single-ended input swing	250		1050	mV	Peak-to-peak single-ended driven with no offset applied
Z_{SE_TERM}	Single-ended input impedance	40	50	60	Ω	RXIN to RXINCM
Z_{DE_TERM}	Differential input impedance	80	100	120	Ω	RXIN+ to RXIN–
$S11_{DIFF}$	Differential input return loss[1]	10			dB	0.1 GHz to 7.5 GHz 7.5 GHz to 15 GHz
S11	Single-ended input return loss	6			dB	0.1 GHz to 15 GHz
I_{TERM}	Termination resistor current			25	mA	RXIN to RXINCM
RXINCM	RXDATA input common mode		0.75 * V_{DD12RX}		V	

1. Return loss is calculated according to the equation $S11_{DIFF}(dB) = 10 – 16.6\ Log10(f / 7.5)$, with f in GHz.

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Table 23. XFI Receiver Specifications for CRU Performance

Symbol	Parameter	Minimum	Maximum	Unit	Condition
Δf_{REFCLK}	Difference between REFCLK frequency (with appropriate multiplier) and 10 G input data frequency	–100	100	ppm	
$TOL_{JIT\_p\text{-}p}$	Total jitter tolerance, peak-to-peak	0.65	0.65	UI p-p	
$NDD_{JIT\_P\text{-}P}$	Total non-DDJ jitter tolerance, peak-to-peak	0.45	0.45	UI p-p	
S_J	Sinusoidal jitter tolerance, peak-to-peak				See Figure 40.
X1	Eye mask (X1)		0.325	UI	See Figure 39.
Y1	Eye mask (Y1)	55		mV	See Figure 39.
Y2	Eye mask (Y2)		525	mV	See Figure 39.

Figure 39. XFI Receiver Compliance Mask

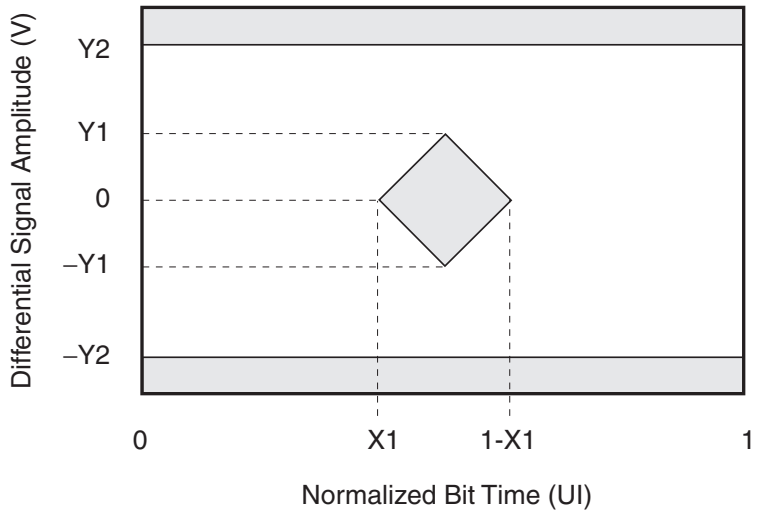

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Figure 40. XFI Receiver Input Sinusoidal Jitter Tolerance

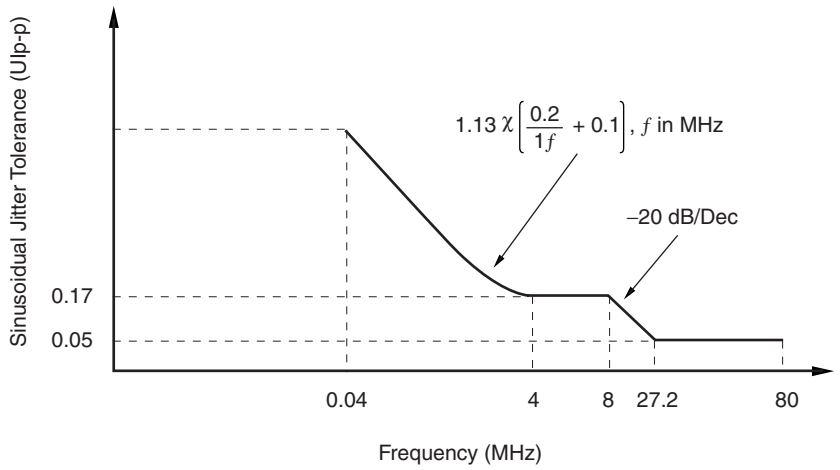

Table 24. XAUI Input Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
f	Input baud rate	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
UI	Unit interval		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm
V_{IN_DIFF}	Differential input amplitude	75		1600	mVp-p	AC-coupled, peak-to-peak each side (both sides driven)
V_{IN_CM}	Common-mode input voltage	.75		V_{DDA12} – 0.05	V	Midpoints between high and low voltages, measured at DC
RLI_{DIFF}	Differential return loss	10			dB	100 Ω differential reference impedance
RLI_{CM}	Common-mode return loss	6			dB	100 MHz to 2.5 GHz, 25 Ω reference impedance
SK_{DIFF}	Differential skew			75	ps	Between true and complement inputs
TOL_{TJ}	Jitter tolerance, total	0.65			UI p-p	See IEEE802.3ae-2002, clause 47.3.4
TOL_{DJ}	Jitter tolerance, deterministic	0.37			UI p-p	See IEEE802.3ae-2002, clause 47.3.4
TOL_{DJ+RJ}	Jitter tolerance, deterministic plus random jitter	0.55			UI p-p	See IEEE802.3ae-2002, clause 47.3.4

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Figure 41. XAUI Receiver Input Sinusoidal Jitter Tolerance

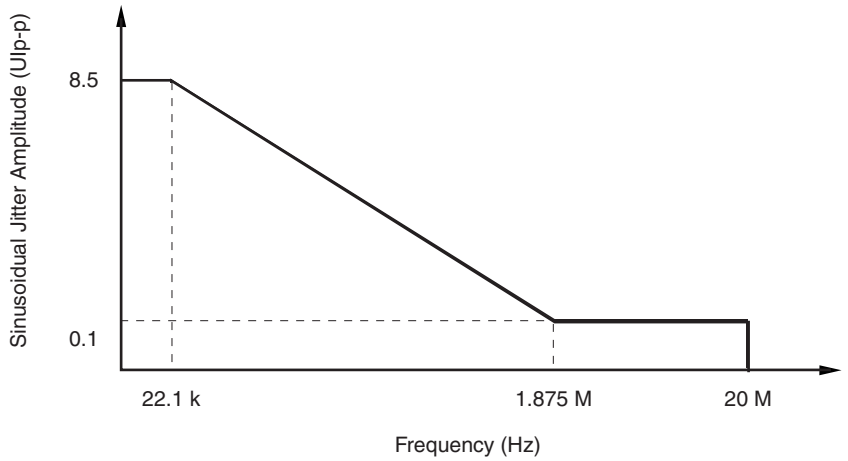

Table 25. XGMII Input Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{REF}	Input reference voltage	0.68	0.75	0.9	V	Peak-to-peak AC noise on V_{REF} may not exceed 2% V_{REF}(DC)
V_{IH_DC}	DC input logic high	V_{REF} + 0.1		V_{DDHTL} + 0.3	V	
V_{IL_DC}	DC input logic low	–0.3		V_{REF} – 0.1	V	
V_{IH_AC}	AC input logic high	V_{REF} + 0.2			V	
V_{IL_AC}	AC input logic low			V_{REF} – 0.2	V	

Figure 42. XGMII I/O Level Reference Diagram

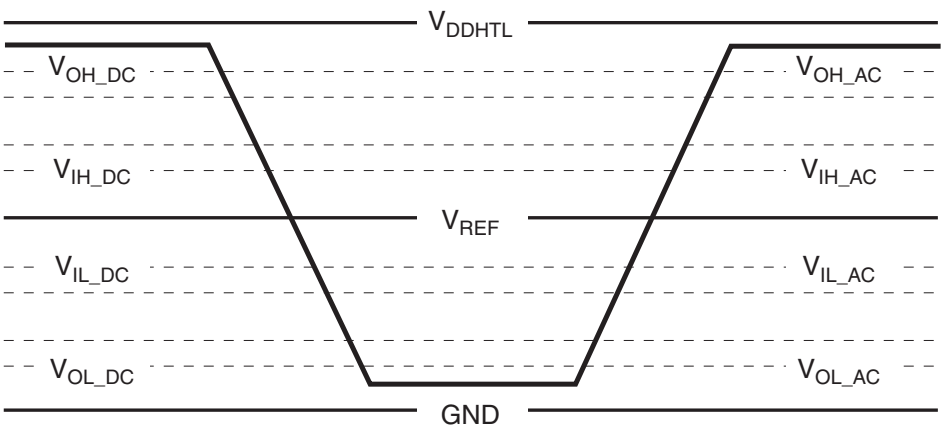

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Table 26. Reset Timing

Symbol	Parameter	Minimum	Units	Condition
T_{RESET}	Minimum reset pulse width	0.1	µs	All power supplies are stable and asynchronous.

Figure 43. Reset Input Timing

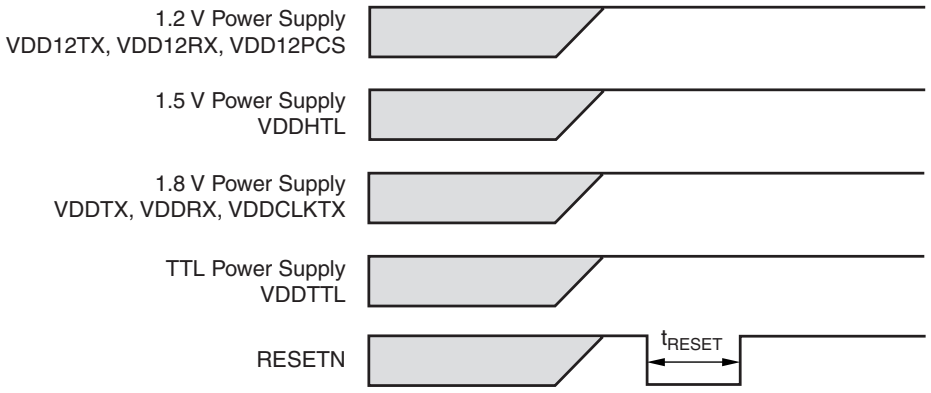

Table 27. XFI Output Specifications for MUX Performance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
$VDOUT_{DIFF}$	TXDOUT ± peak-to-peak differential output swing	180		385	mV	Each side, AC-coupled differential signal AC-coupled terminated 50 Ω to V_{DDTX}
V_{CM}	Common-mode output voltage TXDOUT		0.8		V	
$t_{R,}$ t_F	TXDOUT ± rise time and fall time	24	35		ps	20% to 80% into 50 Ω load
Z_{SE_TERM}	Single-ended output impedance	40	50	60	Ω	TXDOUT to VDDTX
Z_{DE_TERM}	Differential output impedance	80	100	120	Ω	TXDOUT+ to TXDOUT–
$S22_{DIFF}$	Differential output return loss[1]	10			dB	0.1 GHz to 7.5 GHz 7.5 GHz to 15 GHz
S22	Single-ended output return loss	6			dB	0.1 GHz to 15 GHz
I_{TERM}	Termination resistor current			25	mA	TXDOUT to VDDTX

1. Return loss is calculated by equation $S22_{DIFF}(dB) = 10 – 16.6\ Log10(f / 7.5)$, with f in GHz.

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Table 28. XFI Output Specifications for CMU Performance

Symbol	Parameter	Minimum	Maximum	Unit	Condition
DJ_{DOUT}	TXDOUT ± deterministic jitter, peak-to-peak		0.15	UI p-p)	Soldered down f = 10.5 GHz; 657.4 MHz reference clock with 500 mV minimum swing.
TJ_{DOUT}	TXDOUT ± total jitter, peak-to-peak		0.30	UI p-p	
JG_{C64}	CLK64 ± jitter generation, peak-to-peak[1]		0.01	UI p-p	
ΔV	CLK64 ± peak-to-peak output swing	320	800	mV	
X1	Eye mask		0.15	UI	See Figure 44.
X2	Eye mask		0.4	UI	See Figure 44.
Y1	Eye mask	180		mV	See Figure 44.
Y2	Eye mask		385	mV	See Figure 44.

1. JG_{C64} is referenced to 164.35 (161.13) MHz.

Figure 44. XFI Output Compliance Mask

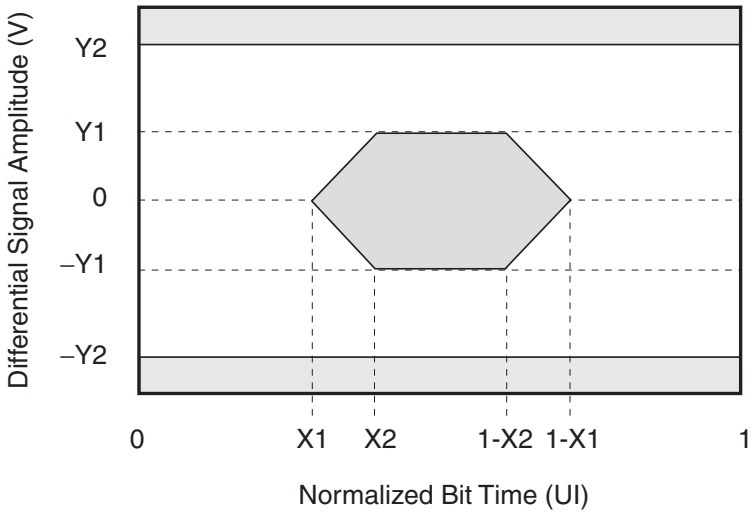

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Table 29. Reference Clock Specifications

Symbol	Parameter	Minimum	Maximum	Unit	Condition
f_{REFCLK}	REFCLK frequency	644.53 MHz – 100 ppm	657.4 MHz +100 ppm	MHz	Pins: REFSEL[1:0] = 10
f_{REFCLK}	REFCLK frequency	161.13 MHz – 100 ppm	164.35 MHz + 100 ppm	MHz	Pins: REFSEL[1:0] = 01
f_{REFCLK}	REFCLK frequency	156.25 MHz – 100 ppm	159.37 MHz + 100 ppm	MHz	Pins: REFSEL[1:0] = 00
SSB_{REFCLK}	REFCLK single-side band phase noise[1]		–85 –105 –125 –125 –135	dBc/Hz	1 kHz 10 kHz 100 kHz 1 MHz 10 MHz
DC_{REFCK}	REFCLK ± duty cycle	40	60	%	

1. For 1/16 reference clock mode input only.

Table 30. XAUI Output Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
f	Output baud rate	3.125 – 100 ppm		3.1875 + 100 ppm	Gbps	
UI	Unit interval		320		ps	3.125 Gbps – 100 ppm to 3.1875 Gbps + 100 ppm.
XV_{OUT_DIFF}	Differential output voltage	400		650	mVp-p	Each side, AC-coupled, peak-to-peak both sides driven with no offset applied. HISWNG = 1.
		250		500	mVp-p	Each side, AC-coupled, peak-to-peak both sides driven with no offset applied. HISWNG = 0. (Minimum value violates XAUI specification.)
V_{ABS}	Absolute output voltage	–0.4		2.3	V	
Z_{OUT}	Output impedance	40	50	60		Single-ended.
		80	100	120		Differential.
RLO_{DIFF}	Differential output return loss	10			dB	100 MHz to 781.25 MHz, reducing 20 dB per decade up to 3.5 GHz. Includes on-chip circuitry, packaging, and off-chip components. 100 Ω test source.
RLO_{CM}	Common-mode output return loss	6			dB	100 MHz to 2.5 GHz over valid output levels. Includes on-chip circuitry, packaging, and off-chip components. 25 Ω test source.

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Table 30. XAUI Output Specifications *(continued)*

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
T_R, T_F	Rise time and fall time	60		130	ps	20% for rise time 80% for fall time
T_J	Total jitter			0.35	UI p-p	No pre-emphasis
DJ	Deterministic jitter			0.17	UI p-p	No pre-emphasis
X1	Eye mask			0.175	UI	See Figure 45.
X2	Eye mask			0.390	UI	See Figure 45.
A1	Eye mask	250			mV	See Figure 45. HISWNG = 0
A1	Eye mask	400			mV	See Figure 45. HISWNG = 1
A2	Eye mask			800	mV	See Figure 45.

Figure 45. XAUI Output Compliance Mask

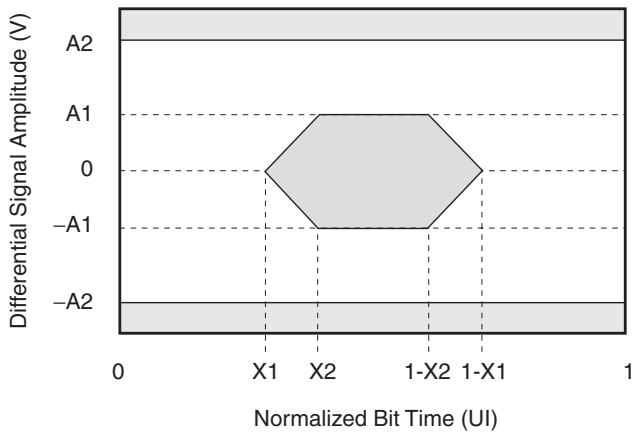

Table 31. XGMII Output Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DDHTL}	Output supply voltage	1.4	1.5	1.6	V	
V_{OH}	DC output logic high	V_{DDHTL}–0.4			V	I_{OH} = 6 mA (V_{TT} = V_{DDHTL} / 2, R_T = 50 Ω)
V_{OL}	DC output logic low			0.4	V	I_{OH} = |–6 mA| (V_{TT} = V_{DDHTL} / 2, R_T = 50 Ω)
JG_{RXCLK}	RXCLK jitter generation, peak-to-peak[1]			0.005	UI p-p	
DC_{RXCLK}	RXCLK output duty cycle	45		55	%	

1. JG_{RXCLK} referenced to 159.37(156.25) MHz.

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Figure 46. XGMII Interface Timing Diagram

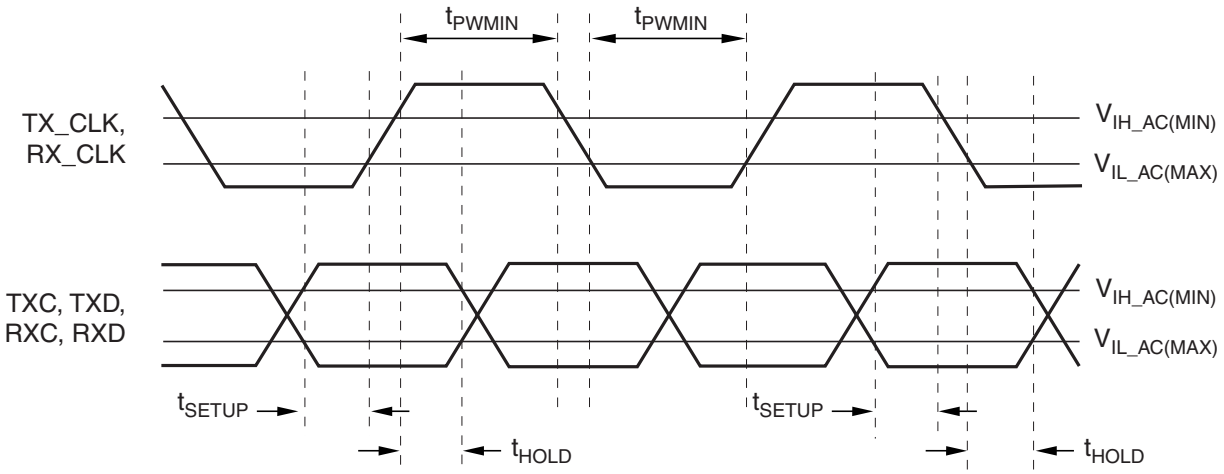

Table 32. TX_CLK and RX_CLK Timing Parameters

Symbol	Parameter	Driver	Receiver	Units	Condition
t_{SETUP}	Setup time	960	480	ps	V_{DDHTL} is 1.5 V to 1.6 V.
t_{SETUP}	Setup time	860	480	ps	V_{DDHTL} is 1.43 V to 1.58 V.
t_{HOLD}	Hold time	960	480	ps	V_{DDHTL} is 1.5 V to 1.6 V.
t_{HOLD}	Hold time	860	480	ps	V_{DDHTL} is 1.43 V to 1.58 V.
t_{PWMIN}	Minimum pulse width	2.5		ns	

Figure 47. Parametric Measurement Setup

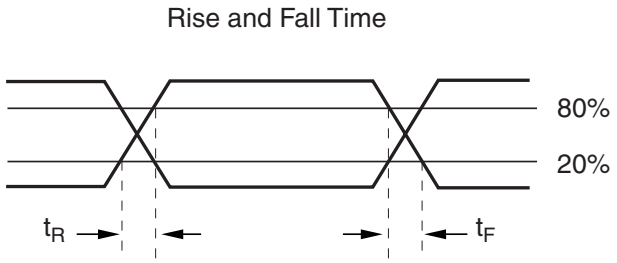

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Figure 48. Timing with MDIO Sourced by the Station Management Entity (STA)

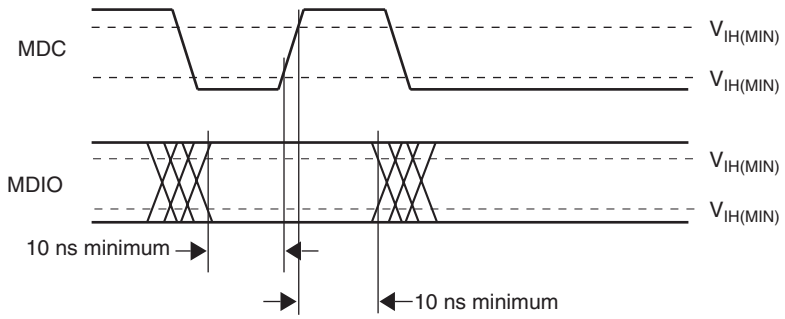
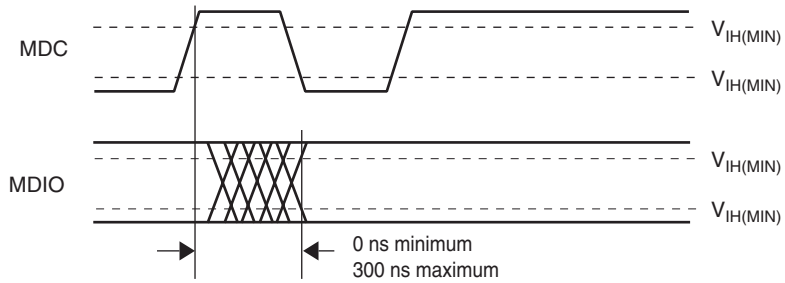


Figure 49. Timing with MDIO Sourced by the MMD



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3.3 Operating Conditions

Table 33. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DDHTL}	1.5 V power supply voltage	1.43	1.5	1.58	V	
I_{DDHTL}	1.5 V power supply current		150 10 1		mA	Outputs terminated 50 Ω to V_{REF}, data toggling with 50% duty cycle. Outputs unterminated, data toggling with 50% duty cycle. Outputs unterminated, static data.
V_{DD12TX} V_{DD12RX} $V_{DD12PCS}$	1.2 V power supply voltage	1.14	1.2	1.26	V	
I_{DD12}	1.2 V power supply current		950		mA	
V_{DD12X} V_{DD12AX}	1.2 V power supply voltage, PHYXS block	1.14	1.2	1.26	V	
I_{DD12PX}	1.2 V power supply current, PHYXS block		415		mA	
V_{DDTTL}	TTL I/O power supply voltage	2.97 2.25 1.71 1.43	3.3 2.5 1.8 1.5	3.63 2.75 1.89 1.58	V	
I_{DDTTL}	TTL I/O power supply current		3		mA	V_{DDTTL} = 3.3 V, 2.5 V, 1.8 V, 1.5 V.
T	Operating temperature[1]	0		85	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

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3.4 Stress Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 34. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDTTL}	3.3 V power supply voltage, potential to ground	–0.5	3.8	V
V_{DDHTL}	1.5 V power supply voltage, potential to ground	–0.5	1.65	V
V_{DD12}	1.2 V power supply voltage, potential to ground	–0.5	1.32	V
	DC input voltage (differential)	V_{SS} – 0.3	V_{DDTTL}, V_{DDHTL}, or V_{DD12} + 0.3	V
	Output current (differential)	–16	16	mA
	Output current (LVTTL)	–50	50	mA
T_S	Storage temperature	–65	150	°C
V_{ESD}	Electrostatic discharge voltage, human body model:			
	CML pins	–100	100	V
	HSTL pins	–100	100	V
	MDIO pins	–1500	1500	V
	LVPECL pins	–250	250	V
	LVTTL pins (except M6 and M7 pins)	–100	100	V
	M6 and M7 pins (two-wire serial interface pins)	–1000	1000	V

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

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4 Pin Descriptions

The VSC8476 device has 256 pins. This section contains the VSC8476 pin diagram and describes the pin assignments.

4.1 Pin Diagram

Figure 50. Pin Diagram, Top View

A1 Corner

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	REFCLK+	GND	TXD1	TXD5	TXD8	TXD12	TXC1	TXD18	TXD22	XTX3–	XTX3+	TXD27	XRX3–	XRX3+	NC	A
B	REFCLK–	REFTERM	GND	TXD0	TXD4	TXC0	TXD11	TXD15	TXD17	TXD21	TXC2	TXD25	TXD26	TXD29	TXD30	TXD31	B
C	GND	GND	GND	RXALARM	TXD3	TXD7	TXD10	TXD14	TXD16	TXD20	TXD23	TXD24	HVREF	TXD28	TXC3	XTX2–	C
D	NC	GND	GND	NC	TXD2	TXD6	TXD9	TXD13	TXCLK	XD19	NC	NC	NC	NC	LP_XAUI	XTX2+	D
E	NC	GND	CMUFILT	TXALARM	LASI	NC	REFSEL0	SPLITLOOPN	NC	TXONOFFI	GND	GND	NC	NC	NC	NC	E
F	GND	GND	GND	NC	GND	NC	REFSEL1	NC	NC	GND	VDDA12	VDDA12	GND	NC	XAUIFILT	XRX2–	F
G	GND	GND	NC	VDD12TX	GND	VDDTTL	GND	VDDHTL	VDD12PCS	GND	VDDA12	VDDA12	GND	VDD12X	GND	XRX2+	G
H	TXDOUT+	GND	GND	VDD12TX	VDD12TX	VDD12RX	GND	VDDHTL	VDDHTL	GND	VDDA12	VDDA12	GND	VDD12X	NC	GND	H
J	TXDOUT–	GND	CLK64+	NC	NC	VDD12RX	GND	VDDHTL	VDDHTL	GND	VDDA12	VDDA12	GND	VDD12X	NC	GND	J
K	GND	GND	CLK64–	GND	GND	VDDTTL	GND	VDDHTL	VDD12PCS	GND	VDDA12	NC	GND	VDD12X	GND	XTX1–	K
L	CRUFILT	GND	GND	MDIO	GND	NC	MDC	RESETN	MSTCODE2	MSTCODE1	VDDA12	NC	GND	VDD12X	NC	XTX1+	L
M	GND	GND	NC	NC	RXINOFFEN	STWSDA	STWSCL	PRTAD4	PRTAD3	MSTCODE0	GND	GND	NC	NC	NC	IOMODESEL	M
N	RXIN+	GND	RXINCM	TMS	RXD2	RXD6	RXD9	RXD13	RXCLK	RXD19	PRTAD2	PRTAD1	PRTAD0	NC	NC	XRX1–	N
P	RXIN–	NC	GND	TDI	RXD3	RXD7	RXD10	RXD14	RXD16	RXD20	RXD23	RXD24	STWWP	RXD28	RXC3	XRX1+	P
R	GND	NC	TDO	RXD0	RXD4	RXC0	RXD11	RXD15	RXD17	RXD21	RXC2	RXD25	RXD26	RXD29	RXD30	RXD31	R
T	NC	TRSTB	TCK	RXD1	RXD5	RXD8	RXD12	RXC1	RXD18	RXD22	XRX0+	XRX0–	RXD27	XTX0+	XTX0–	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

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4.2 Pin Identifications

Table 35. Pin Identifications

Pin	Name	I/O	Level	Description
A1	NC			No connect.
A2	REFCLK+	I	LVPECL	Reference clock input, true.
A3	GND	Power		Ground.
A4	TXD1	I	HSTL	XGMII input for lane 0, bit 1.
A5	TXD5	I	HSTL	XGMII input for lane 0, bit 5.
A6	TXD8	I	HSTL	XGMII input for lane 1, bit 0.
A7	TXD12	I	HSTL	XGMII input for lane 1, bit 4.
A8	TXC1	I	HSTL	XGMII control bit for lane 1, bits 8 to 15.
A9	TXD18	I	HSTL	XGMII input for lane 2, bit 2.
A10	TXD22	I	HSTL	XGMII input for lane 2, bit 6.
A11	XTX3–	O	CML	XAUI channel 3 serial data output, complement. SL3<N> per IEEE Standard 802.3ae.
A12	XTX3+	O	CML	XAUI channel 3 serial data output, true. SL3<P> per IEEE Standard 802.3ae.
A13	TXD27	I	HSTL	XGMII input for lane 3, bit 3.
A14	XRX3–	I	CML	XAUI channel 3 serial data input, complement. DL3<N> per IEEE Standard 802.3ae.
A15	XRX3+	I	CML	XAUI channel 3 serial data input, true. DL3<P> per IEEE Standard 802.3ae.
A16	NC			No connect.
B1	REFCLK–	I	LVPECL	Reference clock input, complement. Terminated 50 Ω to REFTERM.
B2	REFTERM	I	LVPECL	REFCLK input termination center tap.
B3	GND	Power		Ground.
B4	TXD0	I	HSTL	XGMII input for lane 0, bit 0.
B5	TXD4	I	HSTL	XGMII input for lane 0, bit 4.
B6	TXC0	I	HSTL	XGMII control bit for lane 0, bits 0 to 7.
B7	TXD11	I	HSTL	XGMII input for lane 1, bit 3.
B8	TXD15	I	HSTL	XGMII input for lane 1, bit 7.
B9	TXD17	I	HSTL	XGMII input for lane 2, bit 1.
B10	TXD21	I	HSTL	XGMII input for lane 2, bit 5.
B11	TXC2	I	HSTL	XGMII control bit for lane 2, bits 16 to 23.
B12	TXD25	I	HSTL	XGMII input for lane 3, bit 1.
B13	TXD26	I	HSTL	XGMII input for lane 3, bit 2.
B14	TXD29	I	HSTL	XGMII input for lane 3, bit 5.
B15	TXD30	I	HSTL	XGMII input for lane 3, bit 6.
B16	TXD31	I	HSTL	XGMII input for lane 3, bit 7.
C1	GND	Power		Ground.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
C2	GND	Power		Ground.
C3	GND	Power		Ground.
C4	RXALARM	O	LVTTL	Logic OR for alarms in register 30x1003 (see "Rx_ALARM Status," page 179) as enabled by register 30x1000 (see "Rx_Alarm Control," page 177).
C5	TXD3	I	HSTL	XGMII input for lane 0, bit 3.
C6	TXD7	I	HSTL	XGMII input for lane 0, bit 7.
C7	TXD10	I	HSTL	XGMII input for lane 1, bit 2.
C8	TXD14	I	HSTL	XGMII input for lane 1, bit 6.
C9	TXD16	I	HSTL	XGMII input for lane 2, bit 0.
C10	TXD20	I	HSTL	XGMII input for lane 2, bit 4.
C11	TXD23	I	HSTL	XGMII input for lane 2, bit 7.
C12	TXD24	I	HSTL	XGMII input for lane 3, bit 0.
C13	HVREF	I	Analog	HSTL I/O reference voltage input. No connect for most applications.
C14	TXD28	I	HSTL	XGMII input for lane 3, bit 4.
C15	TXC3	I	HSTL	XGMII control bit for lane 3, bits 24 to 31.
C16	XTX2–	O	CML	XAUI channel 2 serial data output, complement. SL2<N> per IEEE Standard 802.3ae.
D1	NC			No connect.
D2	GND	Power		Ground.
D3	GND	Power		Ground.
D4	NC			No connect.
D5	TXD2	I	HSTL	XGMII input for lane 0, bit 2.
D6	TXD6	I	HSTL	XGMII input for lane 0, bit 6.
D7	TXD9	I	HSTL	XGMII input for lane 1, bit 1.
D8	TXD13	I	HSTL	XGMII input for lane 1, bit 5.
D9	TXCLK	I	HSTL	Double data rate reference for the transfer of TXD[31:0] and TXC[3:0] signals. Typically 1/64 of the overall XGMII data transfer rate.
D10	TXD19	I	HSTL	XGMII input for lane 2, bit 3.
D11	NC			No connect.
D12	NC			No connect.
D13	NC			No connect.
D14	NC			No connect.
D15	LP_XAUI	I	LVTTL	Loops back the traffic in both directions in the XAUI block. On-chip pull-down resistor disables loopback.
D16	XTX2+	O	CML	XAUI channel 2 serial data output, true. SL2<P> per IEEE Standard 802.3ae.
E1	NC			No connect.
E2	GND	Power		Ground.
E3	CMUFILT		Analog	CRU filter capacitor (1µF) from this ball to ground.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
E4	TXALARM	O	LVTTL	Logical OR for alarms in register 30x1004 as enabled by register 30x1001.
E5	LASI	O	LVTTL	Link alarm status interrupt. Logic OR for RXALARM, TXALARM, and LSALARM. Requires an external pull-up resistor.
E6	NC			No connect.
E7	REFSEL0	I	LVTTL	Reference clock multiplier selection pins. Internally pulled down. 00: 66x (156 or 159 MHz) 01: 64x (161 or 164 MHz) 10: 16x (644 or 657 MHz)
E8	SPLITLOOPN	I	LVTTL	Simultaneous parallel (XGMII and XAUI) and XFI loopback enable. When set low, loopbacks 3 and 4 are enabled. Internally pulled up.
E9	NC			No connect.
E10	TXONOFFI	I	LVTTL	Transmitter data mute. When set high, transmitter is on. When set low, transmitter is off. Internally pulled up.
E11	GND	Power		Ground.
E12	GND	Power		Ground.
E13	NC			No connect.
E14	NC			No connect.
E15	NC			No connect.
E16	NC			No connect.
F1	GND	Power		Ground.
F2	GND	Power		Ground.
F3	GND	Power		Ground.
F4	NC			No connect.
F5	GND	Power		Ground.
F6	NC			No connect.
F7	REFSEL1	I	LVTTL	Reference clock multiplier selection pins. 00: 66x (156 or 159 MHz) 01: 64x (161 or 164 MHz) 10: 16x (644 or 657 MHz)
F8	NC			No connect.
F9	NC			No connect.
F10	GND	Power		Ground.
F11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
F12	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
F13	GND	Power		Ground.
F14	NC			No connect.
F15	XAUIFILT		Analog	XAUI CRU filter capacitor (1µF) from this ball to ground.
F16	XRX2–	I	CML	XAUI channel 2 serial data input, complement. DL2<N> per IEEE Standard 802.3ae.
G1	GND	Power		Ground.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
G2	GND	Power		Ground.
G3	NC			No connect.
G4	VDD12TX	Power		1.2 V power supply (Tx).
G5	GND	Power		Ground.
G6	VDDTTL	Power		TTL power supply (1.5 V, 1.8 V, or 3.3 V).
G7	GND	Power		Ground.
G8	VDDHTL	Power		HSTL I/O 1.5 V power supply.
G9	VDD12PCS	Power		1.2 V power supply for PCS.
G10	GND	Power		Ground.
G11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
G12	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
G13	GND	Power		Ground.
G14	VDD12X	Power		1.2 V power supply for XAUI I/O.
G15	GND	Power		Ground.
G16	XRX2+	I	CML	XAUI channel 2 serial data input, true. DL2<P> per IEEE Standard 802.3ae.
H1	TXDOUT+	O	CML	Tx serial 10G data output, true.
H2	GND	Power		Ground.
H3	GND	Power		Ground.
H4	VDD12TX	Power		1.2 V power supply for PMA serial 10 G Tx.
H5	VDD12TX	Power		1.2 V power supply for PMA serial 10 G Tx.
H6	VDD12RX	Power		1.2 V power supply for PMA serial 10 G Rx.
H7	GND	Power		Ground.
H8	VDDHTL	Power		HSTL I/O 1.5 V power supply.
H9	VDDHTL	Power		HSTL I/O 1.5 V power supply.
H10	GND	Power		Ground.
H11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
H12	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
H13	GND	Power		Ground.
H14	VDD12X	Power		1.2 V power supply for XAUI I/O.
H15	NC			No connect.
H16	GND	Power		Ground.
J1	TXDOUT–	O	CML	Tx serial 10G data output, complement.
J2	GND	Power		Ground.
J3	CLK64+	O	LVPECL	Tx divide-by-64 serial clock output, true.
J4	NC			No connect.
J5	NC			No connect.
J6	VDD12RX	Power		1.2 V analog power supply for PMA serial 10 G Rx.
J7	GND	Power		Ground.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
J8	VDDHTL	Power		HSTL I/O 1.5 V power supply.
J9	VDDHTL	Power		HSTL I/O 1.5 V power supply.
J10	GND	Power		Ground.
J11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
J12	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
J13	GND	Power		Ground.
J14	VDD12X	Power		1.2 V power supply for XAUI I/O.
J15	NC			No connect.
J16	GND	Power		Ground.
K1	GND	Power		Ground.
K2	GND	Power		Ground.
K3	CLK64–	O	CML	Tx divide-by-64 serial clock output, complement.
K4	GND	Power		Ground.
K5	GND	Power		Ground.
K6	VDDTTL	Power		TTL power supply for 1.5 V, 1.8 V, or 3.3 V.
K7	GND	Power		Ground.
K8	VDDHTL	Power		HSTL I/O 1.5 V power supply.
K9	VDD12PCS	Power		1.2 V power supply for PCS.
K10	GND	Power		Ground.
K11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
K12	NC			No connect.
K13	GND	Power		Ground.
K14	VDD12X	Power		1.2 V power supply for XAUI I/O.
K15	GND	Power		Ground.
K16	XTX1–	O	CML	XAUI channel 1 serial data output, complement. SL1<N> per IEEE Standard 802.3ae.
L1	CRUFILT		Analog	CRU filter capacitor (1 µF) from this ball to ground.
L2	GND	Power		Ground.
L3	GND	Power		Ground.
L4	MDIO	I/O	MDIO	Management data I/O. Requires external 4.7 kΩ pull-up resistor.
L5	GND	Power		Ground.
L6	NC			No connect.
L7	MDC	I	MDIO	Management data clock.
L8	RESETN	I	LVTTL	Global chip reset. Active low. Internally pulled up.
L9	MSTCODE2	I	LVTTL	Two-wire serial interface master code, bit 2.
L10	MSTCODE1	I	LVTTL	Two-wire serial interface master code, bit 1.
L11	VDDA12	Power		1.2 V analog power supply for XAUI I/O.
L12	NC			No connect.
L13	GND	Power		Ground.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
L14	VDD12X	Power		1.2 V power supply for XAUI I/O.
L15	NC			No connect.
L16	XTX1+	O	CML	XAUI channel 1 serial data output, true. SL1<P> per IEEE Standard 802.3ae.
M1	GND	Power		Ground.
M2	GND	Power		Ground.
M3	NC			No connect.
M4	NC			No connect.
M5	RXINOFFEN	I	LVTTL	High-speed input receiver DC offset correction loop enable. 0: Disable DC offset correction loop. Normal operation (internally pulled down). 1: Enable DC offset correction loop.
M6	STWSDA	I/O	LVTTL	Serial input/output data for the two-wire serial interface. Requires external 10 kΩ pull-up resistor.
M7	STWSCL	I/O	LVTTL	Two-wire serial interface clock. If unused, leave it as NC.
M8	PRTAD4	I	LVTTL	Port address bit 4 (low = 0). Internally pulled down.
M9	PRTAD3	I	LVTTL	Port address bit 3 (low = 0). Internally pulled down.
M10	MSTCODE0	I	LVTTL	Two-wire serial interface master code, bit 0. Internally pulled down.
M11	GND	Power		Ground.
M12	GND	Power		Ground.
M13	NC			No connect.
M14	NC			No connect.
M15	NC			No connect.
M16	IOMODESEL	I	LVTTL	Parallel interface mode selection pin. Internally pulled down. 0: XGMII 1: XAUI
N1	RXIN+	I	CML	Rx serial 10 G data input true.
N2	GND	Power		Ground.
N3	RXINCM		Analog	Rx serial 10 G data input resistor termination center tap.
N4	TMS	I	LVTTL	JTAG test access port test mode select input. Internally pulled up.
N5	RXD2	O	HSTL	XGMII output for lane 0, bit 2.
N6	RXD6	O	HSTL	XGMII output for lane 0, bit 6.
N7	RXD9	O	HSTL	XGMII output for lane 1, bit 1.
N8	RXD13	O	HSTL	XGMII output for lane 1, bit 5.
N9	RXCLK	O	HSTL	Double data rate reference for the transfer of RXD[31:0] and RXC[3:0] signals. Typically 1/64 of the overall XGMII data transfer rate.
N10	RXD19	O	HSTL	XGMII output for lane 2, bit 3.
N11	PRTAD2	I	LVTTL	Port address bit 2. Internally pulled down.
N12	PRTAD1	I	LVTTL	Port address bit 1. Internally pulled down.
N13	PRTAD0	I	LVTTL	Port address bit 0. Internally pulled down.
N14	NC			No connect.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
N15	NC			No connect.
N16	XRX1–	I	CML	XAUI channel 1 serial data input, complement. DL1<N> per IEEE Standard 802.3ae.
P1	RXIN–	I	CML	Rx 10G serial data input inverted.
P2	NC			No connect.
P3	GND	Power		Ground.
P4	TDI	I	LVTTL	JTAG test access port test data input. Internally pulled up.
P5	RXD3	O	HSTL	XGMII output for lane 0, bit 3.
P6	RXD7	O	HSTL	XGMII output for lane 0, bit 7.
P7	RXD10	O	HSTL	XGMII output for lane 1, bit 2.
P8	RXD14	O	HSTL	XGMII output for lane 1, bit 6.
P9	RXD16	O	HSTL	XGMII output for lane 2, bit 0.
P10	RXD20	O	HSTL	XGMII output for lane 2, bit 4.
P11	RXD23	O	HSTL	XGMII output for lane 2, bit 7.
P12	RXD24	O	HSTL	XGMII output for lane 3, bit 0.
P13	STWWP	I	LVTTL	Two-wire serial interface write protect. Disables writes to read-only EEPROM.
P14	RXD28	O	HSTL	XGMII output for lane 3, bit 4.
P15	RXC3	O	HSTL	XGMII control bit for lane 3, bits 24 to 31.
P16	XRX1+	I	CML	XAUI channel 1 serial data input, true. DL1<P> per IEEE Standard 802.3ae.
R1	GND	Power		Ground.
R2	NC			No connect.
R3	TDO	O	LVTTL	JTAG test access port test data output.
R4	RXD0	O	HSTL	XGMII output for lane 0, bit 0.
R5	RXD4	O	HSTL	XGMII output for lane 0, bit 4.
R6	RXC0	O	HSTL	XGMII control bit for lane 0, bits 0 to 7.
R7	RXD11	O	HSTL	XGMII output for lane 1, bit 3.
R8	RXD15	O	HSTL	XGMII output for lane 1, bit 7.
R9	RXD17	O	HSTL	XGMII output for lane 2, bit 1.
R10	RXD21	O	HSTL	XGMII output for lane 2, bit 5.
R11	RXC2	O	HSTL	XGMII control bit for lane 2, bits 16 to 23.
R12	RXD25	O	HSTL	XGMII output for lane 3, bit 1.
R13	RXD26	O	HSTL	XGMII output for lane 3, bit 2 .
R14	RXD29	O	HSTL	XGMII output for lane 3, bit 5.
R15	RXD30	O	HSTL	XGMII output for lane 3, bit 6.
R16	RXD31	O	HSTL	XGMII output for lane 3, bit 7.
T1	NC			No connect.
T2	TRSTB	I	LVTTL	JTAG test access port test logic reset input. Internally pulled up. For JTAG test operation, this input must be pulled low.

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Table 35. Pin Identifications *(continued)*

Pin	Name	I/O	Level	Description
T3	TCK	I	LVTTL	JTAG test access port test clock input. Internally pulled up.
T4	RXD1	O	HSTL	XGMII output for lane 0, bit 1.
T5	RXD5	O	HSTL	XGMII output for lane 0, bit 5.
T6	RXD8	O	HSTL	XGMII output for lane 1, bit 0.
T7	RXD12	O	HSTL	XGMII output for lane 1, bit 4.
T8	RXC1	O	HSTL	XGMII control bit for lane 1, bits 8 to 15.
T9	RXD18	O	HSTL	XGMII output for lane 2, bit 2.
T10	RXD22	O	HSTL	XGMII output for lane 2, bit 6.
T11	XRX0+	I	CML	XAUI channel 0 serial data input, true. DL0<P> per IEEE Standard 802.3ae.
T12	XRX0–	I	CML	XAUI channel 0 serial data input, complement. DL0<N> per IEEE Standard 802.3ae.
T13	RXD27	O	HSTL	XGMII output for lane 3, bit 3.
T14	XTX0+	O	CML	XAUI channel 0 serial data output, true. SL0<P> per IEEE Standard 802.3ae.
T15	XTX0–	O	CML	XAUI channel 0 serial data output, complement. SL0<N> per IEEE Standard 802.3ae.
T16	NC			No connect.

4.3 Control I/O Default Configuration

Table 36. Control I/O Default Configuration

Pin Number	Pin Name	I/O	Level	Description[1]	Default Without External Connection
P13	STWWP	I	LVTTL	Two-wire serial interface write protect. Disables writes to read-only EEPROM.	Pull-up
M16	IOMODESEL	I	LVTTL	Low-speed interface mode selection. 0: XGMII mode 1: XAUI mode	Pull-down
M10	MSTCODE0	I	LVTTL	High-speed mode two-wire serial interface master code.	Pull-down
L10	MSTCODE1	I	LVTTL	High-speed mode two-wire serial interface master code.	Pull-down
L9	MSTCODE2	I	LVTTL	High-speed mode two-wire serial interface master code.	Pull-down
N13	PRTAD0	I	LVTTL	Port address bit 0 (low = 0).	Pull-down
N12	PRTAD1	I	LVTTL	Port address bit 1 (low = 0).	Pull-down
N11	PRTAD2	I	LVTTL	Port address bit 2 (low = 0).	Pull-down
M9	PRTAD3	I	LVTTL	Port address bit 3 (low = 0).	Pull-down

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Table 36. Control I/O Default Configuration *(continued)*

Pin Number	Pin Name	I/O	Level	Description[1]	Default Without External Connection
M8	PRTAD4	I	LVTTL	Port address bit 4 (low = 0).	Pull-down
E7	REFSEL0	I	LVTTL	01: 64x (161 or 164 MHz). 10: 16x (644 or 657 MHz).	Pull-down
F7	REFSEL1	I	LVTTL	Reference clock multiplier selection pins. 00: 66x (156/159 MHz)	Pull-down
L8	RESETN	I	LVTTL	Global chip reset. Active low.	Pull-up
M5	RXINOFFEN	I	LVTTL	High-speed input receiver DC offset correction loop enable. 0: Disable DC offset correction loop. Normal operation (internally pulled down). 1: Enable DC offset correction loop.	Pull-down
E8	SPLITLOOPN	I	LVTTL	Simultaneous parallel and serial loopback enable. When set high, normal operation. When set low, loopback 3 and loopback 4 are enabled.	Pull-up
T3	TCK	I	LVTTL	JTAG test access port test clock input.	Pull-up
P4	TDI	I	LVTTL	JTAG test access port test data input.	Pull-up
N4	TMS	I	LVTTL	JTAG test access port test mode select input. Internally pulled up.	Pull-up
T2	TRSTB	I	LVTTL	JTAG test access port test logic reset input. Internally pulled up.	Pull-up
E10	TXONOFFI	I	LVTTL	Transmitter data mute. When set high, transmitter is on. When set low, transmitter is off. Internally pulled up. No connect or pull high for normal operation.	Pull-up

1. In the case of inconsistencies, the values in this table override all other descriptions.

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5 Package Information

The VSC8476 device is available in two package types. VSC8476SN is a 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 3.22 mm body thickness, and 1.0 mm pitch. The device is also available in a lead-free package, VSC8476XSN.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

5.1 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 37. Thermal Resistances

Part Number	Θ_{JC}	Θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC8476SN	0.9	18	16	14
VSC8476XSN	0.9	18	16	14

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

5.2 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

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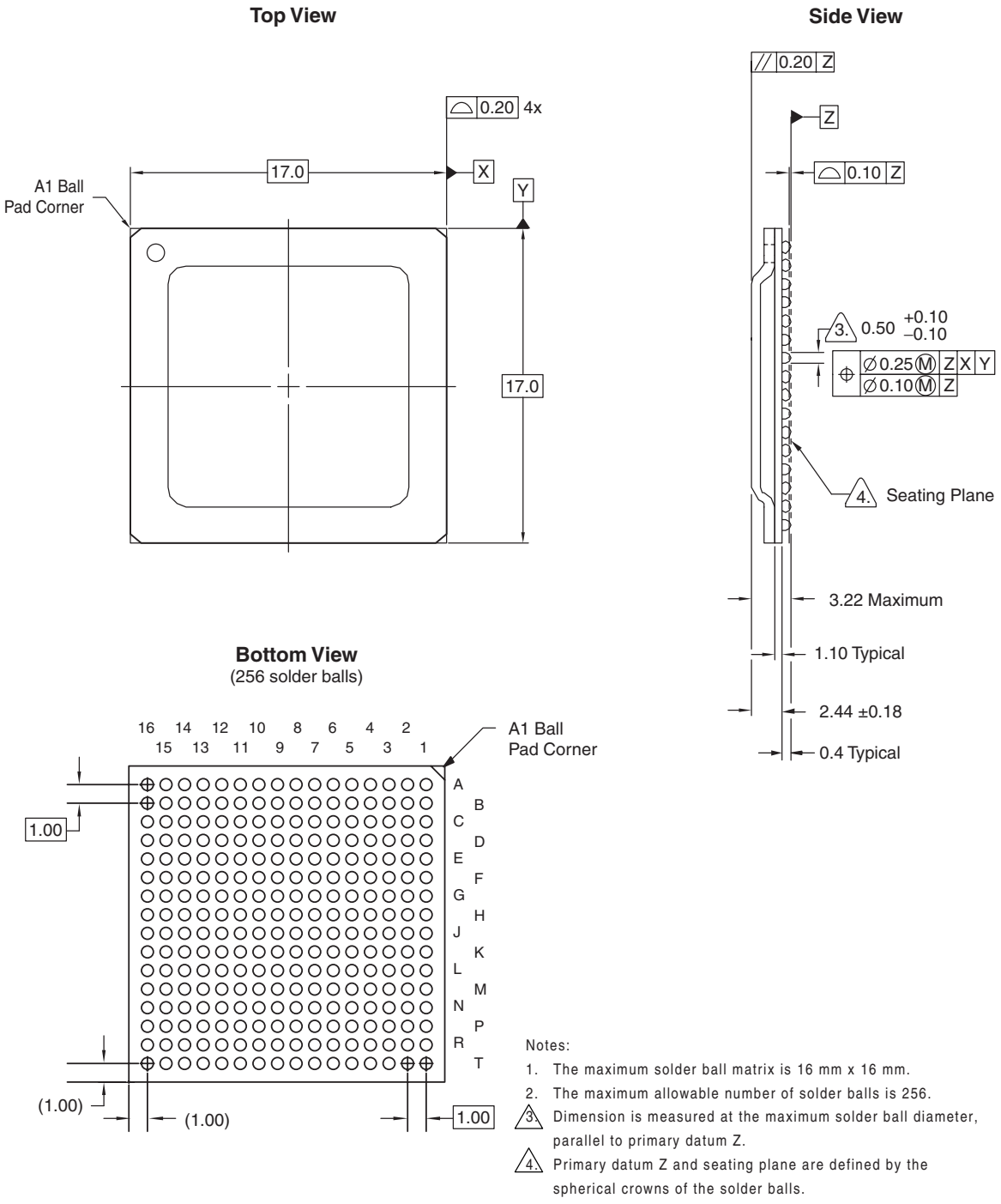
5.3 Package Drawing

Figure 51. Package Drawing



Notes:
1. The maximum solder ball matrix is 16 mm x 16 mm.
2. The maximum allowable number of solder balls is 256.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.

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6 Design Considerations

This section provides information about the design considerations for the VSC8476 device.

6.1 Check End Deviation

Feature: IEEE 802.3ae standard clause 48.2.6.1.4

Description:

The IEEE 802.3ae standard D5.0 specification, dated May 1, 2002 defines the 10 GbE protocol. Paragraph 48.2.6.1.4 specifies the Check End function as part of the physical coding sublayer (PCS) receive process. The VSC8476 deviates from the functionality as defined in the specification. This deviation results in a negligibly low probability that the VSC8476 PCS will process a bad packet.

The VSC8476 does not perform /K/ character validation in a XAUI lane at the end of a frame that does not contain the terminate character /T/. The probability of processing a bad packet is reduced to approximately 1 in 10^{19} for only one very specifically corrupted XAUI lane. This specific case mandates that two bit errors must occur in the same XAUI lane: one in a prescribed 10-bit code group that occurs a prescribed number of code groups apart from the other bit error that must also occur in an idle /K/ character. This corresponds to a possible occurrence about once every 310,000 years.

Workaround: None

Fix: None required

6.2 XFI Receiver Differential Return Loss SDD11

Feature: XFI Receiver compliance

Description:

The specification requirement for XFI receiver differential return loss, SDD11 is 10 dB as shown in Table 22, page 203. The VSC8476 device exceeds this specification by approximately 3 dB to 4 dB above 5 GHz. With proper design, this result does not impact the VSC8476 XFI stressed-eye performance, which is fully compliant with the XFP version 4.0 MSA.

Workaround:

In general results for the return loss measurements and S-parameters are important and should be considered as an indicator of overall 10 G serial link robustness. Exact compliance to these limits is no guarantee that a 10 G transmission link is optimally designed. The best solution involves attention to transmission line construction including printed circuit board (PCB) material selection and layer stack-up.

Fix: Proper attention to PCB layout and material selection effectively mitigates this issue.

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6.3 XAUI Receiver Differential Return Loss SDD11

Feature: XAUI Receiver compliance

Description:

The specification requirement for XAUI receiver differential return loss, SDD11 is 10 dB, as shown in Table 24, page 205. The VSC8476 device exceeds this specification by about 1.9 dB in lane 0, and 0.5 dB in lanes 1 and 2. This result does not impact the VSC8476SN XAUI performance, which is fully compliant with the IEEE 802.3ae standard, clause 47 far-end driver specifications.

Workaround:

Return loss measurements and S-parameters results in general are important and should be considered as an indicator of overall 3.125 G XAUI serial link robustness. Exact compliance to these limits is no guarantee that a 3.125 G transmission link is optimally designed The best solution involves attention to transmission line construction, including printed circuit board material selection and layer stack-up.

Fix: Proper attention to PCB layout and material selection, effectively mitigates this issue.

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7 Ordering Information

The VSC8476 device is available in two package types. VSC8476SN is a 256-pin, flip chip ball grid array (FCBGA) with a 17 mm × 17 mm body size, 3.22 mm body thickness, and 1.0 mm pitch. The device is also available in a lead-free package, VSC8476XSN.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8476 device.

Table 38. Ordering Information

Part Order Number	Description
VSC8476SN	256-pin, FCBGA with a 17 mm × 17 mm body size, 3.22 mm body thickness, and 1.0 mm pitch
VSC8476XSN	Lead-free 256-pin, FCBGA with a 17 mm × 17 mm body size, 3.22 mm body thickness, and 1.0 mm pitch

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