

P-Channel Enhancement Mode Field Effect Transistor

● Features

$V_{DS}(V) = -30V$, $I_D = -5.2A$,

$R_{DS(ON)} = 51m\Omega$ @ $V_{GS} = -10V$.

$R_{DS(ON)} = 68m\Omega$ @ $V_{GS} = -4.5V$.

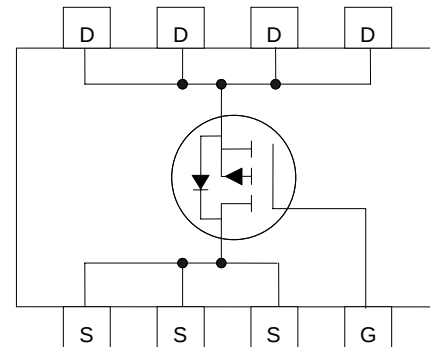
High density cell design for low $R_{DS(ON)}$.

very small outline surface mount package.

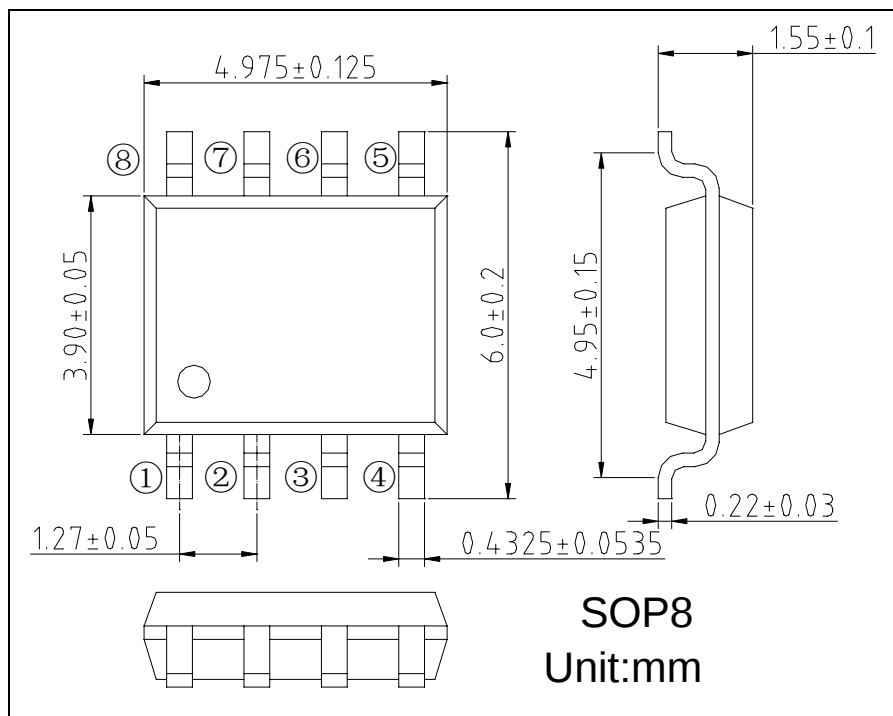
● General Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a

● Pin Configuration



● Package Information





● **Absolute Maximum Ratings** @ $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current (Note 1)	Continuous $T_A=25^\circ\text{C}$	I_D	-5.2	A
	Pulsed (Note 2)		-50	A
Total Power Dissipation (Note 1)		P_D	1.5	W
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

● **Electrical Characteristics** @ $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μ A	-30	-36	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	--	0.02	-1	μ A
Gate–Body Leakage Current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V	--	±1.5	±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = -250 μ A	-1	-1.46	-3	V
Drain–Source On–State Resistance	R _{DS(ON)}	V _{GS} = -10 V, I _D = -4.6 A	--	51	60	m Ω
		V _{GS} = -4.5 V, I _D = -2 A	--	68	82	
Forward Transconductance	G _{FS}	V _{DS} = -5 V, I _D = -6 A	--	12	--	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz	--	550	--	pF
Output Capacitance	C _{OSS}		--	60	--	
Reverse Transfer Capacitance	C _{RSS}		--	50	--	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	T _{D(ON)}	V _{DS} = -15 V, R _L = 2.5 Ω , V _{GS} = -10V, R _{GEN} =3 Ω	--	8.6	--	nS
Turn–Off Delay Tim	T _{D(OFF)}		--	28.2	--	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1 A	--	-0.81	--	V

Note: 1. The value of P_D is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the DC thermal resistance rating.

2. Repetitive rating, pulse width limited by junction temperature.

Typical Performance Characteristics

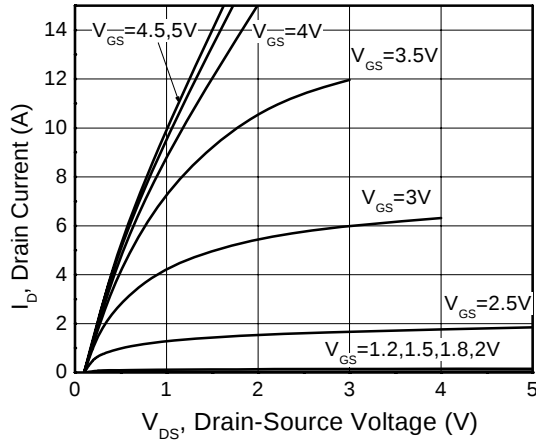


Figure 1. Output Characteristics

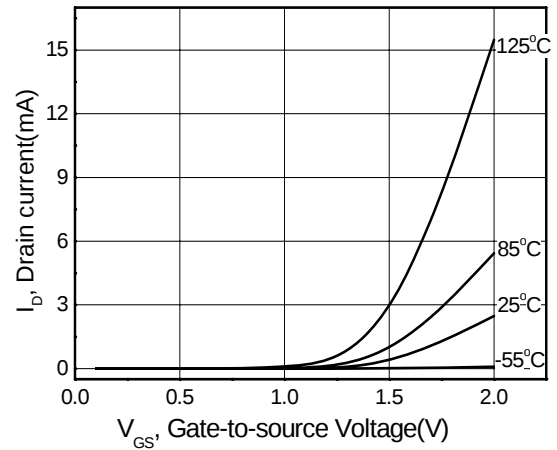


Figure 2. Transfer Characteristics

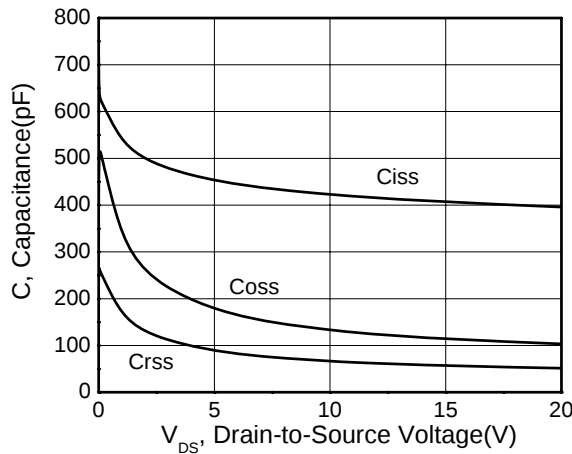


Figure 3. Capacitance

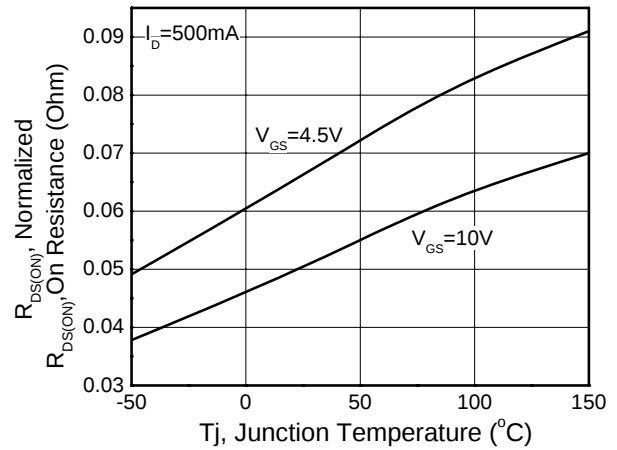


Figure 4. On Resistance Vs. Temperature

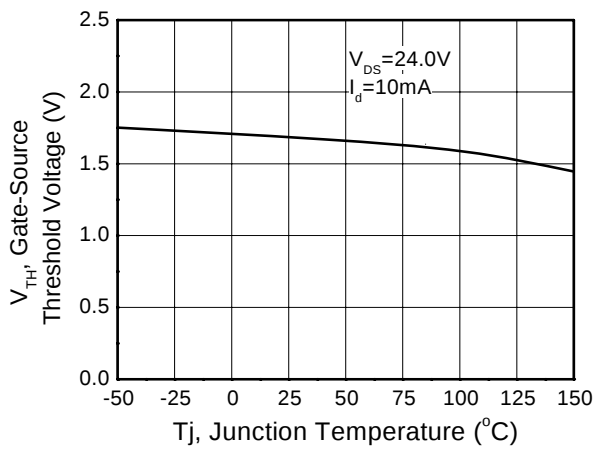


Figure 5. Gate Thershold Vs. Temperature

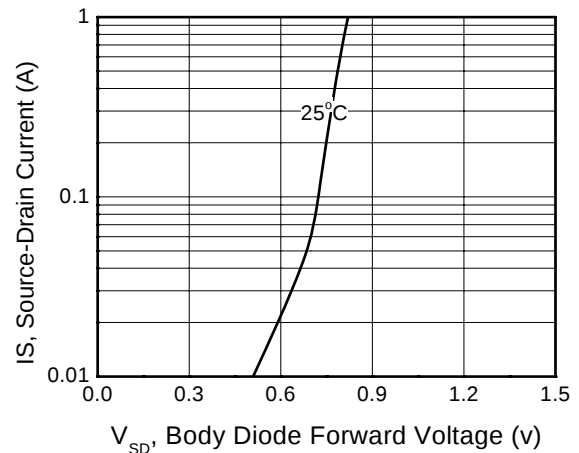


Figure 6. Body Diode Forward Voltage



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