

Pentium/SDRAM Clock Generator with Integrated Buffers

FEATURES

- Generates all clock frequencies for Pentium, AMD and Cyrix system requiring multiple CPU clocks (SDRAM, Shared memory architecture).
- Supports up to 12 Synchronous CPU clocks.
- 6 PCI BUS clocks selectable between synchronous and asynchronous mode.
- One 14.318Mhz reference clock
- One 24Mhz floppy clock and one 48Mhz USB clock.
- Proven power-on strapping techniques to minimize four input pins. In any cases, no glitches will be produced from the output pins during power on.
- 3.3V and 5V operation.
- Available in 300mil 28 pin SOIC and 32 pin SOJ.

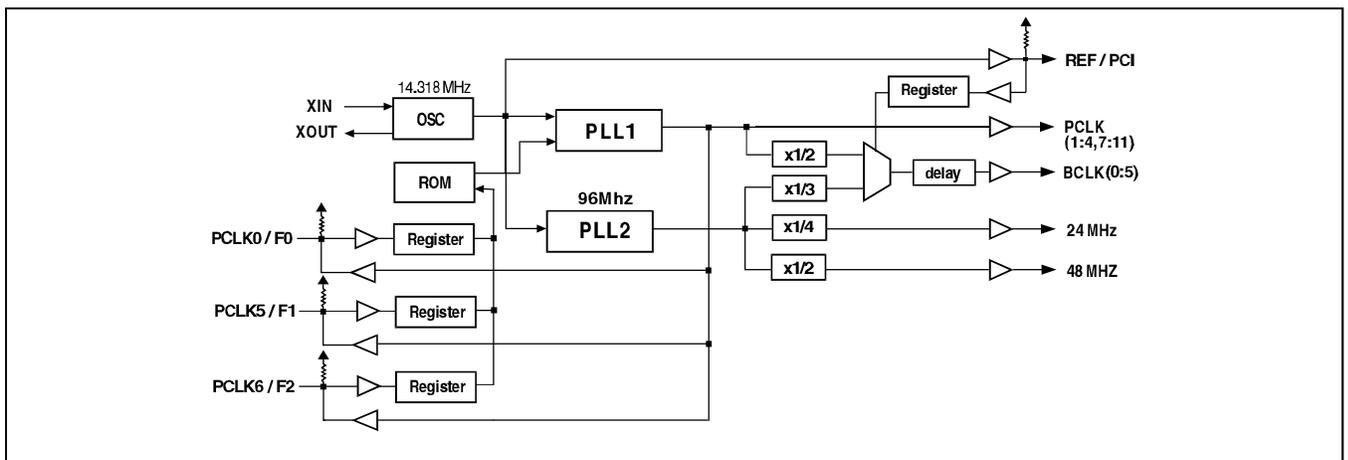
DESCRIPTION

The PLL52C61-01HA and -21HA are high performance system clock generators designed to support INTEL 430VX PCIs set's motherboard with SDRAM Pentium based systems. All output clocks skew and jitter performance are designed to be fully compliant with INTEL Pentium CPU timing requirements.

TIMING SPECIFICATIONS

PCLK-PCLK skew	<250 ps
PCLK-BCLK skew	1~5 ns (PCLK leads)
PCLK,BCLK slew rate	> 1 V/ns (0.4 ~2.4V)
PCLK Jitter	±200 ps cycle-cycle

BLOCK DIAGRAM



PIN INFORMATION

VDD	1	28	REF/PCI	VDD	1	32	REF/PCI
XIN	2	27	48MHz	XIN	2	31	48MHz
XOUT	3	26	24MHz	XOUT	3	30	24MHz
VSS	4	25	VDD	VSS	4	29	VDD
PCLK0/F0	5	24	BCLK5	PCLK0/F0	5	28	BCLK5
PCLK1	6	23	BCLK4	PCLK1	6	27	BCLK4
PCLK2	7	22	VSS	PCLK2	7	26	VSS
CPUVDD	8	21	BCLK3	CPUVDD	8	25	BCLK3
PCLK3	9	20	BCLK2	PCLK3	9	24	BCLK2
PCLK4	10	19	BUSVDD	PCLK4	10	23	BUSVDD
VSS	11	18	BCLK1	VSS	11	22	BCLK1
PCLK5/F1	12	17	BCLK0	PCLK5/F1	12	21	BCLK0
PCLK6/F2	13	16	VSS	PCLK6/F2	13	20	VSS
CPUVDD	14	15	PCLK7	CPUVDD	14	19	PCLK11
				PCLK7	15	18	PCLK10
				PCLK8	16	17	PCLK9

PLL52C61-01HA

PLL52C61-21HA

FREQUENCY SELECTION (MHz)

F2	F1	F0	PCLK (0:11)	BCLK(0:5)	
				PCI=1	PCI=0
0	0	0	50	25	32
0	0	1	60	30	32
0	1	0	66.6	33.3	32
0	1	1	Test	Test	Test
1	0	0	55	27.5	32
1	0	1	75	37.5	32
1	1	0	83.3	41.7	32
1	1	1	68.4	34.2	32

Note: F2,F1,F0 and PCI are selectable only during Power-on. They are HIGH by default and Low when 10K Ω pull-down is attached.

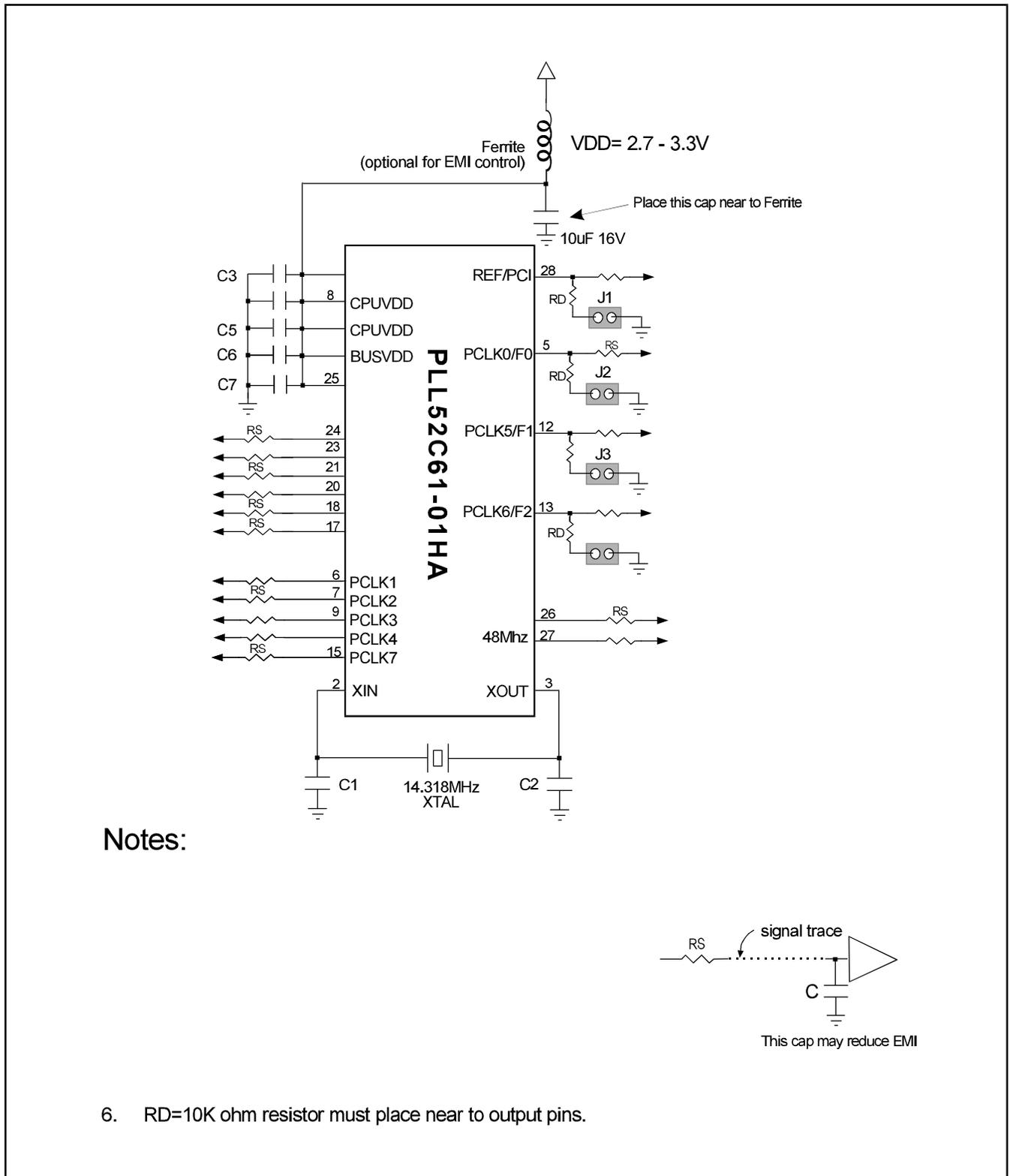
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SIGNAL DESCRIPTIONS

NAME	PIN NUMBER		PIN TYPE	DESCRIPTION
VDD	-01HA	1,25	P	Power supply (3V ~ 5V)
	21HA	1,29		
XIN	2		I	14.318Mhz crystal input to be connected to one end of the crystal. This input can also be connected directly to other available source of 14.318Mhz from the PC board. During TEST mode, this pin is served as TCLK input and can be driven externally.
XOUT	3		O	14.318Mhz crystal output
VSS	-01HA	4,11,16,22	P	Ground.
	-21HA	4,11 20,26		
PCLK0/F0	5		B	At power-up, these pins act as input and the default value are HIGH. If any of these pins is connected to a pull down of 10K ohm resistor, the input will be considered as LOW. After the input sampling, these three pins will generate CPU clocks (see FREQUENCY SELECTION).
PCLK5/F1	12			
PCLK6/F2	13			
PCLK(1:4,7)	6,7,9,10,15		O	CPU clock output, In TEST mode, these pins generate TCLK/4 output frequency.
PCLK(8:11)	-21HA	16,17,18,19	O	
CPUVDD	8,14		P	VDD for PCLK output pins
BCLK(0:5)	-01HA	17,18,20 21,23,24	O	PCI bus clock output. In TEST mode, these pins generate TCLK/8 output frequency.
	-21HA	21,22,24 25,27,28		
BUSVDD	-01HA	19	P	VDD for bus clock output pins.
	-21HA	23		
24Mhz	-01HA	26	O	Fixed output at 24Mhz for disk controller or super I/O applications. In TEST mode, this pin generates TCLK/8 frequency.
	-21HA	30		
48 Mhz	-01HA	27	O	Fixed output at 48Mhz for USB applications. In TEST mode, this pin generates TCLK/4 frequency.
	-21HA	31		
REF/PCI	-01HA	28	B	At power-on, this pin acts as input and the default value is HIGH. If this pin is connected to pull down of 10K ohm resistor, the input will be considered as LOW and setting BUS clock to asynchronous mode (see FREQUENCY SELECTION table). After the input sampling, this pin will generate 14.318Mhz buffered reference clock. In TEST mode, this pin generates TCLK reference frequency.
	-21HA	32		

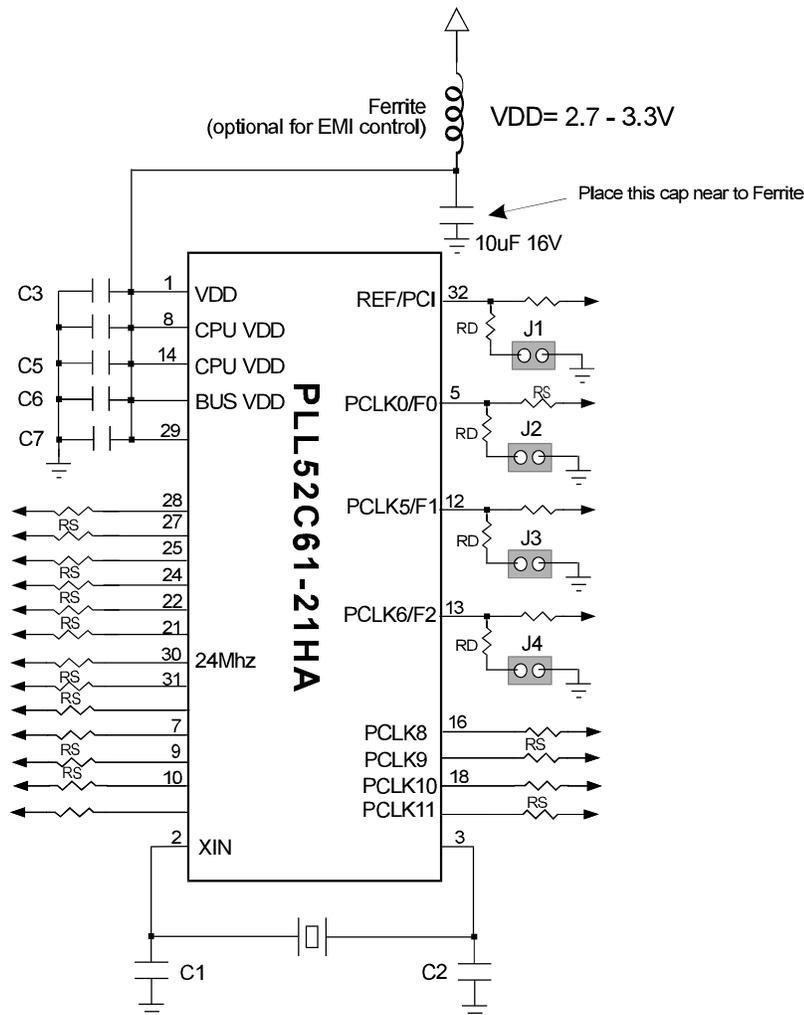
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APPLICATION CIRCUITS FOR P52C61-01HA



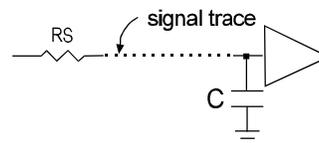
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APPLICATION CIRCUITS FOR P52C61-21HA



Notes:

1. J1: Bus clock mode selection jumper
2. J2-J4: Frequency selection jumpers
3. C1-C2: (optional) for fine tuning the crystal frequency.
4. RS: Series clock terminating resistor is recommended using 22 ohm resistor. To further reduce signal ringing and EMI, a capacitor could be placed near the receiving end of the clock line. (as the drawing shows)
5. C3-C7 are 0.1uF power bypass capacitors, should be placed as close to each VDD pin as physically possible.
6. RD=10K ohm must place near to output pins.



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MAXIMUM RATINGS

SUPPLY VOLTAGE	VSS-0.5 TO 7V
INPUT VOLTAGE	VSS-0.5V to VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	0.75W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

AC SPECIFICATIONS

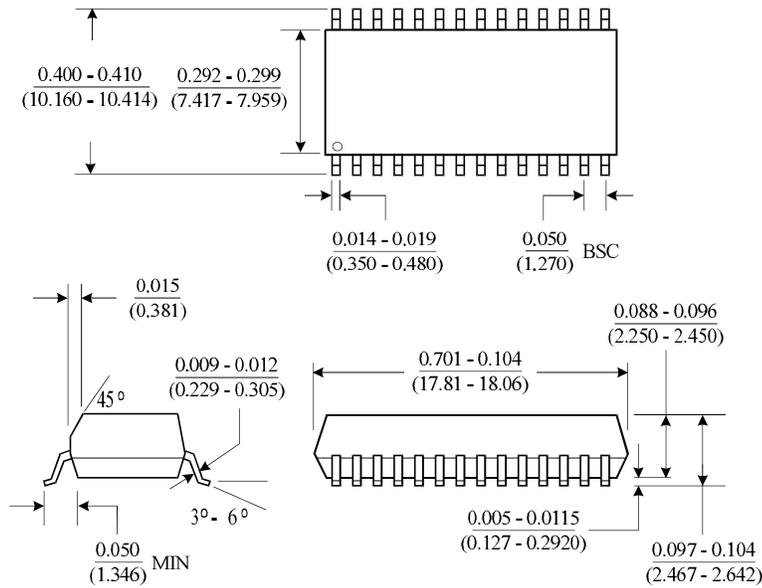
VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference input clock rise time	T _{IR}	From 0.8 V to 2V			20	ns
Reference input clock fall time	T _{IF}	From 2V to 0.8V			20	ns
Output rise time	T _{OR}	From 0.8V to 2V 25pF load		1	2	ns
		From 10% to 90% 25pF load		2	4	ns
Output fall time	T _{OF}	From 2V to 0.8V 25pF load		1	2	ns
		From 90% to 10% 25pF load		2	4	ns
Duty cycle	D _T	15pF load.	45	50/50	55	%
Clock Skew (20pF load, @ 1.4V)	T _{SKW}	PCLK to PCLK		50	250	ps
		BCLK to BCLK		90	500	ps
		PCLK to BCLK	1	2	5	ns
Jitter, Absolute (20pF load)	T _{JA}	PCLK, BCLK	-250		250	ps
Jitter, One Sigma (20pF load)	T _{JO}	PCLK, BCLK		50	200	ps

DC SPECIFICATIONS

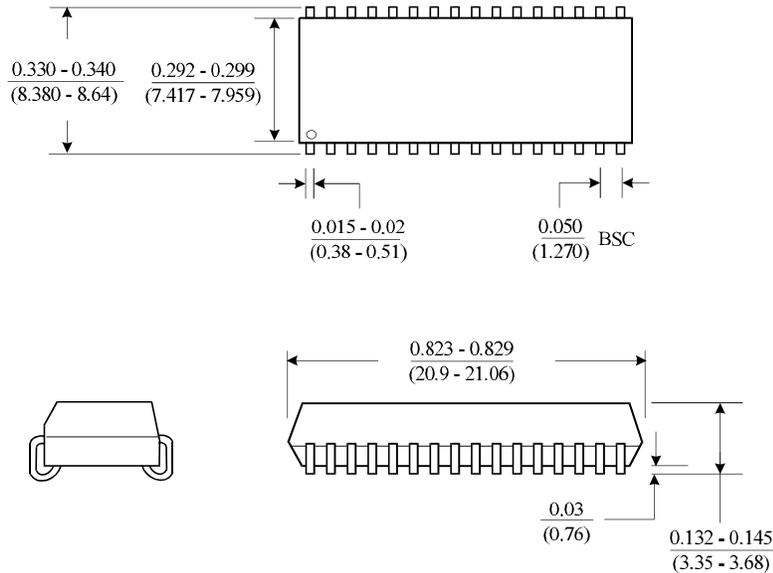
VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Current	I _{DYN}	PCLK at 66.6 MHz no load		55	110	mA
Static Current	I _{STAT}	All internal circuitry off, XIN=0		25	50	μA
Input High Voltage	V _{IH}	All Inputs except XIN	2			V
Input Low Voltage	V _{IL}	All Inputs except XIN			0.8	V
Output High Current @VOH=2.0V	I _{OH}	PCLK(0:11), BCLK(0:5)		-50		mA
		24Mhz, 48Mhz, REF/PCI		-35		mA
Output Low Current @VOL=0.4V	I _{OL}	PCLK(0:11), BCLK(0:5)		35		mA
		24Mhz, 48Mhz, REF/PCI		25		mA
Pull-up resistor	R _{Pu}	Pin PCLK0/F0,PCLK5/F1,PCLK6/F2,REF/PCI		25		Kohm
Output Impedance	R _O	PCLK(0:11), BCLK(0:5)		30		ohm

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PACKAGE INFORMATION



28 PIN SOIC



32 PIN SOJ

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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

45437 Warm Springs Blvd., Fremont, CA 94539, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
device number, package type and operating temperature range.

PLL52C61-XXHA S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL

PACKAGE TYPE
S=SOIC, J=SOJ

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