



FDD8453LZ

N-Channel PowerTrench[®] MOSFET

40V, 50A, 6.7mΩ

Features

- Max $r_{DS(on)}$ = 6.7mΩ at $V_{GS} = 10V$, $I_D = 15A$
- Max $r_{DS(on)}$ = 8.7mΩ at $V_{GS} = 4.5V$, $I_D = 13A$
- HBM ESD protection level >7kV typical (Note 4)
- RoHS Compliant

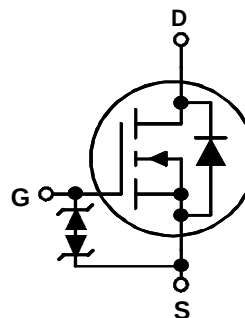
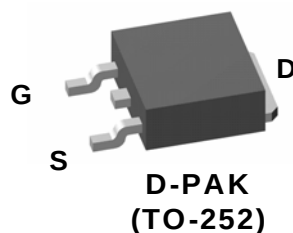


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

Applications

- Inverter
- Synchronous Rectifier



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	50	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	75	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	16.4	
	-Pulsed	100	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	253	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	65	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8453LZ	FDD8453LZ	D-PAK (TO-252)	13"	16mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		36		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}$, $V_{GS} = 0\text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6.0		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 15\text{A}$		5.8	6.7	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 13\text{A}$		6.8	8.7	
		$V_{GS} = 10\text{V}$, $I_D = 15\text{A}$, $T_J = 125^\circ\text{C}$		9.1	10.6	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}$, $I_D = 15\text{A}$		77		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		2640	3515	pF
C_{oss}	Output Capacitance			320	425	pF
C_{rss}	Reverse Transfer Capacitance			190	285	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		2.3		Ω

Switching Characteristics

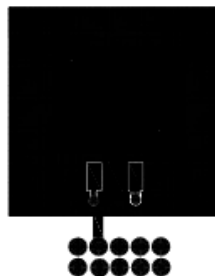
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}$, $I_D = 15\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$		11	19	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			37	58	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 20\text{V}$, $I_D = 15\text{A}$	46	64	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{V}$ to 5V		24	33	nC
Q_{gs}	Gate to Source Charge			7		nC
Q_{gd}	Gate to Drain "Miller" Charge			8		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = 2.0\text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{V}$, $I_S = 15\text{A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 15\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		25	40	ns
Q_{rr}	Reverse Recovery Charge			20	32	nC

Notes:

- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3: Starting $T_J = 25^\circ\text{C}$, $L = 3\text{mH}$, $I_{AS} = 13\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$.

4: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

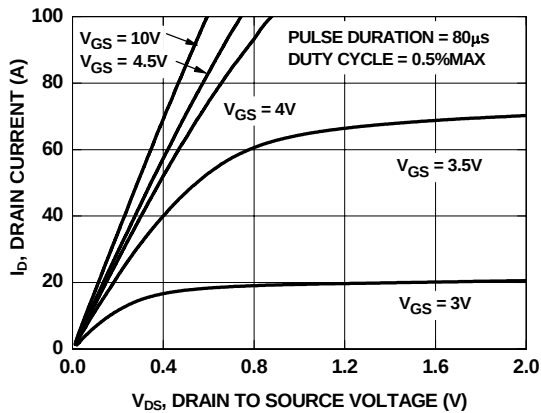


Figure 1. On-Region Characteristics

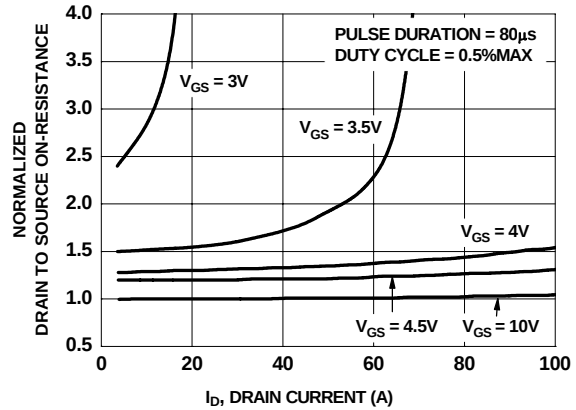


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

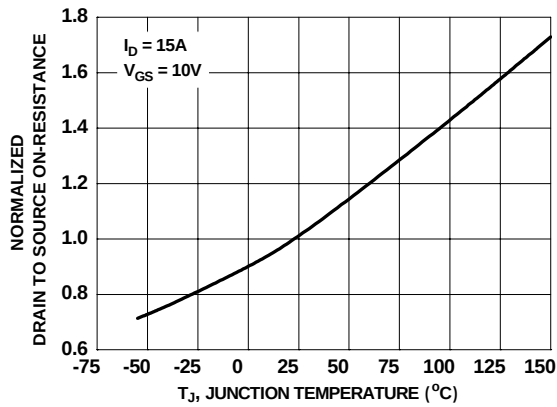


Figure 3. Normalized On-Resistance vs Junction Temperature

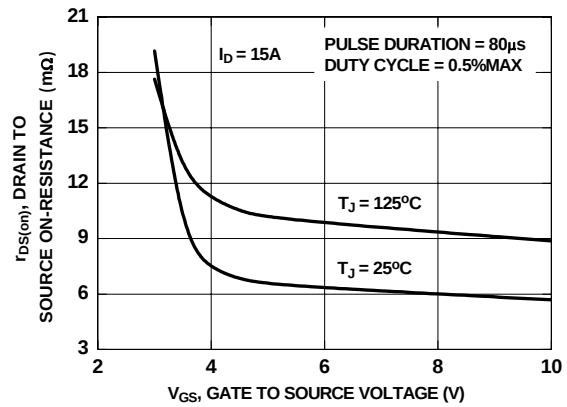


Figure 4. On-Resistance vs Gate to Source Voltage

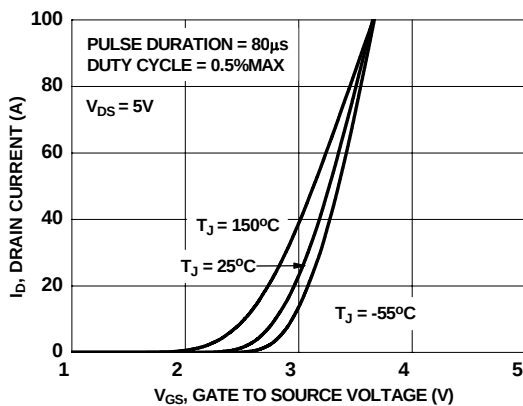


Figure 5. Transfer Characteristics

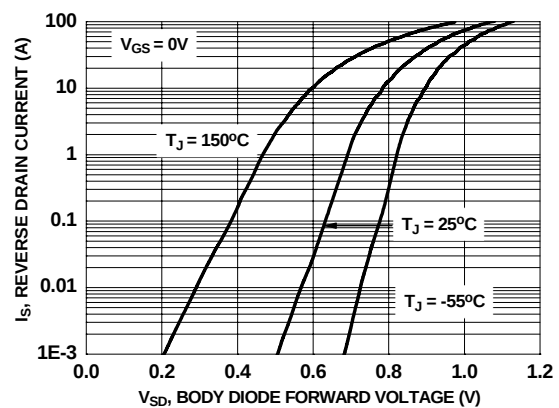


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

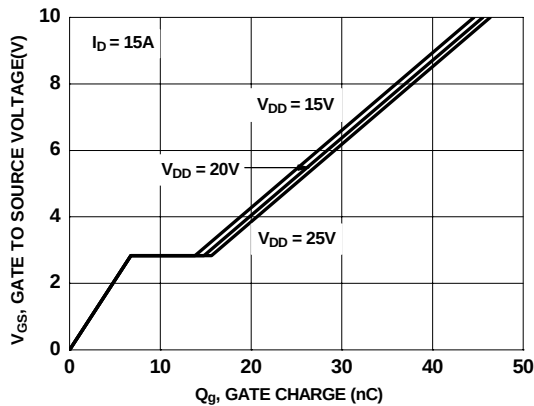


Figure 7. Gate Charge Characteristics

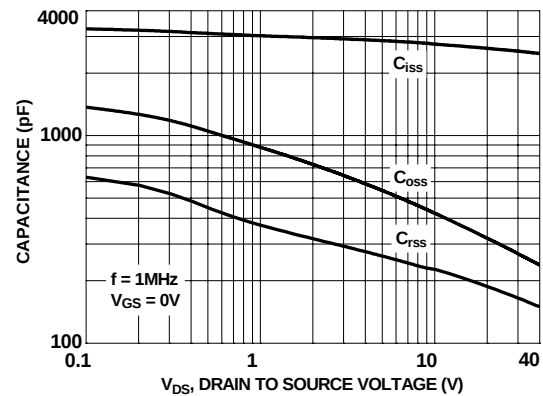


Figure 8. Capacitance vs Drain to Source Voltage

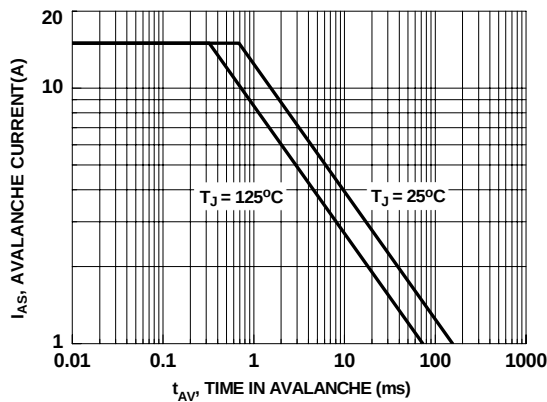


Figure 9. Unclamped Inductive Switching Capability

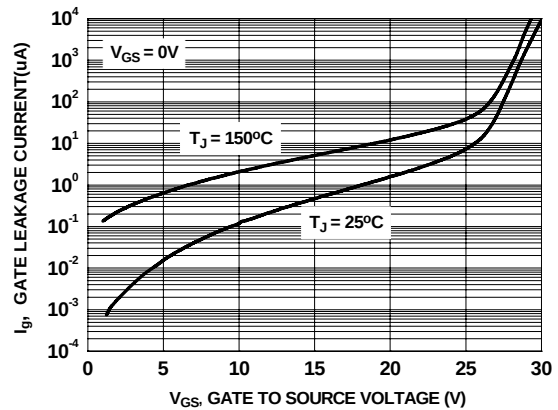


Figure 10. Gate Leakage Current vs Gate to Source Voltage

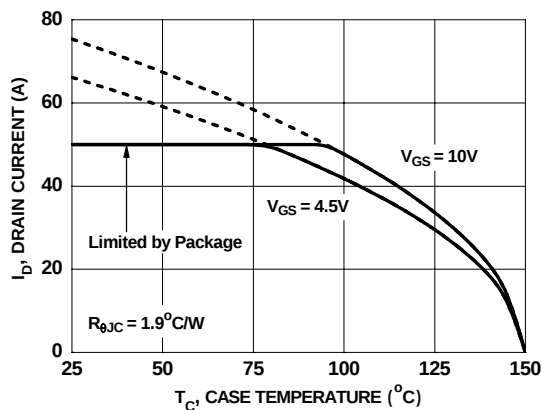


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

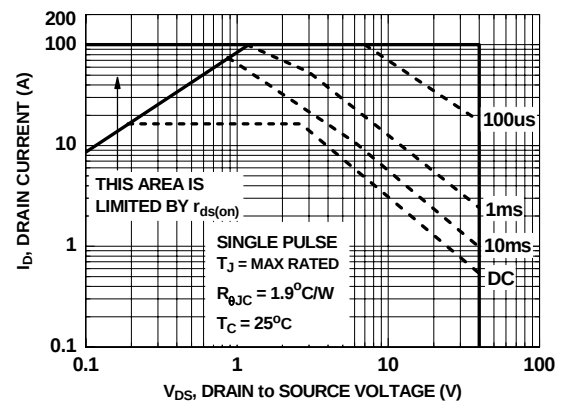


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

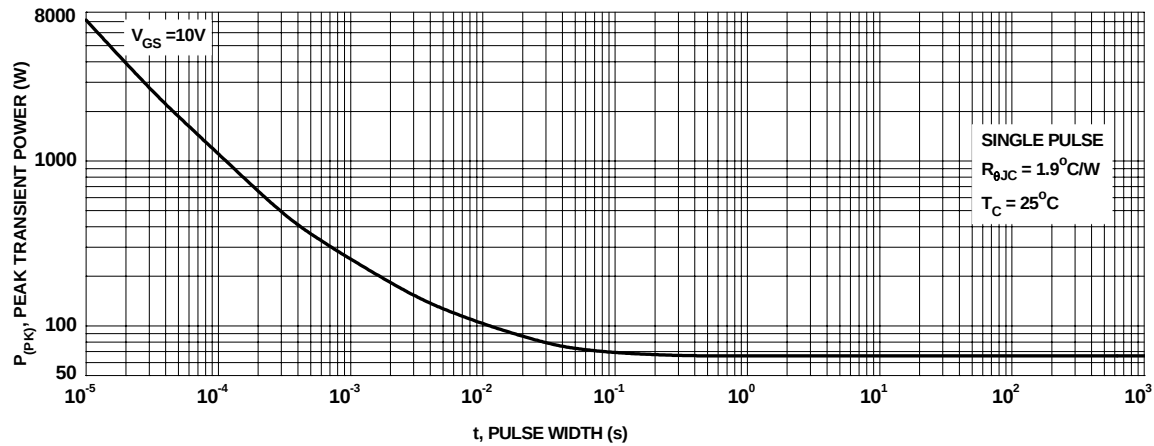


Figure 13. Single Pulse Maximum Power Dissipation

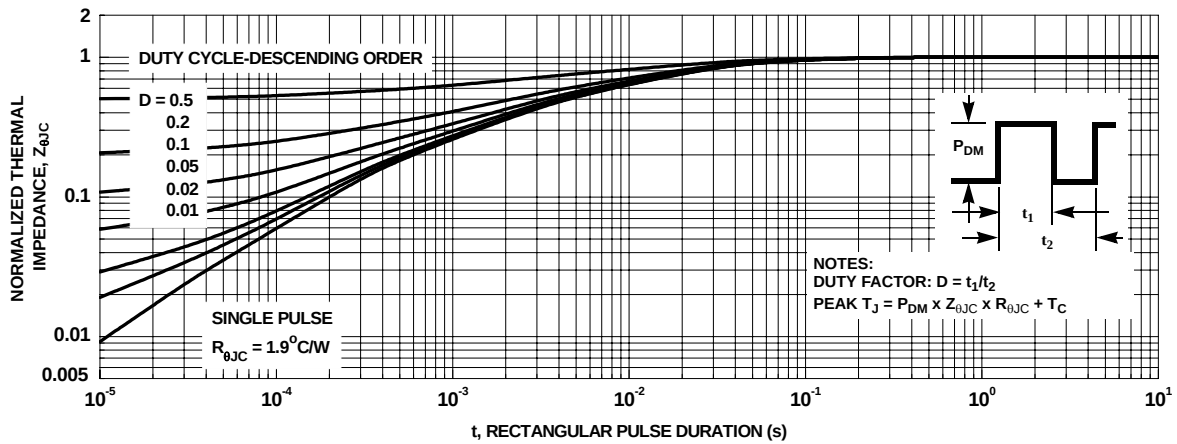


Figure 14. Transient Thermal Response Curve

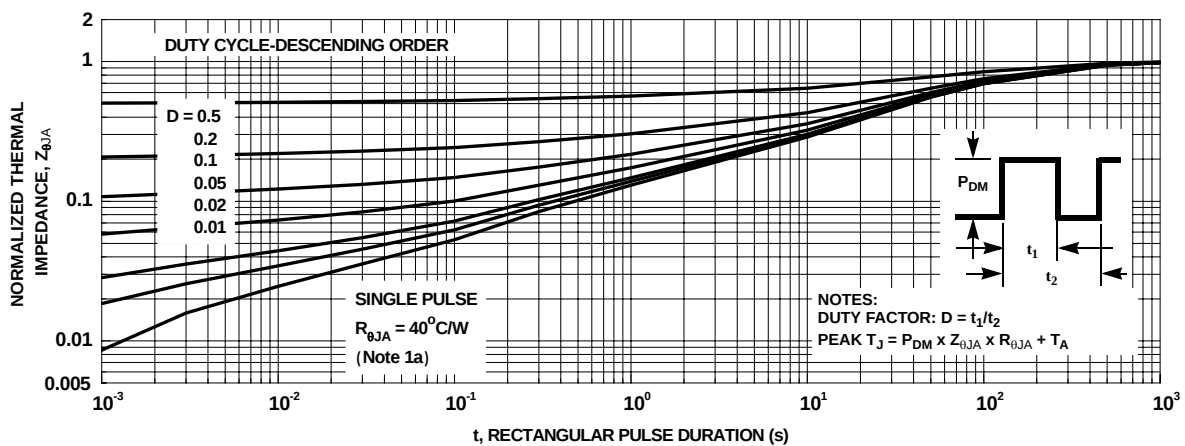
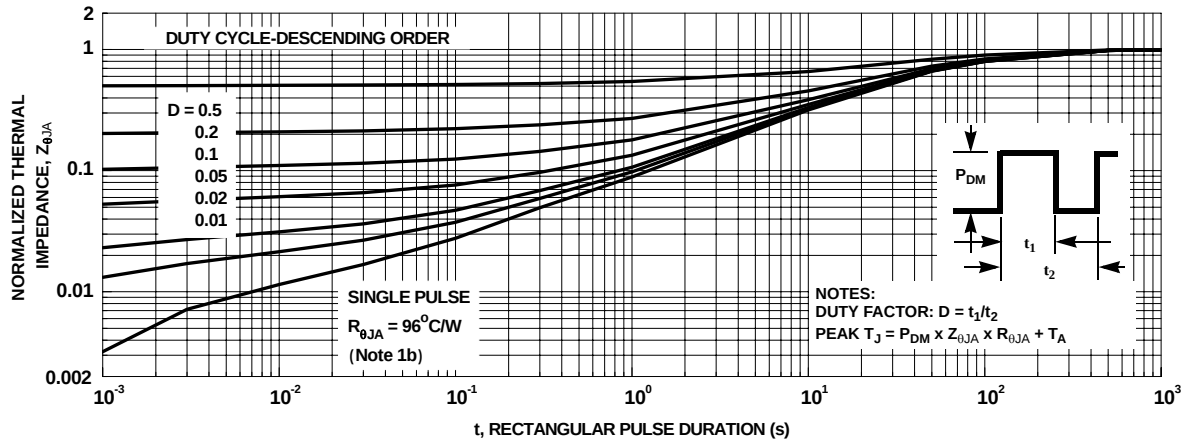
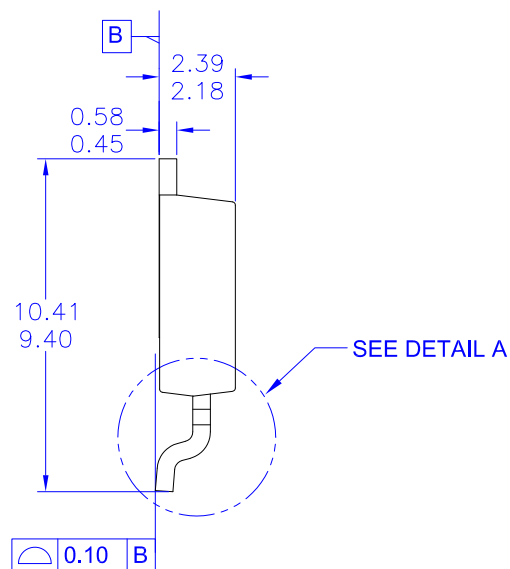
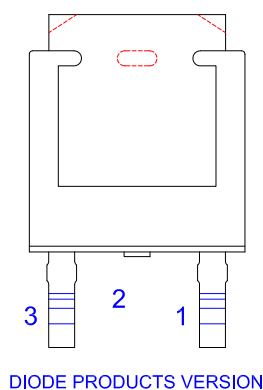
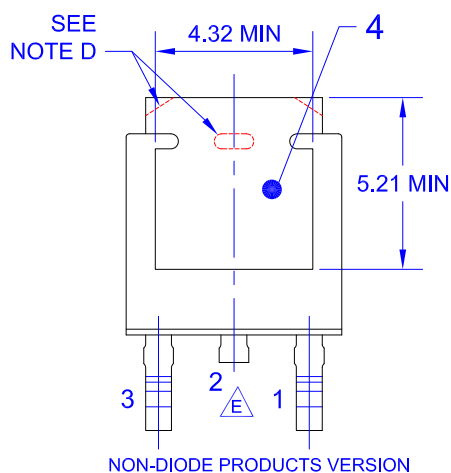
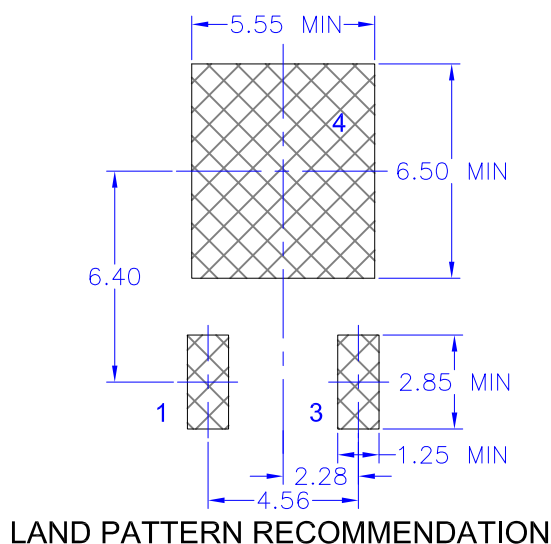
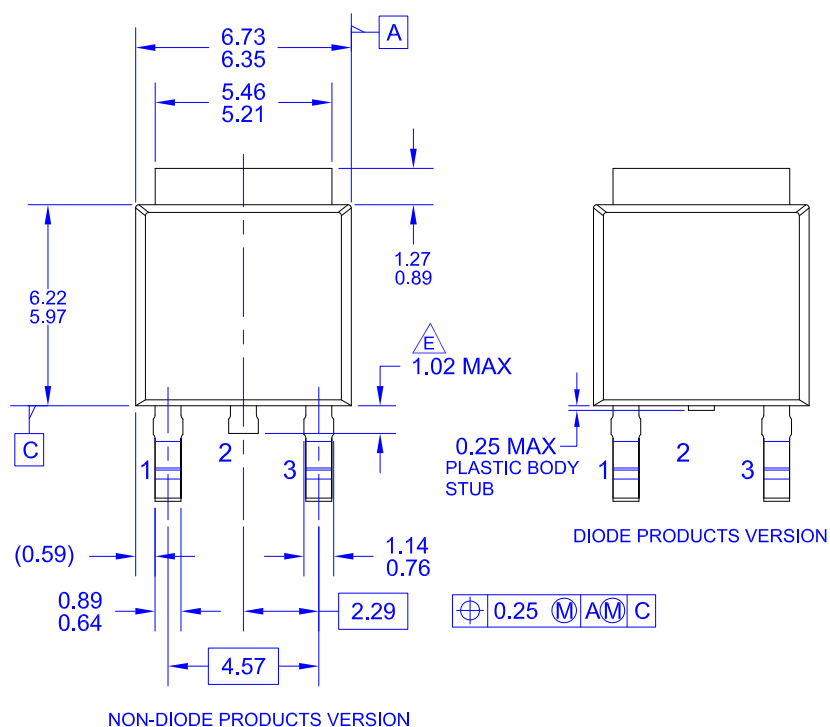


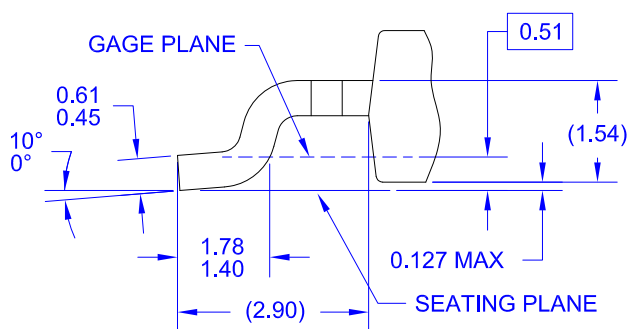
Figure 15. Transient Thermal Response Curve

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted





- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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