

MOS FIELD EFFECT TRANSISTOR
 NP80N055CLE, NP80N055DLE, NP80N055ELE

SWITCHING
 N-CHANNEL POWER MOS FET
 INDUSTRIAL USE

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 11 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
 $R_{DS(on)2} = 13 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 40 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2900 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N055CLE	TO-220AB
NP80N055DLE	TO-262
NP80N055ELE	TO-263

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

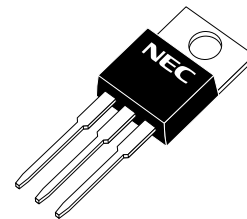
Drain to Source Voltage	V_{DSS}	55	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC) ^{Note1}	$I_{D(DC)}$	± 80	A
Drain Current (Pulse) ^{Note2}	$I_{D(pulse)}$	± 200	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	120	W
Single Avalanche Current ^{Note3}	I_{AS}	45 / 30 / 10	A
Single Avalanche Energy ^{Note3}	E_{AS}	2.0 / 90 / 100	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

- Notes**
1. Calculated constant current according to MAX. allowable channel temperature.
 2. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$ (see Figure 4.)

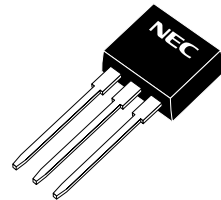
THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.25	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

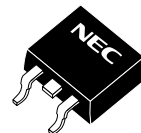
(TO-220AB)



(TO-262)



(TO-263)

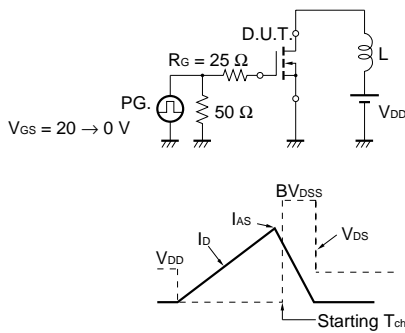


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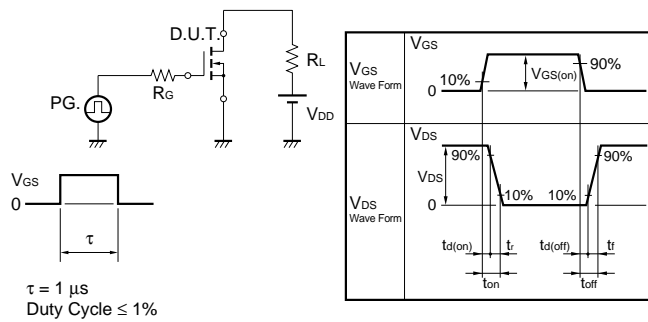
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 40 A		8.4	11	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 40 A		10.3	13	mΩ
	R _{DS(on)3}	V _{GS} = 4.5 V, I _D = 40 A		11.3	15	mΩ
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 40 A	20	40		S
Drain Leakage Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		2900	4400	pF
Output Capacitance	C _{oss}			380	570	pF
Reverse Transfer Capacitance	C _{rss}			170	310	pF
Turn-on Delay Time	t _{d(on)}	I _D = 40 A, V _{GS(on)} = 10 V, V _{DD} = 28 V, R _G = 1 Ω		22	48	ns
Rise Time	t _r			10	25	ns
Turn-off Delay Time	t _{d(off)}			62	120	ns
Fall Time	t _f			11	27	ns
Total Gate Charge 1	Q _{G1}		I _D = 80 A, V _{DD} = 44 V, V _{GS} = 10 V		50	75
Total Gate Charge 2	Q _{G2}	I _D = 80 A, V _{DD} = 44 V, V _{GS} = 5 V		26	39	nC
Gate to Source Charge	Q _{GS}			12		nC
Gate to Drain Charge	Q _{GD}			15		nC
Body Diode Forward Voltage	V _{F(S-D)}		I _F = 80 A, V _{GS} = 0 V		1.0	
Reverse Recovery Time	t _{rr}	I _F = 80 A, V _{GS} = 0 V, di/dt = 100 A/μs		50		ns
Reverse Recovery Charge	Q _{rr}			100		nC

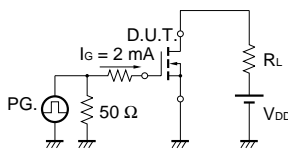
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

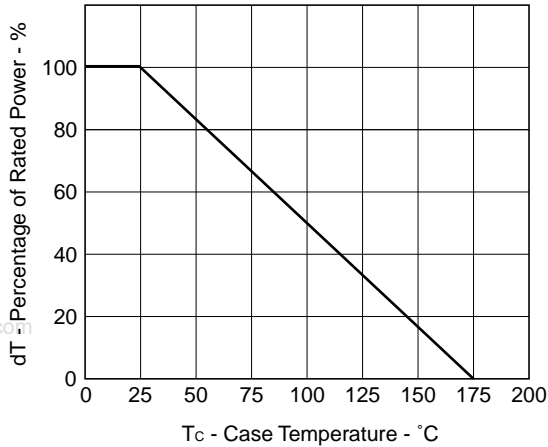
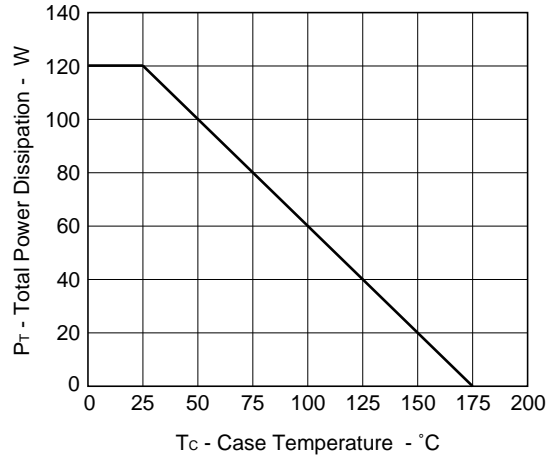


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



★ Figure3. FORWARD BIAS SAFE OPERATING AREA

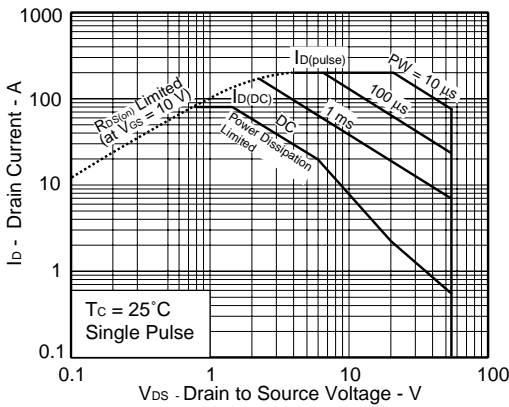


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

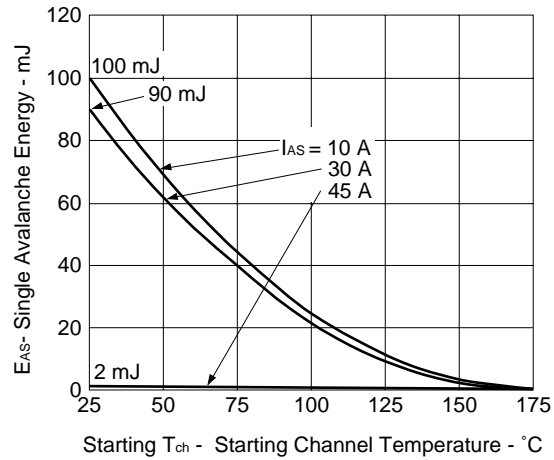


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

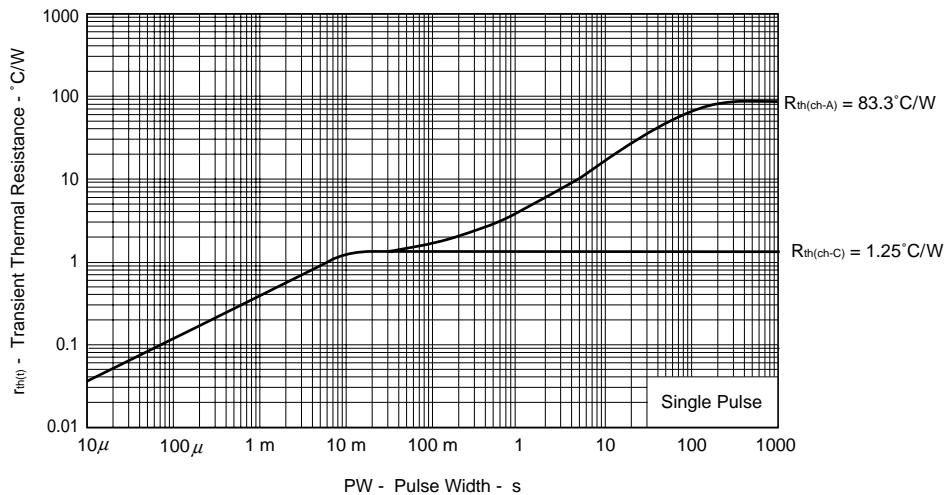
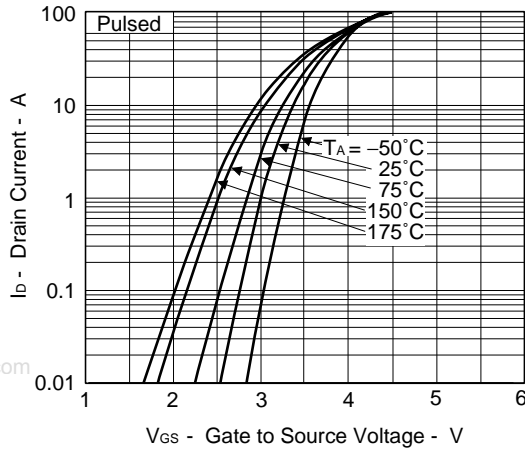


Figure6. FORWARD TRANSFER CHARACTERISTICS



★ Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

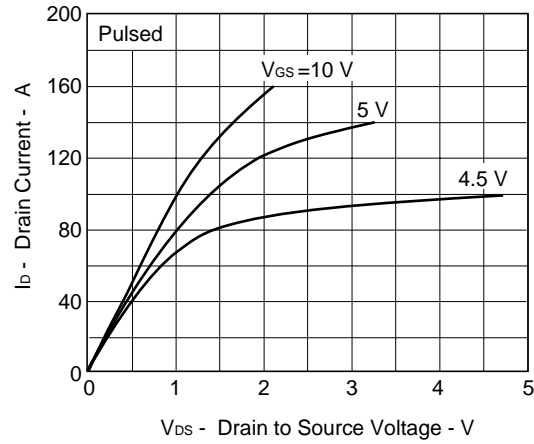


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

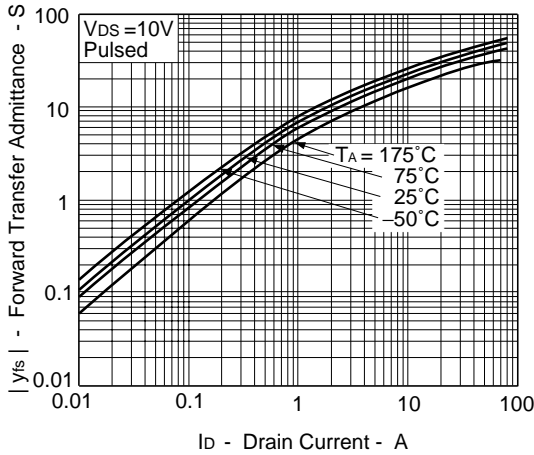


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

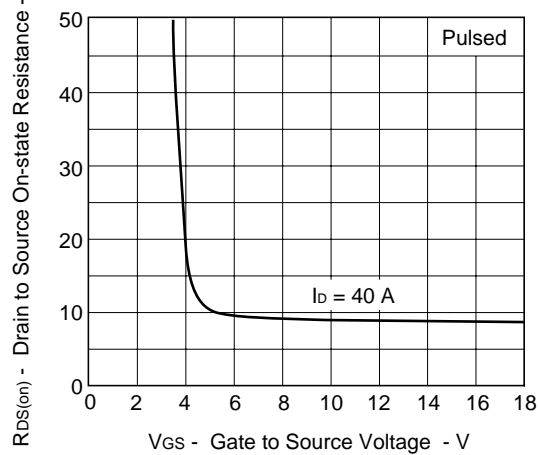


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

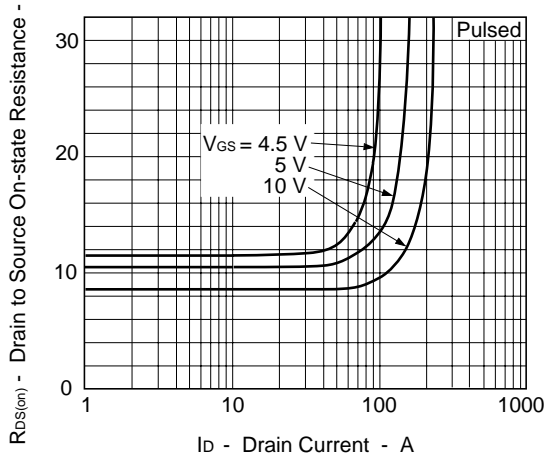


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

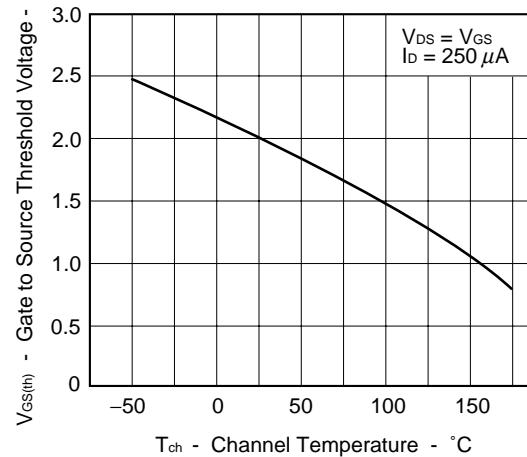


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs CHANNEL TEMPERATURE

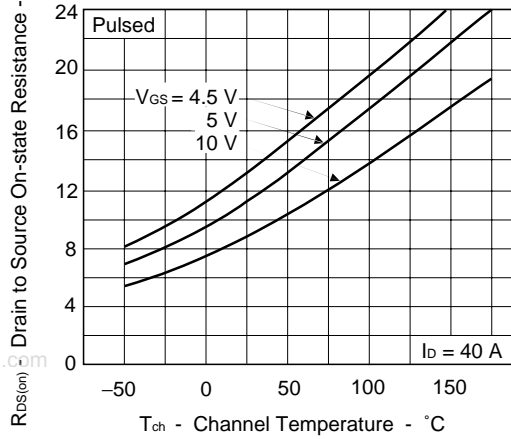


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

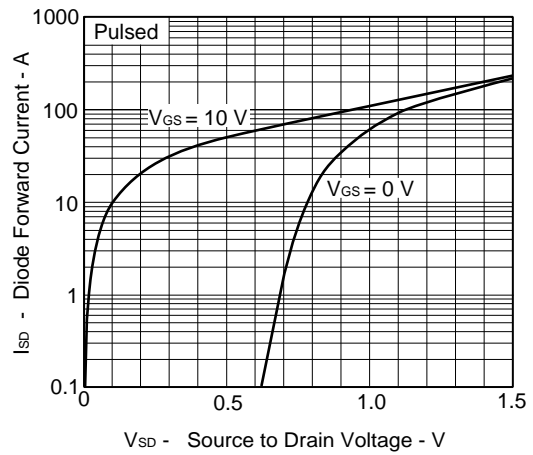


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

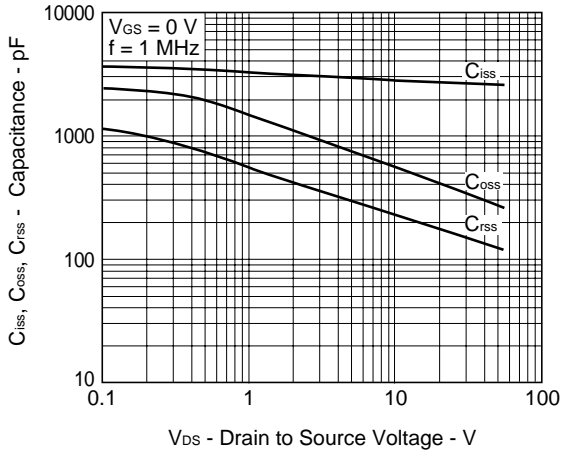


Figure15. SWITCHING CHARACTERISTICS

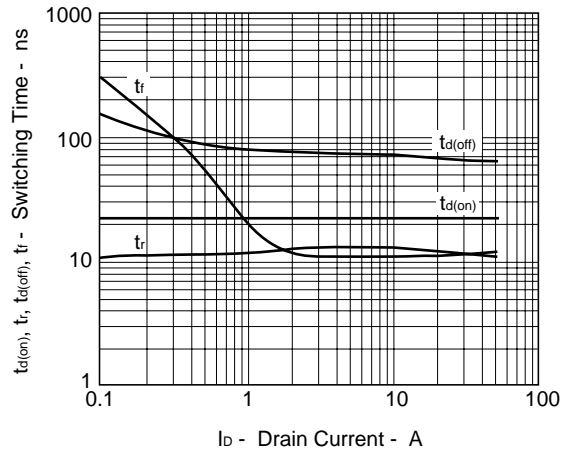


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

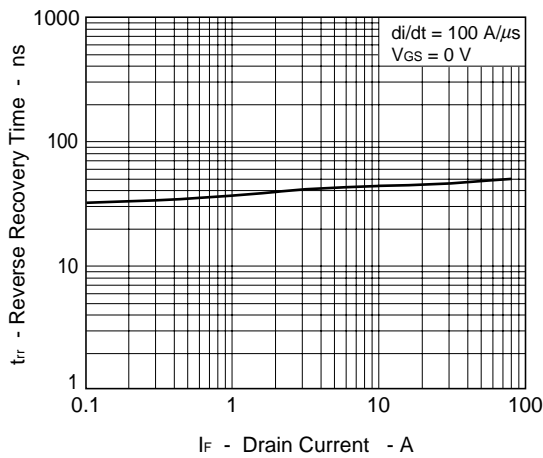
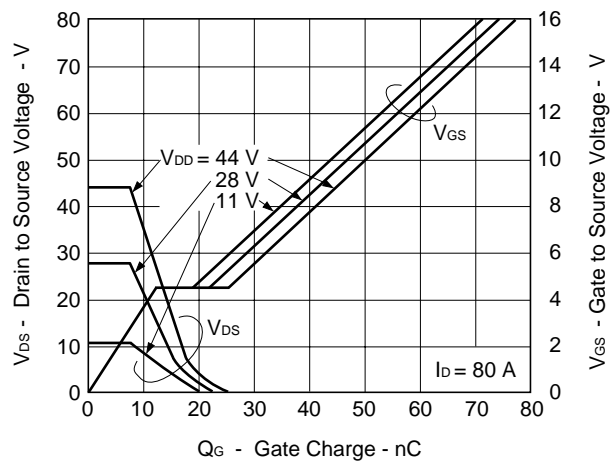
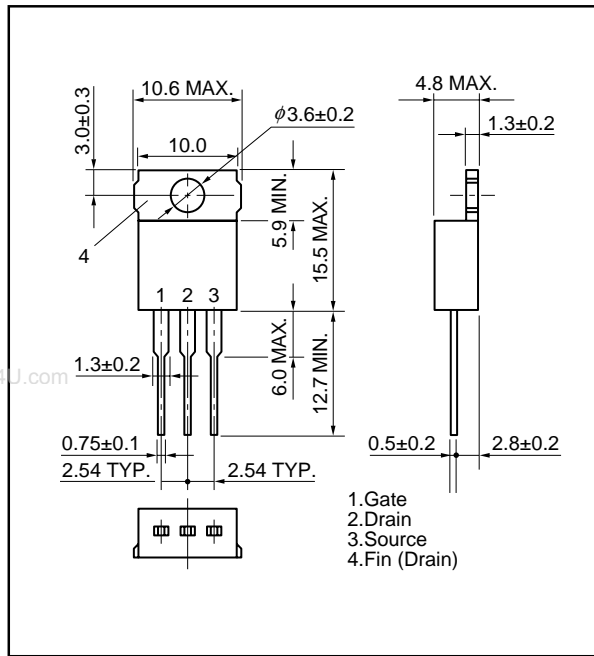


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

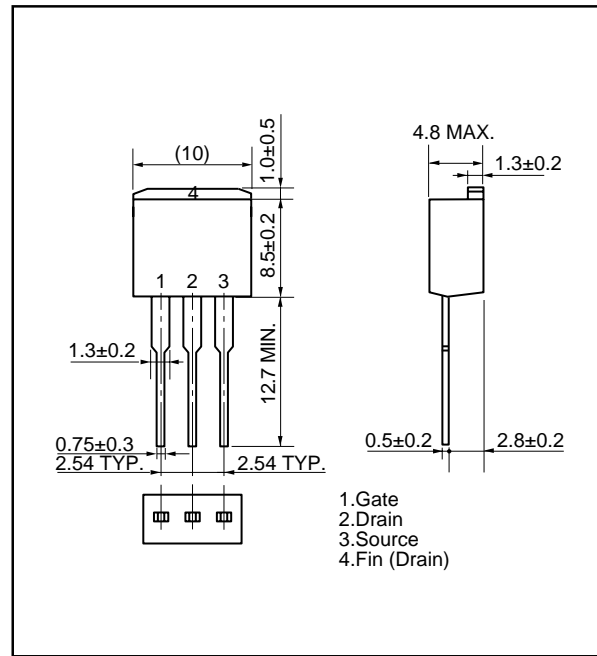


PACKAGE DRAWINGS (Unit: mm)

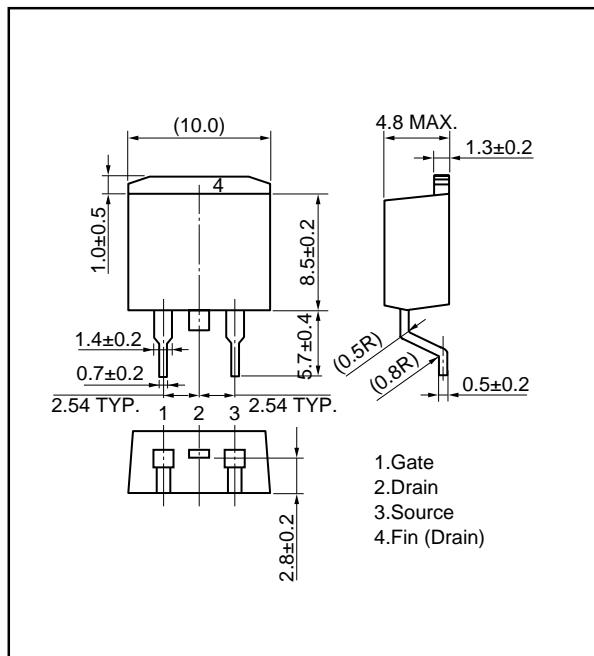
1) TO-220AB (MP-25)



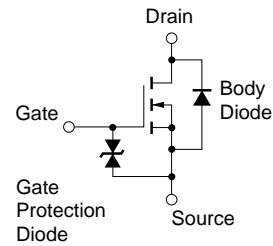
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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