

NTD6414AN, NVD6414AN

N-Channel Power MOSFET 100 V, 32 A, 37 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DS}	100	V	
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	32	A
		$T_C = 100^\circ\text{C}$	22	
Power Dissipation $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	100	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	117	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	32	A	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_{L(pk)} = 32 \text{ A}$, $L = 0.3 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	154	mJ	
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	1.5	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	37	

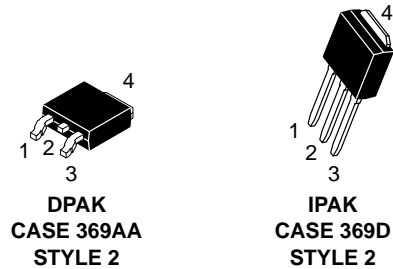
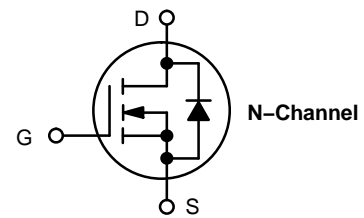
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).



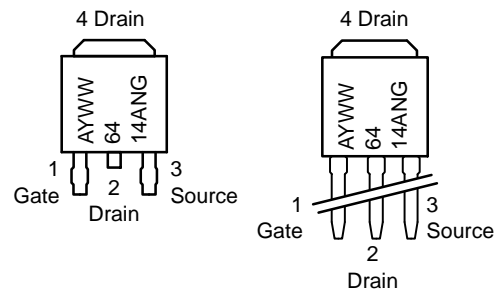
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
100 V	37 mΩ @ 10 V	32 A



MARKING DIAGRAM & PIN ASSIGNMENTS



- A = Assembly Location*
- Y = Year
- WW = Work Week
- 6414AN = Device Code
- G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD6414AN, NVD6414AN

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			107		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25°C			1.0	μA
			T _J = 125°C				100
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V				±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			8.3		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 32 A		30	37	mΩ
Forward Transconductance	g _{FS}	V _{GS} = 5.0 V, I _D = 10 A		18		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		1450		pF	
Output Capacitance	C _{OSS}			230			
Reverse Transfer Capacitance	C _{RSS}			95			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 80 V, I _D = 32 A		40		nC	
Threshold Gate Charge	Q _{G(TH)}			1.7			
Gate-to-Source Charge	Q _{GS}			8.0			
Gate-to-Drain Charge	Q _{GD}			20			
Plateau Voltage	V _{GP}			5.9			V
Gate Resistance	R _G			1.9			Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 80 V, I _D = 32 A, R _G = 6.1 Ω		11		ns
Rise Time	t _r			52		
Turn-Off Delay Time	t _{d(off)}			38		
Fall Time	t _f			48		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 32 A	T _J = 25°C	0.87	1.2	V
			T _J = 125°C	0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 32 A		68		ns
Charge Time	T _a			51		
Discharge Time	T _b			16		
Reverse Recovery Charge	Q _{RR}			195		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD6414AN, NVD6414AN

TYPICAL CHARACTERISTICS

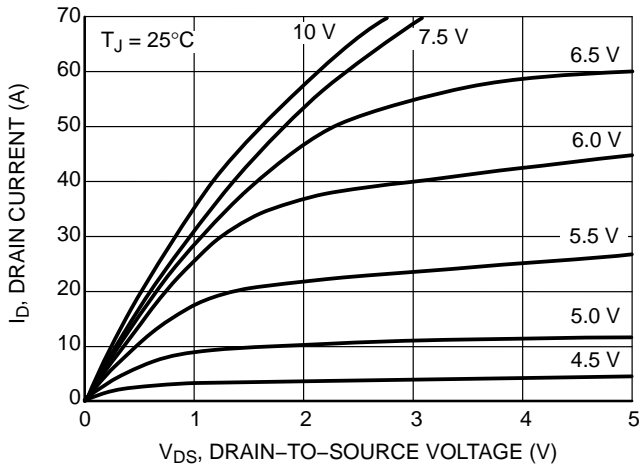


Figure 1. On-Region Characteristics

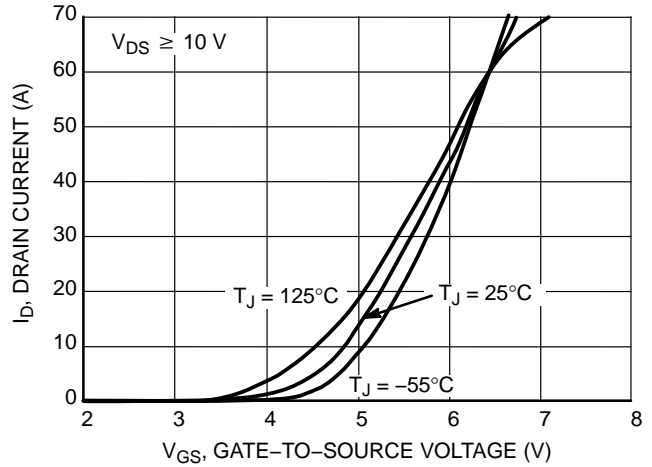


Figure 2. Transfer Characteristics

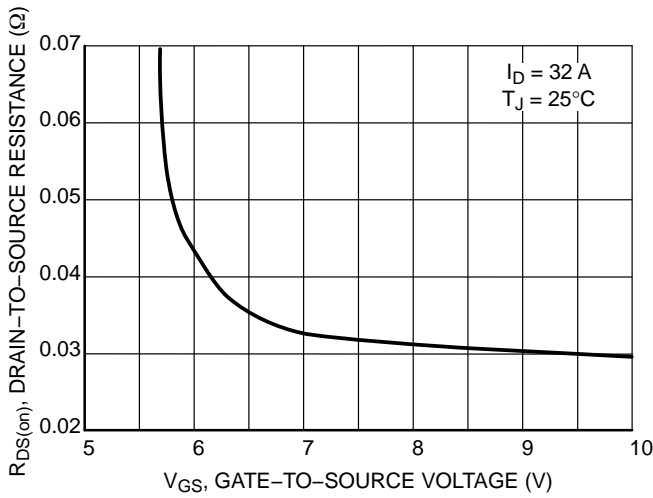


Figure 3. On-Region versus Gate Voltage

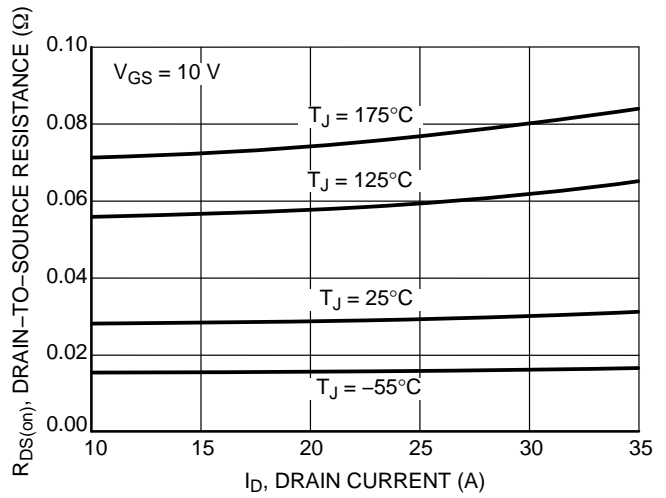


Figure 4. On-Resistance versus Drain Current and Gate Voltage

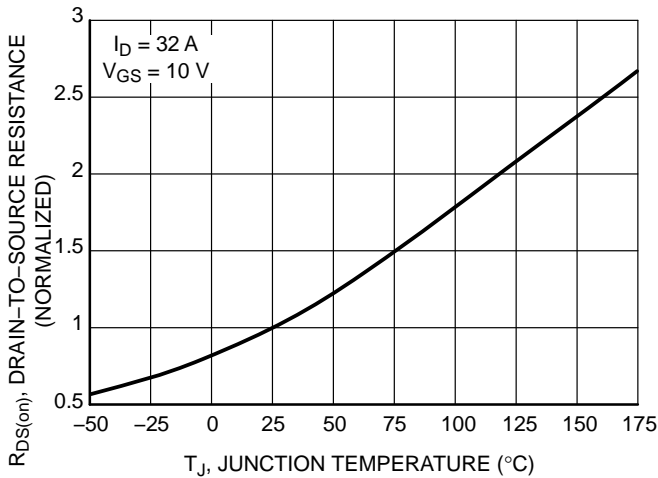


Figure 5. On-Resistance Variation with Temperature

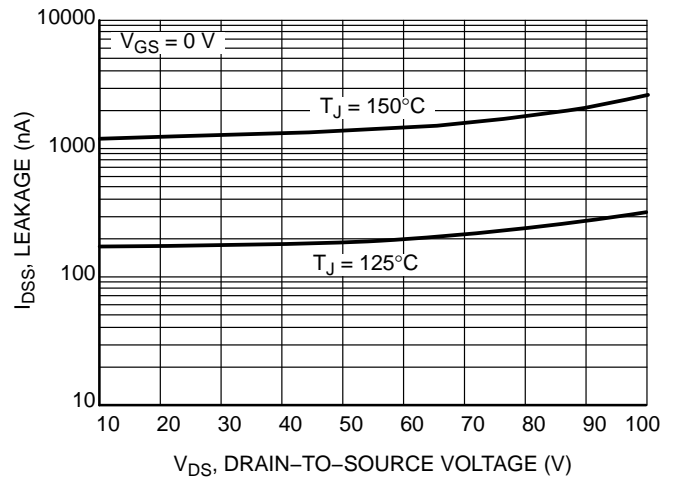


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD6414AN, NVD6414AN

TYPICAL CHARACTERISTICS

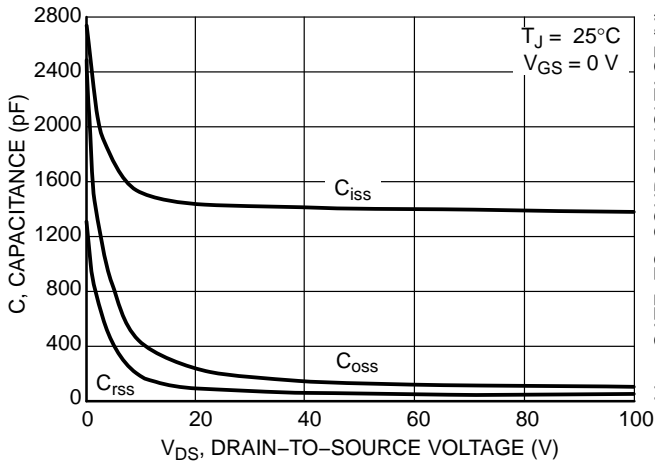


Figure 7. Capacitance Variation

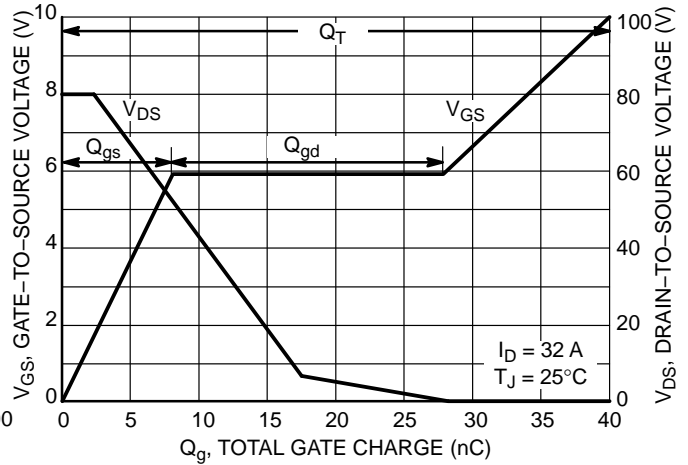


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

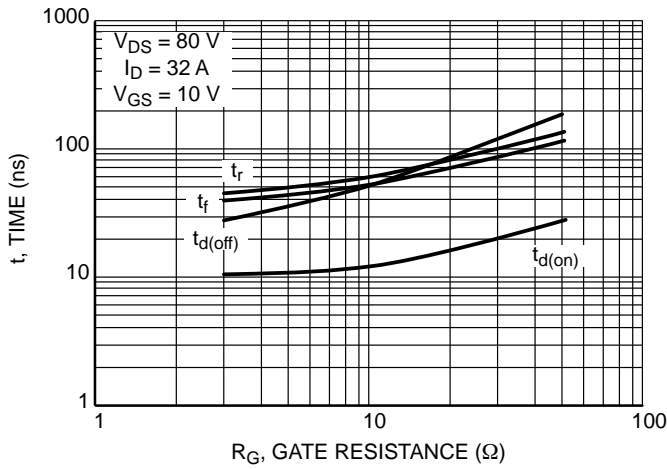


Figure 9. Resistive Switching Time Variation versus Gate Resistance

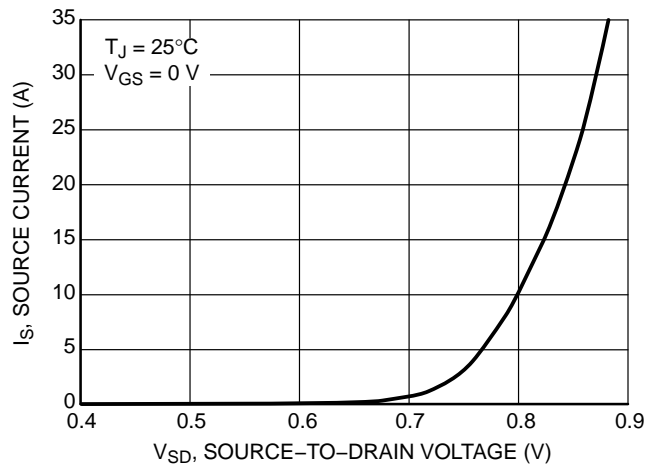


Figure 10. Diode Forward Voltage versus Current

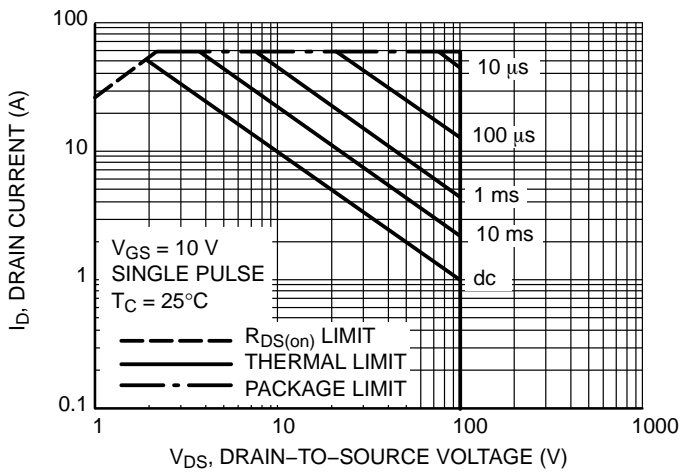


Figure 11. Maximum Rated Forward Biased Safe Operating Area

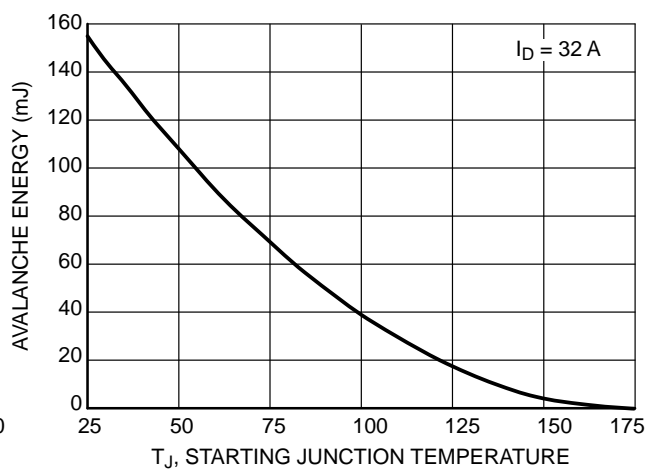


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTD6414AN, NVD6414AN

TYPICAL CHARACTERISTICS

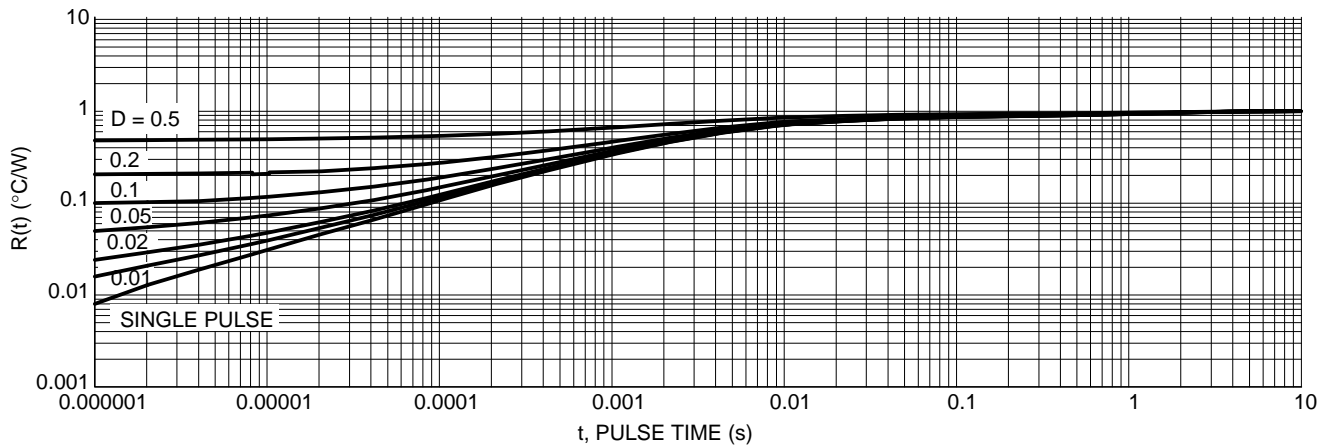


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTD6414ANT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD6414AN-1G	IPAK (Pb-Free)	75 Units / Rail
NVD6414ANT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

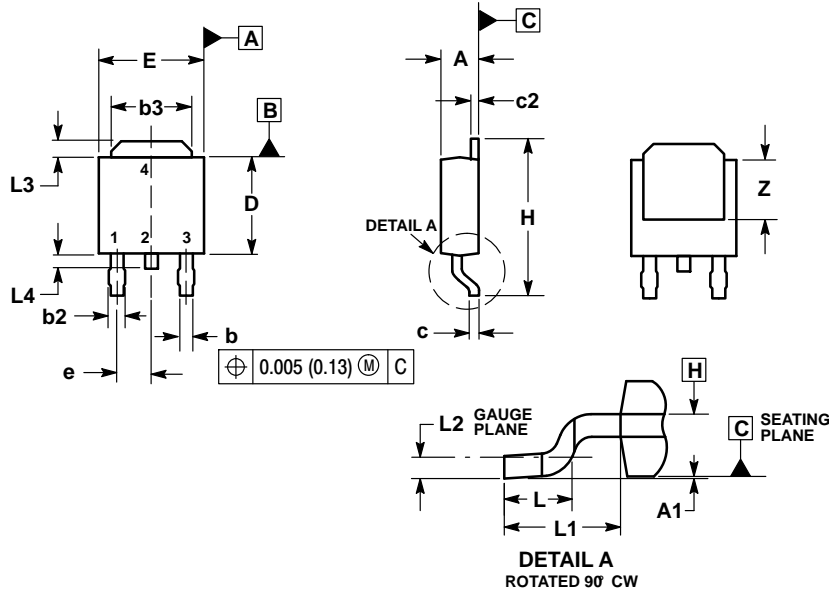
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

NTD6414AN, NVD6414AN

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA ISSUE B



NOTES:

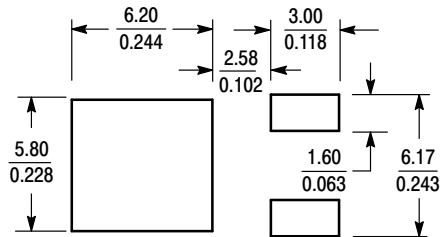
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



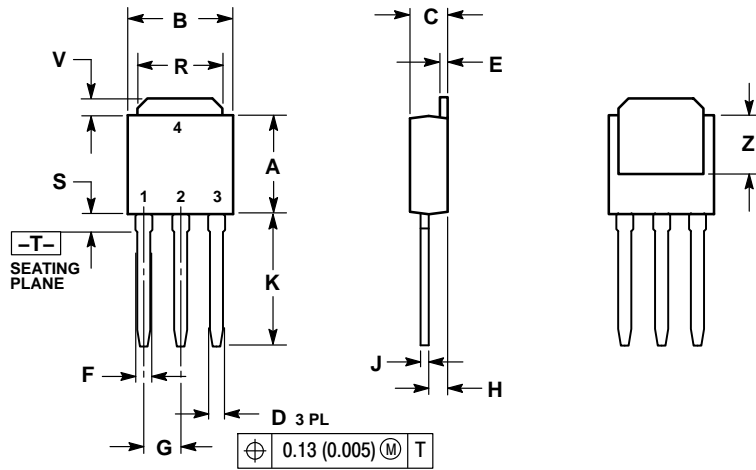
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD6414AN, NVD6414AN

PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1: GATE
 2: DRAIN
 3: SOURCE
 4: DRAIN

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910
Japan Customer Focus Center
 Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative