Sample Approval Sheet

Product Description: 4.66" 720X1280 TFT-LCD Transmissive Cell Product	

AU Model Name: H466TAN03.0

Customer : Standard

Customer Signature	Date	AUO	2014/6/11
		Approved By: Ginie Chou	
		Prepared By: Lesley Chen	

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Product Specification
4.66" COLOR TFT-LCD MODULE

MODEL NAME: H446TAN03.0

< ◆ >Preliminary Specification

<   >Final Specification

Record of Revision

Version	Revise Date	Page	Content
0.1	2014/06/11		First Draft.

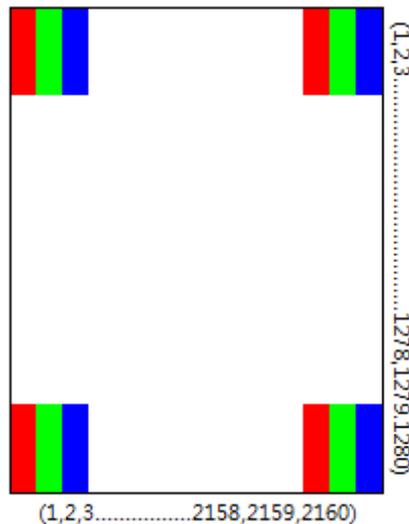# Contents

A. General Information

The specification shall be applicable to the TFT-LCD product, which is designed for cellular phones, with Polarizer and IC attached. (Except remarked with special description)

1. Physical Specifications

NO.	Item	Specification	Remark
1	Screen Size (inch)	4.66	
2	Driving Method	TFT	a-Si
3	Display Mode	Transmissive, AHVA mode	
4	Display Resolution (dot)	720RGB(H)×1280(V)	
5	Active Area (mm)	58.104(H)×103.296(V)	
6	Pixel Pitch (mm)	0.0269(H) RGB×0.0807(V)	
7	Color Configuration	R. G. B. Vertical Stripe	Note 1
8	Color Depth	16.7M Colors	
9	Drive IC	Hx8394A	Ram-less Note 2
		Hx8394D	
		Novatek NT35521	
		Novatek NT35521S	
		Orise OTM1283A	
		Orise OTM1284A	
		Novatek NT35520	HalfRAM
		Raydium RM68210	
10	Interface	MIPI / RGB	
11	Gray Scale Inversion	No GSI	
12	Outline Dimension (mm)	60.104(H) x 110.146(V) x 0.4(T)	
13	Weight (g)	8g	

Note 1: Below figure shows dot stripe arrangement.

Note 2 : Hx8394D and NT35521 is pin-compitable in DrIC, but not in FPC. The following electrical specification is verified by Hx8394D.
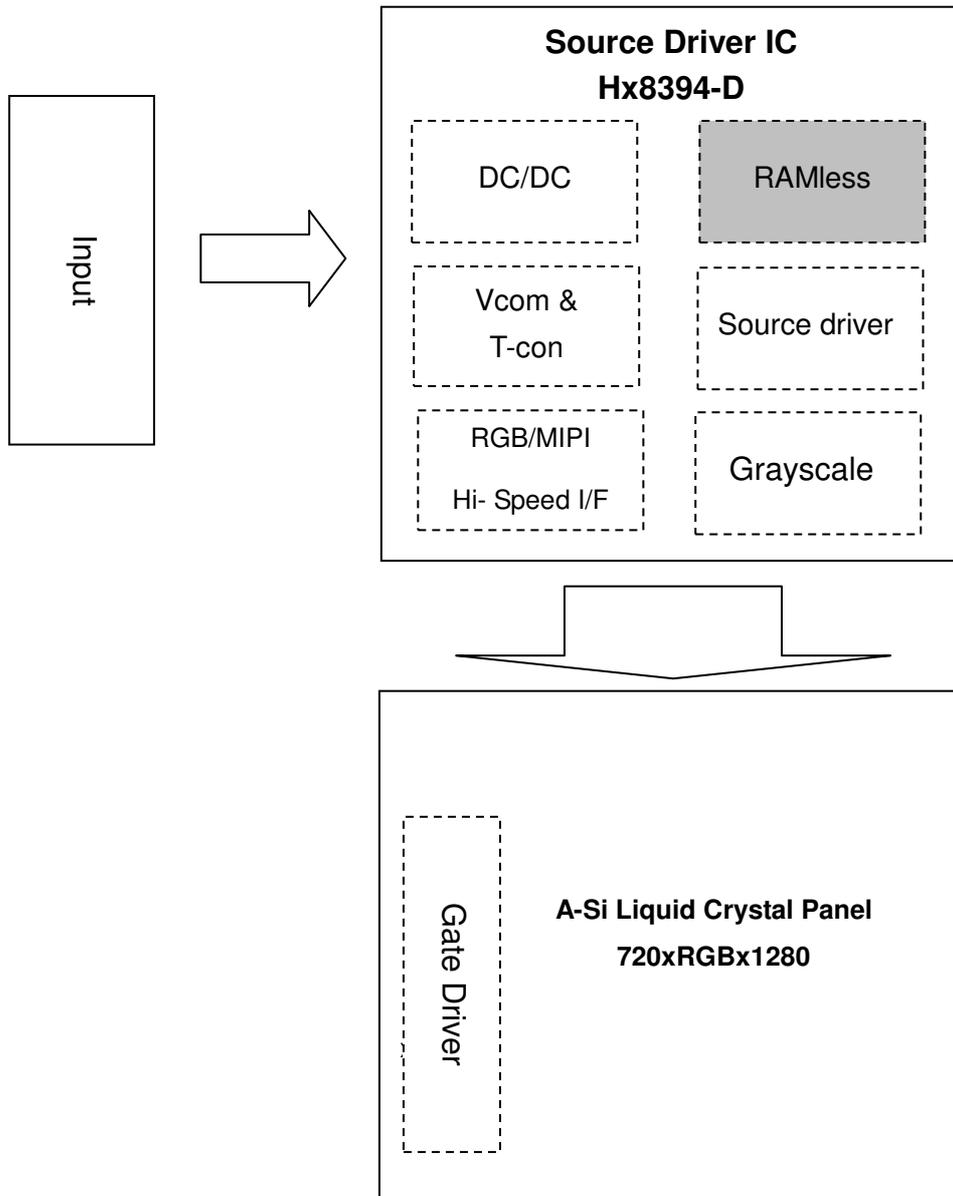
2. Block Diagram

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                        ┌──────────────────────────────────┐
                        │          Source Driver IC         │
                        │            Hx8394-D               │
                        │   ┌─────────┐    ┌─────────┐       │
          ┌─────────┐   │   │  DC/DC  │    │ RAMless │       │
          │         │   │   └─────────┘    └─────────┘       │
          │         │ ➡ │   ┌─────────┐    ┌─────────┐       │
          │  Input  │   │   │ Vcom &  │    │ Source  │       │
          │         │   │   │ T-con   │    │ driver  │       │
          │         │   │   └─────────┘    └─────────┘       │
          └─────────┘   │   ┌─────────┐    ┌─────────┐       │
                        │   │ RGB/MIPI│    │         │       │
                        │   │Hi-Speed │    │Grayscale│       │
                        │   │  I/F    │    │         │       │
                        │   └─────────┘    └─────────┘       │
                        └──────────────────────────────────┘
                                       ⇓
                        ┌──────────────────────────────────┐
                        │ ┌──────┐                           │
                        │ │      │   A-Si Liquid Crystal Panel│
                        │ │ Gate │   720xRGBx1280             │
                        │ │Driver│                           │
                        │ └──────┘                           │
                        └──────────────────────────────────┘
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Fig. 1 Block diagram

B. Electrical Specifications

1. Pin Assignment (For Hx8394D)

1	Align mark	36	HS_VSS	71	DB_22/23
2	GND	37	HS_VSS	72	DUMMY
3	GND	38	HS_VSS	73	DB_18-21
4	VCOM	39	HS_LDO	74	DB_16/17
5	VCOM	40	HS_LDO	75	DB_12-15
6	VSSA	41	HS_LDO	76	DB_4-9
7	VSSA	42	HS_LDO	77	DB_0-3
8	VTESTOUTP	43	HS_VCC	78	DUMMY
9	HS_VSS	44	HS_VCC	79	DUMMY
10	HS_D0N	45	HS_VCC	80	DUMMY
11	HS_D0N	46	HS_VCC	81	DUMMY
12	HS_D0P	47	VDD1	82	DUMMY
13	HS_D0P	48	VDD1	83	DUMMY
14	HS_VSS	49	VDD1	84	DUMMY
15	HS_D1N	50	VDD1	85	DUMMY
16	HS_D1N	51	VDD1	86	DUMMY
17	HS_D1P	52	VDDD	87	HSYNC
18	HS_D1P	53	VDDD	88	VSYNC
19	HS_VSS	54	VDDD	89	DE
20	HS_CN	55	VDDD	90	PCLK
21	HS_CN	56	VDDD	91	DCX
22	HS_CP	57	VDDD	92	CSX
23	HS_CP	58	VSSD	93	SCL
24	HS_VSS	59	VSSD	94	SDI
25	HS_D2N	60	VSSD	95	SDO
26	HS_D2N	61	VSSD	96	CABC_PWM_OUT
27	HS_D2P	62	TS4/5	97	TE
28	HS_D2P	63	TS2/3	98	TE1
29	HS_VSS	64	TS0/1	99	RESX
30	HS_D3N	65	DUMMY	100	TEST1
31	HS_D3N	66	DUMMY	101	TEST1
32	HS_D3P	67	DUMMY	102	TEST2
33	HS_D3P	68	OSC	103	VSSD
34	HS_VSS	69	DUMMY	104	BS0
35	HS_VSS	70	DUMMY	105	VDD1

106	BS1	141	VSSA	176	C21N
107	VSSD	142	DUMMY	177	C21N
108	DUMMY	143	VSPR	178	C22P
109	VDD1	144	VSPR	179	C22P
110	DUMMY	145	DUMMY	180	C22P
111	VSSD	146	VSNR	181	C22N
112	BS2	147	VSNR	182	C22N
113	VDD1	148	VREF	183	VGH
114	PCCS0	149	VREF	184	VGH
115	VSSD	150	VSSD	185	VDD3
116	PCCS1	151	VDD3	186	VDD3
117	VDD1	152	VDD3	187	VDD3
118	VDD1	153	VDD3	188	VSSD
119	VDD1	154	VCL	189	VSSD
120	VDDD	155	VCL	190	C31P
121	VDDD	156	C41P	191	C31P
122	VDDD	157	C41P	192	C31P
123	VSSD	158	C41P	193	C31N
124	VSSD	159	C41N	194	C31N
125	VSSD	160	C41N	195	C31N
126	VCSW2	161	C41N	196	DUMMY
127	VCSW2	162	DUMMY	197	DUMMY
128	VCSW1	163	DUMMY	198	DUMMY
129	VCSW1	164	DUMMY	199	DUMMY
130	VPP	165	DUMMY	200	DUMMY
131	VPP	166	VSPC	201	DUMMY
132	DUMMY	167	VSP	202	DUMMY
133	VDD3	168	VSP	203	VGL
134	VDD3	169	VSN	204	VGL
135	VTESTOUTN	170	VSN	205	DUMMY
136	DUMMY	171	VSNC	206	DUMMY
137	VSSAC	172	C21P	207	DUMMY
138	VSSAC	173	C21P	208	DUMMY
139	DUMMY	174	C21P	209	VGL2
140	VSSA	175	C21N	210	VGL2

211	VGL2
212	VCOMR
213	DUMMY
214	VCOM
215	VCOM
216	GND
217	GND
218	Align mark

2. Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage 1	VDD1~ VSSD	-0.3	-	+3.6	V	Note[1],[2]
Power Supply Voltage 2	VDD3 ~ VSSA	-0.3	-	+3.6	V	Note[1][4]
Power Supply Voltage 3	HS_VCC ~ HS_VSS	-0.3	-	+3.6	V	Note[1][5]
Power Supply Voltage 4	VSP ~ VSSA	-0.3	-	+6.6	V	Note[6]
Power Supply Voltage 5	VSSA ~ VSN	-6.6	-	0	V	Note[7]
Power Supply Voltage 6	VGH ~ VSSA	-0.3	-	+19.6	V	Note[8]
Power Supply Voltage 7	VSSA ~ VGL	-16	-	0	V	Note[9]
Operating Temperature	Topr	-40	-	+85	°C	Note[10]
Storage Temperature	Tstg	-55	-	+110	°C	Note[11]
Input Voltage	V_{IN}	-0.3	-	VDD1+0.3	V	Note[12]
HS Input Voltage	V_{HSIN}	-0.3	-	+2	V	Note[13]

Note:

(1) VDD1, VSSD must be maintained.

(2) To make sure VDD1 ≥ VSSD.

(4) To make sure VDD3≥ VSSA.

(5) To make sure HS_VCC ≥ HS_VSS.

(6) To make sure VSP ≥ VSSA.

(7) To make sure VSSA ≥ VSN

(8) To make sure VGH ≥ VSSA.

(9) To make sure VSSA ≥ VGL, VGH +|VGL| < 32V

(10) For die and wafer products, specified up to +85℃.

(11) This temperature specifications apply to the TCP package.

(12) This specifications include input signals but without following: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.

(13) This specifications include following signals: CP, CN, D0P, D0N, D1P, D1N, D2P, D2N, D3P, D3N.

3. Electrical DC Characteristics

3.1 Typical Operation Condition (VSS=0V)

Item	Symbol	Min.	Typ.	Max.
Positive gate driver output voltage	VGH		15	
Negative gate driver output voltage	VGL		-12	
VCOM	VCOM		TBD	

(VDD3=2.5 ~ 3.6V, VDD1=1.65~3.6V, T_A=-40 ~ 85 °C)

Parameter	Symbol	Test condition	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
Input high voltage	V_{IH}	VDD1= 1.65 ~ 3.6V	0.7 V_{DD1}	-	VDD1	V	-
Input low voltage	V_{IL}	VDD3= 2.5 ~ 3.6V	0	-	0.3 V_{DD1}	V	-
VPP	V_{IH}	VPP	7.25	7.5	7.75	V	(1)
	V_{IL}					V	
Output high voltage (SDO, CABC_PWM_OUT)	V_{OH1}	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V	-
Output low voltage (SDO, CABC_PWM_OUT)	V_{OL1}	VDD1= 1.65 ~ 3.6V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V	-
Logic High level input current	I_{IH}	VSYNC, HSYNC	-	-	1	uA	-
		RESX, DCX, CSX, SCL	-	-	1		-
	I_{IHD}	DB[23:0], SDI, DCX	-	-	1	uA	-
		DB[23:0]	-	-	1		-
Logic Low level input current	I_{IL}	VSYNC, HSYNC	-1	-	-	uA	-
		RESX, DCX, CSX, SCL	-1	-	-		-
	I_{ILD}	DB[23:0], SDI, DCX	-1	-	-	uA	-
		DB[23:0]	-1	-	-		-
Current consumption standby mode (VDD3-VSSA)	$I_{ST(VDD)}$		-	10	30	μA	-
Current consumption standby mode (VDD1– VSSD)	$I_{ST(VDD1)}$	VDD3/HS_VCC=2.8V, VDD1=1.8V T_A =25°C	-	10	30	μA	-
Current consumption standby mode which include HS_VCC (HS_VCC-HS_VSS)	$I_{ST(VDD1)}$	(DSI Ultra Low Power mode)	-	10	30	μA	-
Oscillator tolerance	△OSC	T_A =25°C	-5	-	5	%	-

Note:

(1) The VPP pin is open on normal mode and in used while OTP programming condition.

3.2 MIPI DC Characteristics

Parameter	Description	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note:

(1) Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the tRLP/tFLP specification is met.

Parameter	Description	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	(1)
V_{IDTL}	Differential input low threshold	-70	-	-	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(2)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(2)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(2),(3)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note:

(1) +/-70mV only for reference, related to power and ground noise on system environment, this spec need to check on panel performance to fine tune.

(2) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(3) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Parameter	Description	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Parameter	Description	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

4. Electrical AC Characteristics

MIPI Interface Characteristics

4.1 High Speed Data Transmission: Data-Clock Timing
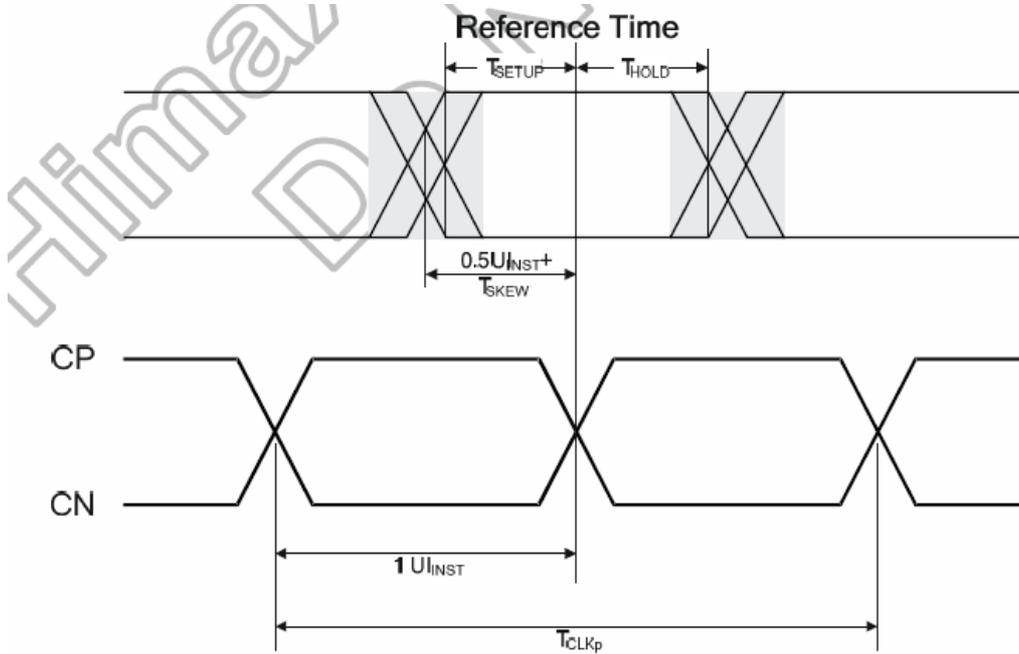
Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5)

Note:

(1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	(1)
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	(1)

Note:

(1) Total setup and hold window for receiver of 0.3*UIINST.

(2) 0.15UI is only for reference, related to the signal jitter caused by the transmittion path, this spec need to check on panel performance to fine tune.

4.2 Low Power Transmission AC Specification

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tableslist AC characteristic for LP-TX.

Parameter	Description	Spec.			Unit	Note
		Min.	Typ.	Max.		
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD}=0pF	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD}=5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD}=20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD}=70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ C_{LOAD}=0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ C_{LOAD}=0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ C_{LOAD}=0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note:

(1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

4.3 Hi-Speed Data Transmission

4.4 Turnaround Procedure

Note: T$_{LPX}$(Master)/T$_{LPX}$(Slave) between 2/3~3/2
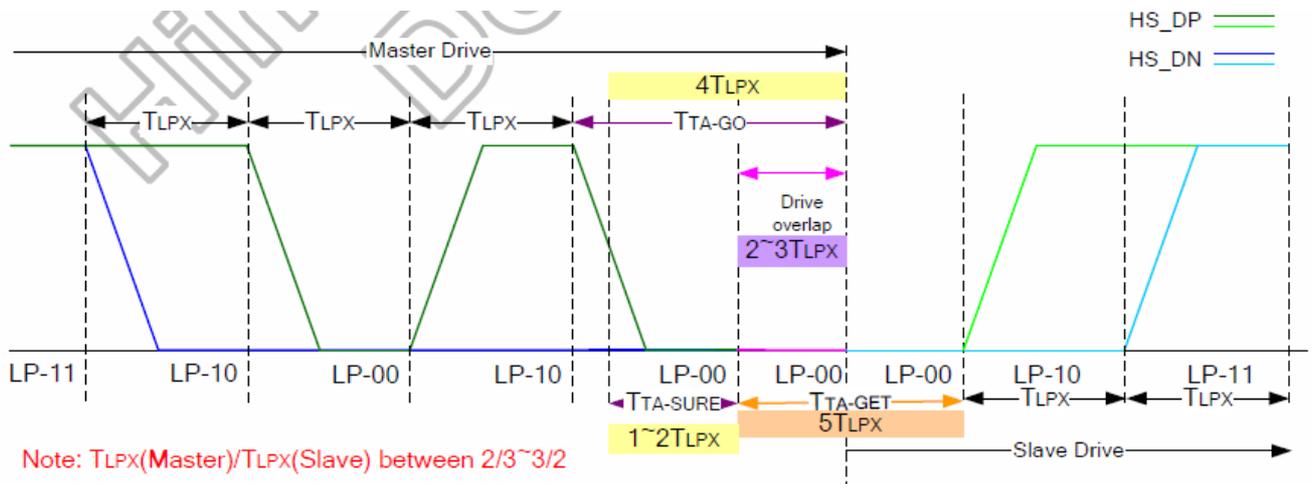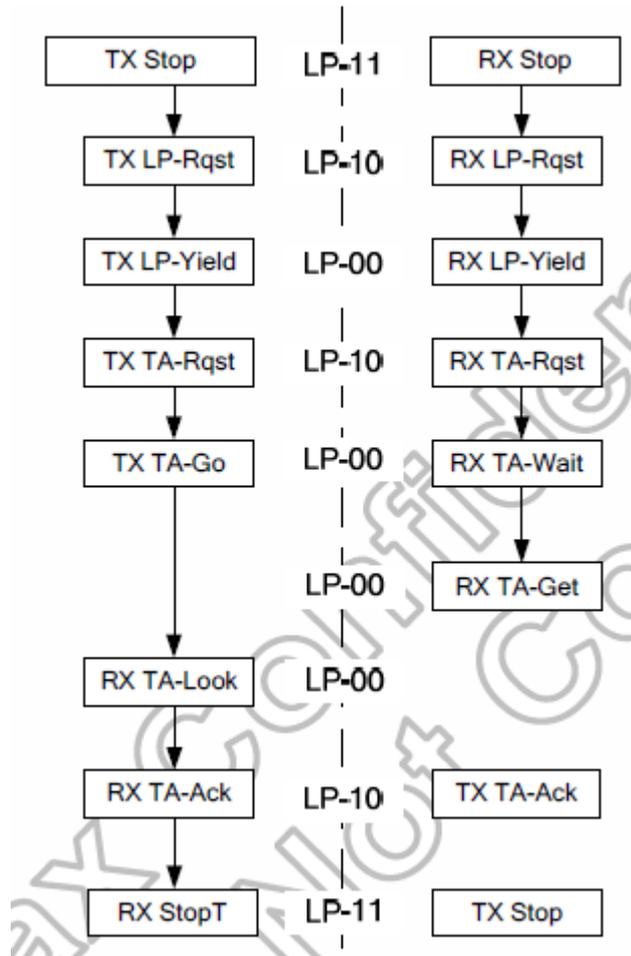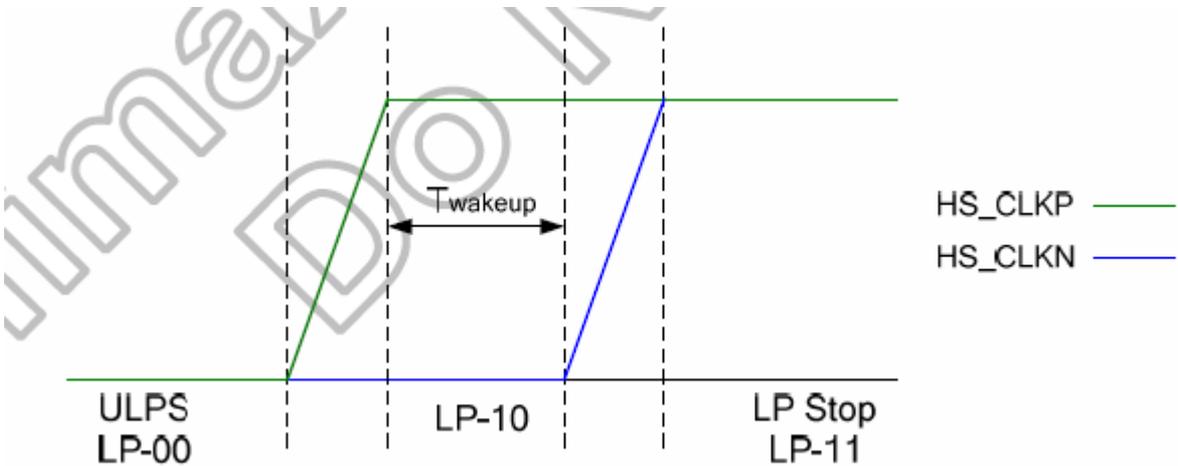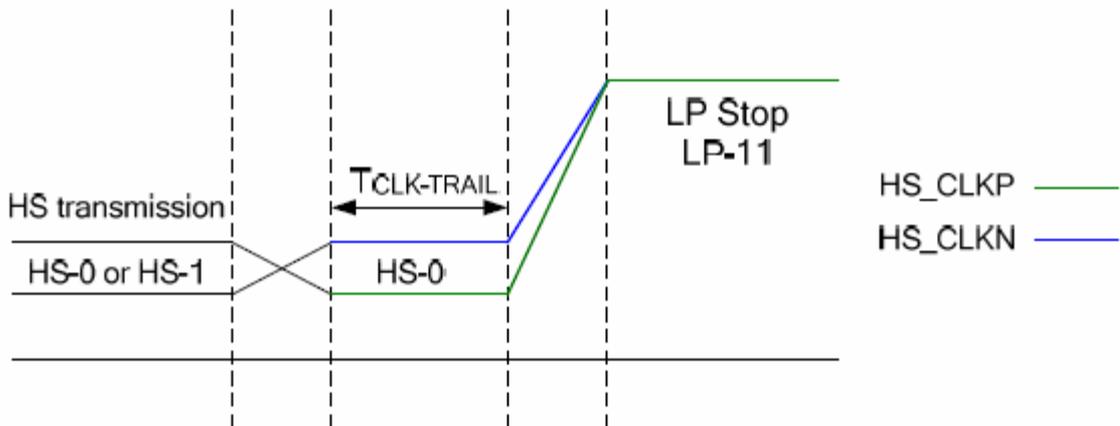
4.5 Clock Lane Mode
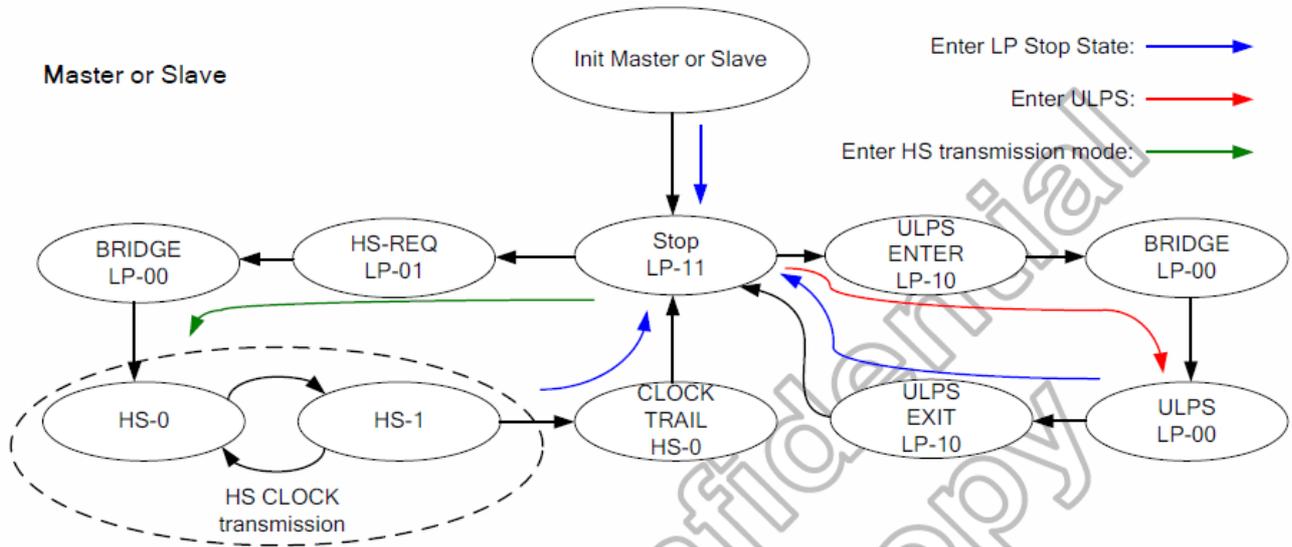
Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

(1) After Initial state. **(HW reset, SW reset, Power on sequence)**

(2) Leaving ULPS: ULPS LP-00 -> LP-10 -> Low Power Stop State LP-11.

(3) Leaving HS clock transmission mode: HS mode **(HS-0 or HS-1)** -> HS-0 -> Low Power Stop State LP-11.

Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-10 -> ULPS LP-00.
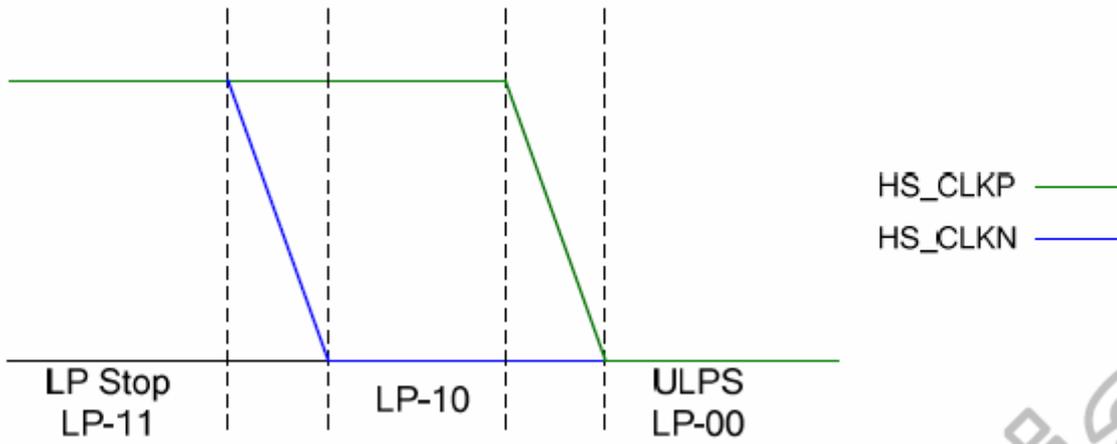
Clock Lane can be High Speed Clock transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11 -> LP-01 -> LP-00 -> HS-0/1.
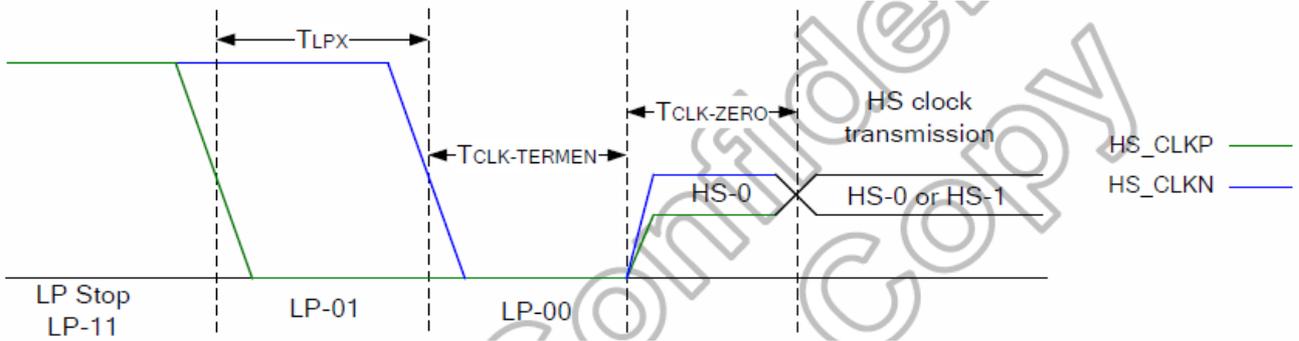
4.6 Data Lane Mode
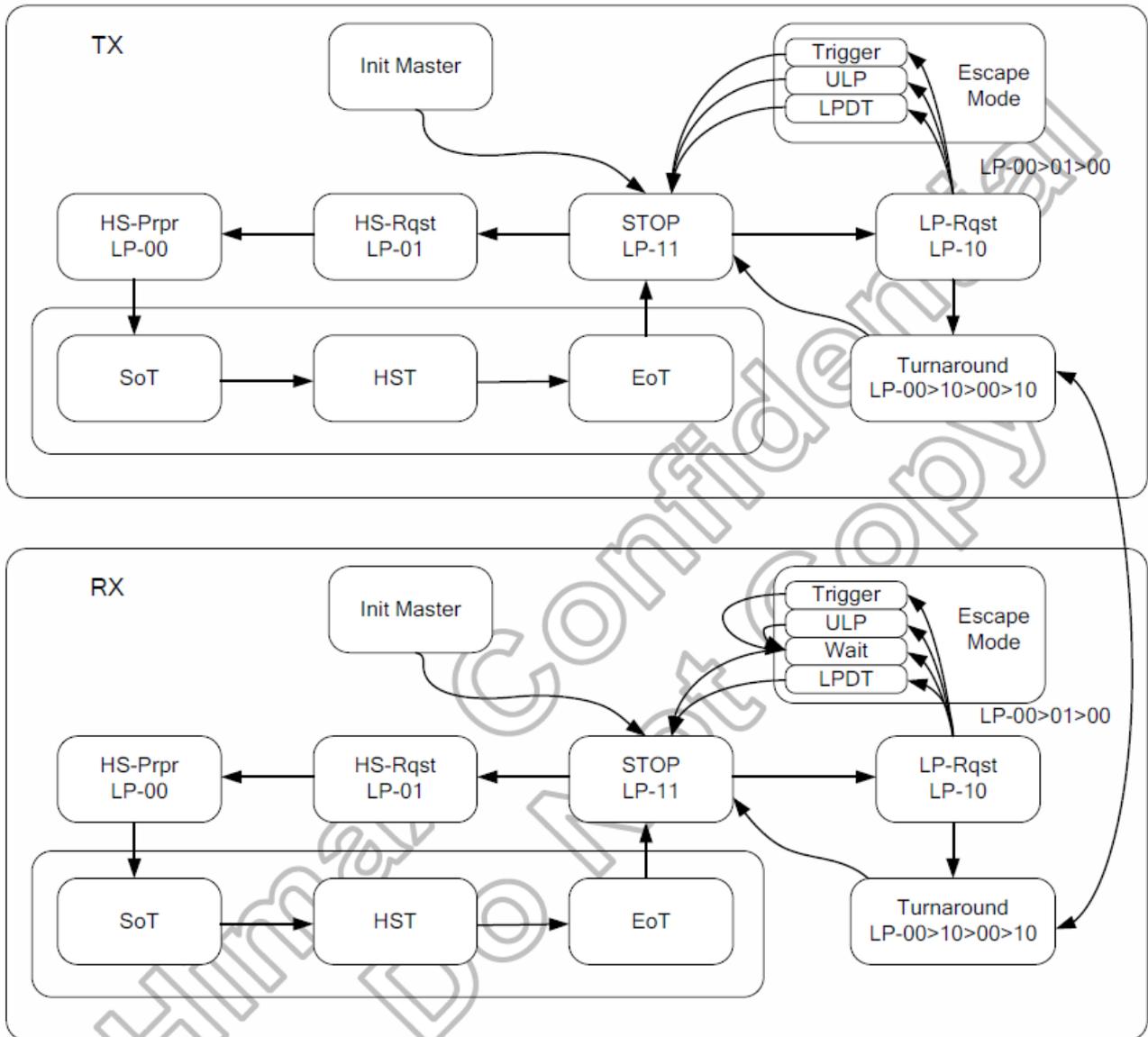
4.7 Escape mode

Data Lane0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-11 -> LP-10 -> LP-00 -> LP-01 -> LP-00 and exit Escape mode via LP-10 -> LP-11.
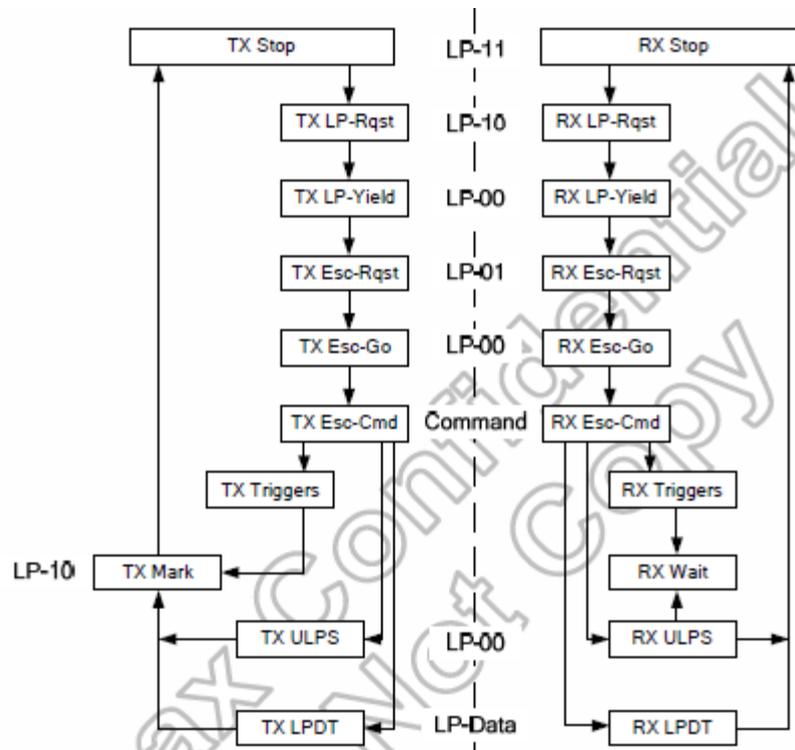
Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action.

The Entry Code as follows:

(1) Trigger **(Reset-Trigger(46h), Tearing effect(BAh), Acknowledge(84h))**

(2) Drive Data Lane to Ultra Low Power State **(78h)**

(3) Send Low Power Data Transmission **(87h)**

Escape Entry Code
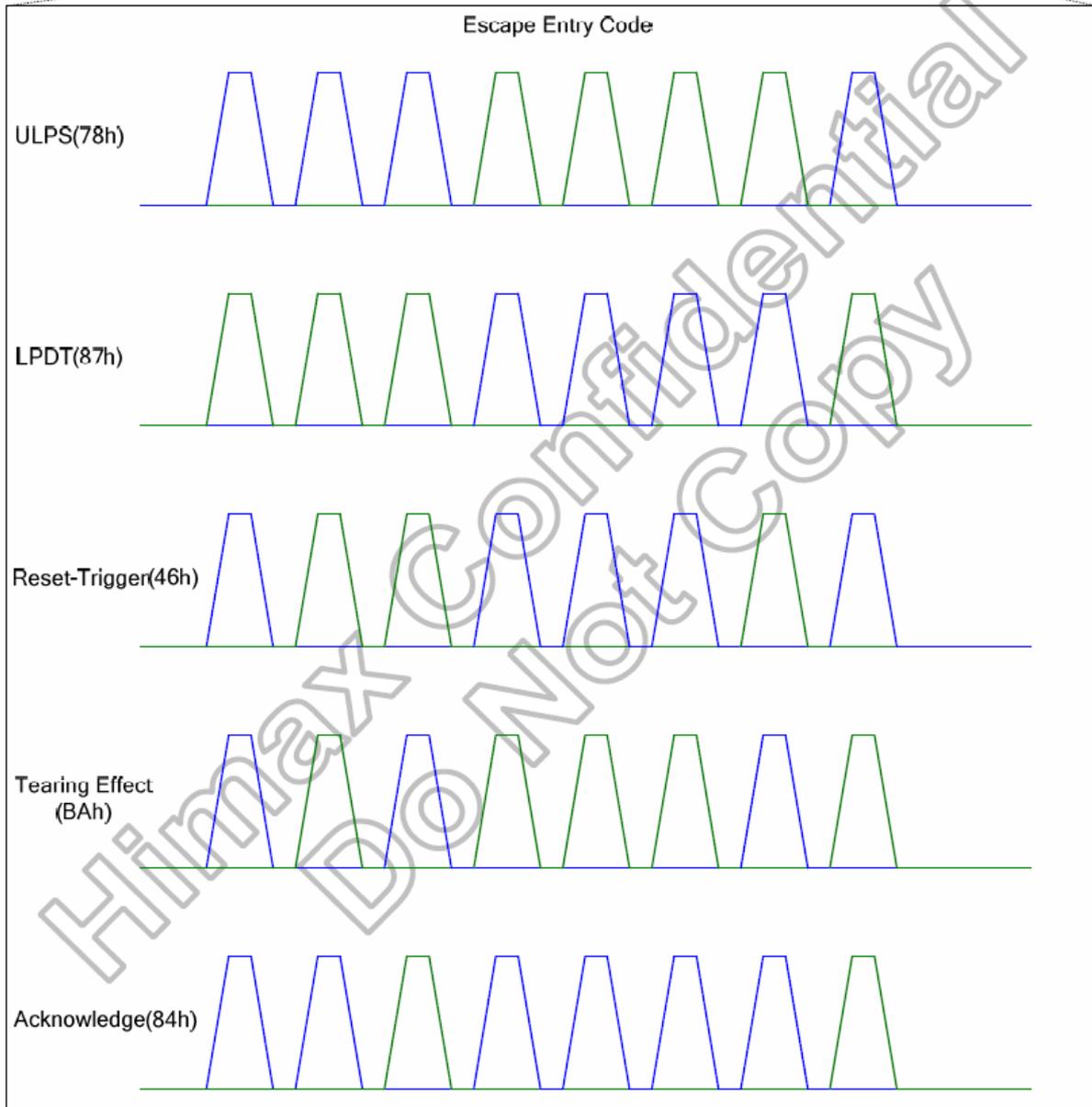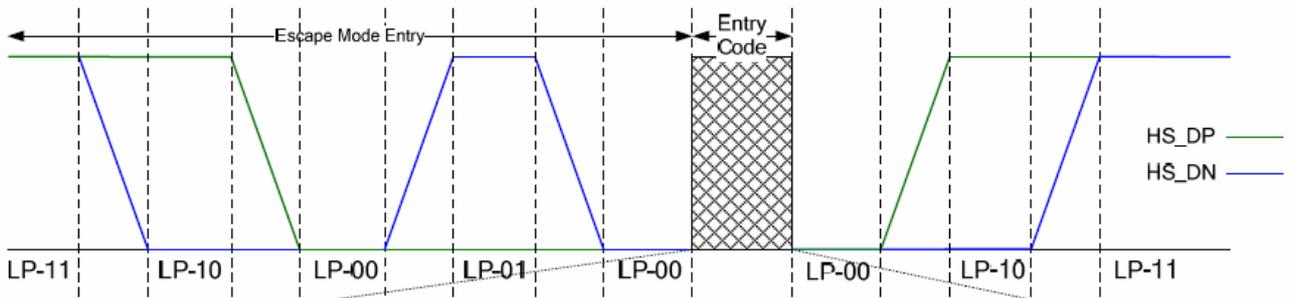
5. RESET Timing Characteristics
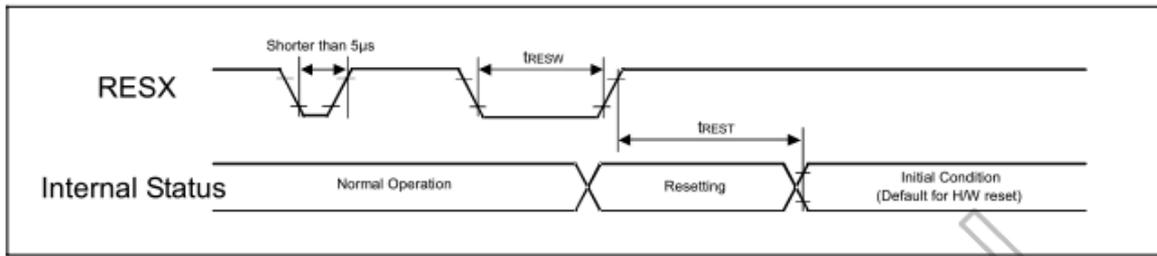
Figure 7.10: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width[1]	RESX	10	-	-	-	µs
t_{REST}	Reset complete time[2]	-		5	-	-	When reset is applied during Sleep In mode	ms
		-		200	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 200 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(3) During Reset Complete Time, OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

(4) Spike Rejection also applies during a valid reset pulse as shown below:
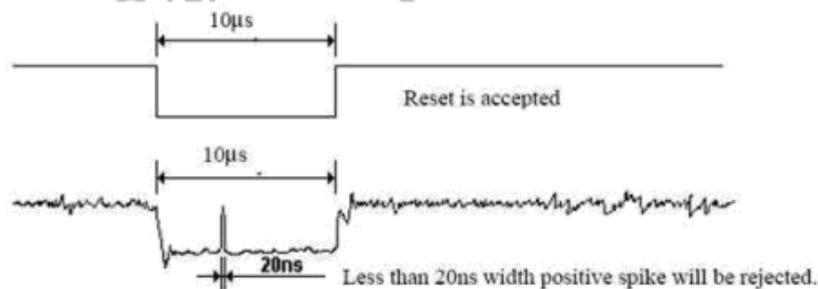
(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 200msec.

6. External Components Connection

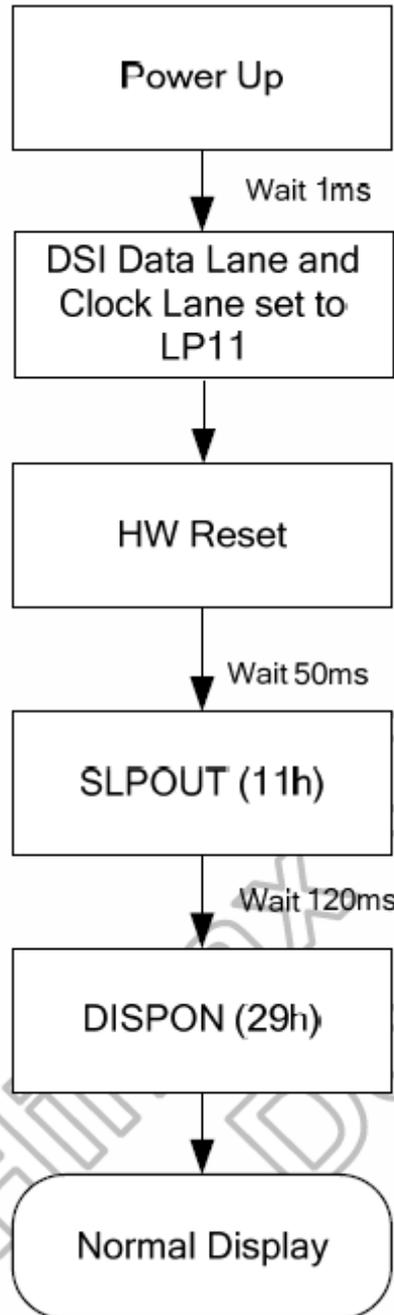### 6.1 External component table with 2 PWR Mode [VDD1, VDD3]

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGL	D2	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----◁--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 16V): VGL ---(-)----| |--- (+)----- VSSA	1.0 µF
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
C21P – C21N	C21PN	Connect to Capacitor (Max 16V): C21P ---(+)----| |--- (-)-----C21N	1.0 µF
C22P – C22N	C22PN	Connect to Capacitor (Max 16V): C22P ---(+)----| |--- (-)-----C22N	1.0 µF
C31P – C31N	C31PN	Connect to Capacitor (Max 16V): C31P ---(+)----| |--- (-)-----C31N	1.0 µF
C41P – C41N	C41PN	Connect to Capacitor (Max 6V): C41P ---(+)----| |--- (-)-----C41N	1.0 µF
VSN	C5	Connect to Capacitor (Max 10V): VSN ---(-)----| |--- (+)-----VSSA	2.2 µF
VSP	C6	Connect to Capacitor (Max 10V): VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VCL	C7	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	1.0 µF
VREF	C8	Connect to Capacitor (Max 6V): VREF ---(+)----| |--- (-)----- VSSA	1.0 µF
VSNR	C9	Connect to Capacitor (Max 10V): VSNR ---(-)----| |--- (+)----VSSA	1.0 µF
VSPR	C10	Connect to Capacitor (Max 10V): VSPR ---(+)----| |--- (-)----VSSA	1.0 µF
VDDD	C12	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
	C13	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
HS_LDO	C14	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS	1.0 µF
VDD3	C15	Connect to Capacitor (Max 10V): VDD3 ---(+)----| |--- (-)-----VSSA	2.2 µF
HX5186-A/B/C	U1	Please refer to HX5186-A/B/C datasheet	-
HX5186-A/B/C	C16	Please refer to HX5186-A/B/C datasheet	1.0uF
HX5186-A/B/C	C17	Please refer to HX5186-A/B/C datasheet	1.0uF
HX5186-A/B/C	C18	Please refer to HX5186-A/B/C datasheet	1.0uF

6.2 External component table with 3 PWR Mode [VDD1, VSP, VSN]

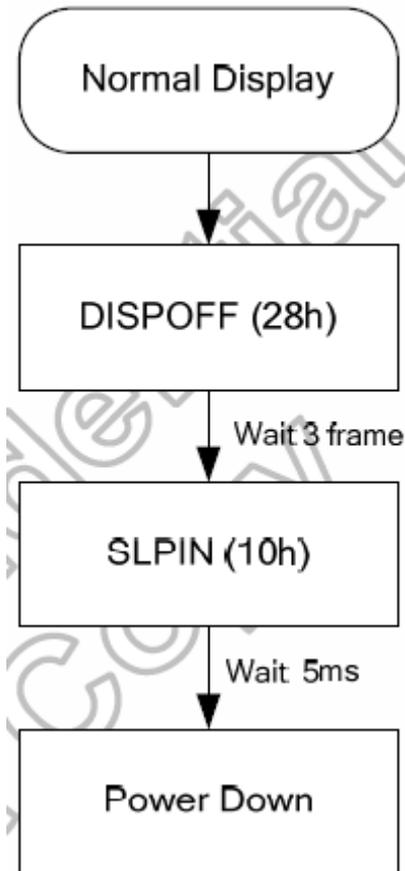| Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGL	D2	Connect to Schottky Diode(VR≥30V): VSN ---(-)----◁--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 16V): VGL ---(-)----| |--- (+)----- VSSA	1.0 µF
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
C21P – C21N	C21PN	Connect to Capacitor (Max 16V): C21P ---(+)----| |--- (-)-----C21N	1.0 µF
C22P – C22N	C22PN	Connect to Capacitor (Max 16V): C22P ---(+)----| |--- (-)-----C22N	1.0 µF
C31P – C31N	C31PN	Connect to Capacitor (Max 16V): C31P ---(+)----| |--- (-)-----C31N	1.0 µF
C41P – C41N	C41PN	Connect to Capacitor (Max 6V): C41P ---(+)----| |--- (-)-----C41N	1.0 µF
VSN	C5	Connect to Capacitor (Max 10V): VSN ---(-)----| |--- (+)-----VSSA	2.2 µF
VSP	C6	Connect to Capacitor (Max 10V): VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VCL	C7	Connect to Capacitor (Max 6V): VCL ---(-)----| |--- (+)----- VSSA	1.0 µF
VREF	C8	Connect to Capacitor (Max 6V): VREF ---(+)----| |--- (-)----- VSSA	1.0 µF
VSNR	C9	Connect to Capacitor (Max 10V): VSNR ---(-)----| |--- (+)-----VSSA	1.0 µF
VSPR	C10	Connect to Capacitor (Max 10V): VSPR ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDD	C12	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
	C13	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
HS_LDO	C14	Connect to Capacitor (Max 6V): HS_LDO ---(+)----| |--- (-)----HS_VSS	1.0 µF
VDD3	C15	Connect to Capacitor (Max 10V): VDD3 ---(+)----| |--- (-)-----VSSA	2.2 µF

7. Power On/Off Characteristics

7.1 Power on Sequence

```
┌─────────────────┐
│    Power Up      │
└─────────────────┘
         │  Wait 1ms
         ▼
┌─────────────────┐
│ DSI Data Lane and│
│ Clock Lane set to│
│      LP11        │
└─────────────────┘
         │
         ▼
┌─────────────────┐
│    HW Reset      │
└─────────────────┘
         │  Wait 50ms
         ▼
┌─────────────────┐
│  SLPOUT (11h)    │
└─────────────────┘
         │  Wait 120ms
         ▼
┌─────────────────┐
│  DISPON (29h)    │
└─────────────────┘
         │
         ▼
 ╭─────────────────╮
 │ Normal Display   │
 ╰─────────────────╯
```

7.2 Power off sequence

Power Off Sequence

```
        ╭───────────────────╮
        │  Normal Display   │
        ╰─────────┬─────────╯
                  │
                  ▼
        ┌───────────────────┐
        │   DISPOFF (28h)   │
        └─────────┬─────────┘
                  │ Wait 3 frame
                  ▼
        ┌───────────────────┐
        │   SLPIN (10h)     │
        └─────────┬─────────┘
                  │ Wait 5ms
                  ▼
        ┌───────────────────┐
        │   Power Down      │
        └───────────────────┘
```

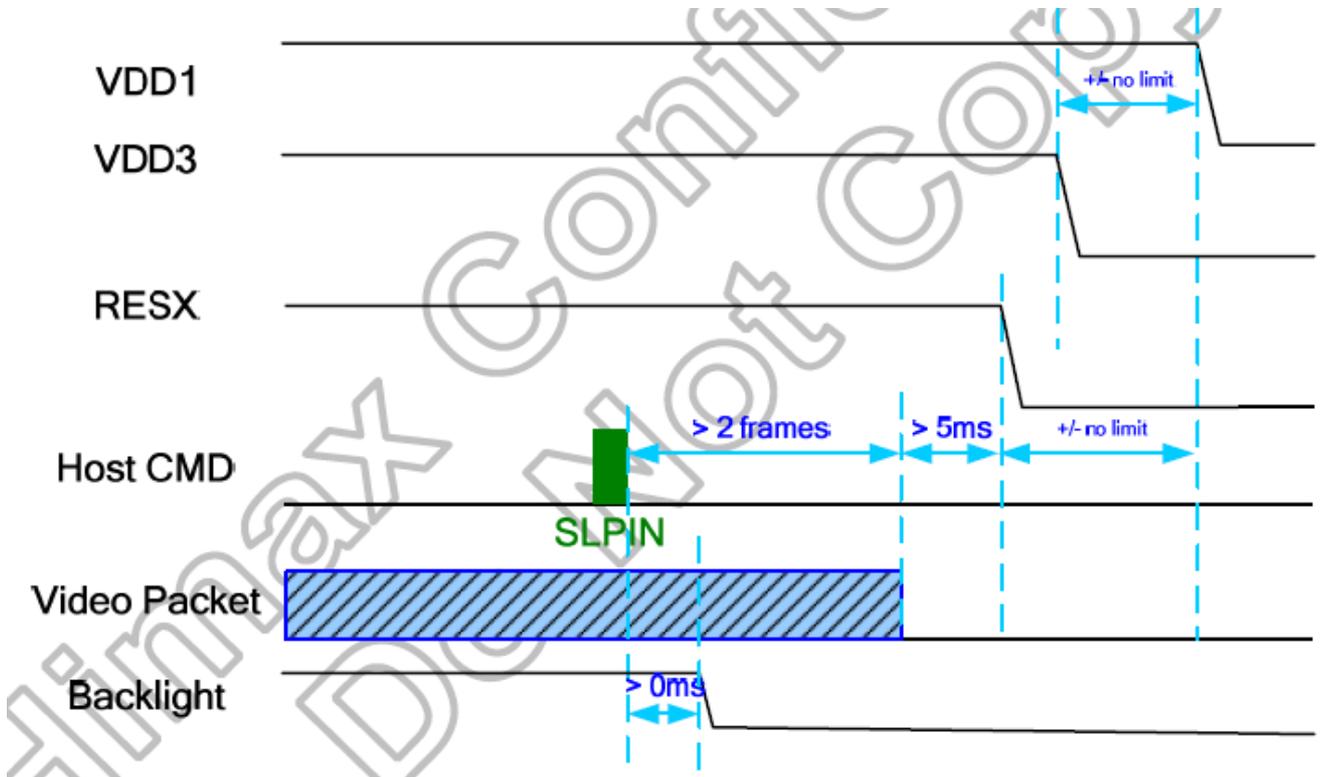## 7.3 Power Supply On/Off setting sequence

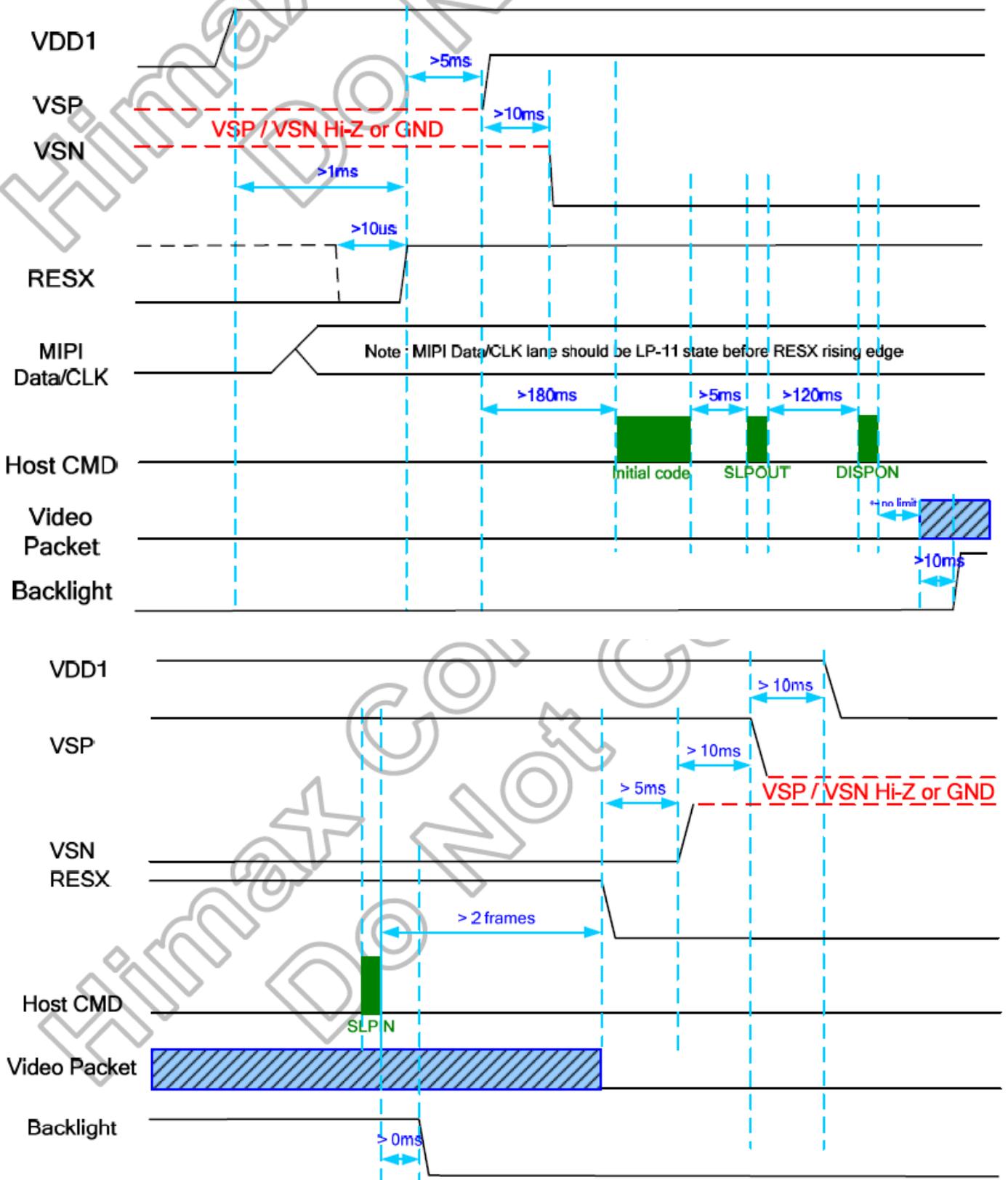### a. VDD1/VDD3 input power sequence (PCCS[1:0]="01", "10")
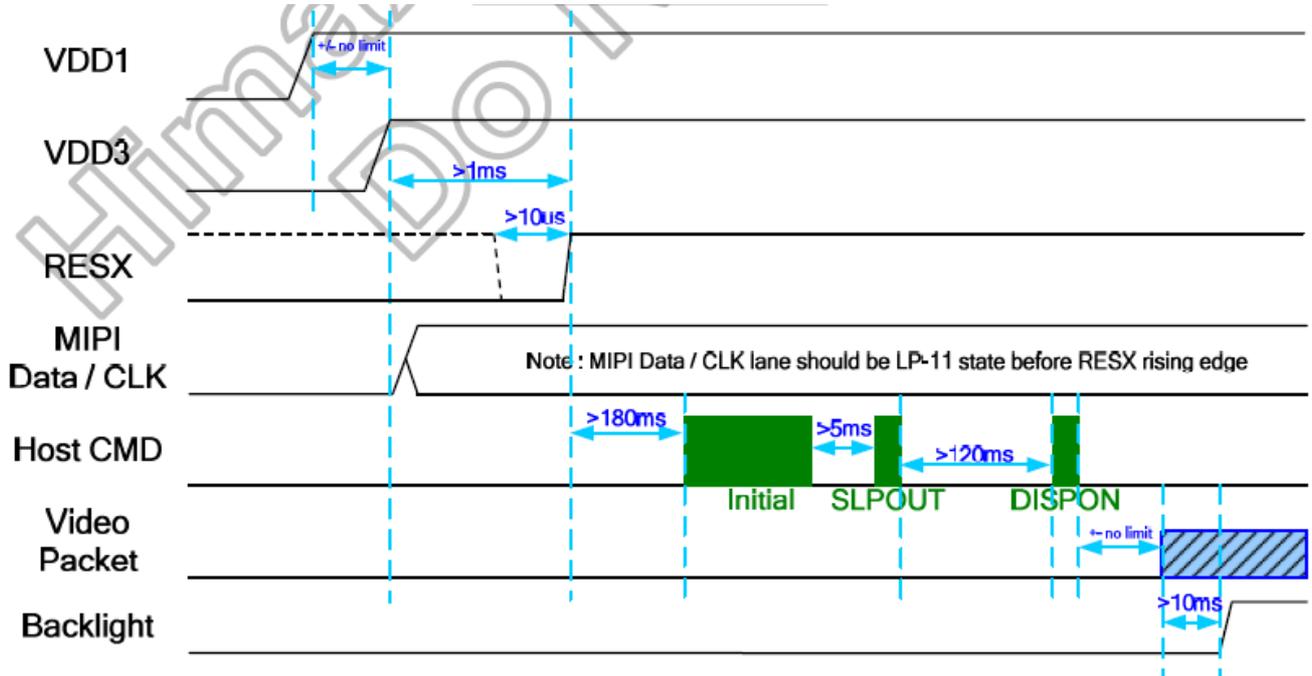
Note: For External Power Mode not need VDD3

Note: For External Power Mode not need VDD3

b. VDD1/VSP/VSN input power sequence (PCCS[1:0]="11")

C. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
NTSC		%	θ=0°	--	70	--		w/o CE
Contrast Ratio		CR	θ=0°	700	1000	--		Note 3
Viewing Angle	Top		CR≧10	--	(80)	--	deg.	Note 4
	Bottom			--	(80)	--		
	Left			--	(80)	--		
	Right			--	(80)	--		
Response Time Rise + Fall		Tr + Tf	θ=0°	--	30	40	ms	Note 5
Chromaticity	White x	x	θ=0°	0.274	0.304	0.334		Measured by Nichia NSSW206B 2c/3c light Source
	White y	y	θ=0°	0.285	0.315	0.345		
	Red x	x	θ=0°	0.615	0.645	0.675		
	Red y	y	θ=0°	0.298	0.328	0.358		
	Green X	X	θ=0°	0.270	0.300	0.330		
	Green Y	Y	θ=0°	0.565	0.595	0.625		
	Blue X	X	θ=0°	0.125	0.155	0.185		
	Blue Y	Y	θ=0°	0.034	0.064	0.094		
Transmittance		%		3.90	4.64	--		w/ APCF
Cross talk Ratio		%		--	--	4		Note 6

Note 1. Measured under Ambient temperature =25℃±2℃.

Note 2. To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation

PHOTO DETECTOR

FIELD=1°
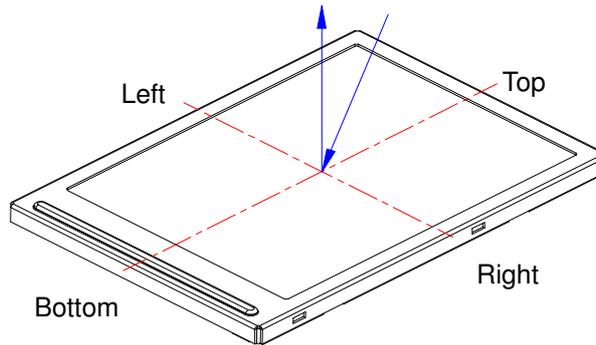
50 cm

LCD PANEL

TFT-LCD MODULE

CENTER OF THE SCREEN
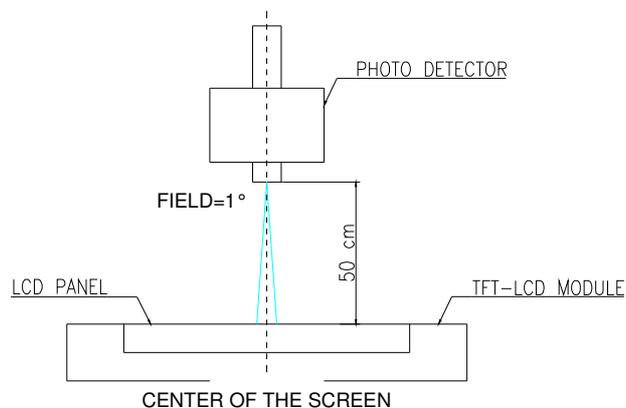
BM-5A

Note 3. Definition of contrast ratio:Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 4. Definition of viewing angle, θ, Refer to figure as below.

Note 5. Definition of response time

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below
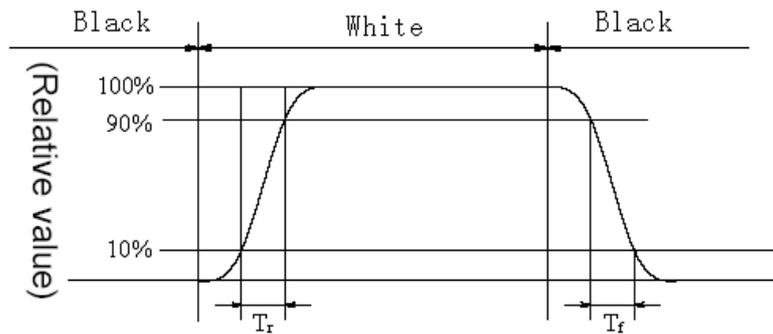
Note 6. Cross-talk ratio is measuring by following pattern and formula:
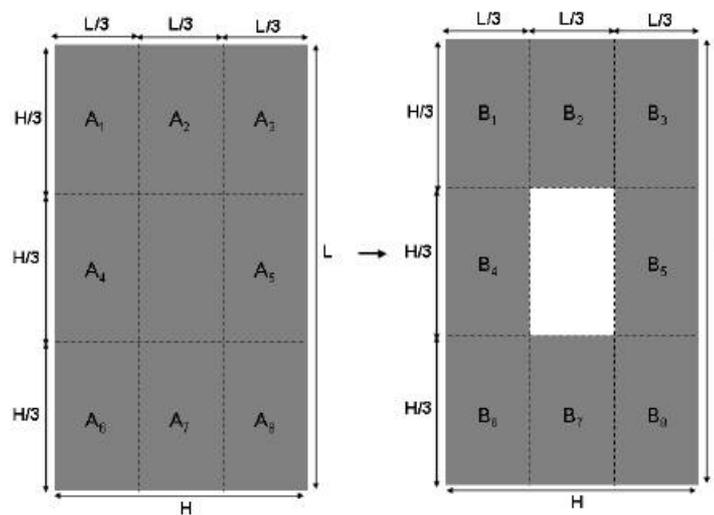
$$\text{Cross talk Ratio} = \underset{i=1\,to\,8}{\text{Max}} \frac{|A_i - B_i \text{ (Photo detector output when LCD is at test pattern)}|}{A_i \text{ (Photo detector output when LCD is at 128L gray pattern)}}$$

The test pattern of cross-talk is 128L gray around one white block, size is defined as picture.

D. Absorption angle of display

Absorption axis θ is the angle of the light absorption direction, which is defined at the protection film side of the polarizer.
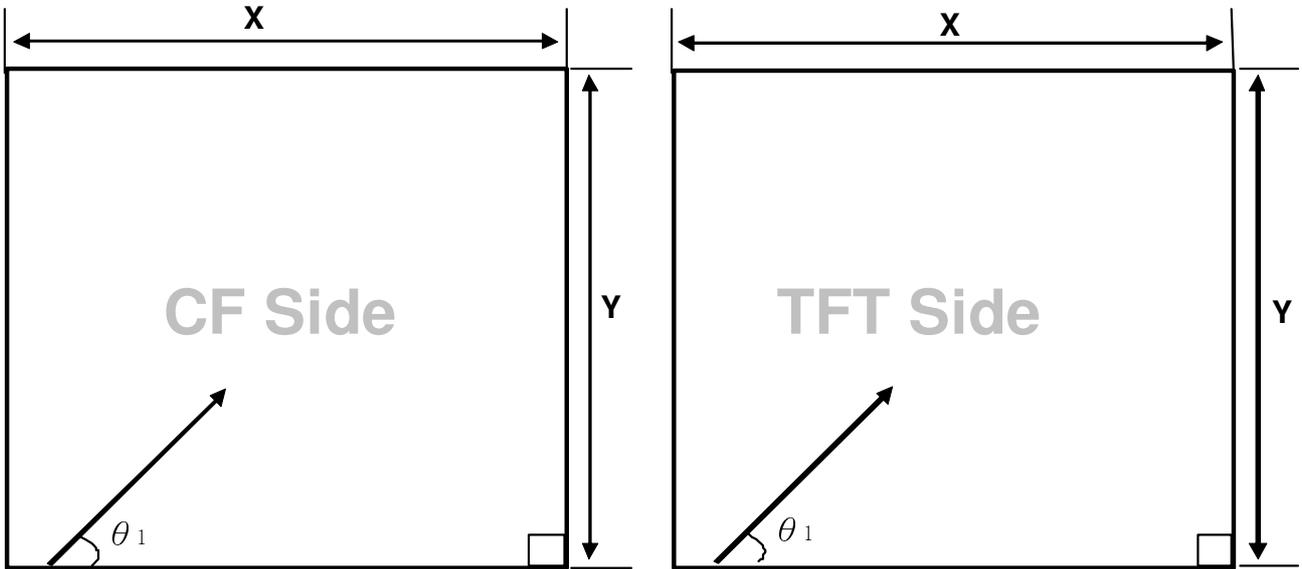
Top view front the protective film

Polarizer Model (Recommended)	※Dimension (mm)		Absorption Angle
	X	Y	θ1(°)
CF side	59.70	105.55	83
TFT side	59.70	105.55	7

Note1: All fields denoted with '※' are applicable to AUO only

E. Reliability test items

The panel performance shall meet the judgment criteria after the testing items have been performed. However, only a single item of these tests shall be executed on a single panel.   No more one test item shall be executed on a single panel.

1. Test items and conditions (Note 1)

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 80℃	240H	
2	Low temperature storage	Ta= -30℃	240H	
3	High temperature operation	Ta= 70℃	240H	Operation
4	Low temperature operation	Ta= -20℃	240H	Operation
5	High temperature and high humidity	Ta= 60℃. 90% RH	240H	Operation
6	Thermal shock Test	-30℃/0.5hr~80℃/0.5hr,Judge 100cycle		Non-operation
7	Vibration Test	Random vibration: 0.015G2/Hz from 5~200Hz, –6dB/Octave from 200~500Hz, 30 minutes each axis.		Non-operation Package
8	Drop Test	Height: 60cm 1 corner, 3 edges, 6 surfaces Each direction,1 time		Non-operation Package

Ta: Ambient temperature.

Note 1: All the tests are performed by whole set of TFT-LCD module with completed driver IC, FPC, and backlight module.

2. Failure Judgment Criteria

a. After the test, the panel should be left at room temperature and room humidity (15℃~35℃, 45%~65% RH).   Then the panel could be inspected for normal operation.

b. Neither abnormality nor significant visible deterioration should be found on display performance.

c. There should be no functions abnormalities on display quality.

F. Packing

① LCD

② 10pcs Modules/Layer
- PET Tray
- EPE Spacer

③ 18+1 Layers Tray/Stack

④
- TAPE
- TAPE
- TAPE
- Desiccants agent

⑤ BAG / OPEN

⑥ 180 pcs Modules/Bag
- BAG

⑦ 1Bag/Inner Box

⑧ 2 Inner Boxes
- AUO
- AUO
- CARTON

⑨ Total 360 pcs LCDs
- TAPE
- CARTON LABEL

G. Outline Dimension

Notes:
1. Transmissive type TFT–LCD Panel.
2. General tolerance: ±0.2mm
3. Resolution: 720 X (RGB) X 1280
4. OLB Pattern tolerance: ±0.03mm
5. Check code: ①~③

4.66" HD
720 RGB 1280

110,146±0.2(TFT)
106,746±0.2(CF)

60.104(TFT)(CTQ)
58.104(AA)
2−1(BORDER)

1.3(BORDER)
2.15(CF TO AA)
5.55(TFT TO AA)
3.4(OLB)
103.296(AA)
106.746(CF)
110.146(TFT)(CTQ)

60.104(TFT)(CTQ)

16,592
26,04
26,92
16,592
16,592

Pin 1
"D"
"C"
"B"

Detail "E" SCALE 10X
0.4 (CTQ)
0.2 (TFT)
0.2 (CF)

AG PAD AREA
1.95
2.2
2.2
Detail "D" SCALE 5X

prealign Mark
Detail "B" SCALE 10X
0.8
0.15
0.2
0.15
0.2
1.35
0.8
6.5

Detail "A" SCALE 200X
0.0807
0.0807
R G B

0.15
0.2
0.2
0.15
0.2
0.15
0.44
0.5
0.75
0.15
pitch=0.12
0.08
0.04
Detail "C" Scale 20X

UNIT mm
SCALE 1:1
WEIGHT -
ANGLE -
GENERAL TOLERANCE ±10'
3rd Angle

ORIGINAL MODEL
H466TAN03.0

TITLE Assy ARRAY–CELL H466TAN03.0
DRAWING NO.(PART NO.) 92.04H68.000

SIZE A4
SHEET 1 of 1
REV. X0

AU Optronics

CRITICAL DIMENSION
MAJOR DIMENSION
CHECK–CODE DIMENSION

MATERIAL -
FINISHED -
APPROVED Yorking Lin   2014/60/11
CHECKED Jackzw wang   2014/60/11
DESIGNED Hardyxiao   2014/60/11

General Tolerance ±
SELECT LEVEL

LEVEL	1	2	3
DIM.			
0 ~ 4	0.05	0.1	0.1
4 ~ 14	0.05	0.1	0.1
14 ~ 63	0.05	0.1	0.2
63 ~ 250	0.1	0.2	0.3
250 ~ 600		0.3	0.5
600 ~ 4000			0.8

REV	ECN NO.	DESCRIPTION	SIGN	DATE
X0	-	-	Hardyxiao	2014/60/11