




Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications

(✓) Final Specifications

Module	15.6"HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B156XTN04.0 (H/W: 4A)
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
_____	_____
Checked & Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Buffy Chen</u>	<u>2014/01/08</u>
Prepared by	Date
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2. General Description

B156XTN04.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B156XTN04.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

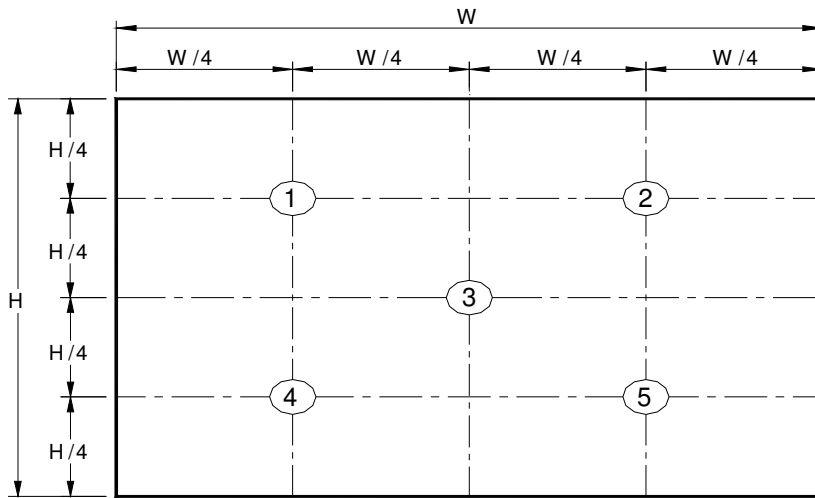
Items	Unit	Specifications			
Screen Diagonal	[mm]	394.9			
Active Area	[mm]	344.2 X193.5			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.252X0.252			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m ²]	220 typ. (5 points average) 187 min.			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ.			
Response Time	[ms]	8 typ/16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	3.5 max. (Include Logic and Blu power)			
Weight	[Grams]	420 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	359.0	359.5	360.0
		Width	223.3	223.8	224.3
		Thickness	-	-	3.8
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			
Temperature Range	[°C]	0 to +50			
	[°C]	-20 to +60			
RoHS Compliance		RoHS Compliance			

2.2 Optical Characteristics

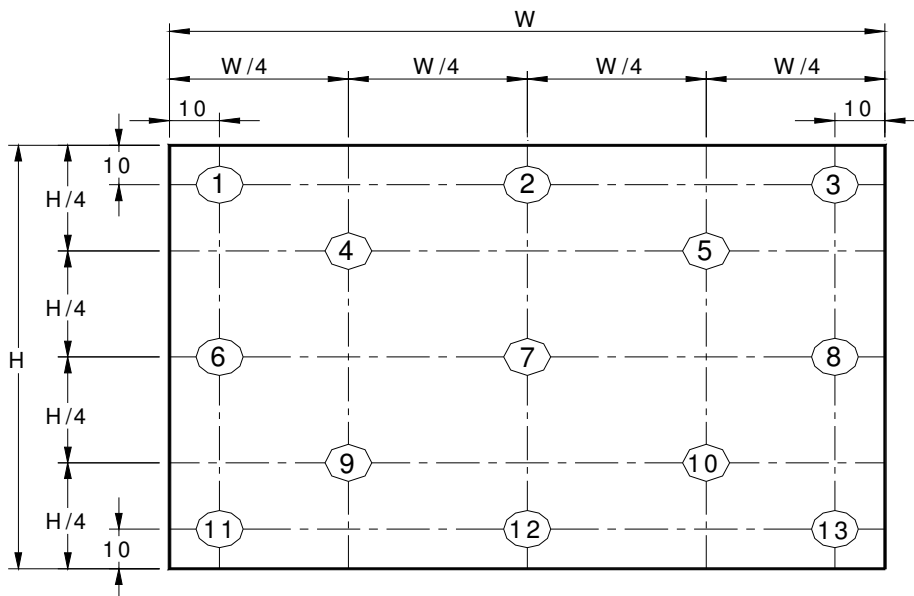
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA		5 points average	187	220	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R θ_L	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
	ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		400	500	-		4, 6
Cross talk	%				4		4, 7
Response Time	T_{RT}	Rising + Falling	-	8	16		4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.550	0.580	0.610	4
		Ry		0.305	0.335	0.365	
	Green	Gx		0.300	0.330	0.360	
		Gy		0.535	0.565	0.595	
	Blue	Bx		0.125	0.155	0.185	
		By		0.110	0.140	0.170	
	White	Wx		0.283	0.313	0.343	
		Wy		0.299	0.329	0.359	
NTSC	%		-	45	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

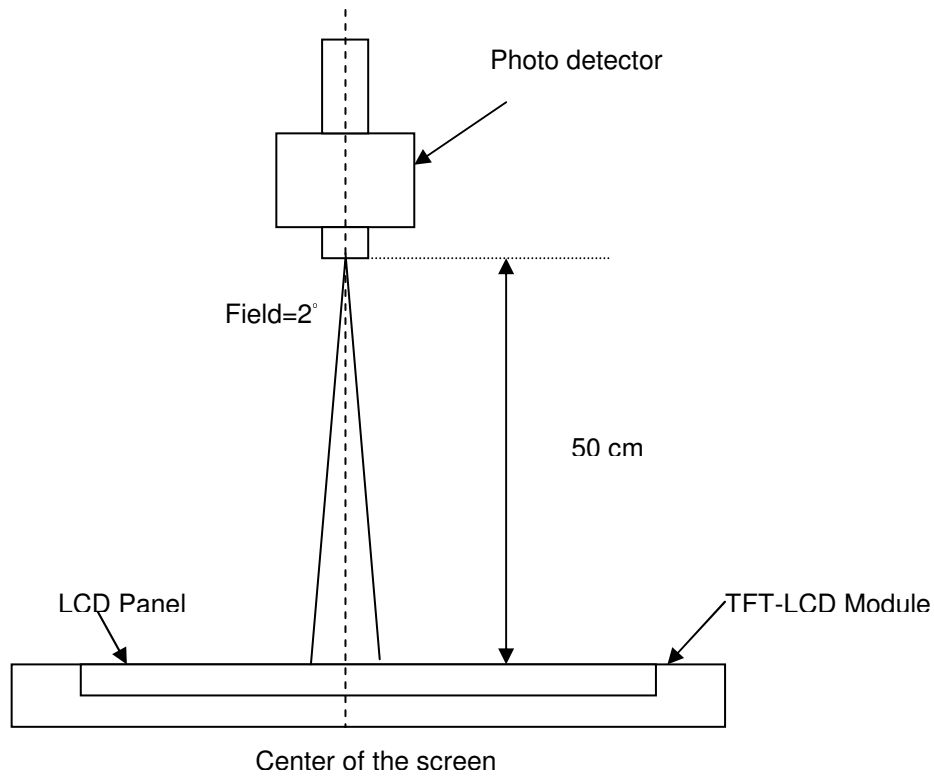
$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the

center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5$

$L (x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

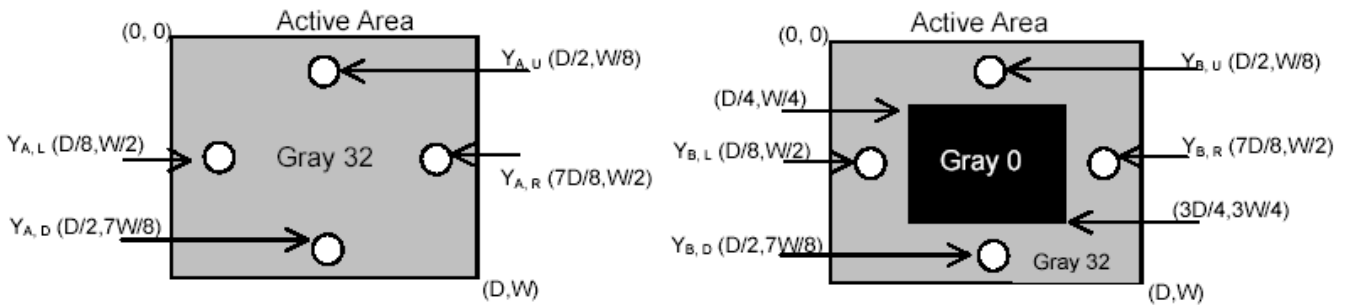
Note 7 : Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

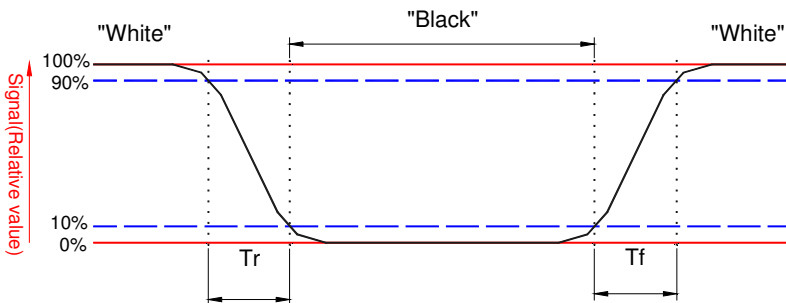
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



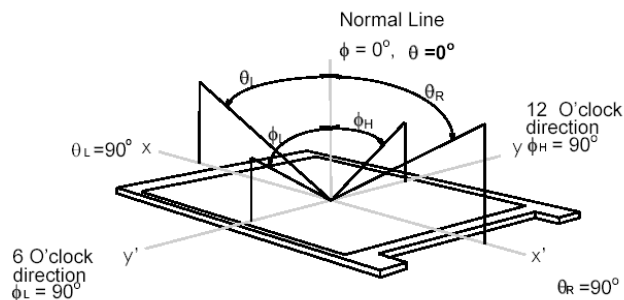
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



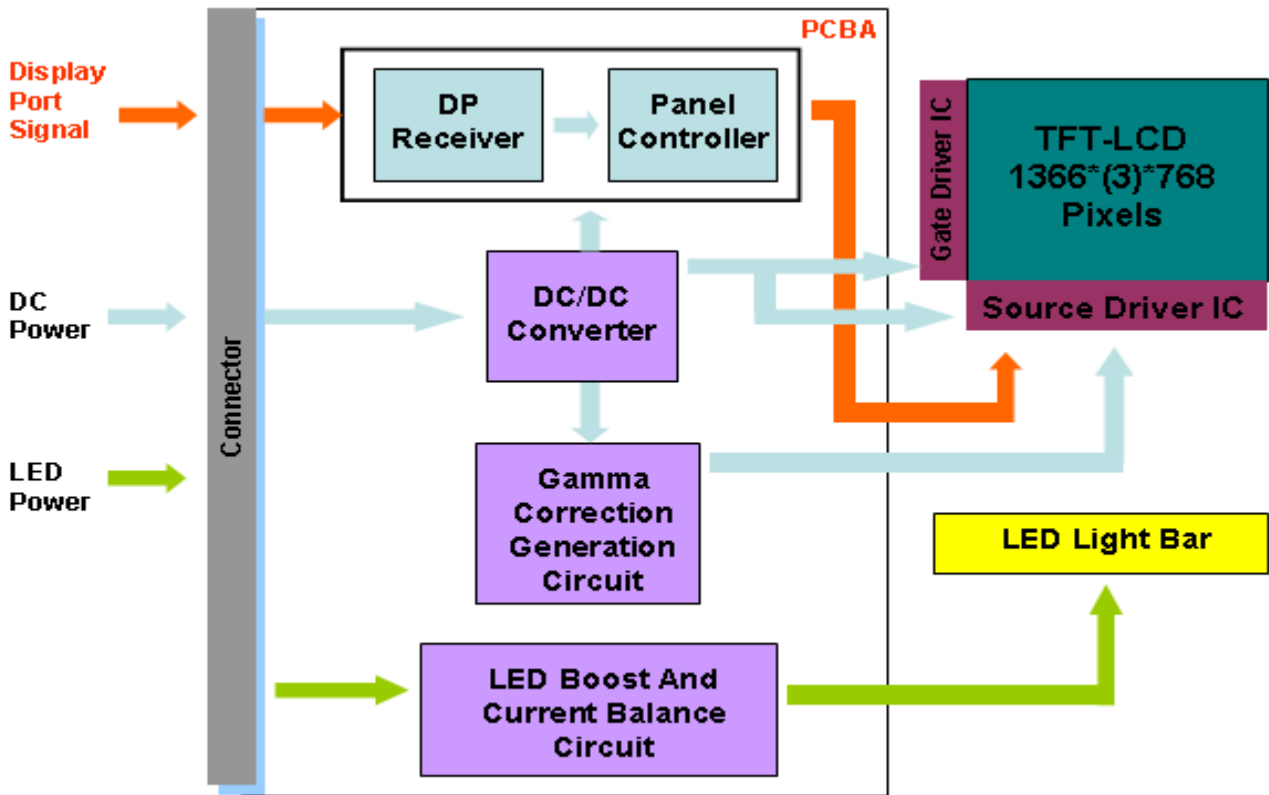
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

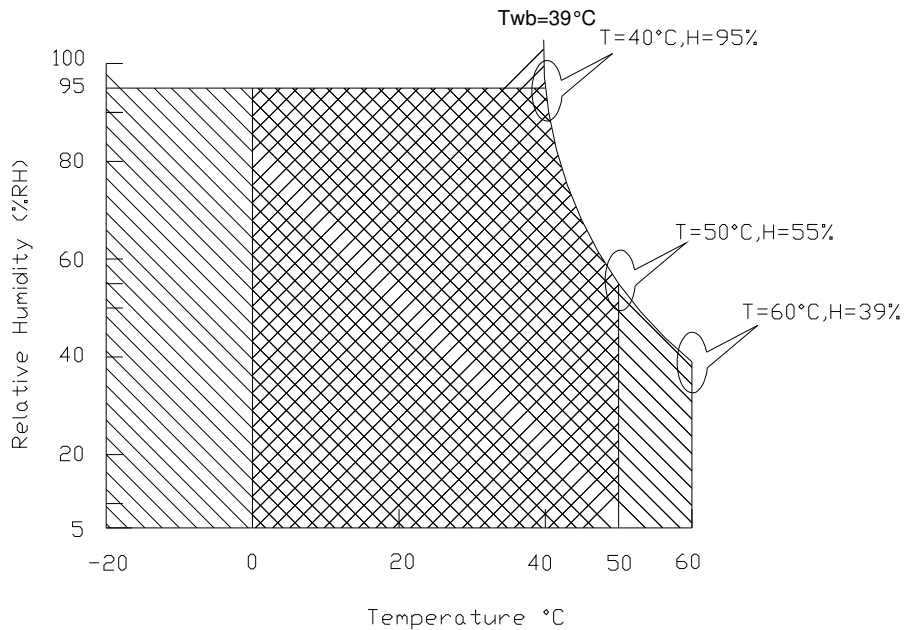
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

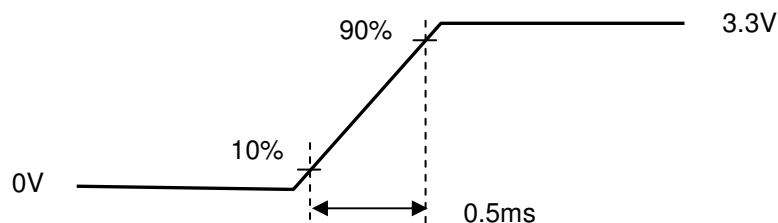
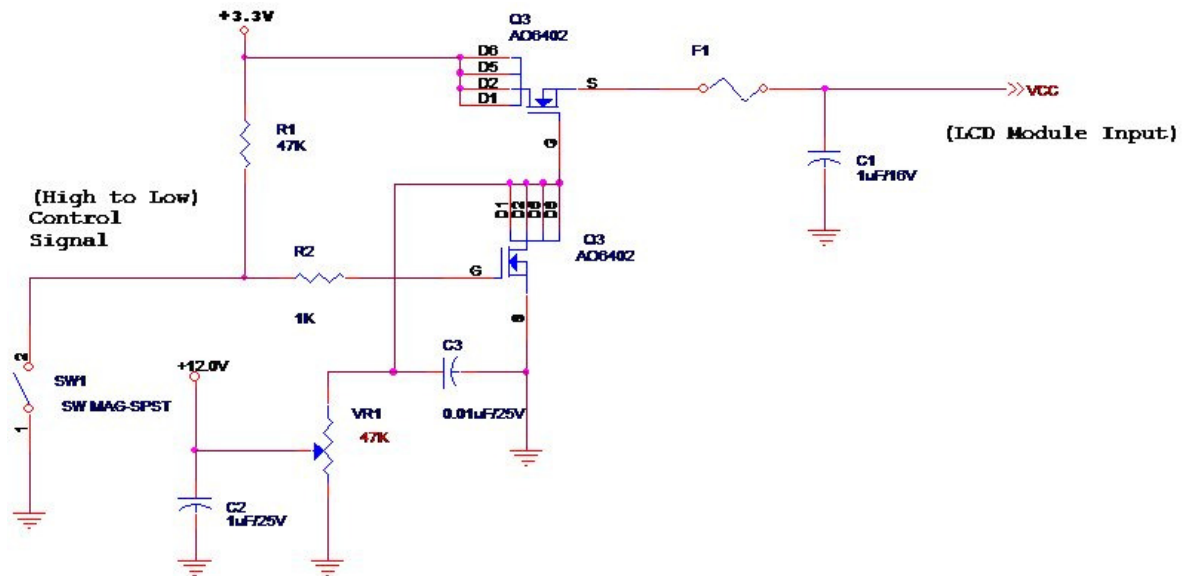
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	250	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2 : Measure Condition

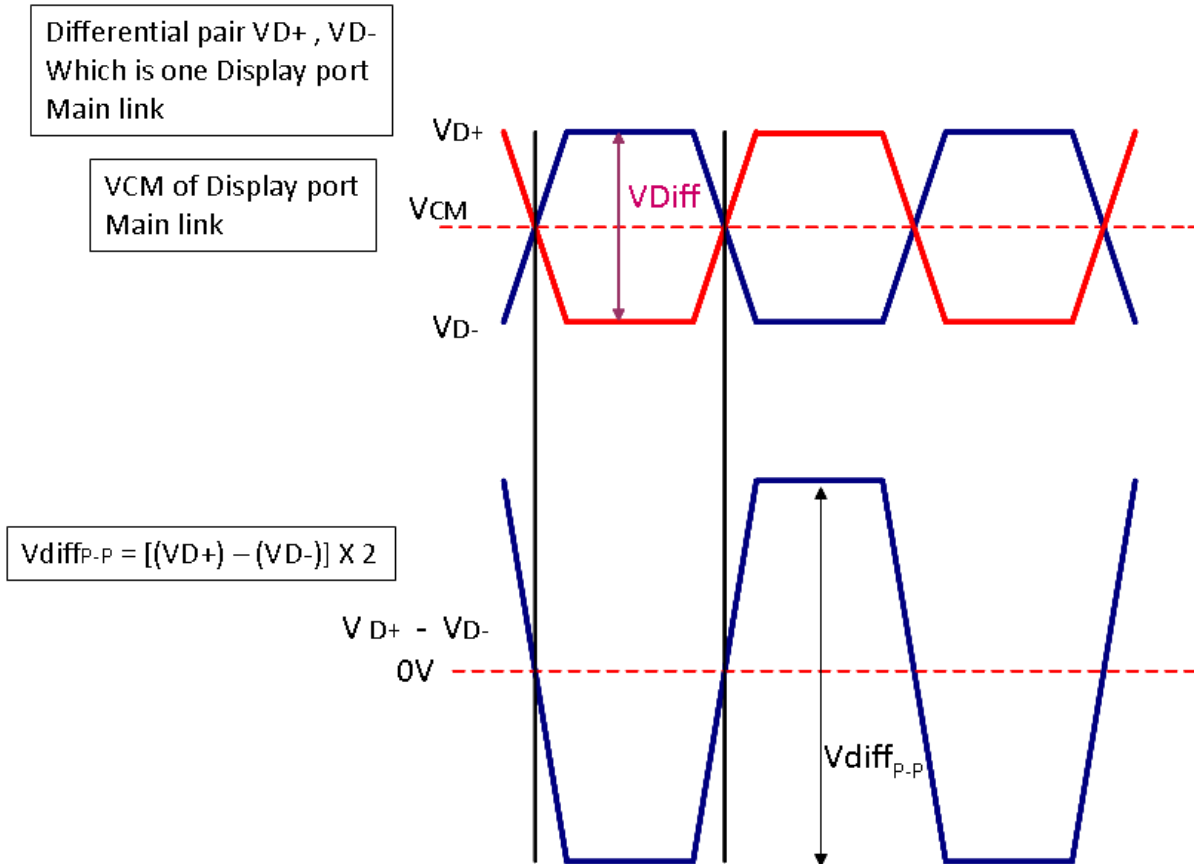


5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:

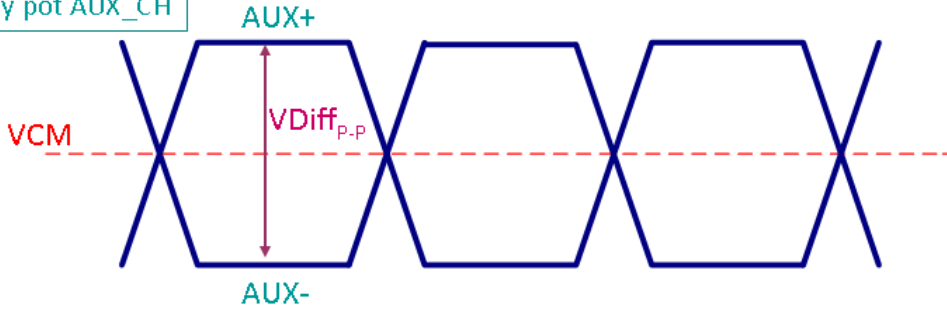


Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:

Differential AUX+ , AUX-
Which is Display port AUX_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff _{p.p}	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.7	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

Note 1: Calculator value for reference $P_{LED} = V_F$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	1 Note 2	-	100	%	

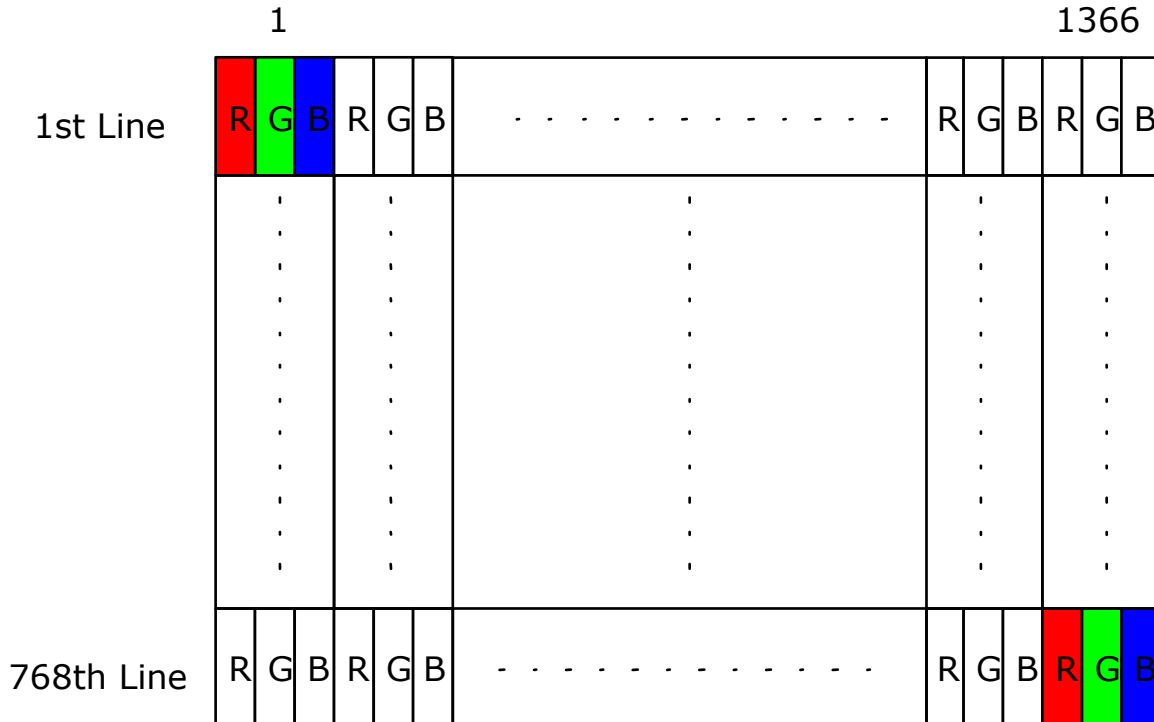
Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : If the PWM duty ratio(min) is set between 5% to 1% , the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

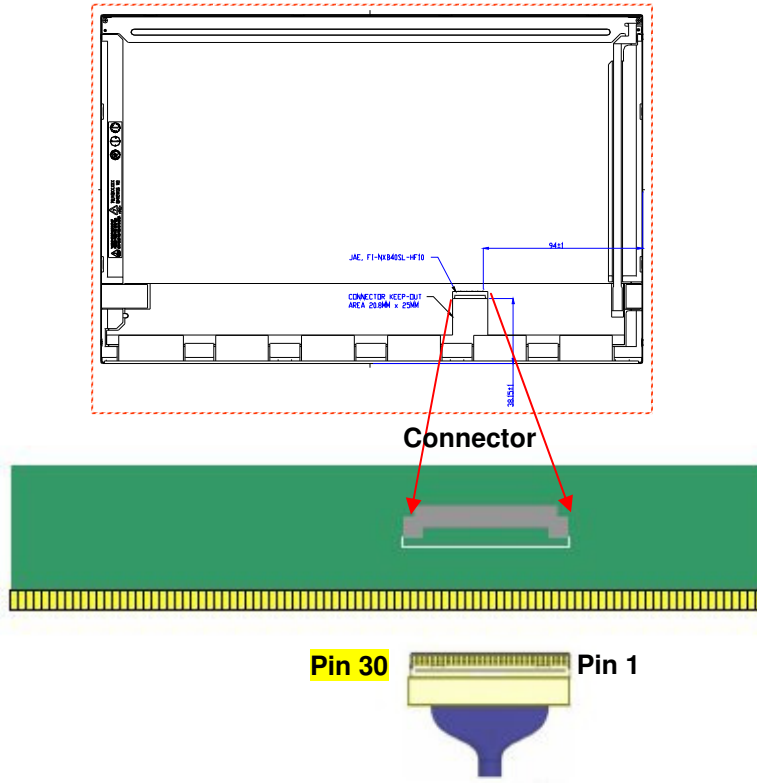
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-02 or compatible
Mating Housing/Part Number	IPEX 20455-030T-01 or compatible

6.2.2 Pin Assignment (1 Lane)

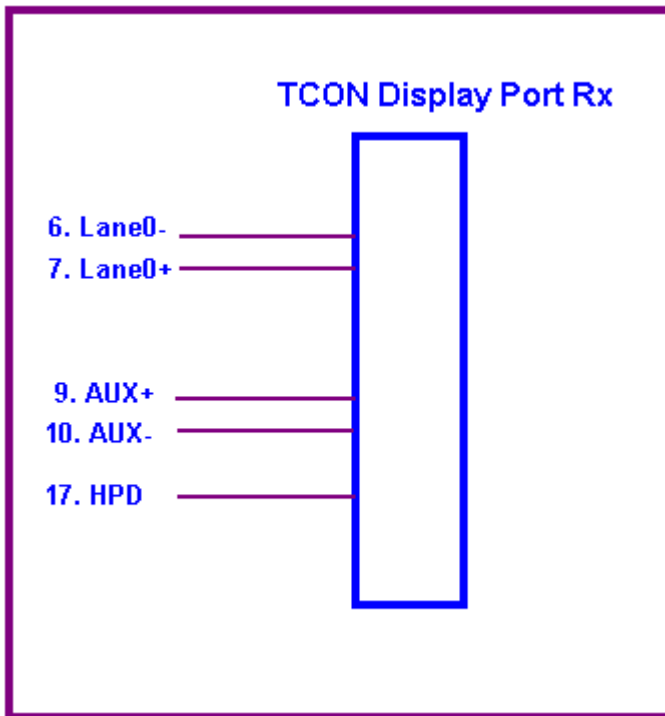
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	NC	No Connect
4	NC	No Connect
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off. Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

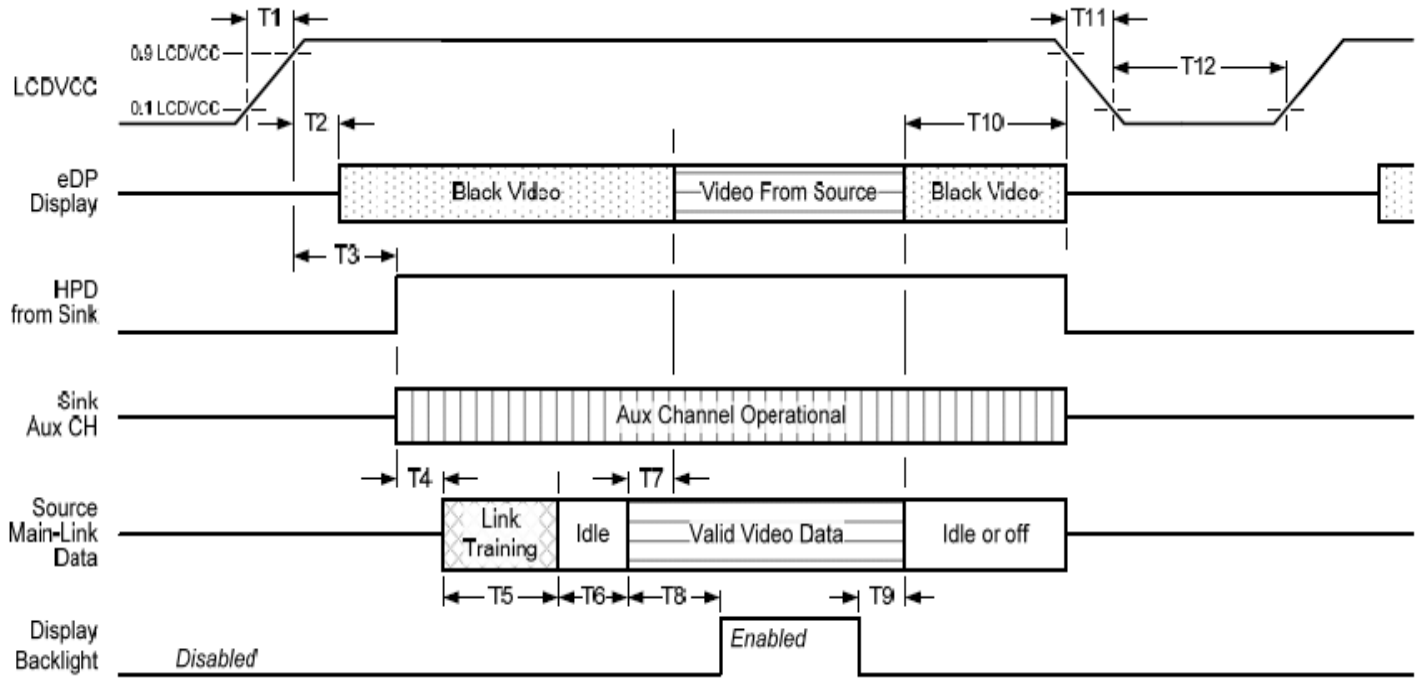
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	-	60	-	Hz	
Clock frequency	1/ T _{Clock}	66.9	72	80	MHz	
Vertical Section	Period	T _V	788	824	768+A	T _{Line}
	Active	T _{VD}	768			
	Blanking	T _{VB}	20	56	A	
Horizontal Section	Period	T _H	1416	1456	1366+B	T _{Clock}
	Active	T _{HD}	1366			
	Blanking	T _{HB}	50	90	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = $(1366+B)*(768+A)*60 < 80\text{MHz}$

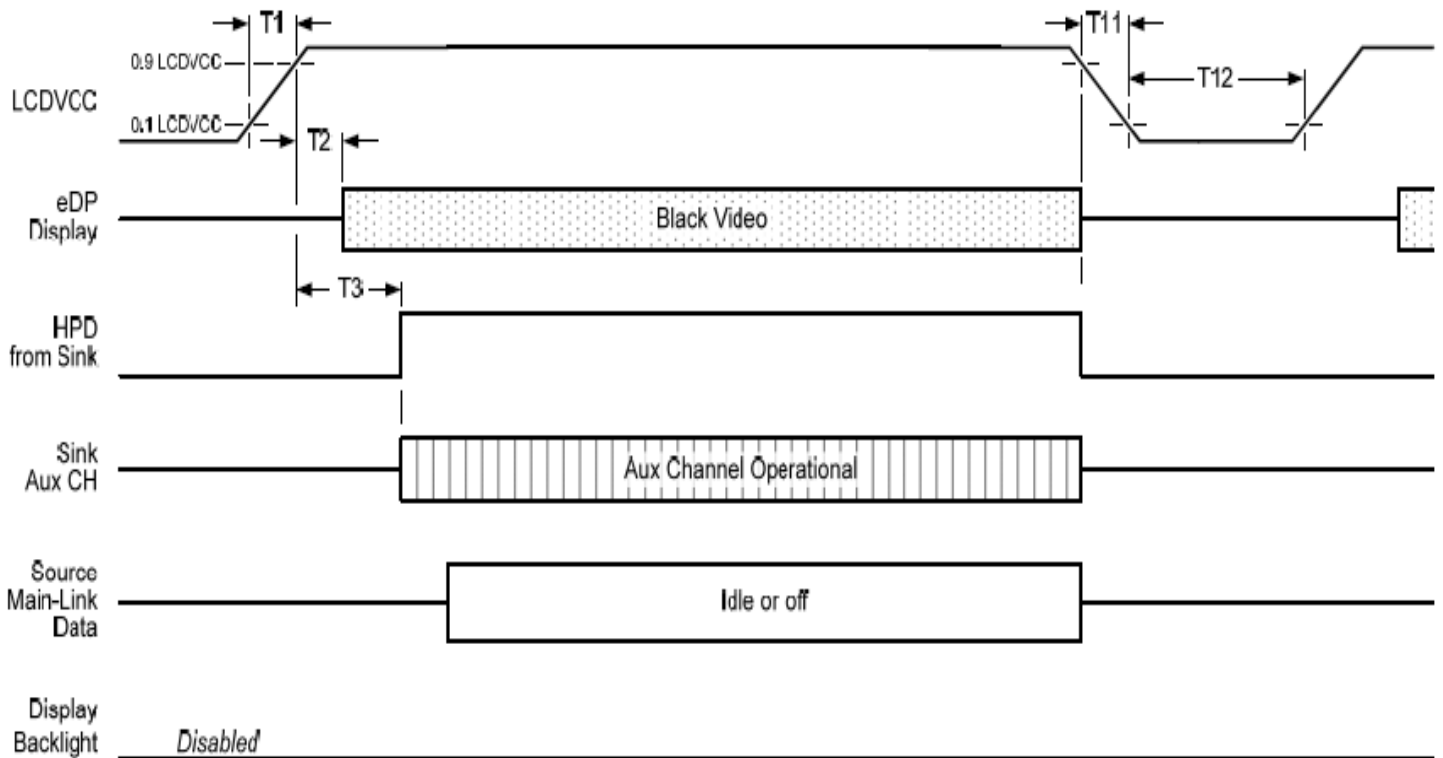
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:





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Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

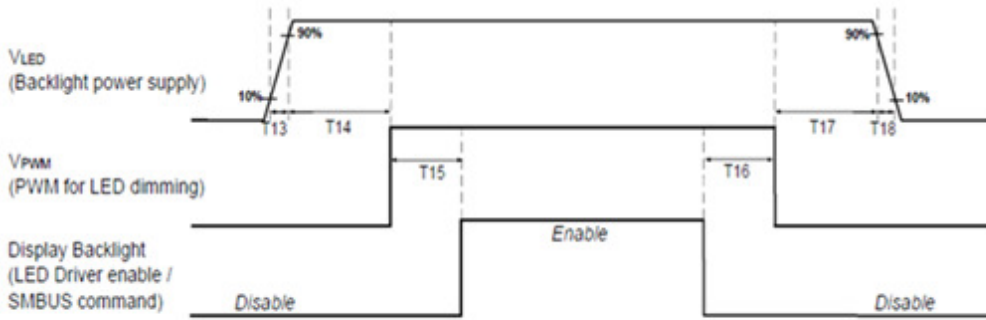
- upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

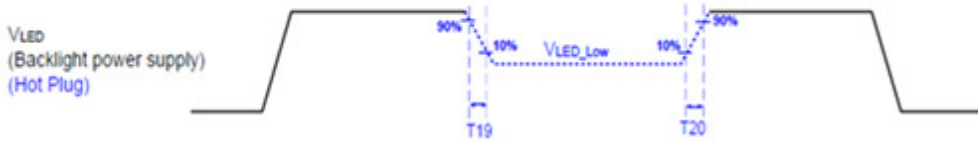
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1 [*]	-
T20	1 [*]	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

^{*} $T_{PWM} = 1/PWM \text{ Frequency}$

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 5 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

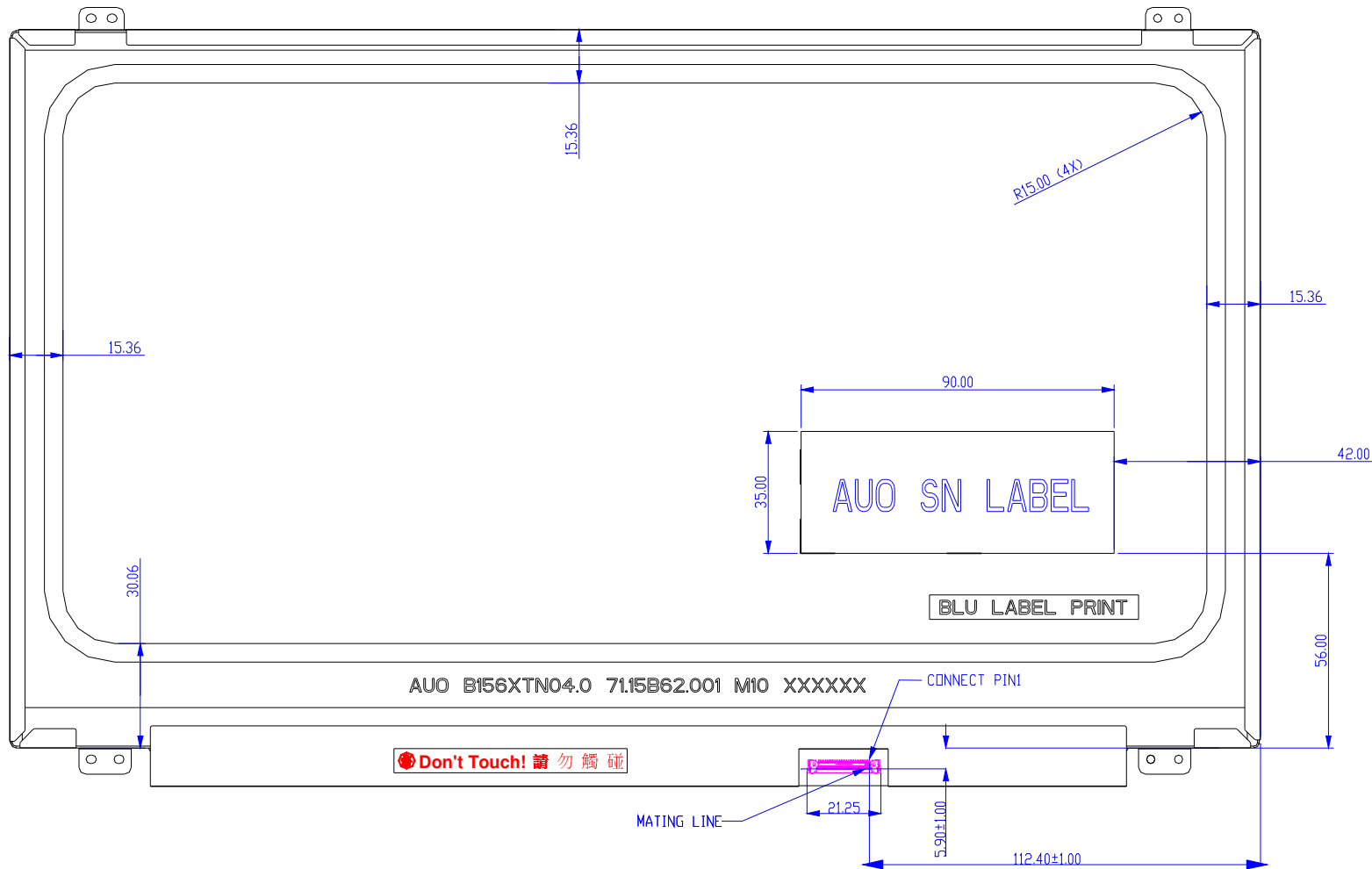
Note 1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed.

Self-recoverable. No data lost, No hardware failures.

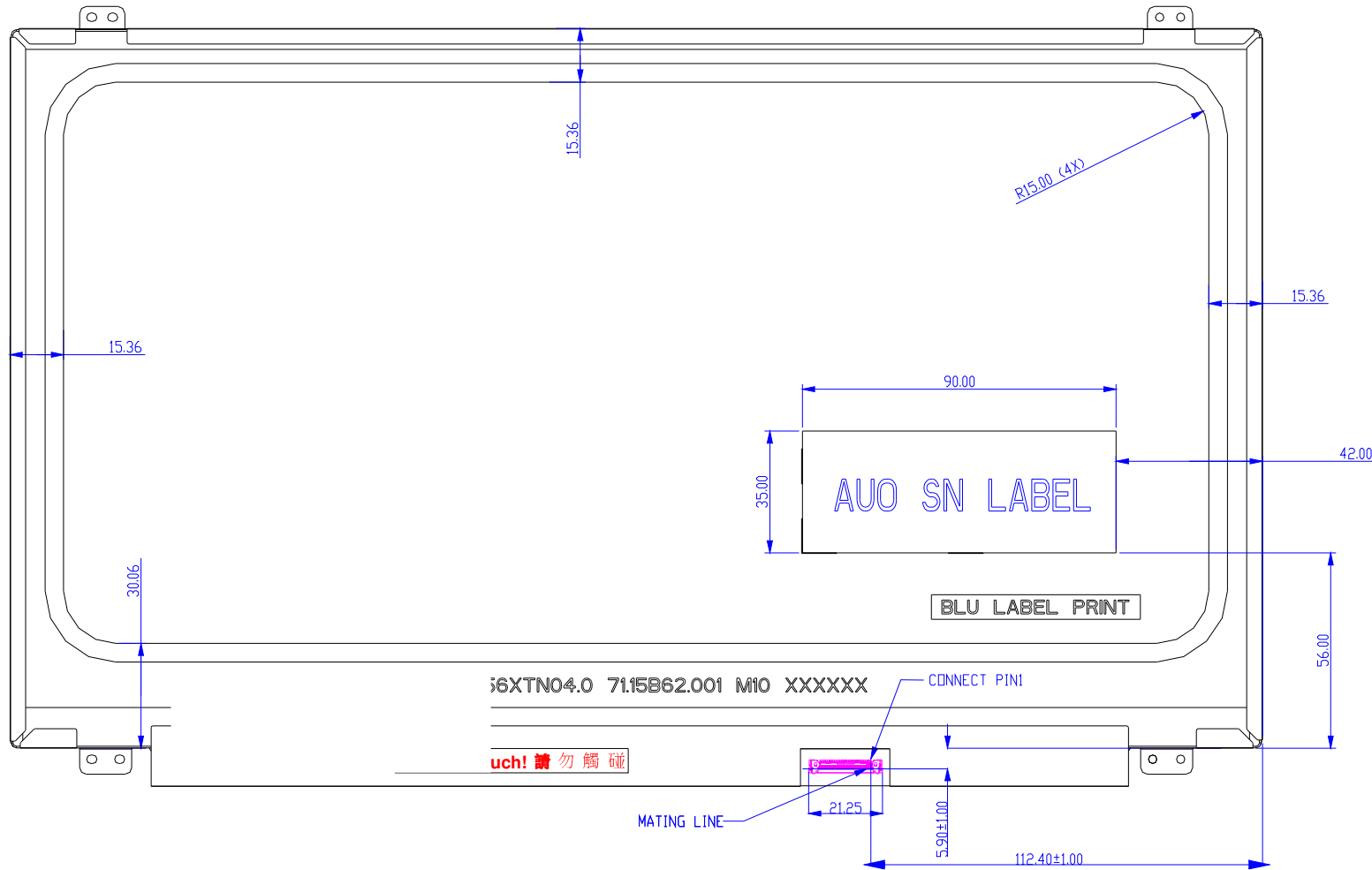
Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension



8.1.2 Standard Rear View





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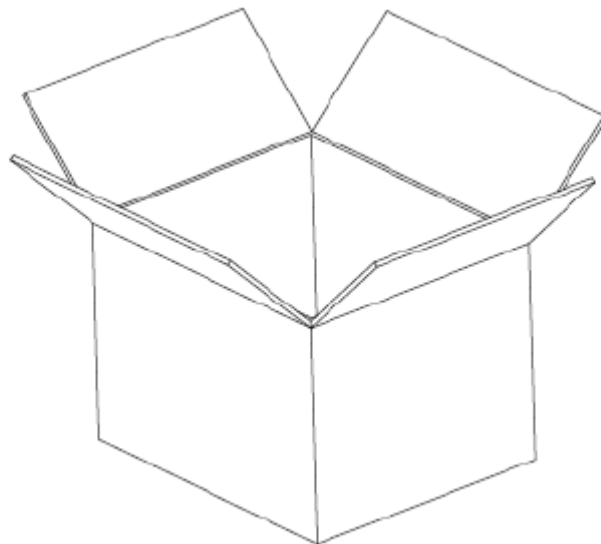
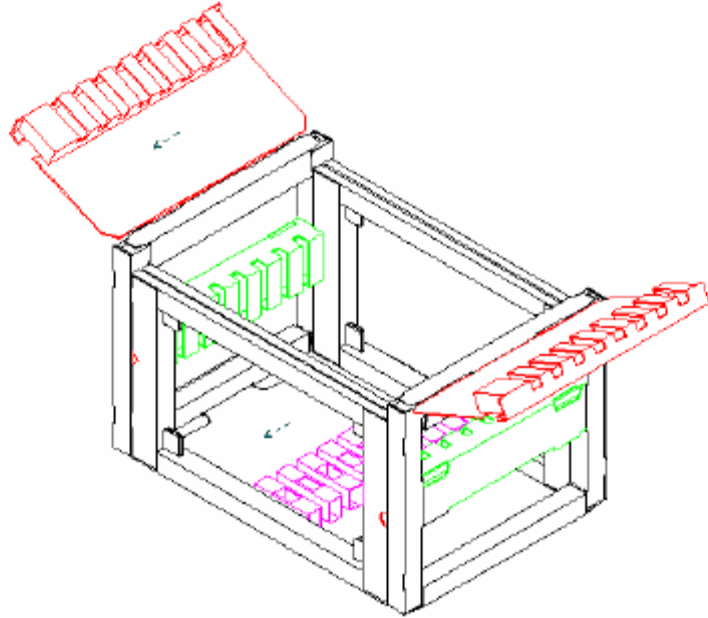
9. Shipping and Package

9.1 Shipping Label Format

	Manufactured MM/WW Model No: B156XTN04.0 AU Optronics MADE IN CHINA (Z31) H/W: 4A F/W:1	c  us E204356	
		RoHS	
B156XTN04.0			

9.2 Carton Package

The outside dimension of carton is 480(L)mm x 341 (W)mm x 302 (H)mm



9.3 Handling guide

This is a thin and slim LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

(1) Handling method notice



Do not lift and hold the panel with single hand at right or left side from tray.



Lift and hold the panel up with both hands from tray.

(2) On the table notice



Do not press edge of panel to avoid glass broken.

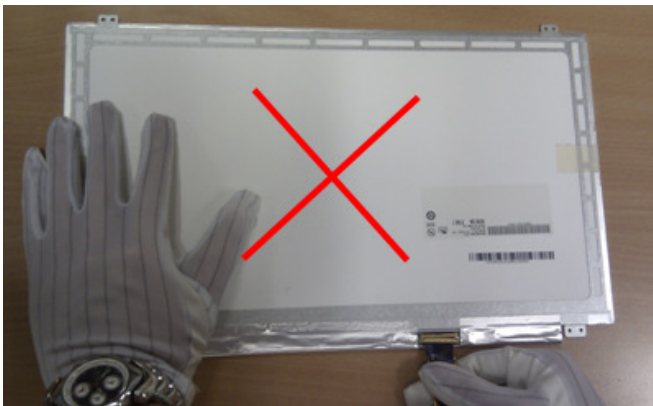


Do not press the surface of the panel to avoid the glass broken or polarizer scratch.



Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

(3) Cable assembly notice

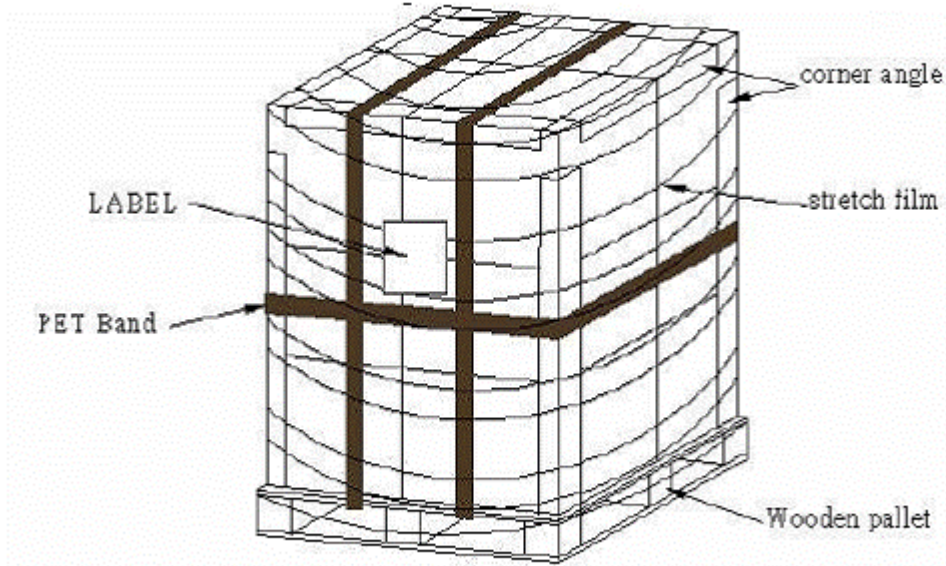


Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

9.4 Shipping Package of Palletizing Sequence





10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	EC	11101100	236
0B	hex, LSB first	40	01000000	64
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	29	00101001	41
11	Year of manufacture	17	00010111	23
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	95	10010101	149
15	Max H image size (<i>rounded to cm</i>)	22	00100010	34
16	Max V image size (<i>rounded to cm</i>)	13	00010011	19
17	Display Gamma (<i>=(gamma*100)-100</i>)	78	01111000	120
18	Feature support (<i>no DPMS, Active OFF, RGB, tmg Blk#1</i>)	02	00000010	2
19	Red/green low bits (Lower 2:2:2:2 bits)	BB	10111011	187
1A	Blue/white low bits (Lower 2:2:2:2 bits)	F5	11110101	245
1B	Red x (Upper 8 bits)	94	10010100	148
1C	Red y/ highER 8 bits	55	01010101	85
1D	Green x	54	01010100	84
1E	Green y	90	10010000	144
1F	Blue x	27	00100111	39
20	Blue y	23	00100011	35
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1



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27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	CE	11001110	206
37	Pixel Clock/10000 USB	1D	00011101	29
38	Horz active Lower 8bits	56	01010110	86
39	Horz blanking Lower 8bits	C0	11000000	192
3A	HorzAct:HorzBlk Upper 4:4 bits	50	01010000	80
3B	Vertical Active Lower 8bits	00	00000000	0
3C	Vertical Blanking Lower 8bits	30	00110000	48
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48
3E	HorzSync. Offset	08	00001000	8
3F	HorzSync.Width	0A	00001010	10
40	VertSync.Offset : VertSync.Width	31	00110001	49
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0
42	Horizontal Image Size Lower 8bits	58	01011000	88
43	Vertical Image Size Lower 8bits	C1	11000001	193
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0
47	Signal <i>(non-intr, norm, no stereo, sep sync, neg pol)</i>	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0



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53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0
5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	35	00110101	53
74	Manufacture P/N	36	00110110	54
75	Manufacture P/N	58	01011000	88
76	Manufacture P/N	54	01010100	84
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	34	00110100	52
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	30	00110000	48
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0



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7F	Checksum	EE	11101110	238
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* We design in EDID Non-rewriting function to prevent from being rewriting EDID in any case.