YAMAHA

YSS952

APPLICATION MANUAL

SPR-2

YAMAHA CORPORATION

YSS952 Application Manual
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PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

v02

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1 Overview

YSS952 (SPR-2) is an audio processing device with two DSPs and FM synthesizer, designed for applications like TV and Karaoke set and home audio system.

1.1 Features

- ○ Two dedicated DSP (MDSP2, SDSP) and FM synthesizer in a single package.
- ○ Voice application DSP (MDSP2: floating point, 73.728 MHz)
  - ・ Instructions RAM (MPRAM) 1.5k by 40 bits
  - ・ Coefficients RAM (CRAM) 1k by 16 bits
  - ・ Work RAM (WRAM0, WRAM1) 1k by 32 bits
  - ・ Delay line RAM (WRAM) 14k by 20 bits or 7k by 32 bits
    (up to 298 ms with f_s = 48 kHz, 'by 20 bits' configuration)
- ○ Auxiliary DSP (SDSP: fixed point)
  - ・ High quality asynchronous sampling rate converter (SRC: 2 channel, 8 to 192 kHz input range)
  - ・ 10 band parametric equalizer (2 channel)
- ○ FM Synthesizer
  - ・ Integrated the Yamaha FM Synthesizer
  - ・ Integrated melody sequencer
  - ・ Up to four voices (with four different tones)
- ○ On chip ROM (Preset ROM) 65k by 8 bits
  - ・ Preset signal processing programs for MDSP2 [Note 1]
  - ・ Preset FM synthesizer data for startup sounds and keypad/alert tones
- ○ MDSP2 runs the signal processing programs download from host controller.
  - ・ Changing coefficients data for the programs possible with downloading.
- ○ Audio interfaces
  - ・ Digital inputs up to 6 channels (2 channels through SRC)
  - ・ Digital outputs up to 4 channels plus 2 channel amplifier outputs
- ○ Operating Supply Range: 3.0V to 3.6V (IOVDD), 1.65V to 1.95V (DVDD18, PLLVDD)
- ○ On chip PLL
- ○ Package information
  - ・ Lead-free 32-pin QFN [with bottom heat pad] (YSS952-QZ)

[Note 1] Use 24.576MHz clock on XIN pin for the MDSP2 preset programs on the on-chip ROM.
All the signal processing after SRC including MDSP2 will use 48 kHz sampling rate.

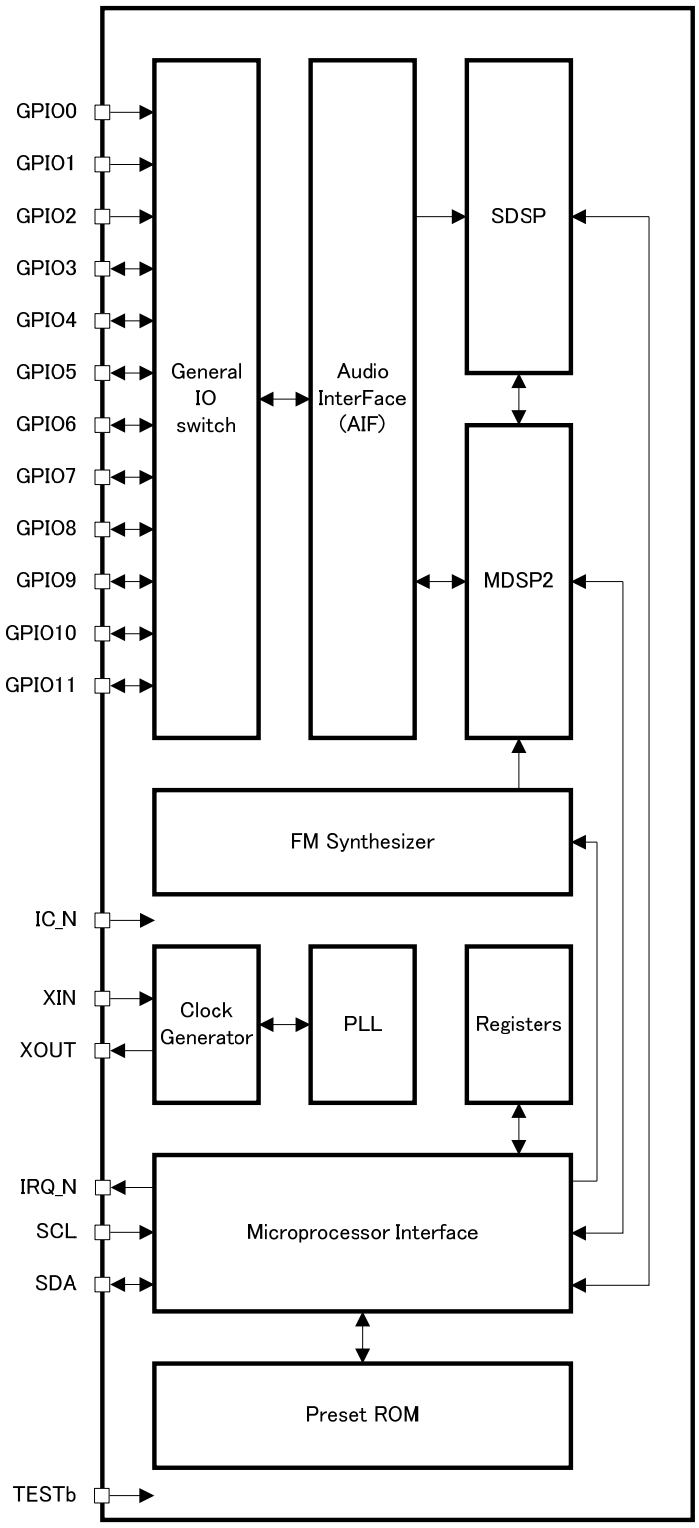
1.2 Applications

- ○ Flat panel TVs
- ○ Karaoke sets
- ○ Home audio systems
- ○ Portable media equipments

1.3 Term Definition

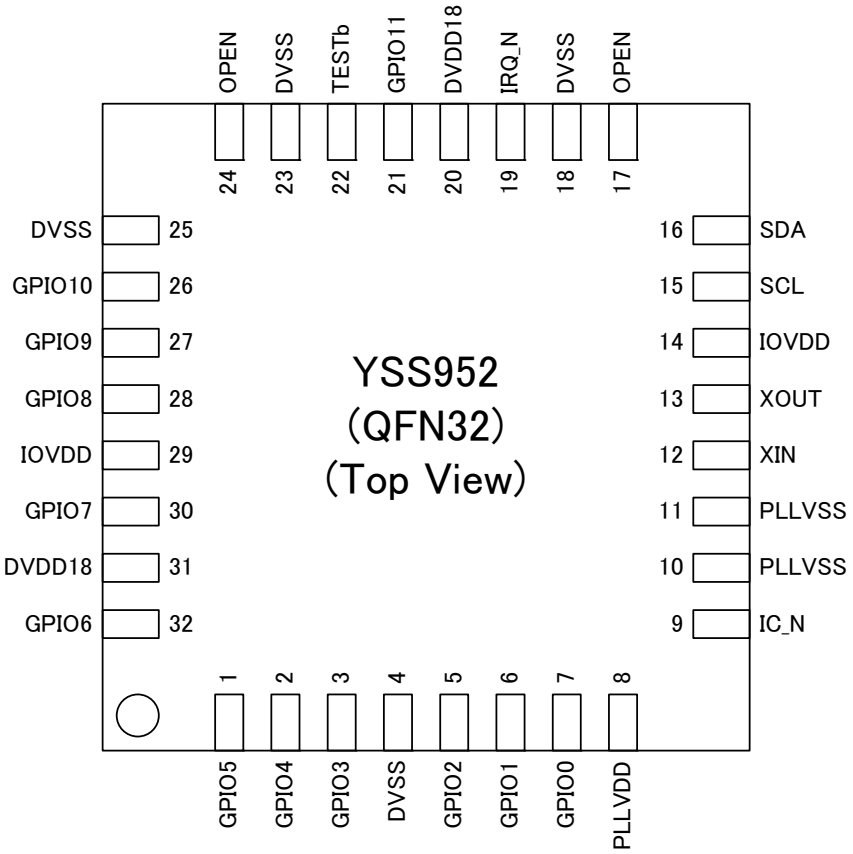
Normal operation	Digital amplifier is active, and ready to amplify its input signals.
DPLL	Digital Phase-Locked Loop; calculates the frequency ratio and phase difference by sampling rate conversions.

1.4 Block Diagram



2 Pin Function

2.1 Pin Assignment



2.2 Pin Descriptions

Function	Pin No.	Pin Name	I/O[Note 1]	Description
I^2C Interface	15	SCL	Is	I^2C control bus clock input pin (not 5V tolerant)
	16	SDA	Is/Od	I^2C control bus data I/o pin (not 5V tolerant)
General-purpose Input/Output	7	GPIO0	Is	General-purpose I/O pins These I/O pin are assigned to the digital audio pins (WCK/BCK/SDIx/SDOx) with AIFMD[3:0] register. (5V tolerant)
	6	GPIO1	Is	
	5	GPIO2	Is	
	3	GPIO3	Is/O	
	2	GPIO4	Is/O	
	1	GPIO5	Is/O	
	32	GPIO6	Is/O	
	30	GPIO7	Is/O	
	28	GPIO8	Is/O	
	27	GPIO9	Is/O	
	26	GPIO10	Is/O	
	21	GPIO11	Is/O	
System	9	IC_N	Is	Hardware reset pin. (5V tolerant)
	12	XIN	I	Clock input pin. Connect a 22.5792MHz or 24.576MHz crystal resonator as shown in the example below: [Notes 2, 3] When a crystal resonator is not used, feed a clock of 22.5792MHz or 24.576MHz to XIN pin. (Change the input clock frequency only when IC_N is at "L" level.)
	13	XOUT	O	Clock output pin Connect the external circuit as shown in the example below. [Note 3] When an external clock is directly fed to XIN pin without a crystal resonator, leave this pin open. Use this pin only for clock generation.
	19	IRQ_N	Od	Interrupt request output pin to the host controller. (Interrupt request generating from DSP block)
Test	22	TESTb	Is	Test pin Connect this pin to the GND.
Power	14	IOVDD	–	Control interface power supply ranging from 3.0V to 3.6V.
	29			
	20	DVDD18	–	Core power supply ranging from 1.65V to 1.95V.

Function	Pin No.	Pin Name	I/O[Note 1]	Description
	31			
	8	PLLVDD	–	PLL power supply ranging from 1.65V to 1.95V. [Note 4]
	4	DVSS	–	GND
	18			
	23			
	25			
	10	PLLVSS	–	PLL GND [Note 4]
	11			
Not used	17	OPEN	–	Leave this pin open. [Note 5]
	24	OPEN	–	Leave this pin open. [Note 5]

[Note 1] I/O symbols

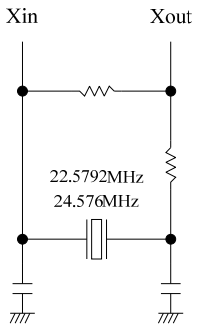
- I : Input pin
- Is : Schmitt trigger input pin
- O : Output pin
- Od : Open-drain output
- Ot : Tri-state output pin
- I/O : I/O pin
- Is/Od : I/O pin (schmitt trigger input pin, Open-drain output pin)
- – : Power supply pin, GND pin

[Note 2] XIN pin Input Frequency

24.576MHz clock should be fed to XIN pin if MDSP2 firmware stored in the on-chip ROM is used.

See "3.7.3.1 Sampling Frequency Setting" for details.

[Note 3] The figure below shows an example of connecting a crystal resonator:



* Select appropriate resistor and capacitor values according to the resonator's specification.

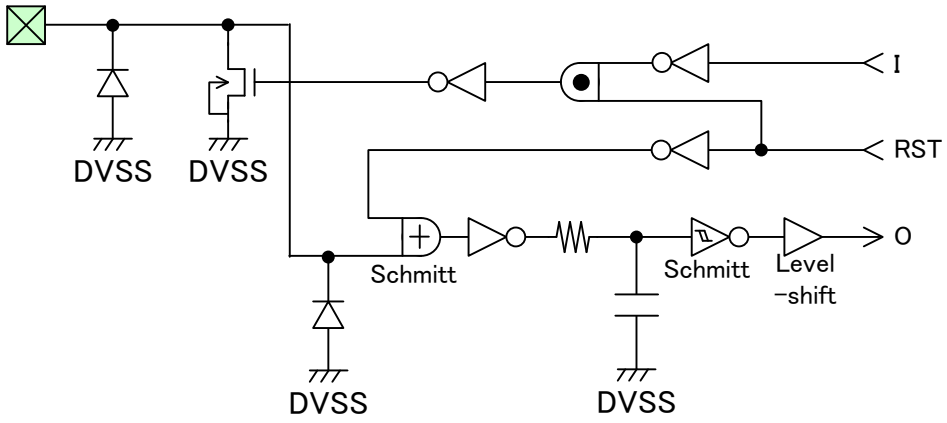
[Note 4] PLLVDD and DVDD18 should be same voltage because they are internally connected each other.

PLLVSS and DVSS pins are also internally connected as well.

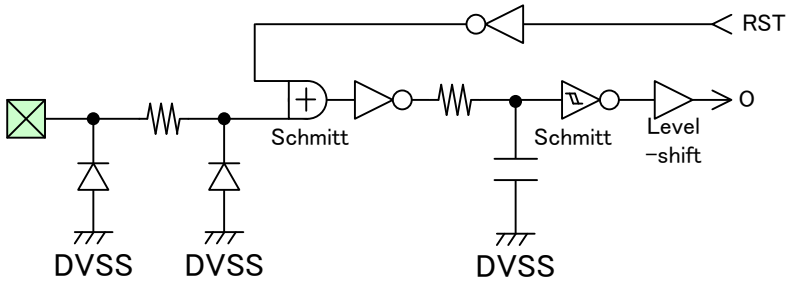
[Note 5] OPEN pins must not be connected each other.

2.3 Pin Circuit Description

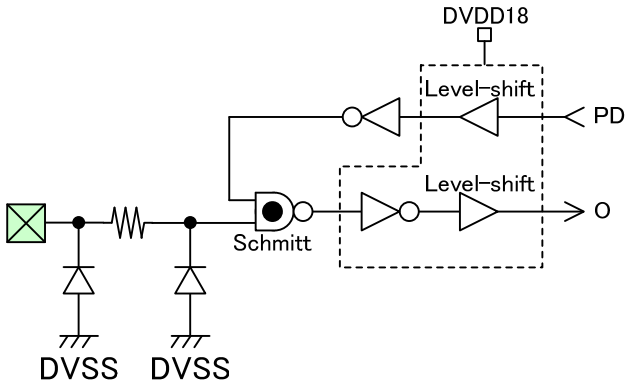
SDA



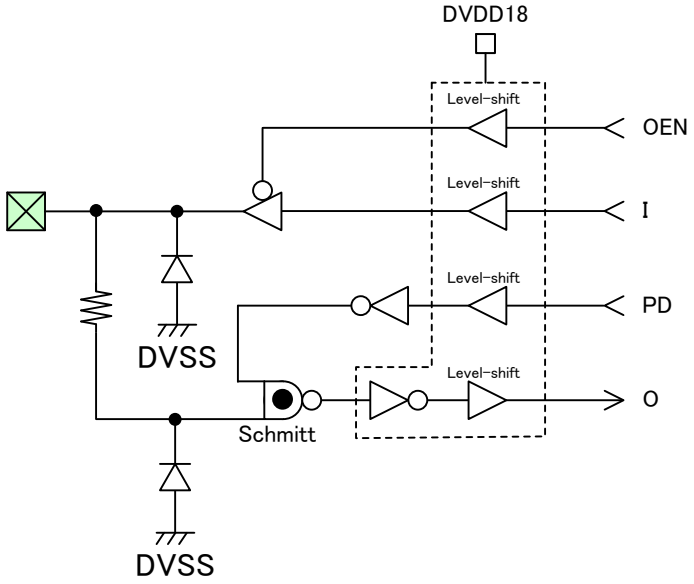
SCL



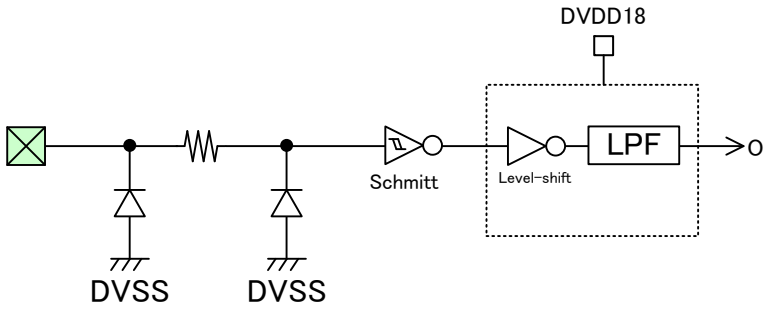
GPIO 0-2



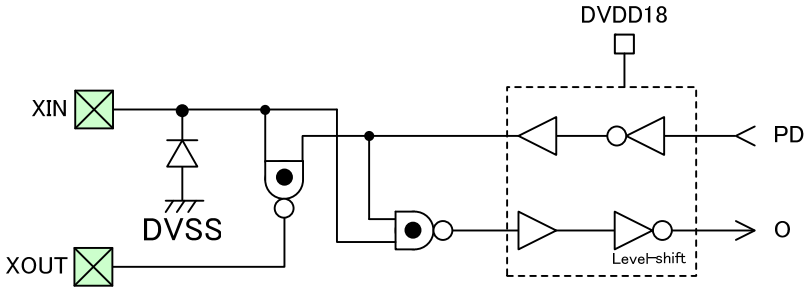
GPIO 3-11



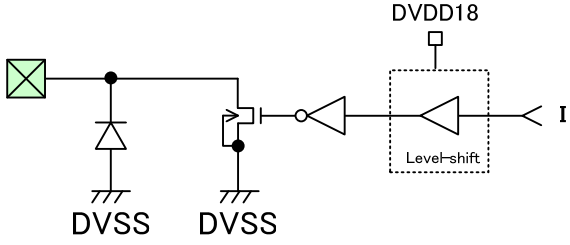
IC_N



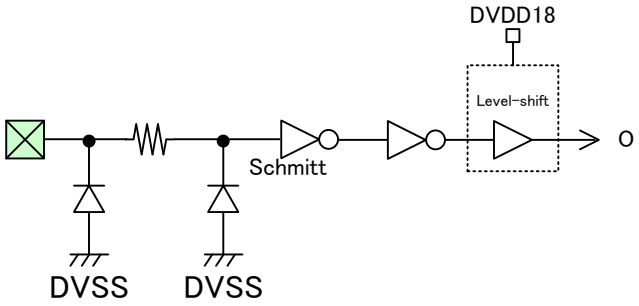
XIN XOUT



IRQ_N



TESTb



2.4 Pin States

2.4.1 Power-Off Mode

Do not supply any voltage to pins other than SDA and SCL pins in this mode.

If there's active signal on input pins when the device is in power-off mode, the signal can power output pins into driving states through the input protection circuit. The output signals become undefined.

SDA pin enters the Hi-Z state in this mode.

2.4.2 Hardware Reset Mode

Pin Name	I/O	State
SCL	Is	H/L input
SDA	Is/Od	Hi-Z output
GPIO11-3	Is/O	H/L open input
GPIO2-0	Is	H/L open input
IC_N	Is	L input
XIN	I	Clock input
XOUT	O	Clock output
IRQ_N	Od	Hi-Z
TESTb	Is	L input

2.4.3 Normal Operation Mode

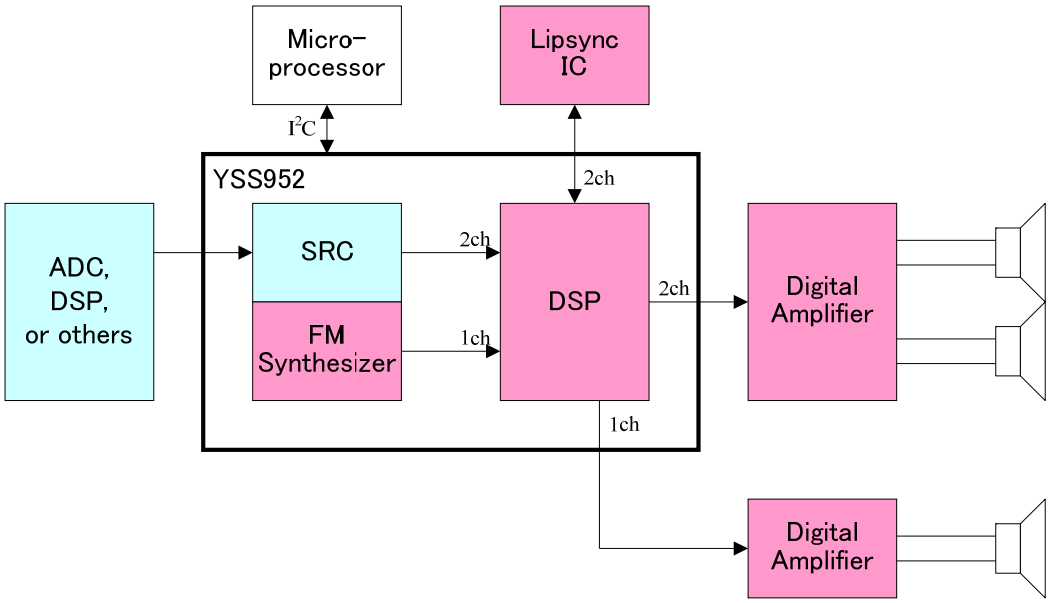
Pin Name	I/O	State
SCL	Is	Clock Input
SDA	Is / Od	Data input or L, Hi-Z output
GPIO11-3	Is / O	Data, Clock input or Data, Clock output
GPIO2-0	Is	Data input
IC_N	Is	H input
XIN	I	Clock input
XOUT	O	Clock output
IRQ_N	Od	Hi-Z / L output
TESTb	Is	L input

2.5 System Configuration Examples

indicates source devices and on-chip blocks that run with the sample rate of the front end source device.

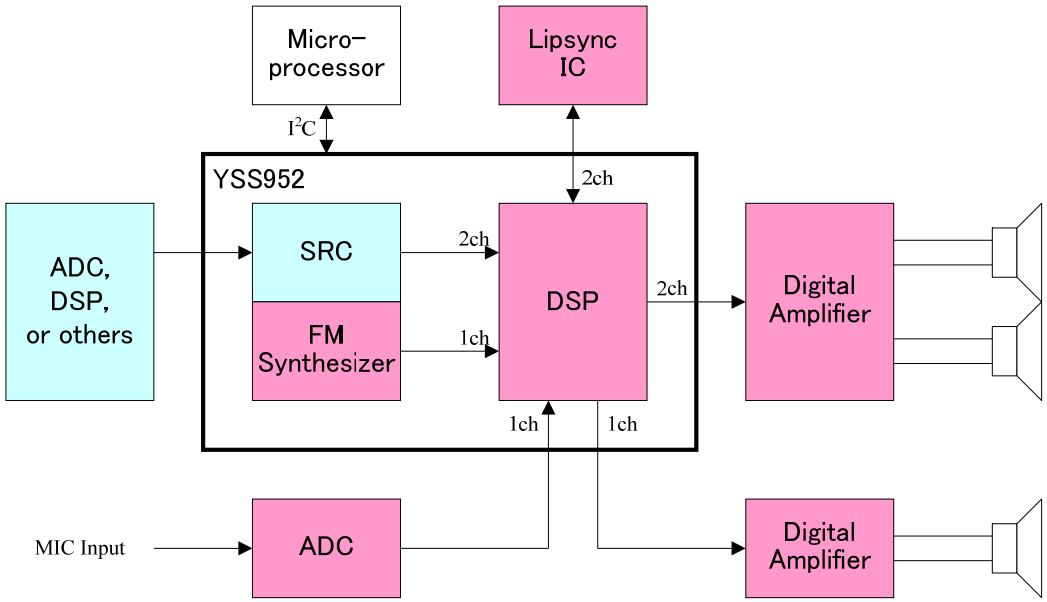
indicates devices and on-chip blocks that run with the sample rate generated by this device.

- TV Set Application

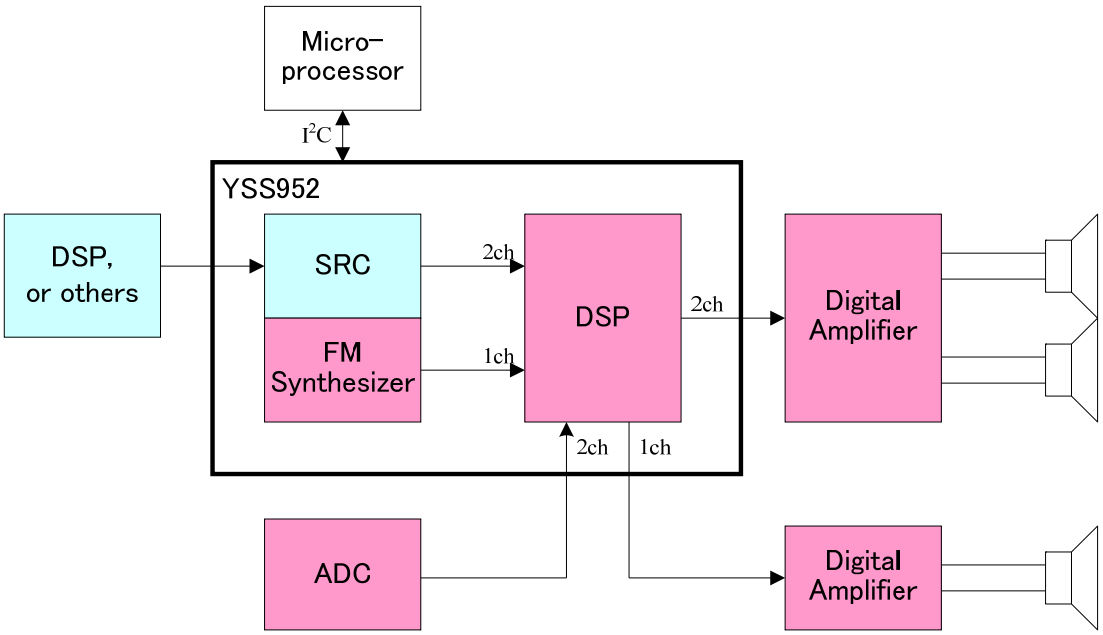


* An external lip sync IC can be connected. The external lip sync device allows longer time adjustments

- Application for TV or Set Top Box with Karaoke



- Application for docking speaker system



2.6 Firmware

The firmware that comes with this device provides a variety of functions that control and improve the playback sound through speakers on TV system, mini compo, etc.

The following two firmware modes can be switched according to customer's requirements.

1) Audio Video Mode (A/V mode)

A/V mode provides surround effect that simulates room/hall reflections, in addition to basic DSP functions such as lip synchronization, equalization, or cross-over filtering.

2) Karaoke Mode

Karaoke mode provides the standard karaoke functions like microphone echoes and key controls, in addition to basic DSP functions such as lip synchronization, equalization, or cross-over filtering.

The firmware that comes with this device handles 2-ch audio signals and supports the sampling rate of 48 kHz.

This firmware also handles 1-ch microphone input signal in Karaoke mode.

The table below summarizes the firmware functions.

Function	Abbr.	Operation Mode		Description
		A/V	Karaoke	
Top	-	✓	✓	Provides runtime transfer service to the other firmware
Lip sync	LPS	✓	✓	Delays audio input signal up to 149 ms.
Level detect	LD		✓	Detects input microphone signal level.
Voice cancel	VC		✓	Cancels the vocal part in the audio signal.
Key Control	KC		✓	Shifts the pitch of played music.
Early reflection	ER	✓	✓	Simulates early- reflections.
Reverb/Echo	RE	✓	✓	Simulates reverberations and microphone echo.
Phantom 3D	P3D	✓	✓	Enhances spatial effect and realistic sensation of a source signal with virtual 3D processing.
Parametric equalizer	PEQ	✓	✓	3-band parametric equalizer for equalization.
Dynamic range compressor 3	DRC3	✓		3-band independent dynamic range compressors for the natural compression.
Graphic equalizer	GEQ	✓	✓	5-band graphic equalizer with tone control for equalization.
Smooth volume	SV	✓	✓	Allows master volume to transition smoothly and provides loudness control at the same time.
Crossover filter	CF	✓	✓	Configures 1-way, 2-way, or 2.1 digital crossover networks.
Output distributor	OD	✓	✓	Selects the output audio signals.

Block Diagram

The figures below show the firmware block diagram.

[Note]

- Top firmware, not related to the signal processing, are omitted in the following diagram.
- A through E in the digram indicate the following output path options.

  A: External lip sync device output path

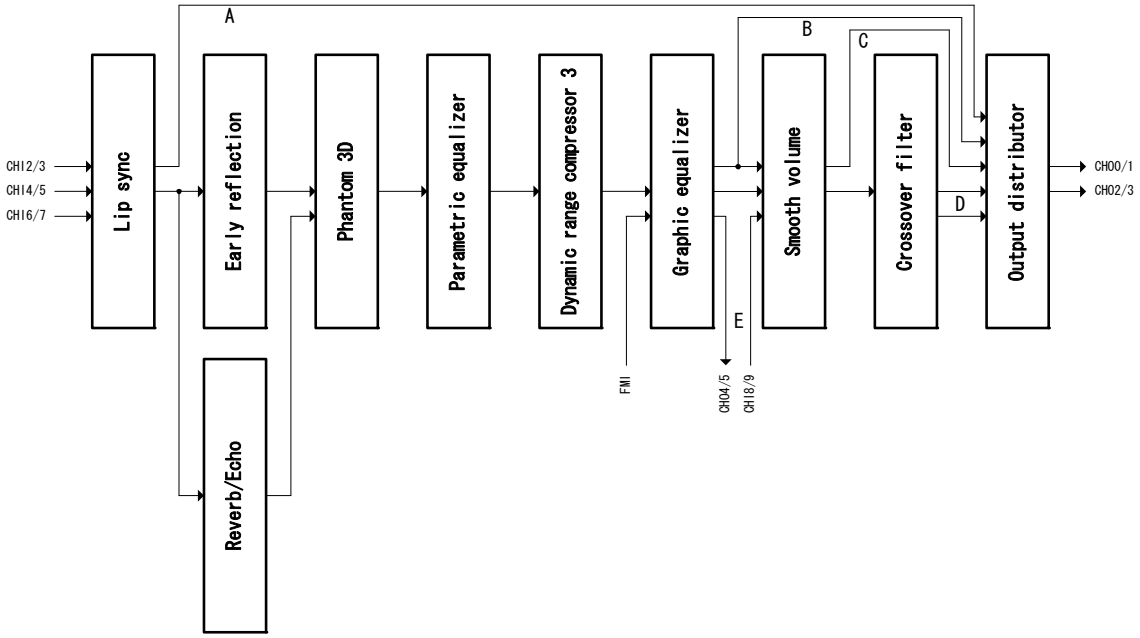
  B: Line output path

  C: Line output with the volume tracking equalizer

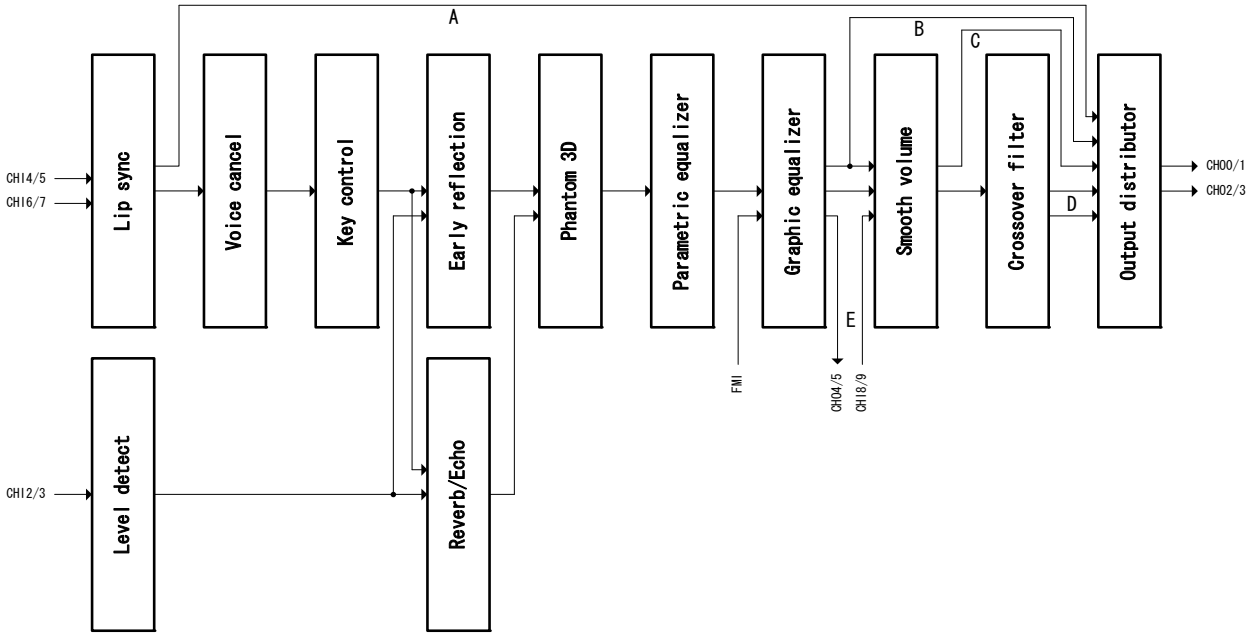
  D: Main output path

  E: SDSP 10-band PEQ processing path

(1) Audio Video Mode



(2) Karaoke Mode



3 FUNCTION DESCRIPTION

3.1 Register Descriptions

3.1.1 Register Map

Address	Name	W/R [Note 1]	Reset value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	POEN0	R/W	0x00	0	0	0	0	POEN[11:8]			
0x01	POEN1	R/W	0x00	POEN[7:3]					0	0	0
0x02	PIDT0	R	0x00	0	0	0	0	PIDT[11:8]			
0x03	PIDT1	R	0x00	PIDT[7:3]					0	0	0
0x04	PODT0	R/W	0x00	0	0	0	0	PODT[11:8]			
0x05	PODT1	R/W	0x00	PODT[7:3]					0	0	0
0x06	SYSMD	R/W	0x00	0	0	0	0	0	DEVMD	HANGUPP	HANGUPR
0x07	AIFMD	R/W	0x10	0	0	PI	PIO	AIFMD[3:0]			
0x08	AIFIFMT	R/W	0x00	0	0	SDIFMT[1:0]		SDIBIT[1:0]		SDIWCKP	SDIBCKP
0x09	AIFOFMT	R/W	0x00	0	0	SDOFMT[1:0]		SDOBIT[1:0]		SDOWCKP	SDOBCKP
0x0A	MDSPMD	R/W	0x00	0	0	0	0	0	0	WRAMRTMD	WRAMMD
0x0B	SDSPMD	R/W	0x00	0	0	0	0	0	0	DEMON	DCM
0x0C			0x60	0	1	1	0	0	0	0	0
0x0D	IRQN	R/W	0x01	0	0	0	0	0	0	0	EXIRQN
0x0E	FSM	R/W	0x00	0	0	0	0	0	0	FSM[1:0]	
0x0F	RAMCLR	R/W	0x00	0	0	0	0	0	MPRAMCLR	WRAMCLR	SWRAMCLR
0x10	MUTE	R/W	0x00	0	0	0	0	0	FMMUTEN	MDSPMUTEN	SDSPMUTEN
0x11	DSPSTART	R/W	0x00	0	0	0	0	0	0	MDSPSTART	SDSPSTART
0x12			0x00	0	0	0	0	0	0	0	0
0x13	MDSPREQ	R/W	0x00	MDSPREQ[7:0]							
0x14	MDSPDAT	R/W	0x00	MDSPDAT[7:0]							
0x15	MIREQ	R/W	0x00	MIREQ[7:0]							
0x16	MIDAT	R/W	0x00	MIDAT[7:0]							
0x17	DPLLFS	R	0x20	DPLLFS[7:0]							
0x18	ZDET	R	0x00	ZDET[7:0]							
0x19	ID	R	0xC0	ID[7:0]							
0x1A	FMST	R/W	0x00	0	0	0	STEN	0	0	0	STFLG
0x1B	MDSPST	R/W	0x00	0	0	0	0	0	0	0	MDSPERR[Note 2]
0x1C			0x00	0	0	0	0	0	0	0	0
0x1D			0x00	0	0	0	0	0	0	0	0
0x1E	STEP0	R	0x00	STEP[15:8]							
0x1F	STEP1	R	0x00	STEP[7:0]							
0x20	SDSPST	R/W	0xF0	SDIERR[Note 2]	1	1	UNLOCK[Note 2]	FSIERR[Note 2]	FSERR[Note 2]	0	SDSPERR[Note 2]
0x21	-		0x00	0	0	0	0	0	0	0	0
0x22	-		0x00	0	0	0	0	0	0	0	0
0x23	PLLERR	R/W	0x00	0	0	0	0	0	PLLERRE	0	PLLERR[Note 2]
0x24			0x04	0	0	0	0	0	1	0	0
0x25			0x00	0	0	0	0	0	0	0	0
0x26			0x00	0	0	0	0	0	0	0	0
0x27			0x00	0	0	0	0	0	0	0	0
0x28			0x00	0	0	0	0	0	0	0	0
0x29			0x04	0	0	0	0	0	1	0	0
0x2A			0x2E	0	0	1	0	1	1	1	0
0x2B			0x00	0	0	0	0	0	0	0	0
0x2C			0x01	0	0	0	0	0	0	0	1
0x2D			0x07	0	0	0	0	0	1	1	1
0x2E			0xFF	1	1	1	1	1	1	1	1

Address	Name	W/R [Note 1]	Reset value	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2F			0x00	0	0	0	0	0	0	0	0
0x30			0x0E	0	0	0	0	1	1	1	0
0x31			0x00	0	0	0	0	0	0	0	0
0x32			0x00	0	0	0	0	0	0	0	0
0x33	PWRDWN	R/W	0x00	0	0	0	0	0	0	0	DPD
0x34 to 0x3F	Reserved	R	0x00	0	0	0	0	0	0	0	0

Indicates this area can be accessed in normal operation mode.

Indicates reserved areas. Write the initial values specified in the above table in a write operation.
The read value is undefined.

Indicates this area can be accessed regardless of whether the PLL is oscillated or not.

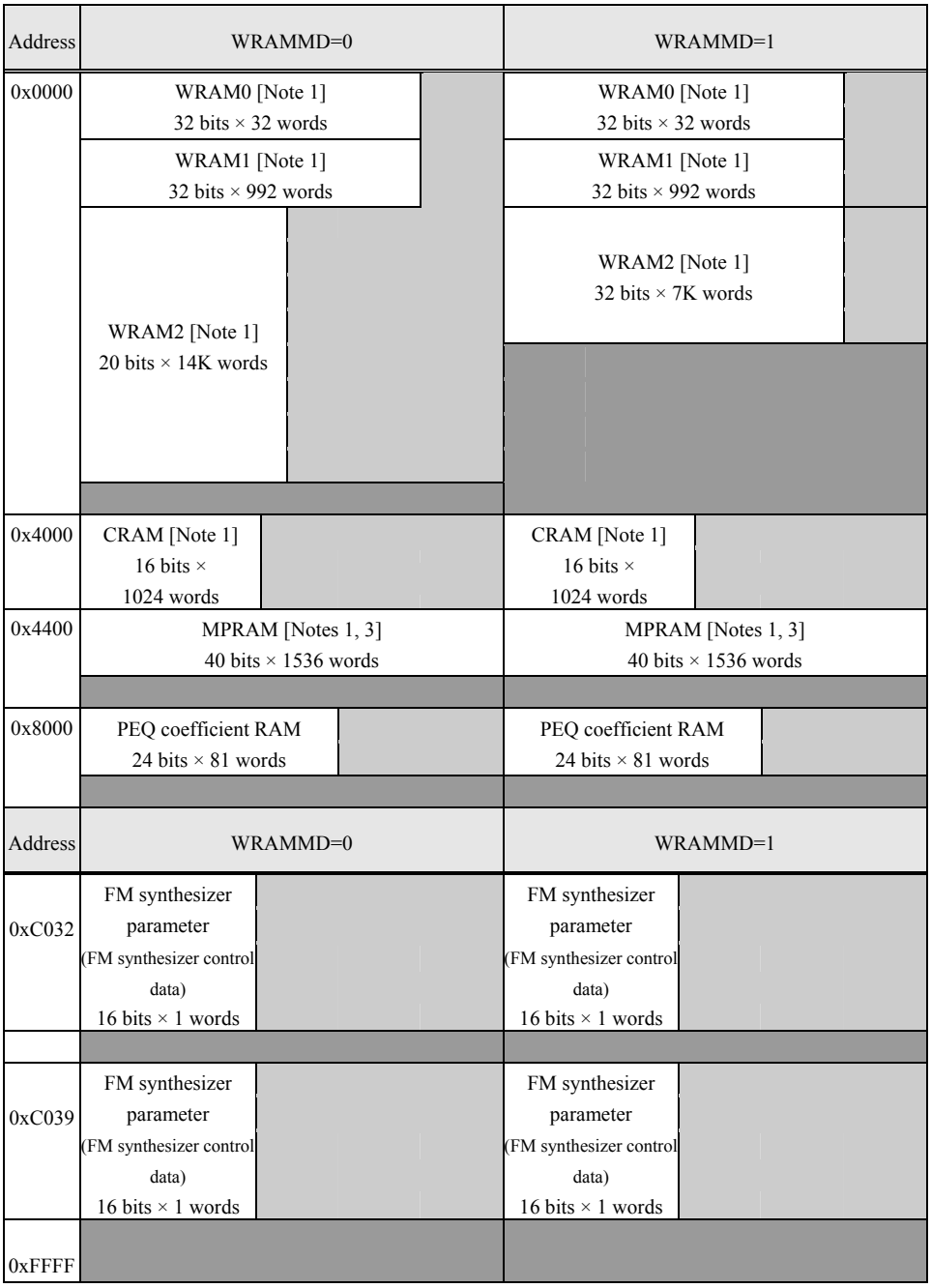
[Note 1] The W/R column shows the access privilege from the host controller.
And, "When written" and "When read" in each register description are represented from the view point of the host controller.

[Note 2] Indicates error registers or status registers, where device errors and its statuses are held until the host controller clears them.

3.1.2 On-Chip RAM Address Map

On-chip RAM is addressed in word unit, even though each region of on-chip RAM has different definition of its word size.

The figure below shows the address map:



[Note 1] WRAM0–2, CRAM, and MPRAM are on-chip RAM areas MDSP2 manages.

[Note 2] The write operation to the Reserved area is ignored. 0 will be read out if this area is read.
Successive read and write accesses to the area including this Reserved area is ignored as well.

[Note 3] Parameters cannot be read from MPRAM (0x4400–0x49FF); however, when attempting to read the data, only 0 is read.
FM synthesizer parameter (0xC032, 0xC039) cannot be read; however, when attempting to read the data, only 0 is read.

3.1.3 On-Chip ROM Access Settings

The ROM contains the data that are used to set up this device.

The data are stored there in blocks. The ROM is controlled in units of a block.

1. Initial Setting

The block 0 contains the set up data to initialize this device.

This device is initialized on IC_N transition from “L” to “H” using the configuration data in the on-chip ROM block 0. See "3.7.7.1 Powering Up, Initialization" for details of the settings.

2. Issuing On-chip ROM Access Commands

When an access command (PRESETROM0–3) is issued, this device is initialized with the configuration data in the on-chip ROM. A block number is specified with four kinds of on-chip ROM access commands as its one-byte argument (Address Table [7:0]). See "Firmware Manual" for the details of the data stored in each block.

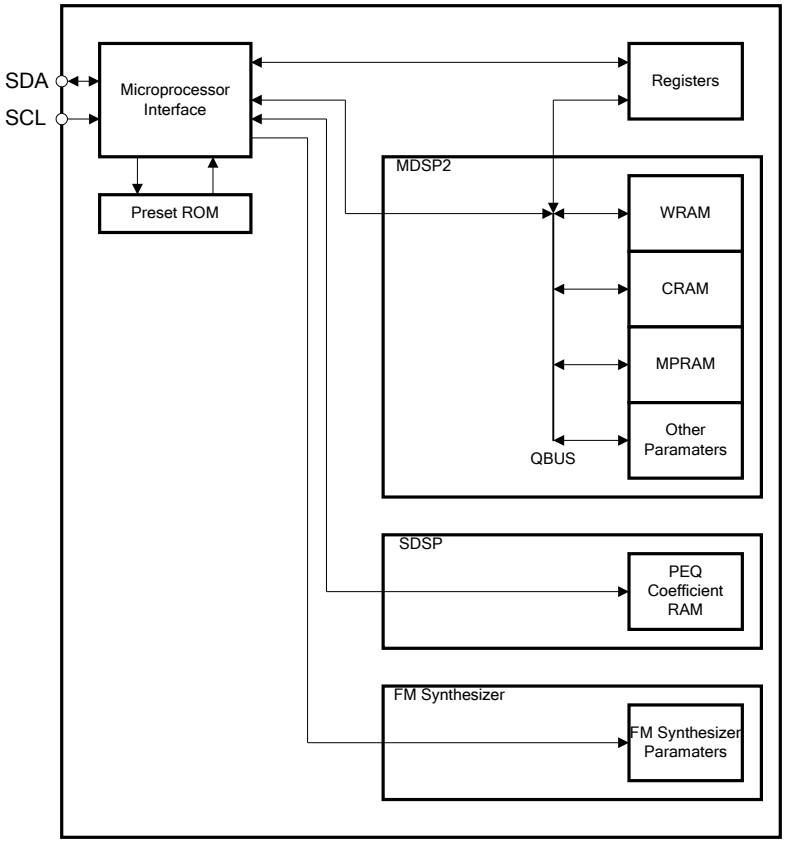
On-chip ROM Access Command	Block Number	Block Number Setting
PRESETROM0	0– 255	Address Table [7:0] +0
PRESETROM1	256– 511	Address Table [7:0] +256
PRESETROM2	512– 767	Address Table [7:0] +512
PRESETROM3	768–1023	Address Table [7:0] +768

3.2 Host Controller Interface

This device has an I^2C interface.

Connect SCL and SDA pins to the host microprocessor.

These control signals allow registers and on-chip memories to be accessed.



3.2.1 I^2C Interface

I^2C is a serial interface standard defined by Philips.

See "The I^2C-BUS SPECIFICATION" (Philips) for details of the I^2C bus.

This device supports both standard and fast modes but not high-speed mode (Hs mode).

A master device controlling this device is assumed to exist on the I^2C system bus and this device serves as its slave device.

The slave address assigned to this device is "0x6C".

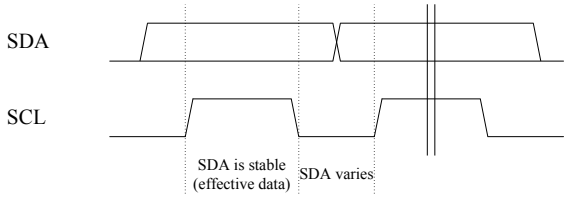
A6	A5	A4	A3	A2	A1	A0
1	1	0	1	1	0	0

[Note] YDA174/YDA156/YSS951 uses the same value for the address. And devices with the same address cannot be connected to the same I^2C bus.

3.2.2 Access Timing Chart

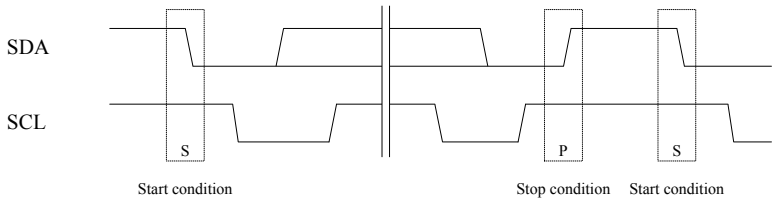
3.2.2.1 Timing Relationship between Data Bit and SCL

The data bit value on the data line (SDA) should be constant while the clock line (SCL) is "H".
The data bit value can be changed on the SDA line only when SCL line is "L".



3.2.2.2 Timing Relationship between Start condition, Stop condition, and SCL

- It is recognized as a Start condition when SDA line is changed from "H" to "L" while SCL is "H".
- It is recognized as a Stop condition when SDA line is changed from "L" to "H" while SCL is "H".
- Access is initiated with a Start condition (S) and is completed with a Stop condition (P).
  And another Start condition will initiate the access again (a repeated Start condition is not preceded a Stop condition).



3.2.2.3 Acknowledge

This device returns Acknowledge signal to the master device through SDA line every time one-byte of data transmitted is received. Likewise, the master device returns Acknowledge signal to this device every time one-byte of data is received. The timing relationship between Acknowledge and SCL is the same as that of SDA.

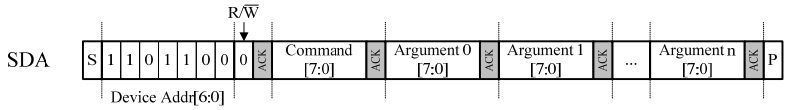
3.2.2.4 Data Tx/Rx

Data is transmitted or received in MSB first format.

3.2.2.4.1 Data Write (to this device)

After issuing a Start bit, input a device address (R/$\overline{W}$=0), command, and arguments to this device.

The figure below shows an example of transmitting a command:



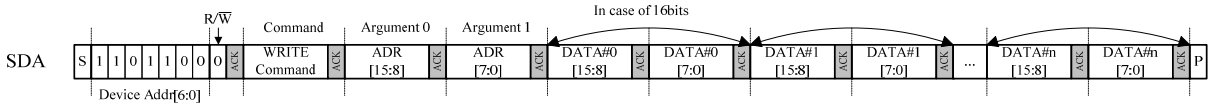
[Note 1] S: Start bit

P: Stop bit

ACK: Acknowledge

[Note 2] The gray parts indicate the outputs from this device.

The figure below shows an example of writing data into the on-chip RAM (16-bit data).

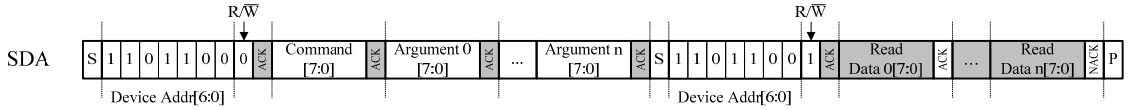


3.2.2.4.2 Data Read (from this device)

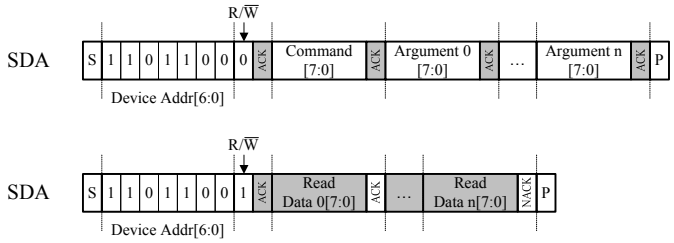
The following steps 2 and 3 are added to the step in the above Data Write.

1. After issuing a Start bit, send a device address (R/$\overline{W}$=0), command, and arguments to this device.
2. After issuing the Start bit again, send a device address (R/$\overline{W}$=1) to this device.
3. The data is output from this device.

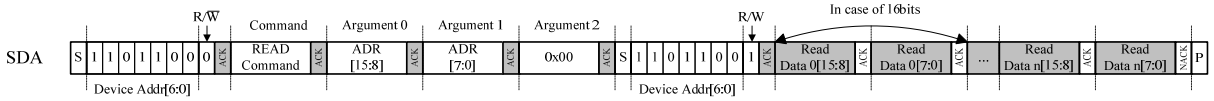
The figures below show examples of transmitting and receiving a command:



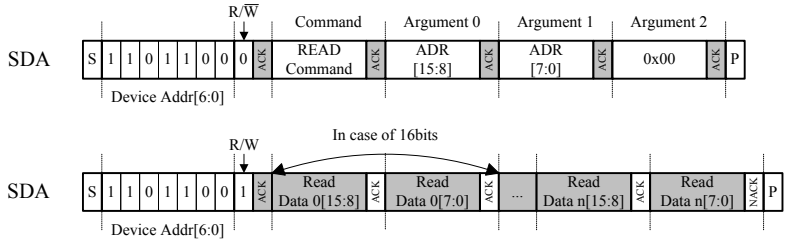
Another Start bit can be issued again following a Stop bit after sending a command and arguments to this device.



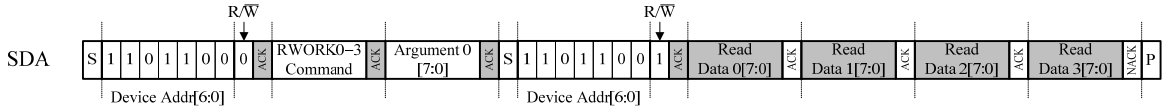
The figure below shows an example of reading data from the on-chip RAM (16-bit data).



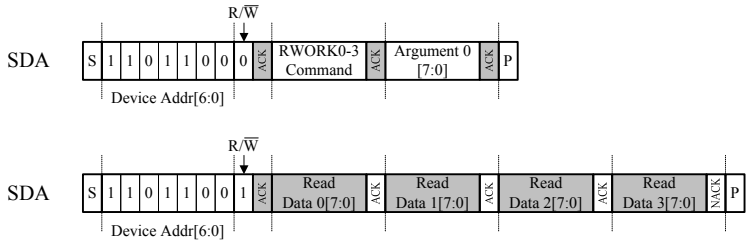
Another Start bit can be issued again following a Stop bit after sending a command and arguments to this device.



The figure below shows an example of the on-chip RAM quick read:



Another Start bit can be issued again following a Stop bit after sending a command to this device.



[Note 1] S: Start condition

P: Stop condition

ACK: Acknowledge (ACK=0)

NACK: Non-Acknowledge (ACK=1)

[Note 2] The gray parts indicate the outputs from this device.

3.2.3 Commands

The host controller accesses to the device registers and on-chip memories via commands.

After inputting an 8-bit command to this device, input one or more argument(s) in increments of 8 bits.

See "3.1.3 On-Chip ROM Access Settings" for details of the on-chip ROM.

3.2.3.1 Host Controller Commands

The table below shows commands transmitting from the host controller to this device via I^2C bus.

Its binary format is shown in the table.

If a bit-string data other than those of the listed commands is transmitted, this device returns NACK (ACK=1). And then the next command from the host controller is received.

Type	Command	7	6	5	4	3	2	1	0
Register Access	Register Access	0	0	ADDR[5:0]					
Register Quick Access	DSPSTART	0	1	0	0	0	0	0	0
	DSPSTOP	0	1	0	0	0	0	0	1
On-chip ROM Access	PRESETROM0	0	1	1	1	0	0	0	0
	PRESETROM1	0	1	1	1	0	0	0	1
	PRESETROM2	0	1	1	1	0	0	1	0
	PRESETROM3	0	1	1	1	0	0	1	1
	PRROMSTOP	0	1	0	0	0	0	1	1
On-chip RAM Access	WRITE, READ	1	0	0	0	0	0	0	0
On-chip RAM Quick Access	WWORK0–3, RWORK0–3	0	1	1	0	0	1	ADDR[1:0]	

3.2.3.1.1 Register Access

Writing Registers

Registers in this device are written.

See "3.1.1 Register Map" and each register description for details of registers.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 …	Description
Register Address	DATA[7:0]					Register Write

Reading Registers

Registers in this device are read.

See "3.1.1 Register Map" and each register description for details of registers.

See "3.2.2.4.2 Data Read (from this device)" for details of obtaining the read data.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 …	Description
Register Address						Register Read

3.2.3.1.2 Register Quick Access

Start and stop of the DSPs (MDSP2, SDSP) are set.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 …	Description
DSPSTART						SDSPSTART=0x1 and MDSPSTART=0x1
DSPSTOP						SDSPSTART=0x0 and MDSPSTART=0x0

3.2.3.1.3 On-Chip ROM Access

Command sequences stored in the on-chip ROM are executed by issuing the commands PRESETROM0–3. PRROMSTOP command can stop the execution.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 …	Description
PRESETROM0	Address Table [7:0]					Executes an on-chip ROM command string that is stored in the block number specified with the address table.
PRESETROM1	Address Table [7:0]					Executes an on-chip ROM command string stored in the block number "the address table value+256".
PRESETROM2	Address Table [7:0]					Executes an on-chip ROM command string stored in the block number "the address table value+512".
PRESETROM3	Address Table [7:0]					Executes an on-chip ROM command string stored in the block number "the address table value+768".
PRROMSTOP						Stops the PRESETROM0–3 command.

[Note 1] If the playback of FM synthesizer contents in the on-chip ROM is stopped with this PRROMSTOP command, set the ST, STEN, and FMMUTEN bits of the FM synthesizer parameters to 0x0. See "3.6.4 Playing Back FM Synthesizer Contents in On-chip ROM".

[Note 2] See "3.1.3 On-Chip ROM Access Settings" for details of setting the address table.

3.2.3.1.4 On-Chip RAM Access

Writing On-Chip RAM

Each regions of on-chip RAM has its definition of 'word' size while all the transaction on I^2C bus is carried out in bytes. Received bytes on I^2C bus are filled from the most significant byte first until the enough bytes to fill the word is received, then the constructed word are written to the on-chip RAM location.

Command	Argument 0	Argument 1	Argument 2…	Description
WRITE	ADR[15:8]	ADR[7:0]	Write Data	On-chip RAM Write

[Note 1] Continuous write up to 2048 words (of the particular region)

[Note 2] See "3.1.2 On-Chip RAM Address Map" for details of the on-chip RAM address map.

[Note 3] Do not write data into the MPRAM (addresses: 0x4400–0x49FF) during the MDSP2 operation (MDSPSTART=0x1).

[Note 4] When writing data from the host controller to WRAM0 with WRAMRTMD set to 0x1, data is written into the memory every 2 bytes, instead of 4 bytes. See "3.7.7.4 Runtime Transfer ".

[Note 5] Use the data in the following format to write to WRAM2 in 20-bit mode (WRAMMD=0x0).

- "16-bit mantissa" for the first 2 bytes
- "0" for the next byte,
- (4 bits of "0", 4-bit exponent) for the last byte

See "7.1.3 20-bit floating-point format".

Reading On-chip RAM

Each regions of on-chip RAM has its definition of 'word' size while all the transaction on I^2C bus is carried out in bytes. Words from each on-chip RAM regions are read out onto I^2C bus the most significant byte first fashion.

See "3.2.2.4.2 Data Read (from this device)" for details of obtaining the read data.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 …	Description
READ	ADR[15:8]	ADR[7:0]	0x00			On-chip RAM read

[Note 1] Continuous read up to 2048 words (of the particular region)

[Note 2] See "3.1.2 On-Chip RAM Address Map" for details of the on-chip RAM address map.

[Note 3] MPRAM (address: 0x4400 to 0x49FF) region is write only.

FM synthesizer parameter (address: 0xC032, 0xC039) region is write only.

0 will be read from MPRAM or FM synthesizer parameter regions.

[Note 4] If the host processor reads from WRAM0 with WRAMRTMD set to "0x1", only most significant 2 bytes of words in the WRAM0 will be read. See "3.7.7.4 Runtime Transfer ".

[Note 5] The same binary code is used for READ and WRITE Command but the different I^2C messages are used for each Command.

For WRITE Command, see "3.2.2.4.1 Data Write (to this device)".

For READ Command, write ($R/\overline{W}=0$) the Command and its arguments (ADR [15:8], ADR [7:0], 0x00) to the slave address of the device in the first I^2C message, then read ($R/\overline{W}=1$) from the same slave addresses in the second message. See "3.2.2.4.2 Data Read (from this device)" for the detail.

[Note 6] Reading from WRAM2 in 20-bit mode (WRAMMD=0x0) will return the following bytes in this sequence.

- "16-bit mantissa" in the first 2 bytes,
- "0" for the next byte,
- {4 bits of "0", 4-bit exponent} for the last bye.

See "7.1.3 20-bit floating-point format" for the detail.

3.2.3.1.5 On-Chip RAM Quick Accesses

On-Chip RAM Quick Write

For writing the first four words of WRAM0, dedicated write Command to each word location is available.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4...	Description
WWORK0	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]		WRAM0[0] (Address 0x0000) write
WWORK1	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]		WRAM0[1] (Address 0x0001) write
WWORK2	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]		WRAM0[2] (Address 0x0002) write
WWORK3	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]		WRAM0[3] (Address 0x0003) write

[Note 1] WRAM0 is located within on-chip RAM. For the on-chip RAM address map, see "3.1.2On-Chip RAM Address Map".

[Note 2] With WRAMRTMD set to "0x1", WWORK0−3 will take two bytes arguments instead of four. See "3.7.7.4 Runtime Transfer " for the detail.

[Note 3] The same binary code is used for the Commands of RWORK0–3 and WWORK0–3 but the different I^2C messages are used for write and read accesses.

For the WWORK0–3 write operations, see "3.2.2.4.1 Data Write (to this device)".

On-Chip RAM Quick Read

For reading the first four words of WRAM0, dedicated read Command to each word location is available.

The section "3.2.2.4.2 Data Read (from this device)" describes the read operation details.

Command	Argument 0	Argument 1	Argument 2	Argument 3	Argument 4 ...	Description
RWORK0	0x00					WRAM0[0] Read
RWORK1	0x00					WRAM0[1] Read
RWORK2	0x00					WRAM0[2] Read
RWORK3	0x00					WRAM0[3] Read

[Note 1] WRAM0 is located within on-chip RAM. For the on-chip RAM address map, see "3.1.2 On-chip RAM Address Map".

[Note 2] With WRAMRTMD set to "0x1", RWORK0−3 will return two most significant bytes of the word instead of four. See "3.7.7.4 Runtime Transfer " for the detail.

[Note 3] The same binary code is used for the Commands of RWORK0–3 and WWORK0–3 but the different I^2C messages are used for write and read accesses.

For RWORK0−3 Commands, write (R/$\overline{W}$=0) the Command and its argument (0x00) to the slave address of the device in the first I^2C message, then read (R/$\overline{W}$=1) from the same slave address in the second message. See "3.2.2.4.2 Data Read (from this device)" for the detail.

3.2.4 ACK/NACK Handshakes

NACK (ACK=1) will be indicated to the host controller when the device fails to receive previous I^2C data. The internal state of the device will be unchanged.

3.2.4.1 NACK Indications When Not Accessing On-Chip ROM

The followings describe how the device may indicate NACK to a different phase of I^2C message when the host controller is not accessing on-chip ROM.

3.2.4.1.1 I^2C Addressing Phase

- If the host controller is not addressing this device, it will indicate NACK (ACK=1).
- If the first I^2C message specifies a write-only Command and the subsequent message comes with read access (R/$\overline{W}$=1), this device will indicate NACK (ACK=1). Write-only Commands are DSPSTART, DSPSTOP, PRESETROM0−3, and PRROMSTOP.

3.2.4.1.2 Command Byte Phase

- This device indicates NACK (ACK=1) when undefined Command is received.

3.2.4.2 NACK Indications When Accessing On-Chip ROM

The followings describe how the device may indicate NACK to a different phase of I^2C message when the host controller is accessing on-chip ROM.

3.2.4.2.1 I^2C Addressing Phase

- If the host controller is not addressing this device, it will indicate NACK (ACK=1).
- If the first I^2C message specifies a write-only Command and the subsequent message comes with read access (R/$\overline{W}$=1), this device will indicate NACK (ACK=1). Write-only Commands are DSPSTART, DSPSTOP, PRESETROM0−3, and PRROMSTOP.
- Other than these two cases, this device may indicate NACK (ACK=1) when internal on-chip ROM access is ongoing.

[Note] While on-chip ROM access is processed within the device, it can fail to respond to the host controller and indicate NACK (ACK=1).
In such case, resend the same Command after sending I^2C stop bit, until it is successfully acknowledged.

3.2.4.2.2 Command Byte Phase

- This device responds with NACK (ACK=1) when undefined command is received.
- This device responds with NACK (ACK=1) when another PRESETROM0−3 Command is received if it already is processing a PRESETROM0−3 Command.
- Other than these two cases, this device may indicate NACK (ACK=1) when internal on-chip ROM access is ongoing.

[Note] While on-chip ROM access is processed within the device, it can fail to respond to the host controller and indicate NACK (ACK=1).
In such case, resend the same command after sending I^2C stop bit, until it is successfully acknowledged.

3.2.4.2.3 Address Byte Phase

- This device responds with NACK (ACK=1) for write operations of FM Synthesizer parameters at 0xC032 and 0xC039.

3.3 Audio Interface

3.3.1 Audio Interface Pin Configurations

GPIO pins can be configured as audio interface with AIFMD [3:0] and PIO registers.

PIO register is 0x1 on device reset.

- The pins in the table below designated as Input or Output will be used as audio interface.
  The combination of AIFMD [3:0] and PIO registers will configure each interface pins as input or output.
  If a pin is configured as an input and unused in your design, connect it to either IOVDD or the ground.
  If a pin is configured as an output and unused in your design, leave it unconnected.

- The pins in the table below designated as IO will be used as GPIO pins.
  POEN [11:3] register will configure each GPIO pin (GPIO11–3) as either input or output.
  For the detail of GPIO pins configuration, see "3.3.8.1GPIO Port Data Direction Registers".
  The bit in POEN register for an unused GPIO pin should be set to 0x0 (reset value) and connect the pin to either IOVDD or the ground.

PIO = 0x0

AIFMD[3:0]	0x0		0x1		0x2		0x3	
Mode Name	2ch SDI + 4ch SDI		2ch SDI on SDI0		2ch SDI on SDI1		2ch SDI on SDI2	
	Signal Name	Direction	Signal Name	Direction	Signal Name	Direction	Signal Name	Direction
GPIO0	WCK input	Input	WCK Input 0	Input	WCK Input 0	Input	WCK Input 0	Input
GPIO1	BCK input	Input	BCK Input 0	Input	BCK Input 0	Input	BCK Input 0	Input
GPIO2	SDI0	Input	SDI0	Input	SDI0	Input	SDI0	Input
GPIO3	SDI1	Input	WCKInput1	Input	WCK Input 1	Input	WCK Input 1	Input
GPIO4	SDI2	Input	BCK Input 1	Input	BCK Input 1	Input	BCK Input 1	Input
GPIO5	GPIO5	IO	SDI1	Input	SDI1	Input	SDI1	Input
GPIO6	GPIO6	IO	WCK Input 2	Input	WCK Input 2	Input	WCK Input 2	Input
GPIO7	MCK output	Output	BCK Input 2	Input	BCK Input 2	Input	BCK Input 2	Input
GPIO8	SDO1	Output	SDI2	Input	SDI2	Input	SDI2	Input
GPIO9	SDO0	Output	SDO0	Output	SDO0	Output	SDO0	Output
GPIO10	WCK output	Output	WCK output	Output	WCK output	Output	WCK output	Output
GPIO11	BCK output	Output	BCK output	Output	BCK output	Output	BCK output	Output
			[Note 1]		[Note 2]		[Note 3]	

[Note 1] GPIO2–0 (SDI0) inputs will be routed to SRC.

[Note 2] GPIO5–3 (SDI1) inputs will be routed to SRC.

[Note 3] GPIO8–6 (SDI2) inputs will be routed to SRC.

PIO = 0x1

AIFMD[3:0]	0x0		0x1		0x2		0x3	
Mode Name	2ch SDI + 4ch SDI		2ch SDI on SDI0		2ch SDI on SDI1		2ch SDI on SDI2	
	Signal Name	Direction	Signal Name	Direction	Signal Name	Direction	Signal Name	Direction
GPIO0	WCK Input	Input	WCK Input 0	Input	WCK Input 0	Input	WCK Input 0	Input
GPIO1	BCK Input	Input	BCK Input 0	Input	BCK Input 0	Input	BCK Input 0	Input
GPIO2	SDI0	Input	SDI0	Input	SDI0	Input	SDI0	Input
GPIO3	GPIO3	IO	WCK Input1	Input	WCK Input 1	Input	WCK Input1	Input
GPIO4	GPIO4	IO	BCK Input1	Input	BCK Input 1	Input	BCK Input1	Input
GPIO5	GPIO5	IO	SDI1	Input	SDI1	Input	SDI1	Input
GPIO6	GPIO6	IO	WCK Input2	Input	WCK Input2	Input	WCK Input 2	Input
GPIO7	GPIO7	IO	BCK Input2	Input	BCK Input2	Input	BCK Input 2	Input
GPIO8	GPIO8	IO	SDI2	Input	SDI2	Input	SDI2	Input
GPIO9	GPIO9	IO	GPIO9	IO	GPIO9	IO	GPIO9	IO
GPIO10	GPIO10	IO	GPIO10	IO	GPIO10	IO	GPIO10	IO
GPIO11	GPIO11	IO	GPIO11	IO	GPIO11	IO	GPIO11	IO
			[Note 1]		[Note 2]		[Note 3]	

[Note 1] GPIO2-0 (SDI0) inputs will be routed to SRC.

[Note 2] GPIO5-3 (SDI1) inputs will be routed to SRC.

[Note 3] GPIO8-6 (SDI2) inputs will be routed to SRC.

	Indicates the following data and clocks. • An external clock and audio signal samples synchronized to the external clock. • Audio clock derived from an external audio clock and audio signal samples synchronized to the derived clock.
	Audio clock derived from XIN clock and audio signal samples synchronized to the derived clock.
	GPIO pins.
	Unused pins, disconnected from the internal circuits.

- GPIO11–0 inputs will be ignored when PI is logic 0. They can tolerate floating voltage levels and it will not propagate inside the device.
- On initialization of the device, set PI to logic 1 when configuring AIFMD [3:0] and PIO registers.
  For the configuration detail of these registers, see "3.7.7.1 Powering Up, Initialization"
- When configuring a GPIO pin for output, set the corresponding bit in POEN register first before setting PI to logic 1. For the detail of GPIO port configuration, see "3.3.8.1 GPIO Port Data Direction Registers".

3.3.1.1 AIF Mode Setting Register

0x07: AIFMD Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	**PI**	**PIO**	**AIFMD[3]**	**AIFMD[2]**	**AIFMD[1]**	**AIFMD[0]**

- **bit5: PI**

This register bit controls the handling of input signals to GPIO11-0 pins.

On reset, inputs will be ignored.

Set this bit to logic 1 only after configuring GPIO11-0 pins.

See "3.3.1 Audio Interface Pin " for the detail.

(Reset value)

0x0

(When written)

0x0: Ignore input signals to GPIO11-0 pins. No signal will be propagated inside the device.

0x1: Signals to GPIO11-0 pins are valid inputs.

(When read)

Current setting.

- **bit4: PIO**

Part of audio interface pins can be configured as General Purpose Input/Output by setting PIO bit to logic 1.

See "3.3.1 Audio Interface Pin for the detail.

(Reset value)

0x1

(When written)

0x0: Non-PIO mode

0x1: PIO mode. Part of audio interface is configured as GPIO.

(When read)

Current setting.

- **bit3-0: AIFMD[3:0]**

This register bit sets the audio interface configuration.

(Reset value)

0x0

(When written)

0x0: 2ch SDI + 4ch SDI.

0x1: 2ch SDI using SD0 input.

0x2: 2ch SDI using SDI1 input.

0x3: 2ch SDI using SDI2 input.

Values other than the above are reserved and must not be used.

(When read)

Current setting.

[Note]

When updating this register, note the followings:

See "3.7.7.1 Powering Up, Initialization" for setting this register during initialization.

The following register bits should be set to logic 0 to update this register during normal operation:

SDSPMUTEN, MDSPMUTEN.

Additionally, the following register bits should be also set to logic 0 to update this register at the same time as DCM register: SDSPSTART, MDSPSTART.

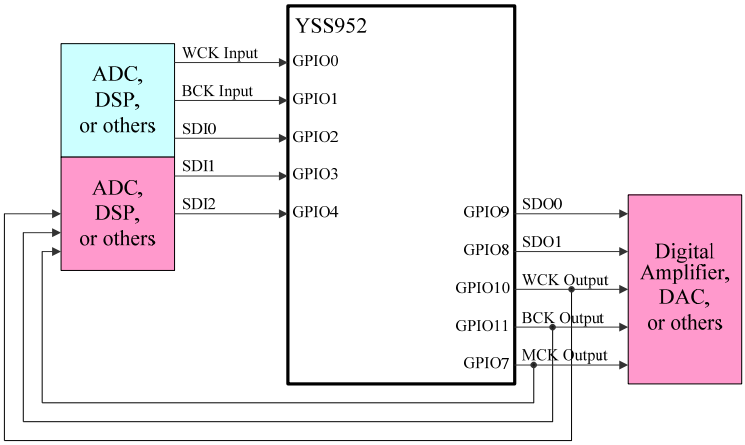
See "3.5.5.3 SDSP Mode Register" for changing the DCM register.

3.3.2 Device Connection Examples

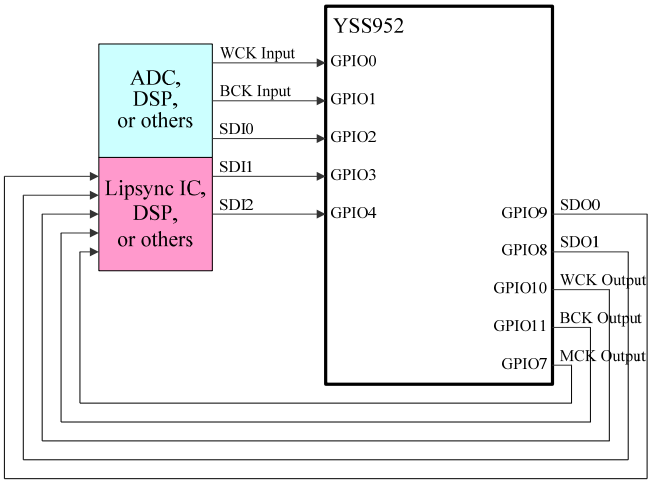
3.3.2.1 AIFMD [3:0]: 0x0 Interface Configuration

The blue device is the master of the audio connection to YSS952, and YSS952 is the master of the audio connections to the red devices in the diagram below. The SDI0 inputs are converted by SRC to its output sampling rate and processed by YSS952 at that rate.

When some of the red devices are not used in your design, those interface pins can be used as GPIO.



Another application with an external processor such as lipsync IC, DSP is illustrated below.

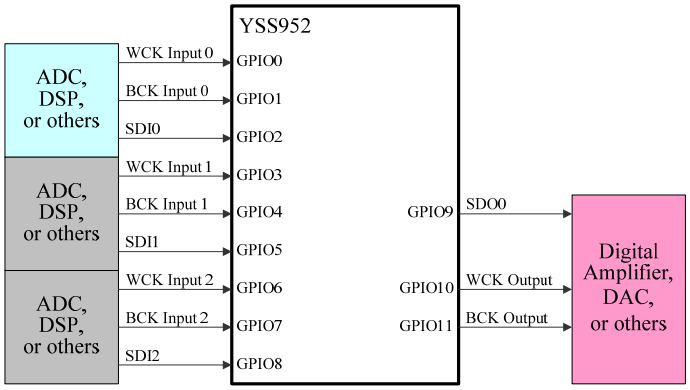


3.3.2.2 AIFMD [3:0]: 0x1, 0x2, 0x3 Interface Configuration

Front-end device (blue) is the source and master of audio signal connection to YSS952, and YSS952 is the master and source of audio signal connection to back-end device (red).

One of three front-end devices is selected and converted by SRC to its output sampling rate and processed by YSS952 at that rate.

Changing AIFMD [3:0] register between 0x1, 0x2, and 0x3 is allowed while SDSP or MDSP2 is running, although with some possible noise. Muting SDSP and MDSP2 during switching is recommended as described in "3.3.1 Audio Interface Pin ".



[Note]

A loudspeaker dissipates heat in the voice coil by air flow caused by the vibration of its diaphragm. When DC signals (several Hz or less) are input, the heat dissipation become inefficient and this may lead to voice-coil burnouts, smokes, or speaker catching fire even when the signal is within the operating limits of the device. Implement one or more measures listed below to prevent such conditions:

1. Never allow DC signal output (contents data with DC offset, or a pause during playback with leftover DC offset).
   (This is additional option after following the 2, 3, or 4 below for these are generally difficult to put into practice.)
2. Filter out DC components in digital signal paths during digital signal processing.
   (Unless stated explicitly in its datasheet, a device does not implements DC rejection within the device.)
3. Filter out DC components in analog signal paths with a DC block capacitor.
   (Never leave out a DC block capacitor from your design where the device vendor specifies it.)
4. When there's an additional device between this device and the speaker, devise some DC blocking on that device.

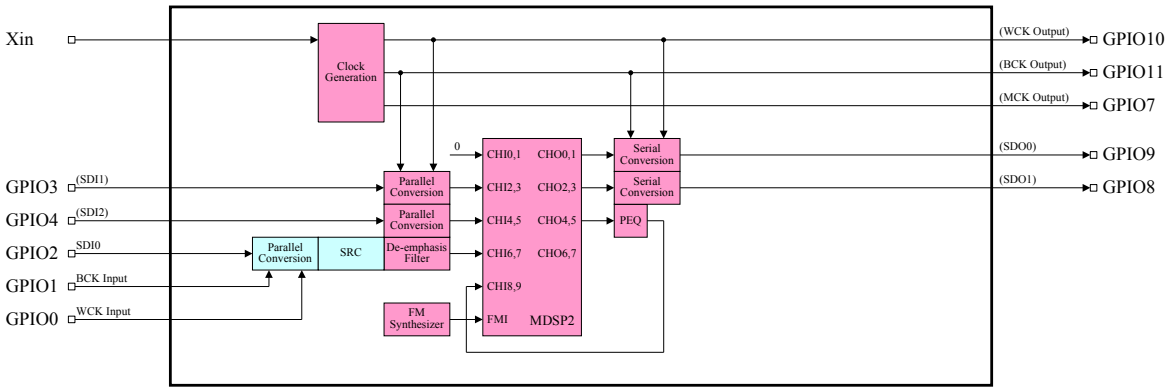
Beware also of the failures of the DC blocking components themselves, the device, DC block capacitors, and design conservatively anticipating such events.

3.3.3 Internal Clock System

3.3.3.1 AIFMD [3:0]: 0x0 Clock Configuration

- SRC will process input data with the sampling rate of WCK and BCK signals on GPIO1-0.pins
- Converted data of SRC will use the internal sampling rate derived from XIN clock.

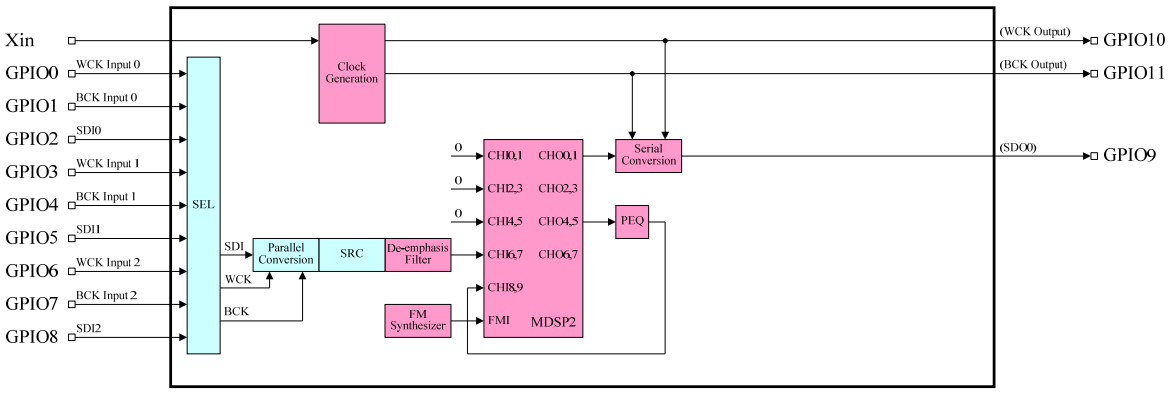
[Note] Pins with signal names in parentheses in the figure below function as GPIO pin when PIO is logic 1.



3.3.3.2 AIFMD [3:0]: 0x1, 0x2, 0x3 Clock Configuration

- SRC will process input data with the sampling rate of WCK and BCK signals on the selected channel from the three alternative inputs.
- Converted data of SRC will use the internal sampling rate derived from XIN clock.

[Note] Pins with signal names in parentheses in the figure below function as GPIO pin when PIO is logic 1.



3.3.4 Audio Signal Interface

This section summarizes the supported range of digital audio input/output sampling rates, and the clocks associated with each data inputs.

See also "5.5.2 Audio Interface" for relevant information.

Exact frequency of WCK outputs depends on the input clock frequency on XIN pin. (See 0x0E: FSM register setting for the detail)

AIFMD[3:0]	Signal	Range
0x0	WCK Input	8–192 kHz
	BCK Input	64 × WCK Input
	SDI0	Synchronized to BCK Input
	SDI2-1	Synchronized to BCK Output
	WCK Output	44.1kHz, 48kHz
	BCK Output	64 × WCK Output
	MCK Output	256 × WCK Output
	SDO1-0	Synchronized to BCK Output
0x1	WCK Input 0	8–192 kHz
	BCK Input 0	64×WCK Input 0
	SDI0	Synchronized to BCK Input 0
	WCK Output	44.1kHz, 48kHz
	BCK Output	64 × WCK Output
	SDO0	Synchronized to BCK Output
0x2	WCK Input 1	8–192 kHz
	BCK Input 1	64 × WCK Input 1
	SDI1	Synchronized to BCK Input 1
	WCK Output	44.1kHz, 48kHz
	BCK Output	64 × WCK Output
	SDO0	Synchronized to BCK Output
0x3	WCK Input 2	8–192 kHz
	BCK Input 2	64 × WCK Input 2
	SDI2	Synchronized to BCK Input 2
	WCK Output	44.1kHz, 48kHz
	BCK Output	64 × WCK Output
	SDO0	Synchronized to BCK Output

Indicates the following data and clocks.
- An external clock and audio signal samples synchronized to the external clock.
- Audio clock derived from an external audio clock and audio signal samples synchronized to the derived clock.

Audio clocks derived from XIN clock and audio signal samples synchronized the derived clock.

3.3.5 Digital Audio Interface Input Signal Format

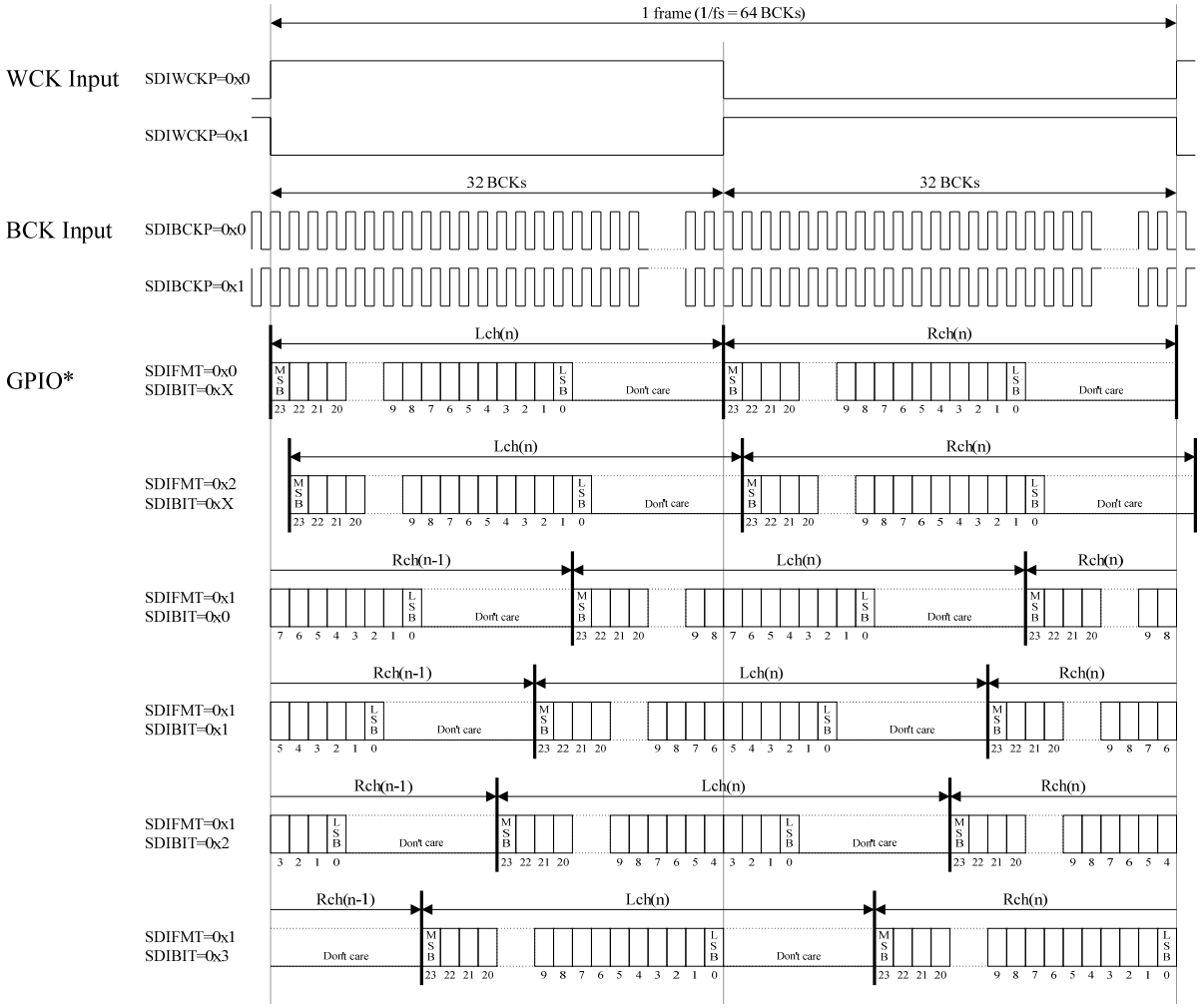
3.3.5.1 Input Signal Timings

This figure below shows the audio clock and audio data input timings.

2ch × 24 bits of data can be input from one interface using these GPIO pins.

(n): Input audio samples in the current frame,

(n-1): Input audio samples in the previous frame



[Note] This device always expects 24 bits of data regardless of the SDIBIT setting (16/18/20/24 bits).

For 16, 18, or 20 bit data, fill '0' in the least significant bits.

3.3.5.2 AIF Input Format Setting Register

0x08: AIFIFMT Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	**SDIFMT[1]**	**SDIFMT[0]**	**SDIBIT[1]**	**SDIBIT[0]**	**SDIWCKP**	**SDIBCKP**

- **bit5-4: SDIFMT[1:0]**

This register sets audio interface input data format.

(Reset value)

0x0

(When written)

0x0: Left-justified data format

0x1: Right-justified data format

0x2, 0x3: I^2S data format

(When read)

Current setting.

- **bit3-2: SDIBIT[1:0]**

This register specifies the size of audio samples in the right-justified data format.

(Reset value)

0x0

(When written)

0x0: 16 bits

0x1: 18 bits

0x2: 20 bits

0x3: 24 bits

(When read)

Current setting.

[Note]

This register setting is valid only when SDIFMT [1:0] is set to logic 1.

This device always read 24 bits of data regardless of this register setting.

- **bit1: SDIWCKP**

This register bit specifies the effective edge of word clock.

(Reset value)

0x0

(When written)

0x0: A frame starts on the rising edge of the word clock.

Word clock is “H” is for Lch; “L” for Rch.

0x1: A frame starts on the falling edge of the word clock.

Word clock is “L” is for Lch; “H” for Rch.

(When read)

Current setting.

- **bit0: SDIBCKP**

This register bit specifies the effective edge of bit clock.

(Reset value)

0x0

(When written)

0x0: Input data must change on the rising edge of bit clock.

(This device latch the data bit on the falling edge.)

0x1: Input data must change on the falling edge of bit clock.

(This device latch the data bit on the rising edge.)

(When read)

Current setting.

3.3.6 Digital Audio Interface Output Signal Format

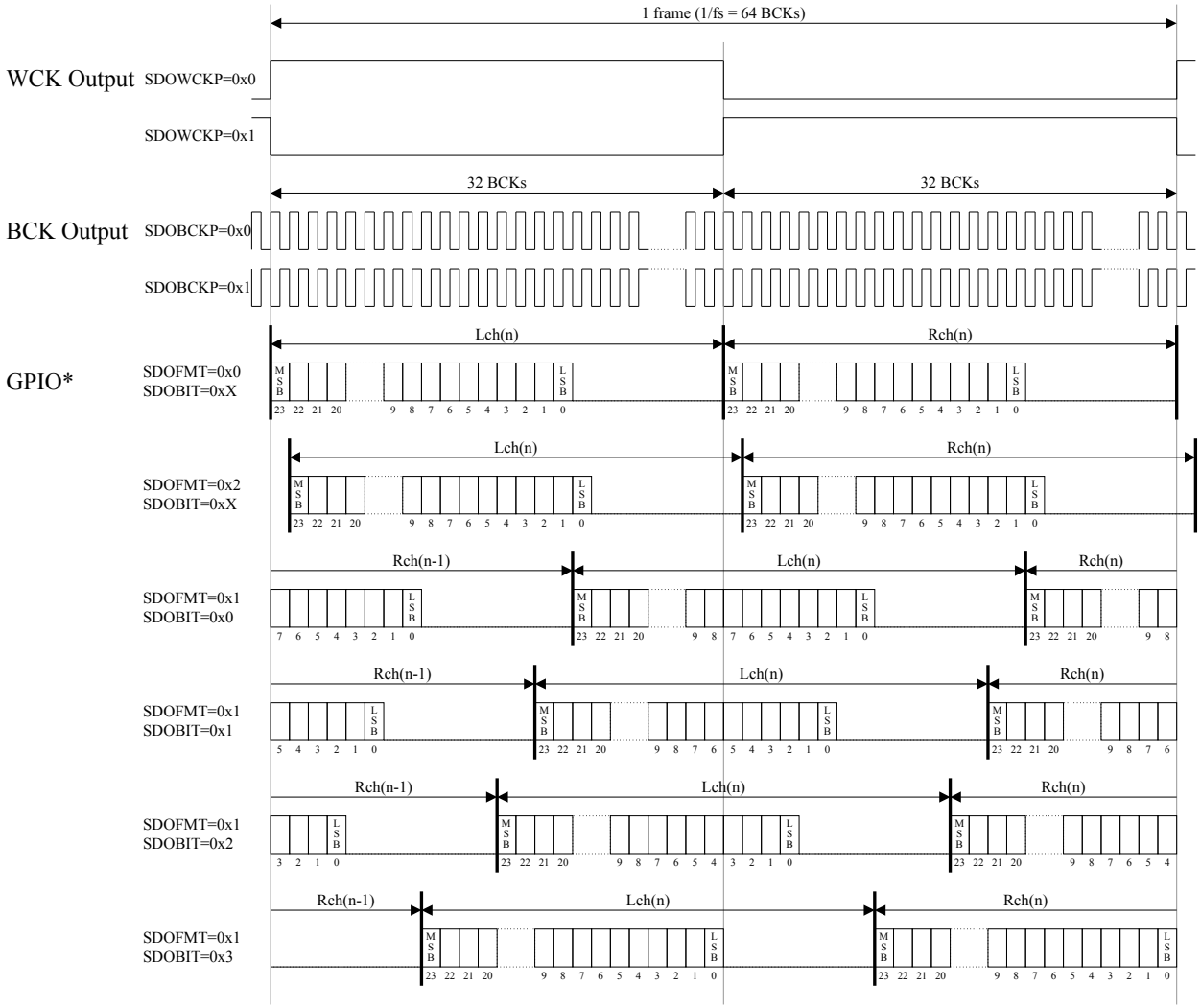
3.3.6.1 Output Signal Timings

The figure below shows the audio clock and audio data output timing.

2ch × 24 bits of data can be output from one interface using these GPIO pins.

(n): Output audio samples in the current frame,

(n-1): Output audio samples in the previous frame



3.3.6.2 AIF Output Format Setting Register

0x09: AIFOFMT Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	**SDOFMT[1]**	**SDOFMT[0]**	**SDOBIT[1]**	**SDOBIT[0]**	**SDOWCKP**	**SDOBCKP**

- **bit5-4: SDOFMT[1:0]**

This register sets audio interface output data format.

(Reset value)

0x0

(When written)

0x0: Left-justified data format

0x1: Right-justified data format

0x2, 0x3: I^2S data format

(When read)

Current setting.

- **bit3-2: SDOBIT[1:0]**

This register specifies the size of audio samples in the right-justified data format.

(Reset value)

0x0

(When written)

0x0: 16 bits

0x1: 18 bits

0x2: 20 bits

0x3: 24 bits

(When read)

Current setting.

[Note]

This register setting is valid only when SDOFMT [1:0] is set to logic 1.

This device always output 24 bits of data always output regardless of this register setting.

- **bit1: SDOWCKP**

This register bit specifies the effective edge of word-clock.

(Reset value)

0x0

(When written)

0x0: A frame starts on the rising edge of word clock.

Word clock is “H” for Lch; “L” for Rch.

0x1: A frame starts on the falling edge of word clock.

Word clock is “L” for Lch; “H” for Rch.

(When read)

Current setting.

- **bit0: SDOBCKP**

This register bit specifies the effective edge of bit clock.

(Reset value)

0x0

(When written)

0x0: Output data change on the rising edge of bit clock.

0x1: Output data change on the falling edge of bit clock.

(When read)

Current setting.

3.3.7 AIF Status

3.3.7.1 AIF Status Register

0x20: SDSPST Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SDIERR	1	1	UNLOCK	FSIERR	FSERR	0	SDSPERR

- **bit7: SDIERR**

This register bit indicates input audio clock framing errors.

(Reset value)

0x1

(When written)

0x0: Clears this error flag.

0x1: Does not clear this error flag.

(When read)

0x0: No input audio clock framing error detected.

0x1: An input audio clock framing error detected.

[Note]

When this error—WCK interval being not equal to 64 times the BCK interval—is detected, the audio input signal and the input and output of SRC are muted.

The mutings are cleared when correct input audio clock framings are detected for a period—WCK interval equal to 64 times the BCK interval for 256 times.

Writing logic 0 does not clear this register until the correct framings are detected.

The table below shows the muted path for each AIF modes.

AIFMD[3:0] register	WCK input	BCK input	SDI0	SDI1	SDI2	SRC input	SRC output
0x0	GPIO0	GPIO1	✓			✓	✓
0x1	GPIO0	GPIO1	✓	–	–	✓	✓
0x2	GPIO3	GPIO4	–	✓	–	✓	✓
0x3	GPIO6	GPIO7	–	–	✓	✓	✓

[Note] ✓ indicates the path is muted when this error detected.

– indicates the path is not part of the connection for the mode.

3.3.7.2 Zero Input Detection

0x18: ZDET Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ZDET[7]	**ZDET[6]**	**ZDET[5]**	**ZDET[4]**	**ZDET[3]**	**ZDET[2]**	**ZDET[1]**	**ZDET[0]**

Shows that the signal levels on input channel CHI0-CHI7 of MDSP2 have been small for certain duration.

When the top 17 bits of samples on a channel remains 0x0_0000 or 0x1_FFFF for 1024 sample rate periods, ZDET for the channel become 1.

MDSP2 input channel to ZDNET register mapping is listed below.

		ZDET[7]	ZDET[6]	ZDET[5]	ZDET[4]	ZDET[3]	ZDET[2]	ZDET[1]	ZDET[0]
MDSP2 Input		CHI7	CHI6	CHI5	CHI4	CHI3	CHI2	CHI1	CHI0
Audio Input	AIFMD=0x0	SDI0		SDI2		SDI1		—	—
	AIFMD=0x1	SDI0		—	—	—	—	—	—
	AIFMD=0x2	SDI1		—	—	—	—	—	—
	AIFMD=0x3	SDI2		—	—	—	—	—	—

[Note] When there's no audio source connected to a channel, ZDET[] is always 0x0.

For the connection between the audio input channels and MDSP2 input channels, see "3.3.3 Internal Clock System".

For example when AIFMD [3:0] is 0x0, ZDET [3:2] become 0x3 if the top 17 bits of SDI1 input samples remained 0x0_0000 or 0x1_FFFF for more than 1024 sample rate periods.

- **bit7-0: ZDET[7:0]**

Indicates the zero input condition detected on some of the input channel.

(Reset value)

0x0

(When written)

The write operation is ignored.

(When read)

0x0: Zero input condition is not detected on the channel.

0x1: Zero input condition is detected on the channel.

[Note]

Zero input detection will not work while the input audio clock framing error is detected.

The zero input condition detected on some of the input channels may not show in this register when SDIERR is logic 1.

3.3.8 GPIO Port Data Directions

3.3.8.1 GPIO Port Data Direction Registers

0x00: POEN0 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	**POEN[11]**	**POEN[10]**	**POEN[9]**	**POEN[8]**

0x01: POEN1 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
POEN[7]	**POEN[6]**	**POEN[5]**	**POEN[4]**	**POEN[3]**	0	0	0

- **POEN0 bit3-0 + POEN1 bit7-3: POEN[11:3]**

This registers set the port data directions of those pins configured as GPIO with AIFMD [3:0] settings.

(Reset value)

0x000

(When written)

0x0: Make GPIO [x] an input port.

0x1: Make GPIO [x] an output port

(When read)

Current setting.

3.3.8.2 GPIO Input Ports

0x02: PIDT0 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	**PIDT[11]**	**PIDT[10]**	**PIDT[9]**	**PIDT[8]**

0x03: PIDT1 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PIDT[7]	**PIDT[6]**	**PIDT[5]**	**PIDT[4]**	**PIDT[3]**	0	0	0

- **PIDT0 bit3-0 + PIDT1 bit7-3: PIDT[11:3]**

Show the logic values of the GPIO input signal.

(Reset value)

Undefined.

(When written)

Ignored.

(When read)

Show the logic value of the input signal on the GPIO pin.

3.3.8.3 GPIO Output Ports

0x04: PODT0 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	**PODT[11]**	**PODT[10]**	**PODT[9]**	**PODT[8]**

0x05: PODT1 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PODT[7]	**PODT[6]**	**PODT[5]**	**PODT[4]**	**PODT[3]**	0	0	0

- **PODT0 bit3-0 + PODT1 bit7-3: PODT[11:3]**

These registers hold output signals on GPIO pins.

(Reset value)

0x000

(When written)

0x0: Outputs 'L' on GPIO[x] pin.

0x1: Outputs 'H' on GPIO[x] pin.

(When read)

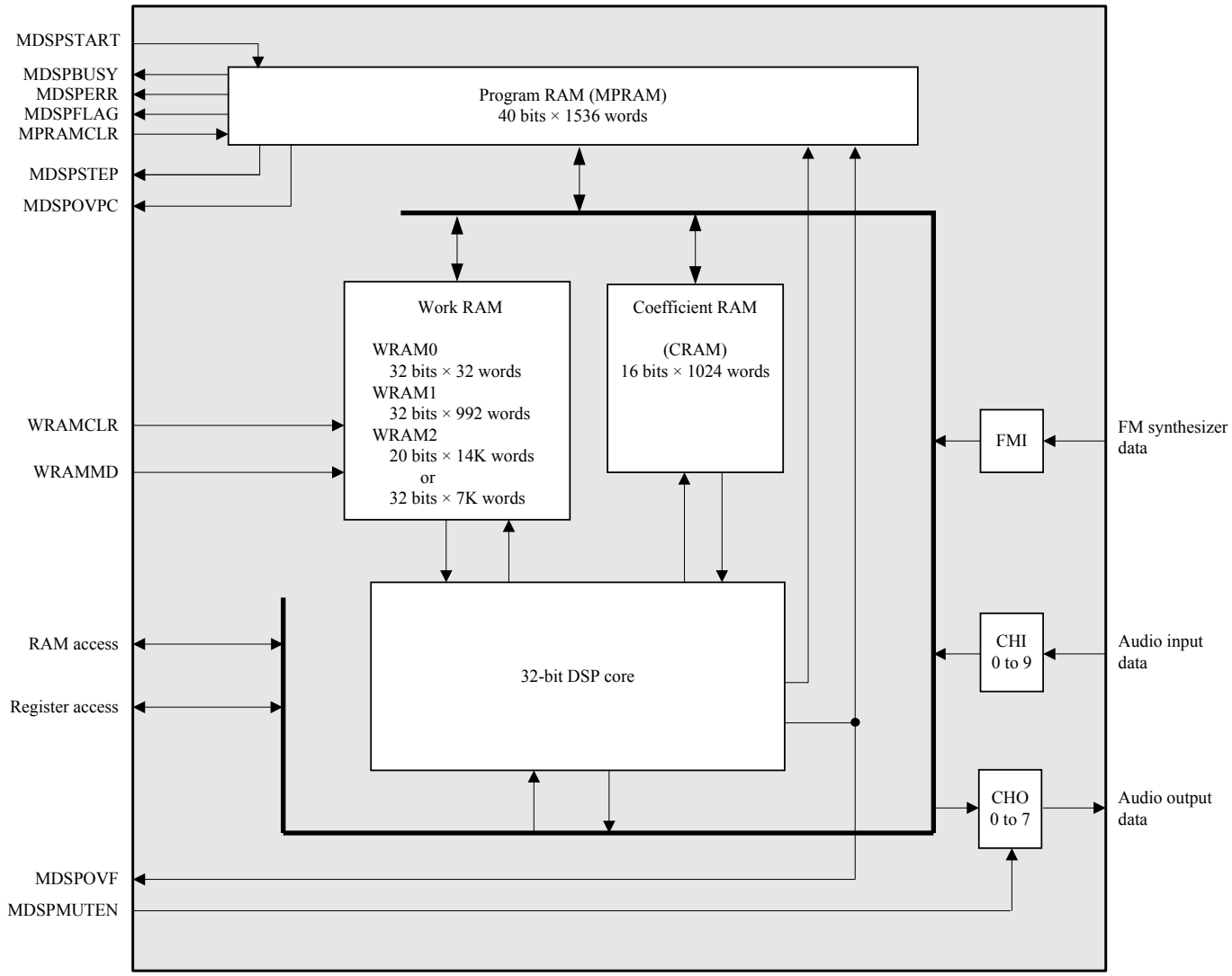
Current output.

3.4 MDSP2

MDSP2 is a DSP specialized for sound field processing. Its firmware is either loaded from on-chip ROM, or downloaded from the host controller.

See "Firmware Manual" for the detail of the on-chip ROM firmware.

The figure below shows the block diagram of the MDSP2:



3.4.1 MDSP2 Controls

3.4.1.1 DSP Start Register

0x11: DSPSTART Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	**MDSPSTART**	SDSPSTART

- **bit1: MDSPSTART**

This register bit starts or stops MDSP2 operation.

(Reset value)

0x0

(When written)

0x0: Stops MDSP2.

0x1: Starts MDSP2.

(When read)

Current setting.

[Note]

We recommend starting and stopping both DSPs—MDSP2 and SDSP—at the same time.

If the MDSPSTART bit is set to logic 1 while the proper MDSP2 firmware is not loaded in the MPRAM, the MDSPERR bit may be set to logic 1 indicating a MDSP2 processing error.

Download the proper MDSP2 firmware to the MPRAM and then set the MDSPSTART bit to logic 1.

"3.7.7.2 Pause and Restart Sequence" describes the proper steps of setting MDSPSTART 0x0 to stop MDSP2 as part of the normal operations.

3.4.1.2 On-Chip RAM Clear Register

0x0F: RAMCLR Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	**MPRAMCLR**	**WRAMCLR**	SWRAMCLR

- **bit2: MPRAMCLR**

This register bit controls zero clear operation of MPRAM contents.

(Reset value)

0x0

(When written)

0x0: Does not start MPRAM zero clear operation.

0x1: Starts MPRAM zero clear operation.

(When read)

0x0: Indicates MPRAM zero clear operation is not ongoing or the previous zero clear operation has finished.

0x1: Indicates MPRAM zero clear operation is ongoing.

[Note]

On-chip ROM firmware block 0 invokes the MPRAM zero clear operation during the device initialization.

When the zero clear operation completes, this register becomes logic 0 when read.

- **bit1: WRAMCLR**

This register bit controls WRAM zero clear operation.

(Reset value)

0x0

(When written)

0x0: Does not start WRAM zero clear operation.

0x1: Starts WRAM zero clear operation.

(When read)

0x0: Indicates WRAM zero clear operation is not ongoing or the previous zero clear operation has finished.

0x1: Indicates WRAM zero clear operation is ongoing.

[Note]

As part of the device initialization, on-chip ROM firmware block 0 invokes the WRAM zero clear operation.

WRAM can be zero cleared using this function during run time after the initialization.

In that case, set both SDSPSTART and MDSPSTART bits to logic 0.

See "3.7.7.2 Pause and Restart Sequence" for the detail.

When the zero clear operation completes, this register becomes logic 0 when read.

3.4.1.3 MDSP2 Mode Register

0x0A: MDSPMD Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	WRAMRTMD	**WRAMMD**

- **bit0: WRAMMD**

This register bit selects WRAM memory word mode.

(Reset value)

0x0

(When written)

0x0: 32 bits × 1K words + 20 bits × 14K words

0x1: 32 bits × 1K words + 32 bits × 7K words

(When read)

Current setting.

[Note]

When changing this register, set both SDSPSTART and MDSPSTART register bits to logic 0 in advance.

See "3.7.7.2 Pause and Restart Sequence" for the detail.

3.4.1.4 MDSP2 Request Register

0x13: MDSPREQ Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MDSPREQ[7]	**MDSPREQ[6]**	**MDSPREQ[5]**	**MDSPREQ[4]**	**MDSPREQ[3]**	**MDSPREQ[2]**	**MDSPREQ[1]**	**MDSPREQ[0]**

- **MDSPREQ bit7-0: MDSPREQ[7:0]**

The host processor will put processing requests to MDSP2 on this register.

(Reset value)

0x00

(When written)

Set a processing request from the host processor to a MDSP2 firmware.

(When read)

The pending processing request from the host processor to a MDSP2 firmware.

See "3.4.3 The Host Controller Requests to MDSP2 Processing" for the detail.

[Note]

This register is used for runtime transfer.

See "3.7.7.4 Runtime Transfer " and "Firmware Manual" for the details.

0x14: MDSPDAT Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MDSPDAT[7]	**MDSPDAT[6]**	**MDSPDAT[5]**	**MDSPDAT[4]**	**MDSPDAT[3]**	**MDSPDAT[2]**	**MDSPDAT[1]**	**MDSPDAT[0]**

- **MDSPDAT bit7-0: MDSPDAT[7:0]**

The host processor will put data for a processing request to MDSP2 on this register.

(Reset value)

0x00

(When written)

Set data for a processing request from the host controller to a MDSP2 firmware.

(When read)

The last set data.

See "3.4.3 The Host Controller Requests to MDSP2 Processing" for the detail.

3.4.1.5 Host Processor Request Register

0x15: MIREQ Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MIREQ[7]	**MIREQ[6]**	**MIREQ[5]**	**MIREQ[4]**	**MIREQ[3]**	**MIREQ[2]**	**MIREQ[1]**	**MIREQ[0]**

- **MIREQ bit7-0: MIREQ[7:0]**

MDSP2 firmware will put requests to the host controller on this register.

(Reset value)

0x00

(When written)

Set a request to the host controller from MDSP2.

(When read)

Pending request to the host controller from MDSP2.

See "3.4.4 MDSP2 Request to the Host Controller" for the detail.

[Note]

MIREQ [7] will indicate system errors when HANGUPR register is 1.

See "3.7.6.2 System Error Handling Setting Register" for the detail.

0x16: MIDAT Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MIDAT[7]	**MIDAT[6]**	**MIDAT[5]**	**MIDAT[4]**	**MIDAT[3]**	**MIDAT[2]**	**MIDAT[1]**	**MIDAT[0]**

- **MIDAT bit7-0: MIDAT[7:0]**

MDSP2 will put data for a request to the host controller on this register.

(Reset value)

0x00

(When written)

Writes to this register from the host controller is possible, although this operation is normally not used.

(When read)

The last data MDSP2 put for a request to the host controller.

See "3.4.4 MDSP2 Request to the Host Controller" for the detail.

3.4.2 MDSP2 Status

3.4.2.1 MDSP2 Status Register

0x1B: MDSPST Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	**MDSPERR**

- **bit0: MDSPERR**

This register bit indicates an MDSP2 processing error has occurred.

(Reset value)

0x0

(When written)

0x0: Clears this error indication.

0x1: Does not clear this error indication.

(When read)

0x0: MDSP2 processing error has not occurred.

0x1: MDSP2 processing error has occurred.

[Note]

MDSP2 will indicate this error when it encounters start instructions or stop instructions two times or more in a row. While this condition persists, writing 0 into this register will not clear the indication.

3.4.2.2 Maximum Steps Counter

0x1E: STEP0 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
STEP[15]	**STEP[14]**	**STEP[13]**	**STEP[12]**	**STEP[11]**	**STEP[10]**	**STEP[9]**	**STEP[8]**

0x1F: STEP1 Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
STEP[7]	**STEP[6]**	**STEP[5]**	**STEP[4]**	**STEP[3]**	**STEP[2]**	**STEP[1]**	**STEP[0]**

- **STEP0 bit7-0 + STEP1 bit7-0: STEP[15:0]**

This register holds the maximum number of instructions executed in the MDSP2 firmware for a cycle.

(Reset value)

0x0000

(When written)

The write value is ignored.

(When read)

The maximum number of instructions executed for a cycle.

[Note]

This register shows the maximum number of instructions executed for one sample cycle.

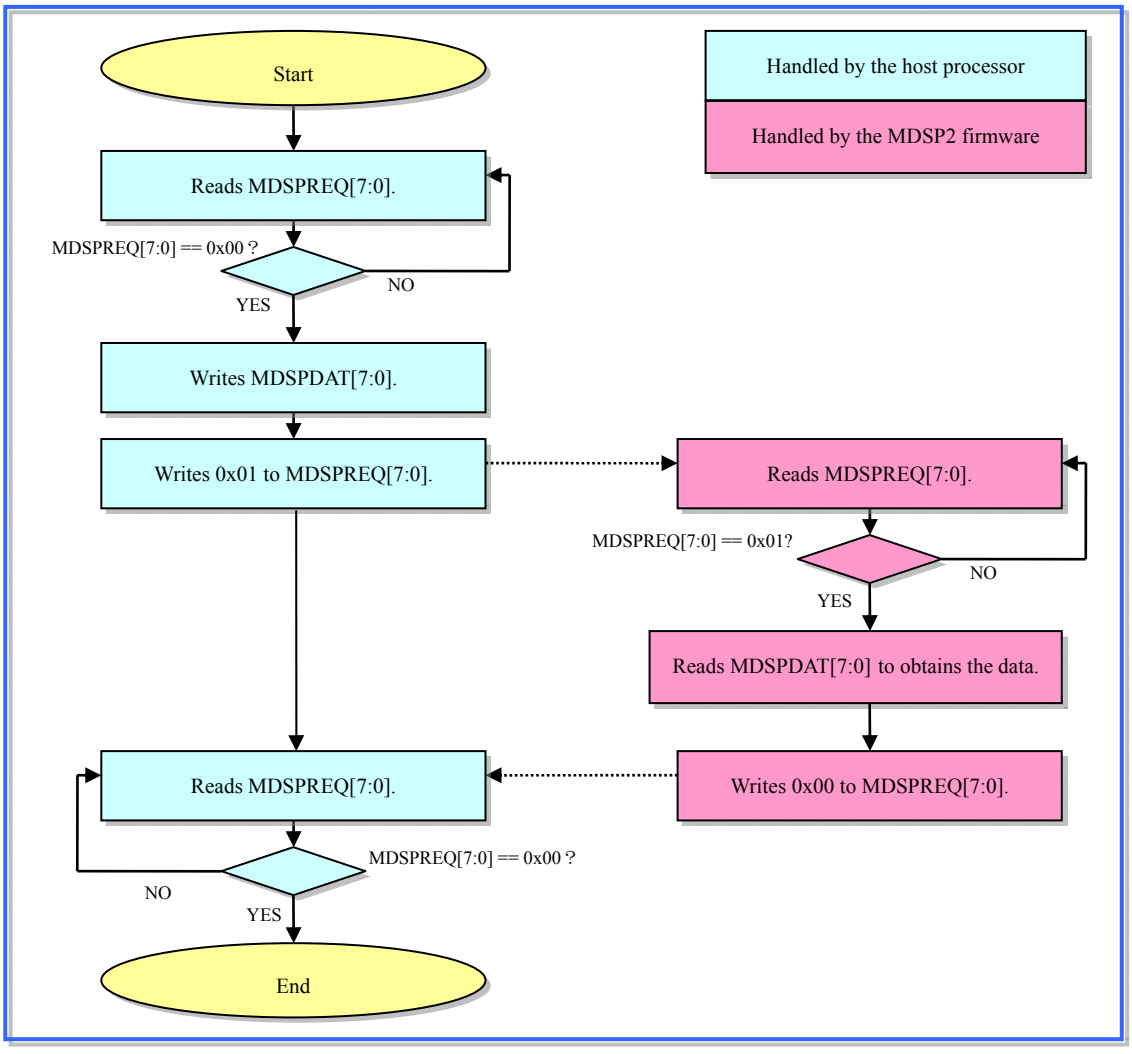
Reading the STEP1 register will reset STEP [15:0] to 0s.

3.4.3 The Host Controller Requests to MDSP2 Processing

The host controller uses MDSPREF [7:0] and MDSPDAT [7:0] to send requests to MDSP2 processing programs. MDSPREQ [7:0] is 0x00 when there's no request pending.

The host controller program and a MDSP2 program can assign and use values in 0x01 through 0xFF in MDSPREQ [7:0] for their agreed upon requests. MDSPDAT [7:0] is used for transferring data of those requests.

In the following example, how a request—MDSPREQ [7:0]=0x01, defined and used to transfer data in MDSPDAT [7:0] written by the host controller to a MDSP2 firmware—is handled by a handshaking protocol is illustrated.



[Note 1] When values of 0x01 through 0xFF in MDSPREQ [7:0] are assigned and used for the host controller–MDSP2 command request, each request requires a dispatching code segment in MDSP2 firmware.

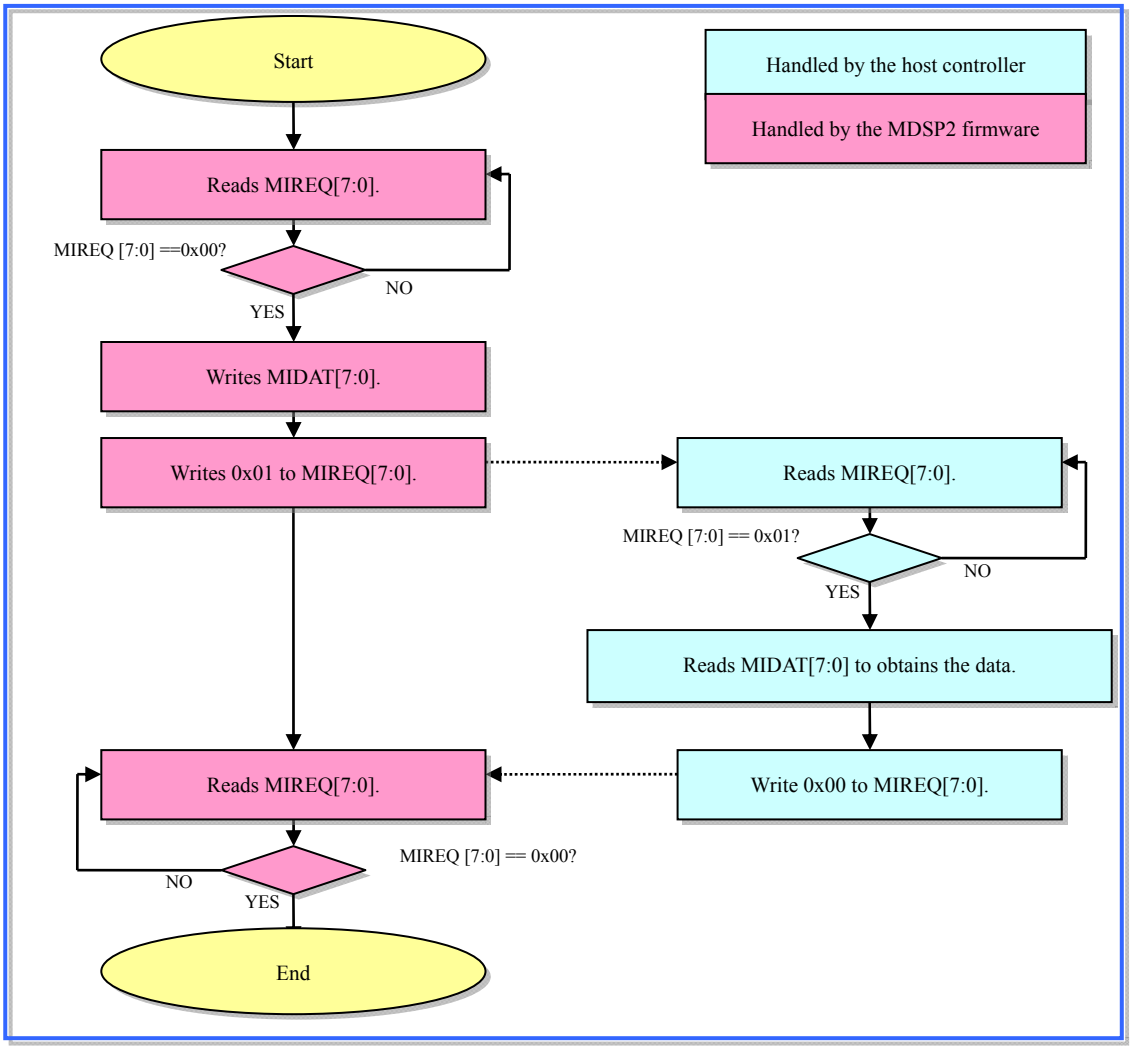
[Note 2] While waiting for MDSPREQ [7:0]==0x00 indication from MDSP2, the host controller can attend other tasks than the polling.

3.4.4 MDSP2 Request to the Host Controller

MDSP2 firmware uses MIREQ [7:0] and MIDAT [7:0] to send requests to the host controller. MIREQ [7:0] is 0x00 when there's no request pending.

The host controller program and a MDSP2 program can assign and use values in 0x01 through 0xFF in MIREQ [7:0] for their agreed upon requests. MIDAT [7:0] is used for transferring data of those requests.

In the following example, how a request—MIREQ=0x01, defined and used to transfer data in MIDAT [7:0] written by MDSP2 to the host controller—is handled by a handshaking protocol is illustrated.



[Note 1] When values from 0x01 through 0xFF in MIREQ [7:0] are assigned and used for the MDSP2–host controller command request, each request requires a dispatching code segment in the host controller program.

[Note 2] While waiting for MIREQ [7:0] == 0x00 indication from MDSP2, MDSP2 can attend other tasks than the polling.

3.5 SDSP

SDSP is a special purpose fixed-point DSP with following functions.

- Sampling Rate Converter (SRC)
- 10-band Parametric Equalizer (PEQ)
- De-Emphasis Filter

SDSP is not programmable and optimized to the functions above.

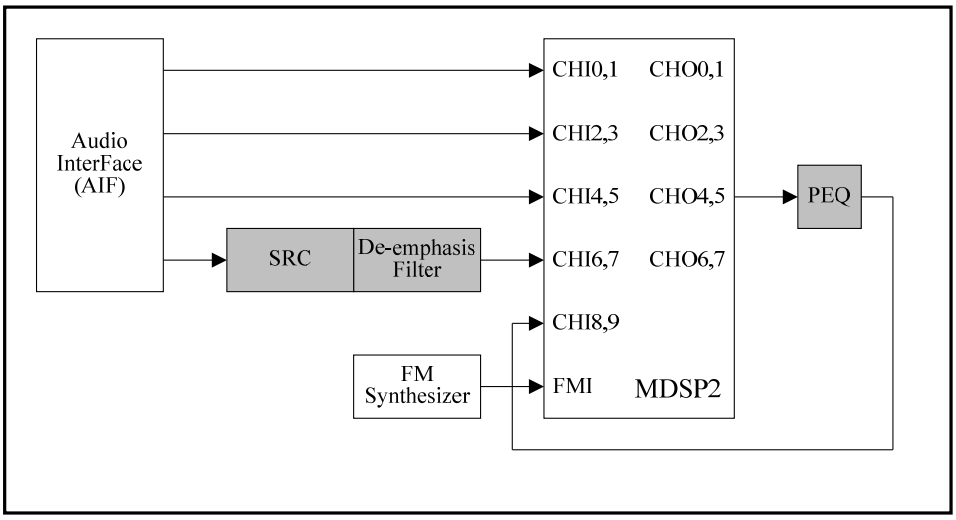
SDSP and MDSP2 signal processing modules are connected in the fixed-point format.

3.5.1 Connections

3.5.1.1 Connection When AIFMD[3:0] is 0x0–0x3

- Audio samples on GPIO pins are routed to CHI0–5 of MDSP2.
- One set of audio samples on GPIO pins goes through SRC and De-Emphasis Filter, then to CHI6–7 of MDSP2.
- FM Synthesizer output goes to FMI of MDSP2.
- CHO4–5 outputs of MDSP2 go through PEQ, then to CHI8–9 of MDSP2.

The following diagram shows connections between SDP modules (hatched blocks) and other blocks on the device.



3.5.2 SRC

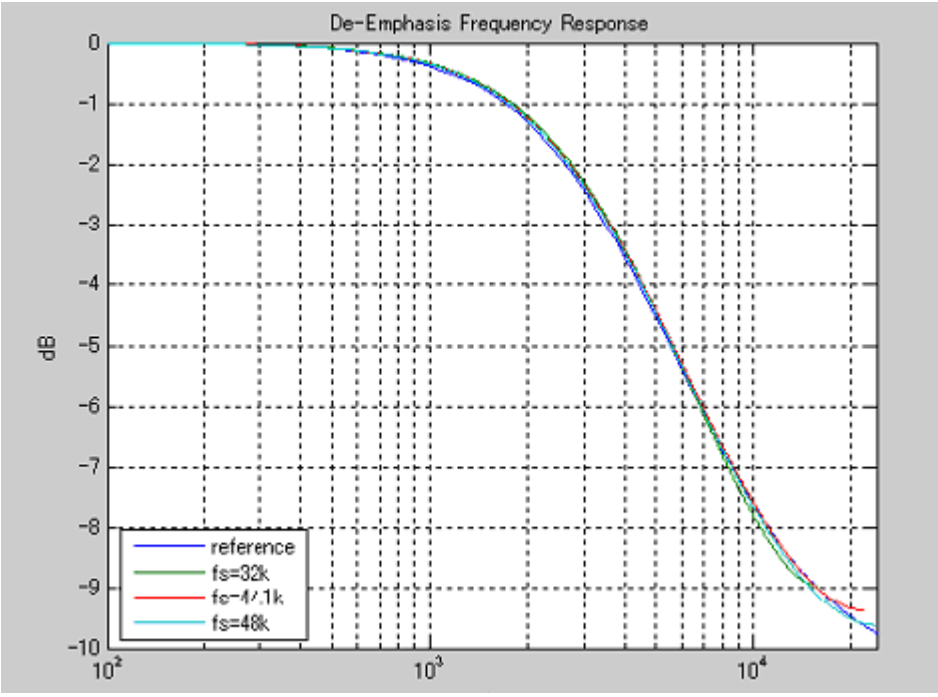
3.5.2.1 SRC Performance Figures

SRC carries out sampling rate conversions between asynchronous input/output samples, with principal performance figures as follows:

- Number of channels — 2 channels
- THD + N (with 1kHz signal) — −108 dB
- S/N ratio — 114 dB
- SRC lock time
  - Input rate transitions between 32 kHz and 48 kHz. — 120 ms (Typ.)
  - Input rate transitions from 48 kHz to192 kHz. — 220 ms (Typ.)
  - Input rate transitions from DC to 48 kHz. — 120 ms (Typ.)
- Latency (Interpolation) — 23 × Input sampling rate
  (Decimation) — 8 × Output sampling rate
- Input sampling rates — 8 kHz to 192 kHz (switched with a register setting)
- Output sampling rates — 44.1 kHz, 48 kHz (accuracy dependent on XIN input)
- Gain — −0.28dB (Interpolation mode)
  −0.33dB (Decimation mode)

3.5.3 De-Emphasis Filter

The figure below shows the frequency response of De-Emphasis Filter.



3.5.4 PEQ

The 10-band parametric equalizer is designed for frequency response correction of a loudspeaker and its enclosure.

The data sizes of PEQ coefficients and sample words are listed below.

Band	Coefficient size	Sample size
0–5	Signed 24 bit	Signed 47 bit
6–9	Signed 47 bit	Signed 47 bit

[Note 1] For the signal send out from MDSP2 to PEQ, give sufficient headroom to prevent saturation.

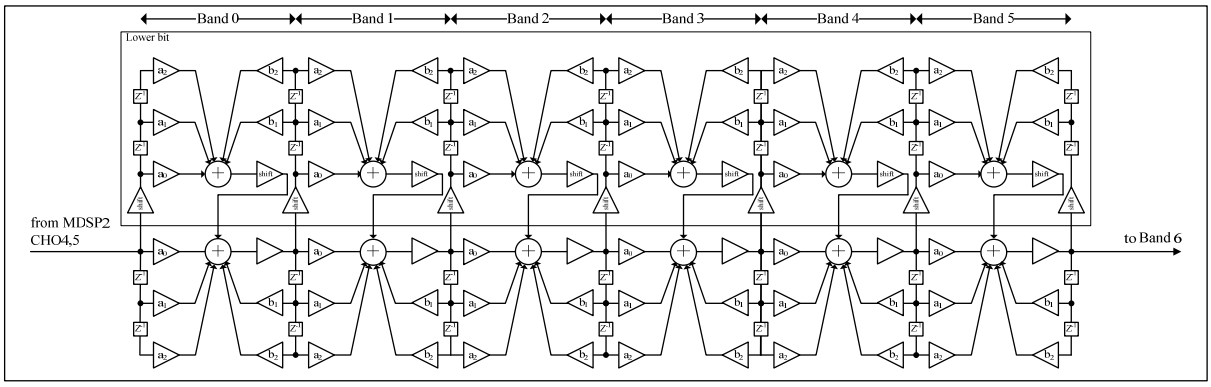
[Note 2] Use band 6–9 for low frequencies as their longer coefficient length provides more accuracy.

3.5.4.1 PEQ Signal Flow

3.5.4.1.1 Bands 0–5

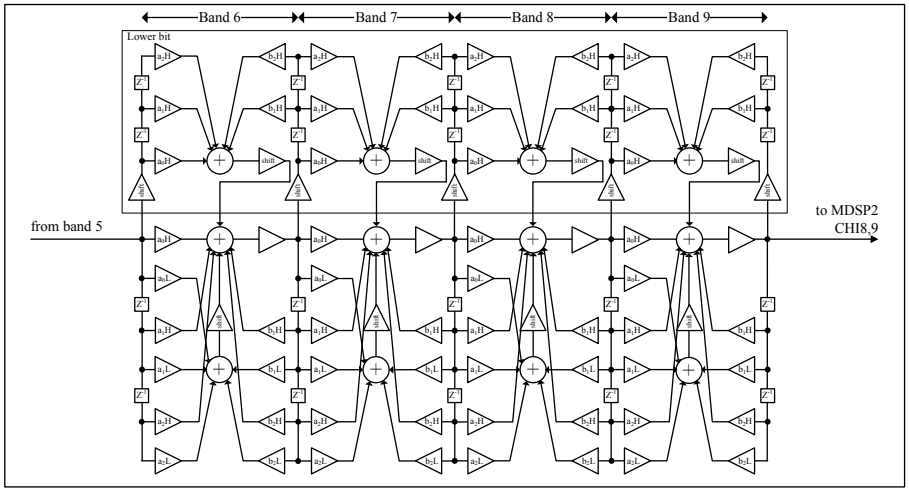
Band0−5 use signed coefficients with 24-bit accuracy, and signed word with 47-bit resolution.

The center frequencies should be 400 Hz or more.



3.5.4.1.2 Bands 6–9

Band6−9 use signed coefficients with 47-bit accuracy, and signed word with 47-bit resolution.



3.5.4.2 Specifying PEQ Coefficients

3.5.4.2.1 Address Map of PEQ Coefficients RAM

PEQ Band0−5 use 24-bit signed coefficients, and PEQ Band6−9 use 47-bit signed coefficients.

Address map in PEQ coefficients RAM of these coefficients are shown below.

Address	Data [23:0]	Region Name
0x8000	PEQ Band 0 Coefficient a0[23:0]	PEQ Coefficients
0x8001	a1[23:0]	
0x8002	a2[23:0]	
0x8003	b1[23:0]	
0x8004	b2[23:0]	
0x8005	PEQ Band 1 Coefficient a0[23:0]	
0x8006	a1[23:0]	
0x8007	a2[23:0]	
0x8008	b1[23:0]	
0x8009	b2[23:0]	
0x800A	PEQ Band 2 Coefficient a0[23:0]	
0x800B	a1[23:0]	
0x800C	a2[23:0]	
0x800D	b1[23:0]	
0x800E	b2[23:0]	
0x800F	PEQ Band 3 Coefficient a0[23:0]	
0x8010	a1[23:0]	
0x8011	a2[23:0]	
0x8012	b1[23:0]	
0x8013	b2[23:0]	
0x8014	PEQ Band 4 Coefficient a0[23:0]	
0x8015	a1[23:0]	
0x8016	a2[23:0]	
0x8017	b1[23:0]	
0x8018	b2[23:0]	
0x8019	PEQ Band 5 Coefficient a0[23:0]	
0x801A	a1[23:0]	
0x801B	a2[23:0]	
0x801C	b1[23:0]	
0x801D	b2[23:0]	
0x801E	PEQ Band 6 Coefficient a0[47:24]	
0x801F	a1[47:24]	
0x8020	a2[47:24]	
0x8021	b1[47:24]	
0x8022	b2[47:24]	
0x8023	a0[23:0]	
0x8024	a1[23:0]	
0x8025	a2[23:0]	
0x8026	b1[23:0]	
0x8027	b2[23:0]	

Address	Data [23:0]	Region Name
0x8028	PEQ Band 7 Coefficient a0[47:24]	PEQ Coefficients
0x8029	a1[47:24]	
0x802A	a2[47:24]	
0x802B	b1[47:24]	
0x802C	b2[47:24]	
0x802D	a0[23:0]	
0x802E	a1[23:0]	
0x802F	a2[23:0]	
0x8030	b1[23:0]	
0x8031	b2[23:0]	
0x8032	PEQ Band 8 Coefficient a0[47:24]	
0x8033	a1[47:24]	
0x8034	a2[47:24]	
0x8035	b1[47:24]	
0x8036	b2[47:24]	
0x8037	a0[23:0]	
0x8038	a1[23:0]	
0x8039	a2[23:0]	
0x803A	b1[23:0]	
0x803B	b2[23:0]	
0x803C	PEQ Band 9 Coefficient a0[47:24]	
0x803D	a1[47:24]	
0x803E	a2[47:24]	
0x803F	b1[47:24]	
0x8040	b2[47:24]	
0x8041	a0[23:0]	
0x8042	a1[23:0]	
0x8043	a2[23:0]	
0x8044	b1[23:0]	
0x8045	b2[23:0]	
0x8046	PEQ Coefficient Transfer Buffer 0[23:0]	PEQ Coefficient Transfer Buffer
0x8047	PEQ Coefficient Transfer Buffer 1[23:0]	
0x8048	PEQ Coefficient Transfer Buffer 2[23:0]	
0x8049	PEQ Coefficient Transfer Buffer 3[23:0]	
0x804A	PEQ Coefficient Transfer Buffer 4[23:0]	
0x804B	PEQ Coefficient Transfer Buffer 5[23:0]	
0x804C	PEQ Coefficient Transfer Buffer 6[23:0]	
0x804D	PEQ Coefficient Transfer Buffer 7[23:0]	
0x804E	PEQ Coefficient Transfer Buffer 8[23:0]	
0x804F	PEQ Coefficient Transfer Buffer 9[23:0]	
0x8050	Transfer parameter / Transfer execution	Transfer parameter/ Transfer execution
0x8051		
	Unused region [Note 1]	
0xC07F		

[Note 1] Do not write in the unused region.

[Note 2] PEQ coefficients RAM is mapped within on-chip RAM address space.

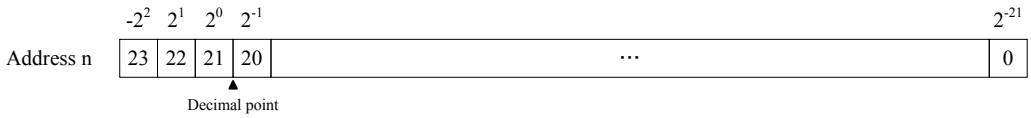
See "3.1.2 On-Chip RAM Address Map" for the detail.

3.5.4.2.2 PEQ Coefficients Formats

The format of each PEQ coefficients will be described below.

24-bit Coefficients Format

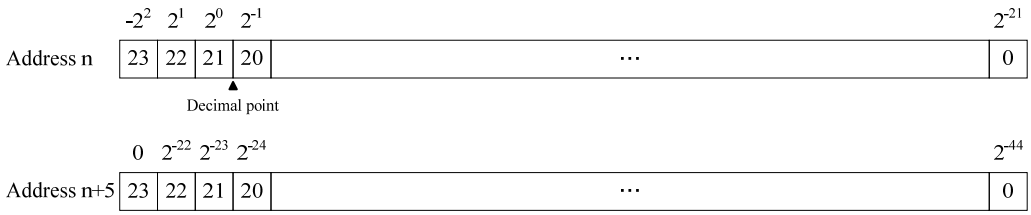
The signed 24-bit coefficients are used in PEQ Band0–5.



47-bit Coefficients Format

The coefficients for PEQ Band6–9 consist of an upper byte and a lower byte.

The most significant bit of the lower byte is always set to logic 0.



3.5.4.2.3 PEQ Coefficients Buffered Transfer Controller

To update PEQ coefficients for a PEQ Band at once in one sampling period, a temporary buffer and a dedicated transfer controller are provided

3.5.4.2.4 PEQ Coefficients Buffered Transfer Parameters/Transfer Execution

The (lower 7bit) address of the first PEQ coefficient to be updated and the coefficient word length are specified in this register.

Writing to this register will initiate copying from the temporary buffer to the updating coefficient locations.

The copying will be complete within two sample rate periods after the writing.

0x8050 (on-chip RAM)

bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
COEFNUM	**PEQAD[6]**	**PEQAD[5]**	**PEQAD[4]**	**PEQAD[3]**	**PEQAD[2]**	**PEQAD[1]**	**PEQAD[0]**

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
0	0	0	0	0	0	0	0

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	0

- **bit23: COEFNUM**

This register specifies the word length of the coefficients to be updated.

(When written)

0x0: Specifies five-word coefficients. Coefficients on the temporary buffer from 0x8046−0x804A will be copied to PEQAD−PEQAD+4.

0x1: Specifies ten-word coefficients. Coefficients on the temporary buffer from 0x8046−0x804F will be copied to PEQAD−PEQAD+9.

- **bit22-16: PEQAD[6:0]**

This register specifies the (lower 7 bit) address of the first PEQ coefficient to be updated.

(When written)

The (lower 7 bit) address of the first PEQ coefficient to be updated.

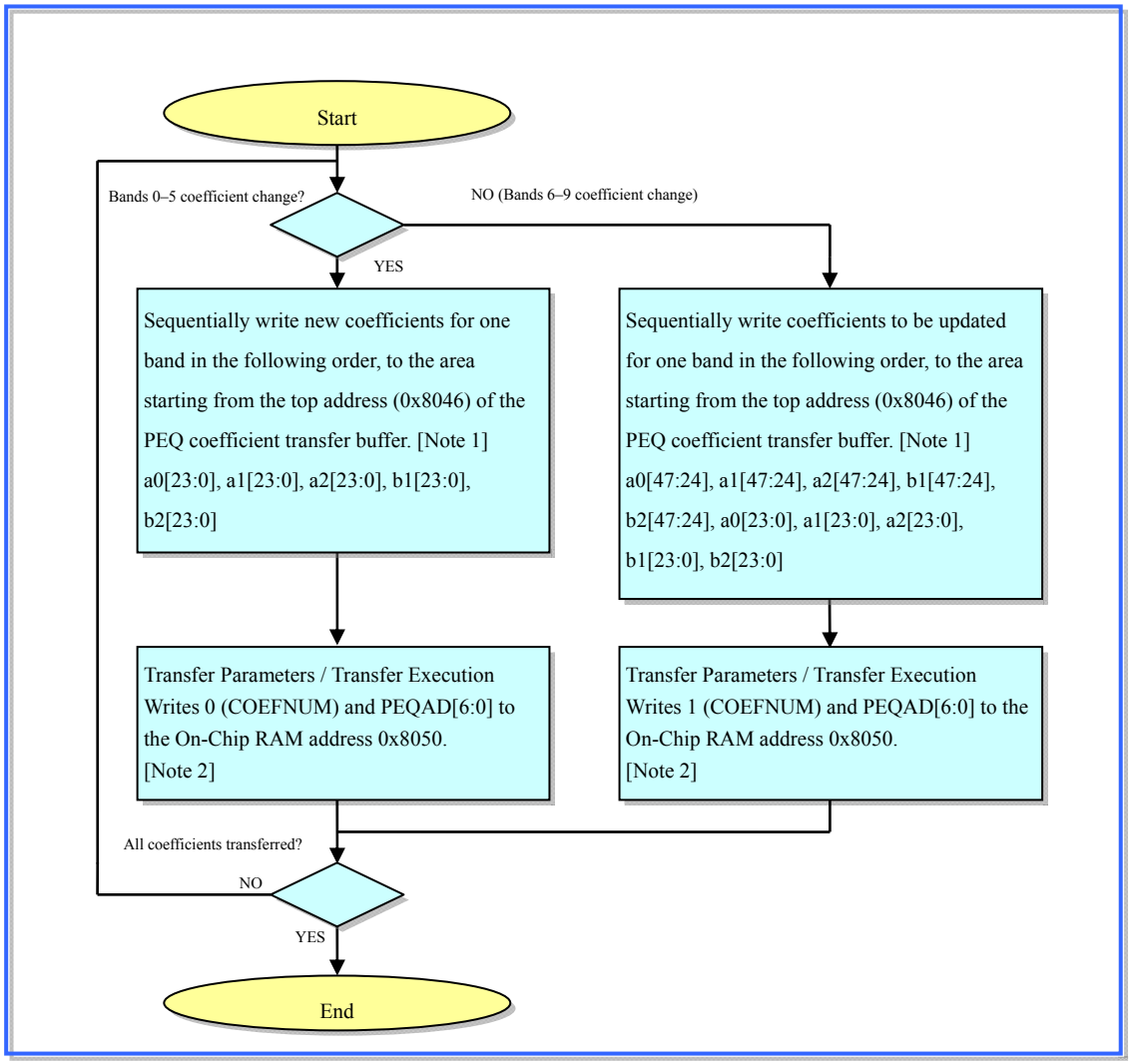
3.5.4.2.5 Updating PEQ Coefficients RAM

Updating Coefficients When SDSP is Not Running.

The coefficients RAM for PEQ Band0–9 (0x8000–0x8045) can be directly updated. Simply write new coefficients in these locations.

Updating Coefficients When DSP is Running.

The flow chart below shows the procedure:



[Note 1] See "3.2.3.1.4 On-Chip RAM Access".

[Note 2] See "3.5.4.2.4 PEQ Coefficients Buffered Transfer Parameters/Transfer Execution".

Band 0: PEQAD [6:0] = 0x00
Band 1: PEQAD [6:0] = 0x05
Band 2: PEQAD [6:0] = 0x0A
Band 3: PEQAD [6:0] = 0x0F
Band 4: PEQAD [6:0] = 0x14
Band 5: PEQAD [6:0] = 0x19
Band 6: PEQAD [6:0] = 0x1E
Band 7: PEQAD [6:0] = 0x28
Band 8: PEQAD [6:0] = 0x32
Band 9: PEQAD [6:0] = 0x3C

3.5.5 SDSP Controls

3.5.5.1 DSP Start Register

0x11: DSPSTART Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	MDSPSTART	**SDSPSTART**

- **bit0: SDSPSTART**

This register starts or stops SDSP operation.

(Reset value)

0x0

(When written)

0x0: Stops SDSP.

0x1: Starts SDSP.

(When read)

Current setting.

[Note]

We recommend starting and stopping both DSPs—MDSP2 and SDSP—at the same time.

See "3.7.7.2 Pause and Restart Sequence" for the detail of the restart procedure from pausing—setting logic 0 in this register—as part of the normal operation.

3.5.5.2 On-chip RAM Clear Register

0x0F: RAMCLR Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	MPRAMCLR	WRAMCLR	**SWRAMCLR**

- **bit0: SWRAMCLR**

This register controls zero clear operation of SWRAM contents.

SWRAM is the work RAM area of SDSP.

(Reset value)

0x0

(When written)

0x0: Does not start SWRAM zero clear operation.

0x1: Starts SWRAM zero clear operation.

(When read)

0x0: Indicates SWRAM zero clear operation is not ongoing or the previous zero clear operation has finished.

0x1: Indicates SWRAM zero clear operation is ongoing.

[Note]

On-chip ROM firmware block 0 executes the SWRAM zero clear operation as part of the device initialization.

SWRAM can be zero cleared using this function during run time after the initialization.

In that case, set both SDSPSTART and MDSPSTART bits to logic 0.

See "3.7.7.2 Pause and Restart Sequence" for the detail.

When the zero clear operation completes, this register becomes logic 0 when read.

3.5.5.3 SDSP Mode Register

0x0B: SDSPMD Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	**0**	**DEMON**	**DCM**

- **bit1: DEMON**

This register bit enables or disables De-Emphasis Filter operation.

(Reset value)

0x0

(When written)

0x0: Disables De-Emphasis Filter.

0x1: Enables De-Emphasis Filter.

(When read)

Current setting.

[Note]

Set both SDSPSTART and MDSPSTART to logic 0, when changing this register.

See "3.7.7.2 Pause and Restart Sequence" for the detail.

- **bit0: DCM**

This register bit selects SRC modes.

(Reset value)

0x0

(When written)

0x0: Interpolation mode

Use this mode when SRC input sampling rate is less than or equal to SRC output sampling rate + 2 kHz.

0x1: Decimation mode

Use this mode when SRC input sampling rate is greater then SRC output sampling rate + 2 kHz.

(When read)

Current setting.

[Note]

Set both SDSPSTART and MDSPSTART to logic 0, when changing this register.

See "3.7.7.2 Pause and Restart Sequence" for the detail.

3.5.6 SDSP Status

3.5.6.1 SDSP Status Register

0x20: SDSPST Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SDIERR	1	1	**UNLOCK**	**FSIERR**	**FSERR**	0	**SDSPERR**

- **bit4: UNLOCK**

This register bit informs that DPLL is not phase-locked.

(Reset value)

0x1

(When written)

0x0: Clears this status flag.

0x1: Does not clear this status flag.

(When read)

0x0: DPLL is phase-locked.

0x1: DPLL is not phase-locked.

[Note]

When this unlocked state is detected, SRC inputs and outputs are muted.

This muting is cancelled when DPLL is locked.

This register cannot be cleared even if attempting to write 0x0 to this register bit while DPLL is in an unlocked state.

- **bit3: FSIERR**

This register bit informs that the SRC I/O sampling frequency ratio is inappropriate.

(Reset value)

0x0

(When written)

0x0: Clears this error flag.

0x1: Does not clear this error flag.

(When read)

0x0: The error not occurred.

0x1: The error occurred.

[Note]

The criterion for this error detection is as follows:

SRC input sampling frequency ≥ SRC output sampling frequency × 5.

This register cannot be cleared even if attempting to write 0x0 to this register bit while SRC I/O sampling frequency ratio is inappropriate.

- **bit2: FSERR**

This register bit informs that the SRC input sampling frequency is inappropriate.

(Reset value)

0x0

(When written)

0x0: Clears this error flag.

0x1: Does not clear this error flag.

(When read)

0x0: The error not occurred.

0x1: The error occurred.

[Note]

An error will occur if a sampling frequency other than the supported frequencies (ranging from 8 kHz to 192 kHz) is fed.

This register cannot be cleared even if attempting to write 0x0 to this register bit while SRC input sampling frequency is inappropriate.

The data read when UNLOCK is equal to 0x1 is invalid.

- **bit0: SDSPERR**

This register bit informs that SDSP is overloaded.

(Reset value)

0x0

(When written)

0x0: Clears this error flag.

0x1: Does not clear this error flag.

(When read)

0x0: The error not occurred.

0x1: The error occurred.

[Note]

An error will occur if SDSP processing does not complete within one sampling period.

This register cannot be cleared even if attempting to write 0x0 to this register bit while SDSP is overloaded.

3.5.6.2 Sampling Frequency Ratio Register

0x17: DPLLFS Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DPLLFS[7]	**DPLLFS[6]**	**DPLLFS[5]**	**DPLLFS[4]**	**DPLLFS[3]**	**DPLLFS[2]**	**DPLLFS[1]**	**DPLLFS[0]**

- **bit7-0: DPLLFS[7:0]**

This register holds the SRC I/O sampling frequency ratio (SRC input sampling frequency / SRC output sampling frequency).

Note that this ratio may vary depending on factors such as the accuracy of clocks.

(Reset value)

0x20

(When written)

The write operation is ignored.

(When read)

A SRC I/O sampling frequency ratio is read.

[Note]

This register can be read only when DPLL is being locked.

Read this register after confirming that 0x0 can be read from UNLOCK register.

For the register value, see the following:

SRC Output Sampling Frequency = 48 kHz

SRC Input Sampling Frequency	216kHz	192kHz	96kHz	48kHz	44.1kHz	32kHz	8kHz	6kHz
DPLLFS register value	0x90	0x80	0x40	0x20	0x1D	0x15	0x05	0x04

SRC Output Sampling Frequency = 44.1 kHz

SRC Input Sampling Frequency	198kHz	192kHz	96kHz	48kHz	44.1kHz	32kHz	8kHz	6kHz
DPLLFS register value	0x90	0x8B	0x46	0x23	0x20	0x17	0x06	0x04

3.6 FM Synthesizer

3.6.1 Features

- Integrated the Yamaha FM synthesizer
- Integrated melody sequencer
- 4-voice polyphonic FM synthesizer (with four different tones)
- Keypad/alert tones, and startup sounds on the on-chip ROM
- Playback of user contents downloaded from the host controller, such as customized keypad/alert tones or startup sounds

3.6.2 FM Synthesizer Parameters

This section describes the parameters that are used to control the FM synthesizer.

Write 0 to the bits that have no parameter assignment.

Reading from the unassigned bit is not valid. (0 is read.)

3.6.2.1 FM Synthesizer Start Register

0xC032 (FM Synthesizer Parameter: On-chip RAM): ST Register

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
0	0	0	0	0	0	0	0

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	**ST**

- **bit0: ST**

This register bit controls the playback from the FM synthesizer.

(Reset value)

0x0

(When written)

0x0: Stops the playback.

0x1: Starts the playback.

3.6.2.2 Clock Setting

0xC039 (FM Synthesizer Parameter: On-chip RAM): CLKSET Register

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
0	0	0	0	0	0	0	**CLKSET[8]**

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CLKSET[7]	**CLKSET[6]**	**CLKSET[5]**	**CLKSET[4]**	**CLKSET[3]**	**CLKSET[2]**	**CLKSET[1]**	**CLKSET[0]**

- **bit8-0: CLKSET[8:0]**

Different XIN input frequency requires different setting in this register.

(Reset value)

0x0

(When written)

Specify a value that matches XIN input frequency.

XIN input frequency	Setting Value
24.576 MHz	0x1B7
22.5792 MHz	0x194

3.6.3 FM Synthesizer Status

3.6.3.1 FM Synthesizer Status Register

0x1A: FMST Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	STEN	0	0	0	**STFLG**

- **bit0: STFLG**

This register bit indicates the playback status of the FM synthesizer contents.

(Reset value)

0x0

(When written)

The write operation is ignored.

(When read)

0x0: Playback stopped.

0x1: Playback running.

3.6.3.2 FM Synthesizer Status Enable Register

0x1A: FMST Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	**STEN**	0	0	0	STFLG

- **bit4: STEN**

This register bit enables a playback status to be sent to the interrupt pin (the IRQ_N pin).

(Reset value)

0x0

(When written)

0x0: Disables the status transmission.

0x1: Enables the status transmission.

(When read)

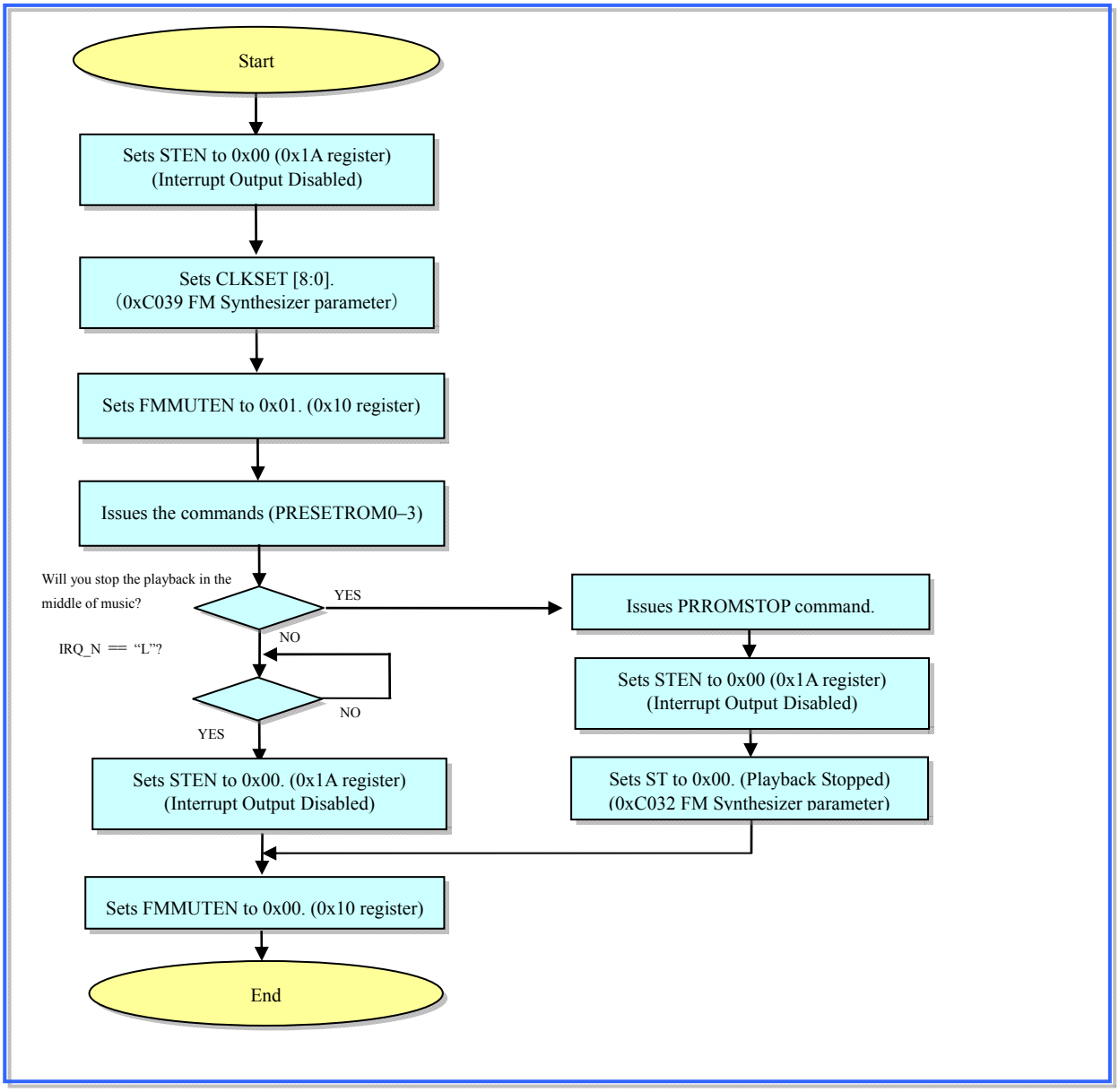
Current setting.

[Note]

When playing back the FM synthesizer contents on the on-chip ROM, this bit automatically becomes logic 1.

3.6.4 Playing Back FM Synthesizer Contents in On-chip ROM

FM synthesizer preset—general and ready to use—contents are stored in the on-chip ROM. The host controller simply specify which preset to play back. The following diagram illustrates the steps to play preset tunes.



3.6.5 FM Synthesizer Contents (On-chip ROM)

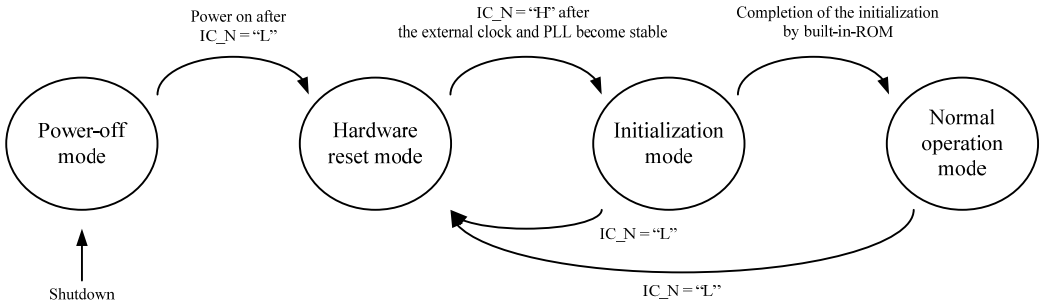
The table below shows the FM synthesizer contents stored in the on-chip ROM:

No.	On-chip ROM Block Number (Dec.)	Content Name	Sound Type	Description
1	32	Power_On_01	Startup sound 1	A high-class sound with a synth pad
2	33	Power_Off_01	Shutdown sound	A high-class sound with a synth pad
3	34	Power_On_02	Startup sound 2	Sound expressing wake-up with bouncy rising sounds
4	35	Power_On_03	Startup sound 3	Sound forefeeling the startup with a single synth pad chord
5	36	Power_On_04	Startup sound 4	Sound expressing the image of a heavy sound
6	37	Power_On_05	Startup sound 5	Jazzy chord with an electric piano
7	38	Power_On_06	Startup sound 6	Airily and adorable sound
8	39	Power_On_07	Startup sound 7	Simple, warm single chord
9	40	Power_On_08	Startup sound 8	Sound with spirit of innovation
10	41	Power_On_09	Startup sound 9	Thrilling sound
11	42	Power_On_10	Startup sound 10	Silver and natural bell sound
12	43	Power_On_11	Startup sound 11	Gradually-thawing chords with expectations
13	44	Power_On_12	Startup sound 12	Jumping sound with a feeling of easiness
14	45	Power_On_13	Startup sound 13	Futuristic sound
17	48	Power_On_16	Startup sound 16	Simple silver bell sound
18	49	Power_On_17	Startup sound 17	Grand and heavy sound
19	50	Power_On_18	Startup sound 18	Grand and heavy sound
20	51	Power_On_19	Startup sound 19	Sound forefeeling changes
21	52	Power_On_20	Startup sound 20	Sound with the image of lighting it up
22	53	Power_On_21	Startup sound 21	Sound with the image of getting light gradually
23	54	Power_On_22	Startup sound 22	Sound like a jazz guitar
24	55	Power_On_23	Startup sound 23	Sound expressing "change" with expectations
25	56	Power_On_24	Startup sound 24	Sound expressing originality with sharpish sounds
26	57	Power_On_25	Startup sound 25	Sound with the image of evoking inspiration
27	58	Power_On_26	Startup sound 26	Sound with the image of ringing a bell
28	59	Power_On_27	Startup sound 27	Sound expressing natural startup without pushing itself
29	60	Power_On_28	Startup sound 28	Sound expressing natural startup without pushing itself
30	61	Power_On_29	Startup sound 29	Sound expressing natural startup simply
31	62	Power_On_30	Startup sound 30	Sound with the image flashing brightly
32	63	Power_On_31	Startup sound 31	Sound with the image singing a tune
33	64	Power_On_32	Startup sound 32	Humorous sound
36	67	Power_On_35	Startup sound 35	Sound expressing a questioning
37	68	Power_On_36	Startup sound 36	Sound expressing the start with melodious arpeggio

No.	On-chip ROM Block Number (Dec.)	Content Name	Sound Type	Description
38	69	Power_On_37	Startup sound 37	Sound expressing an expectation with light bell sound
39	70	Power_On_38	Startup sound 38	Sound like a jazz guitar
40	71	Power_On_39	Startup sound 39	Simple sound with a snappily chord
41	72	Operation_01	Button operation 1	Traditional operation sound 1
42	73	Operation_02	Button operation 2	Traditional operation sound 2
43	74	Operation_03	Button operation 3	Traditional operation sound 3
44	75	Operation_04	Button operation 4	Operation sound with futuristic image
45	76	Operation_05	Button operation 5	Chordal sound as heard in SF movies
46	77	Comical_01	Karaoke sound 1	Sound expressing chagrin and wrong answer
47	78	Pafopafo_01	Karaoke sound 2	Toy trumpet sound
48	79	Chime_01	Karaoke sound 3	Sound expressing the success
49	80	Bicycle_01	Sound effect 1	Sound simulating a bicycle bell
50	81	Telephone_01	Sound effect 2	Sound simulating a call bell
51	82	Announcement_01	Sound effect 3	Sound simulating the start of announcement
52	83	Announcement_02	Sound effect 4	Sound simulating the end of announcement
53	84	School_Bel_01	Sound effect 5	Sound simulating the Westminster bell
54	85	Spring_01	Sound effect 6	Sound simulating the wind-up of a spiral spring
55	86	SL_01	Sound effect 7	Sound simulating a locomotive engine
56	87	Cat_01	Sound effect 8	Sound simulating the call of a cat
57	88	Cuckoo_01	Sound effect 9	Hollow sound simulating chirp of a cuckoo
58	89	Chime_02	Sound effect 10	Right answer sound

3.7 System

3.7.1 Operation Mode



The table below shows the state in each mode except power-off mode:

Function \ Mode	Hardware reset mode	Initialization mode	Normal operation mode
Clock oscillator (for crystals)	(Operating)	Operating	Operating
PLL	(Operating)	Operating	Operating
MDSP2	Stopped	Stopped	Operating
SDSP	Stopped	Stopped	Operating
RAM	Stopped	Not updatable	Updatable
Host processor interface	Stopped	Operating	Operating
Registers	Stopped	Not updatable	Updatable
Audio interface	Stopped	Stopped	Operating
I/O pins	Hi-Z	Hi-Z	Operating

[Note] (Operating) means the function will work after waiting for the specified period of time.

3.7.1.1 Power-off Mode

If the power supplies are shut down, the operation mode will shift from the current operation mode to Power-off mode. Do not apply any voltage to all the input pins except the following pins: SDA pin and SCL pin. The output pin states are undefined.

3.7.1.2 Hardware Reset Mode

The Power-off mode will shift to Hardware Reset mode by powering up each power supply sequentially with IC_N = "L".
And, any mode can be switched to this Hardware Reset mode by setting IC_N = "L".
In this mode, this device is reset to operate the external clocks and PLL.
See Power-ON in "5.5 AC Characteristics" for the details of the start-up sequence of the power supplies and each signal.

3.7.1.3 Initialization Mode

Initialization mode is given by setting IC_N = "H". In this mode, this device is initialized with the configuration data in the on-chip ROM block 0.

3.7.1.4 Normal Operation Mode

This Normal Operation mode is given when the above initialization with the ROM data is completed.
In this mode, all the functions of this device are enabled.

3.7.2 Device ID

This device has an 8-bit device ID.

3.7.2.1 Device ID Register

0x19: ID Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ID[7]	**ID[6]**	**ID[5]**	**ID[4]**	**ID[3]**	**ID[2]**	**ID[0]**	**ID[0]**

- **bit7-0: ID[7:0]**

This register holds the device ID.

(Reset value)

0xC0

(When written)

The write operation is ignored.

(When read)

The device ID is read.

3.7.3 Clock Controls

Clocks, used for the blocks after the SRC output side, are generated in this device.

See "3.3.3 Internal Clock System" for details of clock supply to each block.

3.7.3.1 Sampling Frequency Setting

This device supports the following sampling frequencies for the SRC output side: 48 kHz, 44.1 kHz.

- The XIN input clock frequency is selected according to this sampling frequency.
- FSM [1:0] register is set according to this sampling frequency.

When using MDSP2 firmware stored in the on-chip ROM, feed a clock with the frequency of 24.576 MHz to XIN pin. The SRC output side including MDSP2 operates at the sampling frequency of 48 kHz.

Sampling Frequency	XIN Input Frequency	FSM[1:0] Register
48 kHz	24.576 MHz	0x0
44.1 kHz	22.5792 MHz	0x1

3.7.3.2 Sampling Frequency Setting Register

0x0E: FSM Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	**FSM[1]**	**FSM[0]**

- **bit1-0: FSM[1:0]**

This register bit sets the XIN pin input frequency (sampling frequency at the SRC output).

This setting value will change the time constant of the De-Emphasis filter in the SDSP.

(Reset value)

0x0

(When written)

0x0: XIN pin input frequency is 24.576 MHz. The sampling frequency at the SRC output is 48 kHz.

0x1: XIN pin input frequency is 22.5792 MHz. The sampling frequency at the SRC output is 44.1 kHz.

0x2: Reserved

0x3: Reserved

(When read)

Current setting.

3.7.3.3 PLL Abnormal Oscillation Detection Register

0x23: PLLERR Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	**PLLERRE**	0	**PLLERR**

Indicates the accessible area regardless of whether or not the PLL is activated.

- **bit2: PLLERRE**

This register bit enables or disables the detection of the abnormal PLL oscillation.

(Reset value)

0x0

(When written)

0x0: Disables this error detection.

0x1: Enables this error detection.

(When read)

Current setting.

[Note]

If PLLERR bit is set to 0x1 because of the error, set PLLERRE bit to 0x0 while the PLL is operating properly to reset the PLLERR bit to 0x0 and to enable the error detection again, set PLLERRE bit to 0x1.

- **bit0: PLLERR**

This register bit indicates the abnormal PLL oscillation.

(Reset value)

0x0

(When written)

The write operation is ignored.

(When read)

0x0: No abnormal PLL oscillation occurred.

0x1: Abnormal PLL oscillation occurred.

[Note]

If this error is detected, the audio output is muted. The PLLERR bit is held to logic 0 whenever the PLLERRE bit is 0x0.

3.7.4 Mute Controls

The mute control can be performed by setting registers and MUTE_N pin.

The table below shows the correspondence between mute controls and muted blocks:

Mute Setting	FM Synthesizer Output	MDSP2 CHO7–0	SRC Input	De-Emphasis Filter Output	PEQ Output
FMMUTEN = 0x0	✓				
MDSPMUTEN = 0x0		✓			
SDSPMUTEN = 0x0			✓	✓	✓

3.7.4.1 Mute Setting Register

0x10: MUTE Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	**FMMUTEN**	**MDSPMUTEN**	**SDSPMUTEN**

- **bit2: FMMUTEN**

This register bit sets the FM synthesizer mute.

(Reset value)

0x0

(When written)

0x0: Sets the FM synthesizer mute.

0x1: Cancels the FM synthesizer mute.

(When read)

Current setting.

[Note]

If the FM synthesizer contents are not played back, set FMMUTEN register bit to logic 0.

Abnormal sound may be generated if the FMMUTEN register is set to logic 0 while the FM synthesizer output level remains high; therefore, lower the output level to a sufficient low level before setting the register to logic 0.

- **bit1: MDSPMUTEN**

This register bit sets the MDSP2 mute.

(Reset value)

0x0

(When written)

0x0: Sets the MDSP2 mute.

0x1: Cancels the MDSP2 mute.

(When read)

Current setting.

- **bit0: SDSPMUTEN**

This register bit sets the SDSP mute.

(Reset value)

0x0

(When written)

0x0: Sets the SDSP mute.

0x1: Cancels the SDSP mute.

(When read)

Current setting.

3.7.5 Power-down Control

3.7.5.1 Power-down Setting Register

0x33: PWRDWN Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	**DPD**

- **bit0: DPD**

This register bit enables the power down of the digital block.

(Reset value)

0x0

(When written)

0x0: Powers up the digital block.

0x1: Powers down the digital block.

(When read)

The held value is read; however, 0x1 cannot be read from this register bit because clocks will stop when DPD is set to logic 1.

See "3.7.7.5Power-Down / Power-Up" for details of the power-down/recovery sequences.

3.7.6 System Errors

3.7.6.1 System Error Processing

This device will automatically mute the output for the purpose of preventing abnormal sound if any system error occurs.

The table below shows which part is muted for each system error:

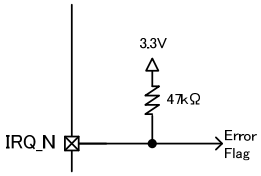
Cause of System Errors (Register Name)		SDI0	SDI 2–1	SDO 1–0	MDSP2 CHO7–0	SRC Input	De-Emphasis Filter Output	PEQ Output	Error Notification
Input audio clock error (SDIERR)	AIFMD[3:0]=0x0	✓				✓	✓		SDIERR register
	AIFMD[3:0]=0x1,0x2,0x3	✓	✓			✓	✓		
DPLL phase unlocked (UNLOCK)						✓	✓		UNLOCK register
PLL abnormal oscillation (PLLERR) [Note 1]				✓					PLLERR register IRQ_N pin [Note 2]
MDSP2 processing error (MDSPERR)	DEVMD=0x0				✓	✓	✓	✓	MDSPERR register IRQ_N pin [Note 2]
SDSP overload error (SDSPERR)	DEVMD=0x0				✓	✓	✓	✓	SDSPERR register IRQ_N Pin [Note 2]

[Note 1] Abnormal sound may be generated because if PLLERR occurs, SDO1–0 is held to 0 in out-of-sync with the sampling period.

[Note 2] Set HANGUPP register 0x1 when using IRQ_N pin for error notifications.

3.7.6.1.1 Error Output Pin (IRQ_N pin)

a) The IRQ_N pin has an open-drain output. Pull them up with a resistor as shown example below:



b) Follow the following steps to pull up the IRQ_N pin outputs externally.
   (1) Pull it up to the external supply voltage of 3.6V or lower.
   (2) In either case, select a resistor value so that the sink current more than 2mA will not flow when IRQ_N is driven to “L”.

c) Do not connect the IRQ_N pin to other pins.

Recovery from System Errors

Cause of System Errors (Register Name)	Recovery Conditions
Input audio clock error (SDIERR)	Recovers from this error state "WCK input period × 256" after the input audio clock is recovered.
DPLL phase unlocked (UNLOCK)	Recovers from this error state when DPLL phase is locked.
PLL abnormal oscillation (PLLERR)	Recovers from this error state by hardware reset and initialization.
MDSP2 processing error (MDSPERR)	Recovers from this error state by hardware reset and initialization.
SDSP overload error (SDSPERR)	Recovers from this error state by hardware reset and initialization.

3.7.6.2 System Error Handling Setting Register

0x06: SYSMD Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	**DEVMD**	**HANGUPP**	**HANGUPR**

- **bit2: DEVMD**

This register bit selects an operation to do in the following errors: MDSPERR, SDSPERR.

(Reset value)

0x0

(When written)

0x0: Sets 0x0 to the following register bits: SDSPMUTEN, MDSPMUTEN, SDSPSTART, and MDSPSTART.

0x1: Does not set 0x0 to the above register bits.

(When read)

Current setting.

[Note]

Set 0x0 to this register bit in normal use.

Set 0x1 to this register bit if it is difficult to find a cause of the system error.

- **bit1: HANGUPP**

This register bit selects which condition should be posted to the IRQ_N pin.

(Reset value)

0x0

(When written)

0x0: EXIRQN register settings

0x1: The result of the logical NOR operation on PLLERR, MDSPERR, and SDSPERR bits.

(When read)

Current setting.

- **bit0: HANGUPR**

This register bit selects which condition should be sent to MIREQ [7] register.

(Reset value)

0x0

(When written)

0x0: Nothing

0x1: The result of the logical OR operation on PLLERR, MDSPERR, and SDSPERR bits.

(When read)

Current setting.

0x0D: IRQN Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	0	**EXIRQN**

- **bit0: EXIRQN**

This register bit specifies a signal status to be sent to the IRQ_N pin while HANGUPP is set to 0x0.

If a malfunction is detected, the host processor can set IRQ_N = “L” with this register bit.

(Reset value)

0x1

(When written)

0x0: The IRQ_N pin status is forced to be a logic low level.

0x1: No signal status is output to the IRQ_N pin.

(When read)

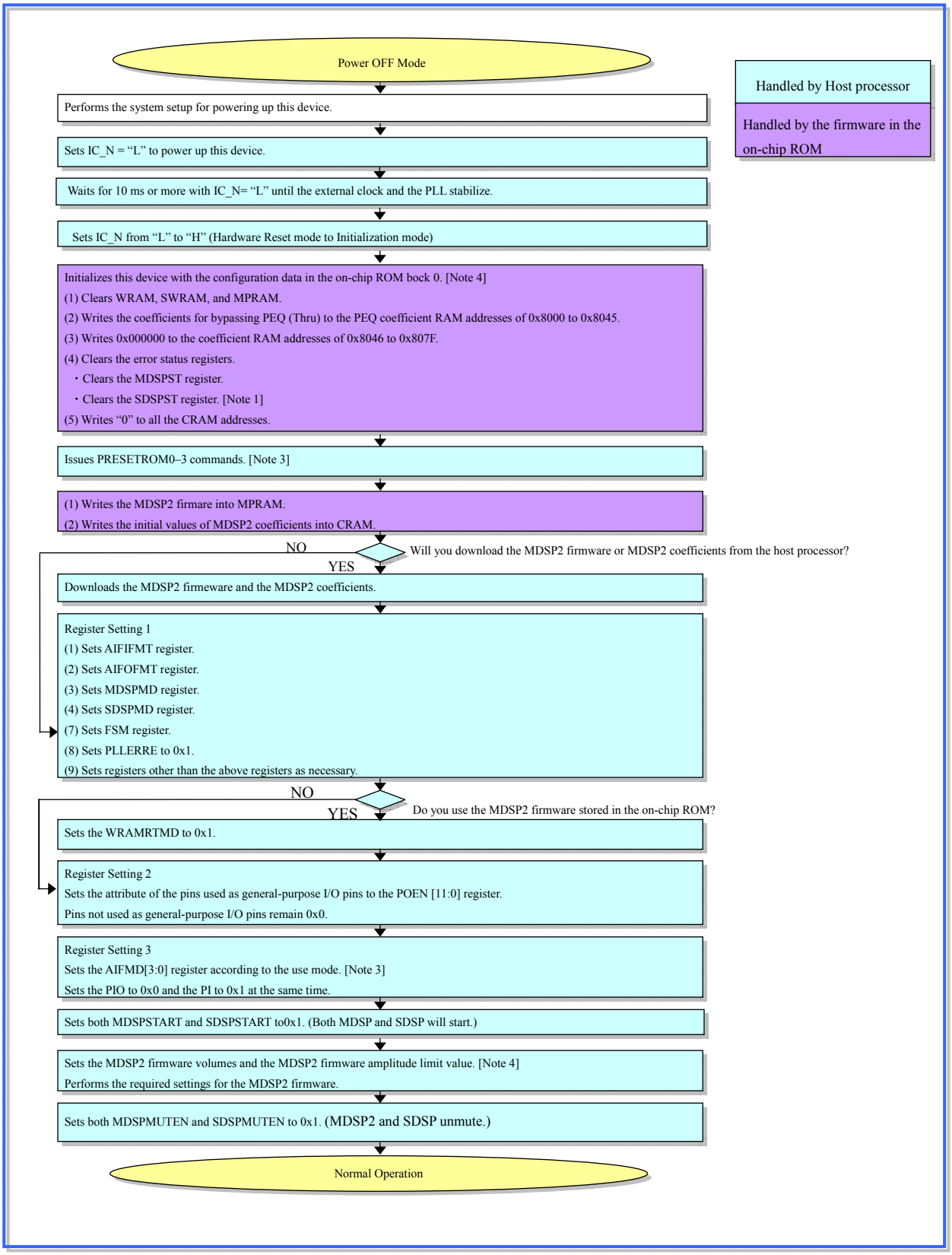
Current setting.

[Note]

With HANGUPP= 0x0, this register bit status is posted to IRQ_N signal.

3.7.7 Device Control Examples

3.7.7.1 Powering Up, Initialization



[Note 1] The host processor must clear SDIERR register after sound playbacks.

It takes 256 sample rate periods or more with valid bit and word clocks supplied after the device initialization, before the host controller can clear this register.

[Note 2] Set a MDSP2 firmware block number with PRESETROM0–3 commands and their arguments.

See "Firmware Manual" for details of block number, firmware functions, and firmware use regulations.

[Note 3] Note that the first one clock is not properly output when attempting to output WCK, BCK, and MCK from this device. In order to prevent abnormal sound from being generated during this one clock period, take action such as muting in the receiving side device.

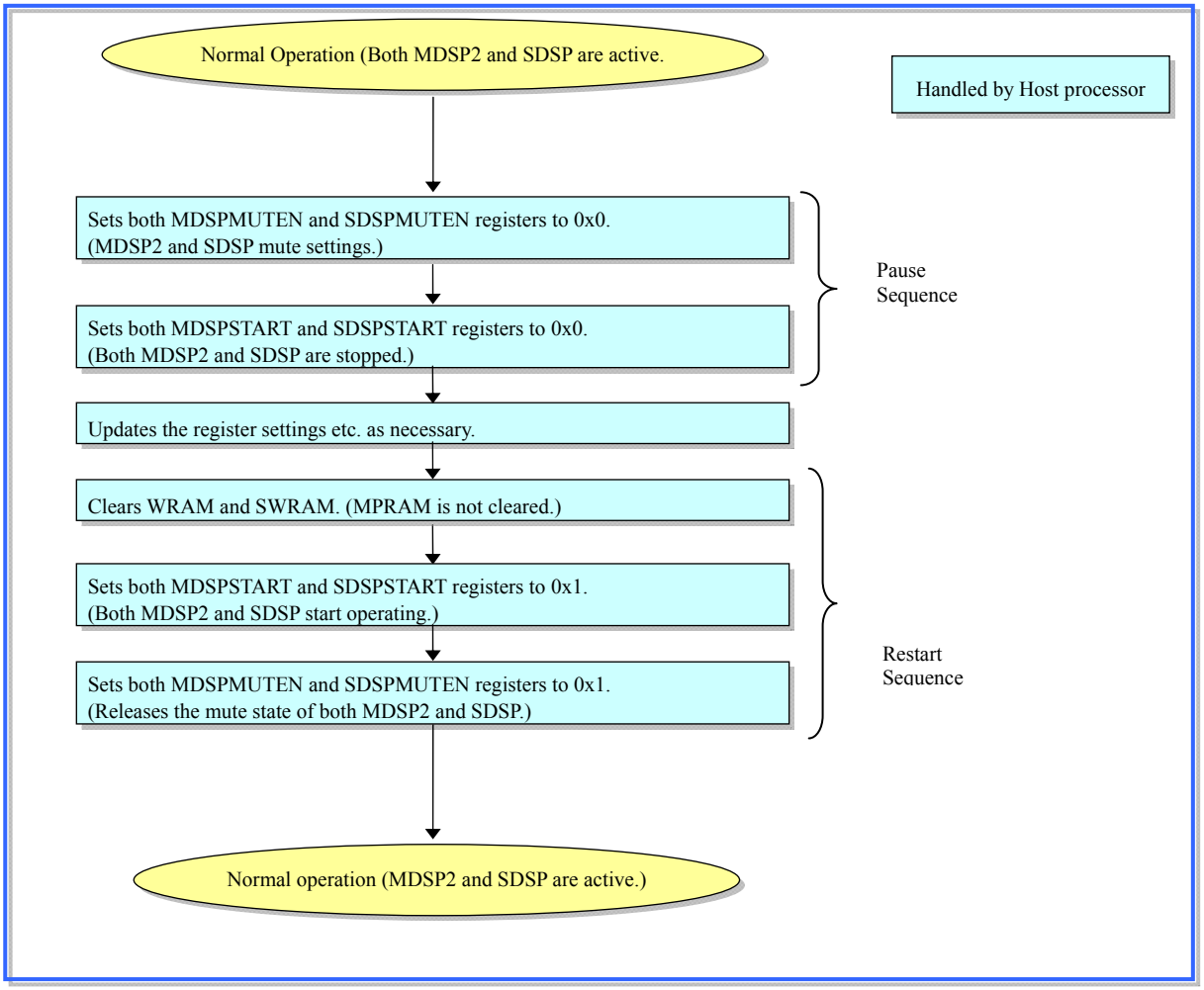
[Note 4] Device initialization requires some period shown below.

Wait this amount of time after the “L” to “H” transition of IC_N, before start accessing the device.

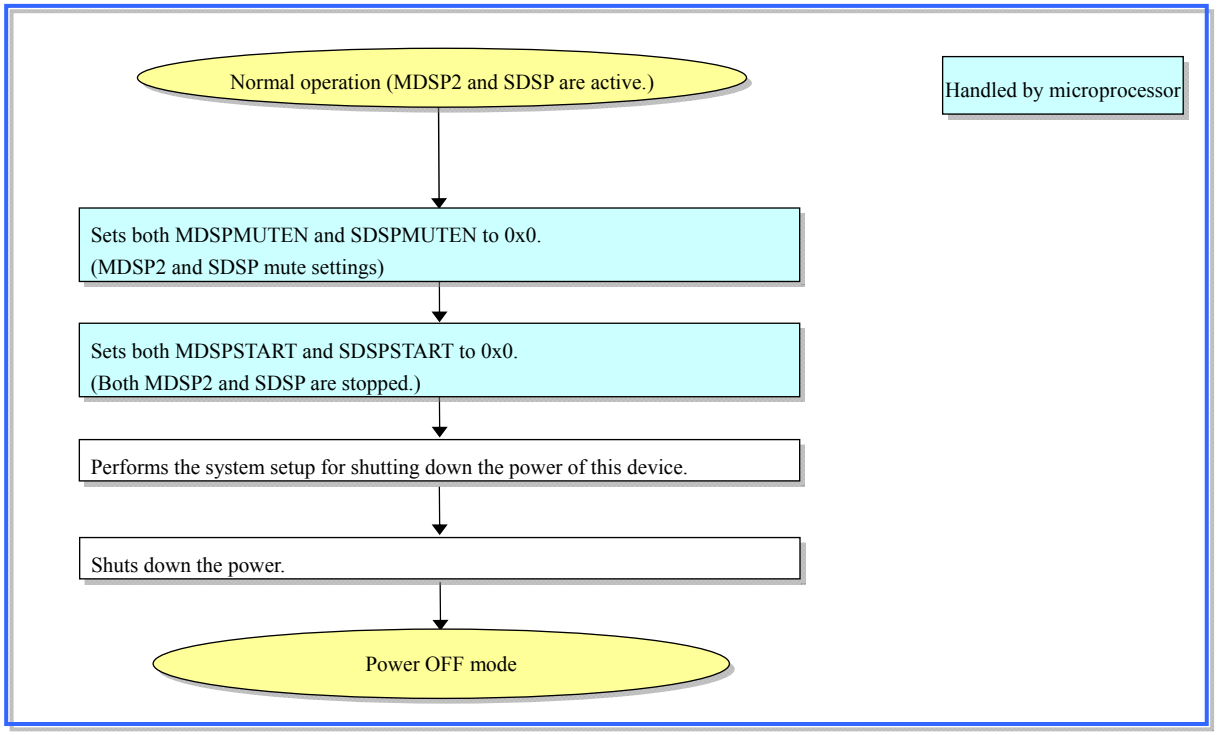
· 220μs at XIN Clock = 24.576MHz

· 240μs at XIN Clock = 22.5792MHz

3.7.7.2 Pause and Restart Sequences



3.7.7.3 Shut Down Sequence



3.7.7.4 Runtime Transfer

The runtime transfer is the way used to transfer firmware coefficients when MDSP2 is operating.
With runtime transfer, the firmware coefficients are read and written via WRAM0 (MDSP2 work RAM0).
This runtime transfer allows multiple firmware coefficients to be read or written in a batch without an intermittent sound break.

Transfer Source	Transfer Destination
· Host (Host processor)	→ On-chip RAM (CRAM)
· On-chip ROM	→ On-chip RAM (CRAM)
· On-chip RAM (CRAM)	→ Host (Host processor)

[Note] This runtime transfer is realized by firmware. See "Firmware Manual" for details.

The table below shows an example of loading data to the runtime transfer buffer:

Address	Upper 16 bits [31:16]	Lower 16 bits [15:0]
0x0000	Transfer start address [15:0]	0x0000
	Transfer data size [15:0]	0x0000
	Coefficient 0[15:0]	0x0000
	Coefficient 1[15:0]	0x0000
	Coefficient 2[15:0]	0x0000
	Coefficient 3[15:0]	0x0000
	Coefficient 4[15:0]	0x0000
	Coefficient 5[15:0]	0x0000
	Coefficient 6[15:0]	0x0000
	Coefficient 7[15:0]	0x0000
	Coefficient 8[15:0]	0x0000
0x000B	Coefficient 9[15:0]	0x0000

[Note] The runtime transfer buffer is reserved in WRAM0.
See "3.1.2 On-Chip RAM Address Map" for details.

WRAMRTMD register is the register used to help this device to read and write to and from the runtime transfer buffer.
When setting 0x1 to the WRAMRTMD register, WRAM0 serves as a 16-bit wide memory to the read/write operation from the host processor and to the write operation from the on-chip ROM.

The description below shows the operation for when the WRAMRTMD register is set to 0x1:
1. Read and Write operation from the host processor

- When data is written to WRAM0 using WRITE commands, the data is loaded to WRAM0 for each 2 bytes of data in the order from the upper 16 bits and then to the lower 16 bits. The lower 16 bits are filled with 0.
- When data is written to WRAM0 using WWORK0–3 commands, 2 bytes of data is loaded as well, with the lower 16 bits filled with 0.
- When data is read from WRAM0 using READ commands, only the upper 2 bytes of WRAM0 are read in the order from the upper byte to the lower byte.

And, if the host processor consecutively reads data from WRAM0, the upper 2 bytes of data in the next address will be read.

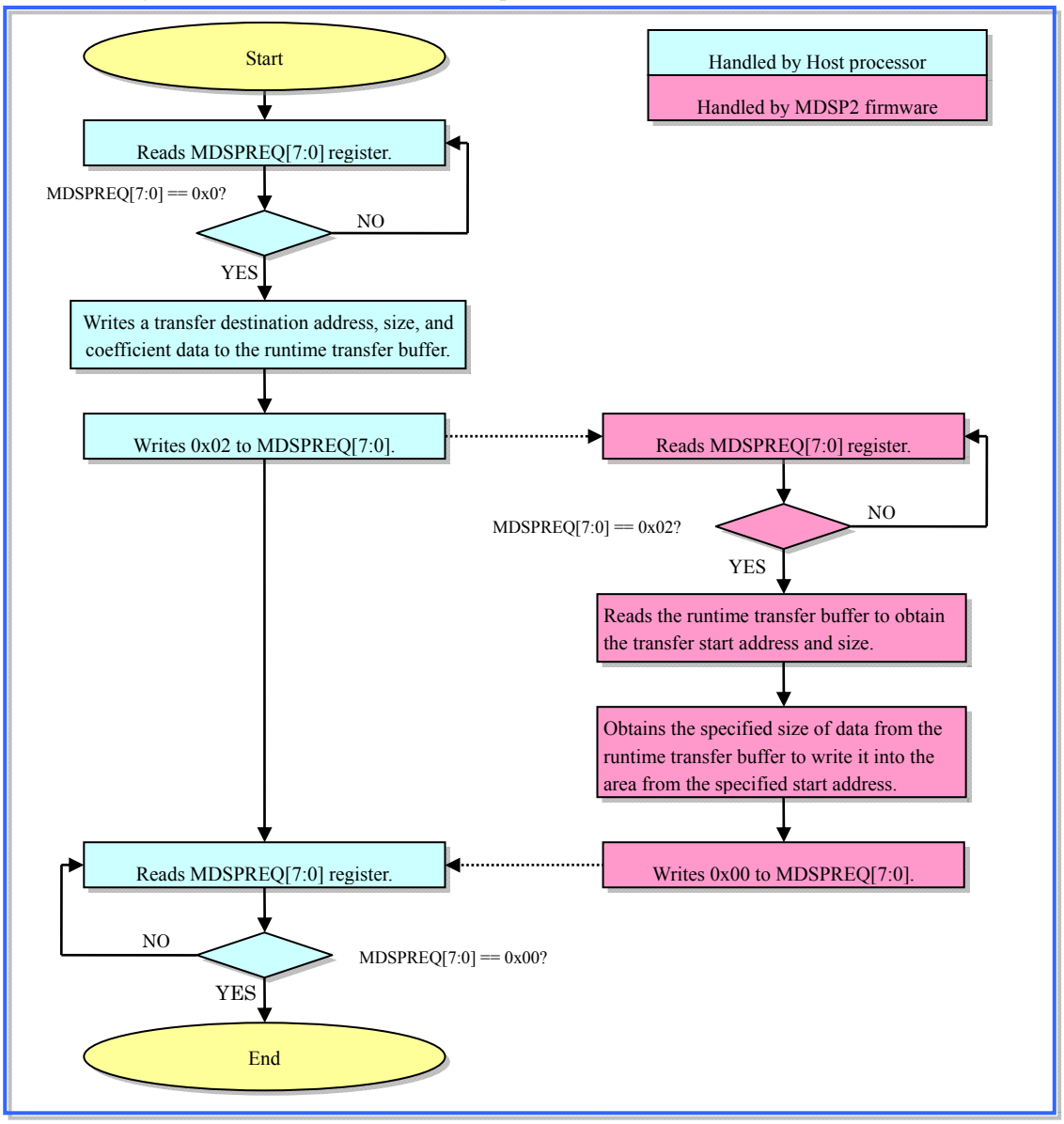
When data is read from WRAM0 using RWORK0–3 commands, only the upper 2 bytes of data are read in the order from the upper byte to the lower byte.

2. Read and Write operation from MDSP2

WRAM0 serves as a 32 bit wide memory regardless of WRAMRTMD register settings.

3.7.7.4.1 Runtime Transfer from Host processor

The flow diagram below shows a control example with MDSPREQ [7:0]=0x2:



[Note 1] The item, shown above as "Handling by MDSP2 firmware", is executed within one sample period.

[Note 2] The host processor can perform the processing other than access to this device during the palling period of MDSPREQ[7:0].

3.7.7.4.2 Runtime Transfer Assist Register

0x0A: MDSPMD Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	0	0	0	**WRAMRTMD**	WRAMMD

- **bit1: WRAMRTMD**

Set the bit width of WRAM0 for the host processor's write/read to WRAM0 or the on-chip ROM's write to WRAM0.

(Reset value)

0x0

(When written)

0x0: Normal mode

WRAM operates as 32-bit width for the host processor's write/read or the on-chip ROM's write.

0x1: Runtime transfer assist mode

WRAM operates as 16-bit width for the host processor's write/read or the on-chip ROM's write.

(When read)

Current setting.

[Note]

WRAM0 is treated as 32-bit width regardless of its bit setting at write or read from MDSP2.

3.7.7.5 Power-Down / Power-Up

To power down this device, set the DPD to 0x1.

To power up this device, be sure to set IC_N = “L” and perform the initialization procedure in advance.

[Note]

Use the DPD register (0x33, bit 0) to power down the digital circuits.

This register controls the following:

Stops the crystal oscillation circuit (by disabling XIN pin).

Powers down the on-chip PLL.

Disables the on-chip memories (SRAM, ROM).

3.7.8 Execution Time

3.7.8.1 Host processor Command

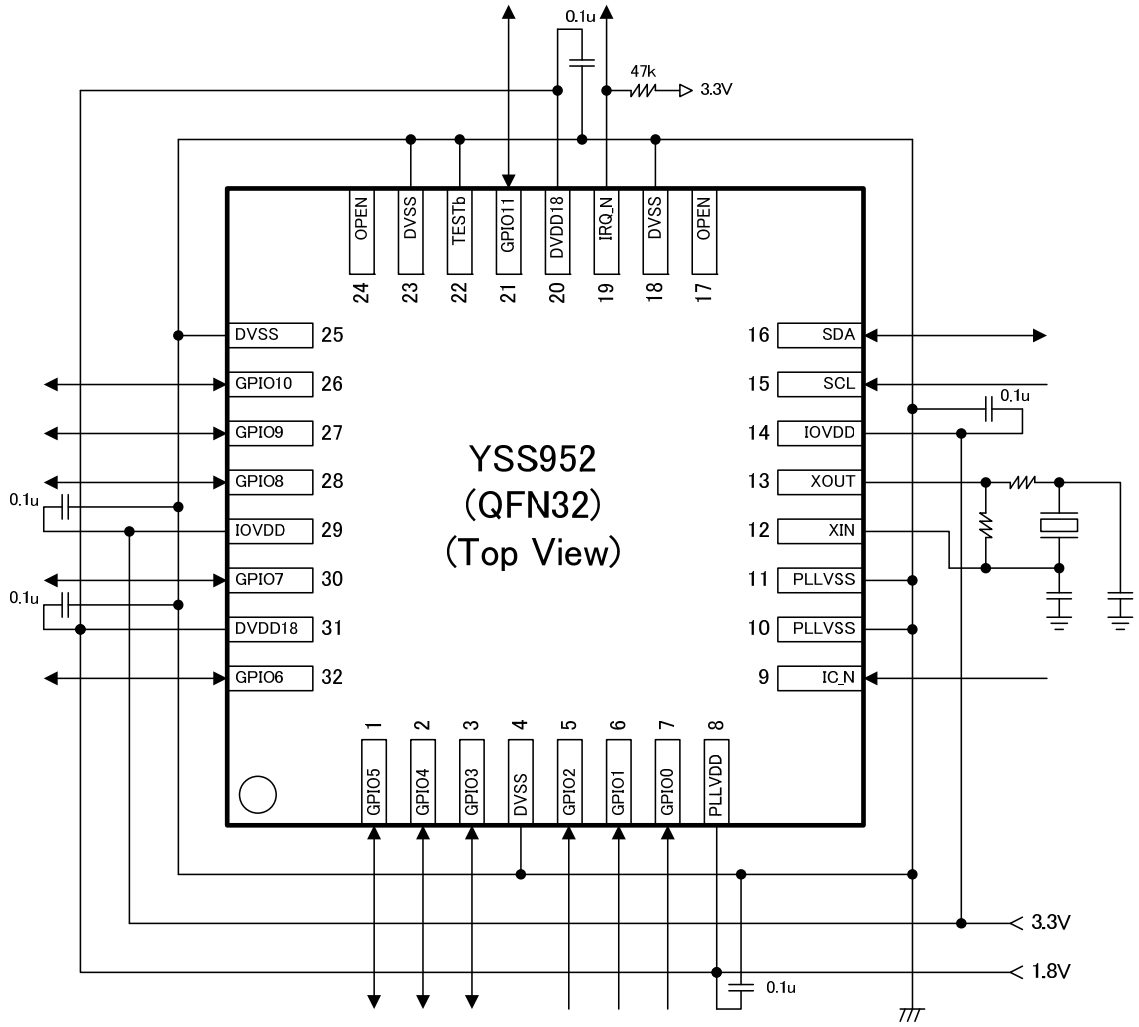
The table below shows the estimated command execution time.

For detailed of execution time, refer to I^2C Bus Specification (Phillips).

And, the execution time may increase depending on the system configuration, the host processor controls, etc.

Item	Condition	Execution time
Start condition + Stop condition + bus free time	f_{SCL}=400 kHz	Approx. 4.0 μs
Repetitive start condition	f_{SCL}=400 kHz	Approx. 1.2 μs
Write and read time per byte	f_{SCL}=400 kHz	Approx. 22.5 μs

4 Application Example



[Note 1] Pull up the IRQ_N pin through a resistor of 47kΩ because it has open-drain output.
[Note 2] Select appropriate resistor and capacitor values according to resonator's specification because these component values depend on the resonator.

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1 (3.3V)	IOVDD	[Note 1]	−0.5		4.6	V
Supply Voltage 2 (1.8V)	DVDD18	[Note 1]	−0.5		2.5	V
	PLLVDD					
Input Voltage 1	V_{I1}	[Notes 1, 2] In the case of IOVDD≦0.9V	−0.3		IOVDD+4.6	V
		[Notes 1, 2] In the case of IOVDD› 0.9V	−0.3		5.5	V
Input Voltage 2	V_{I2}	[Notes 1, 3]	−0.3		4.1	V
Input Voltage 3	V_{I3}	[Notes 1, 4]	−0.3		IOVDD+0.3	V
Storage Temperature	T_{STG}		−40		150	°C

[Note 1] All ground pins are at 0V.
[Note 2] GPIO11-0 and IC_N pins.
[Note 3] SDA and SCL pins.
[Note 4] XIN pin.

5.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1 (3.3V)	IOVDD	[Note 1]	3.0	3.3	3.6	V
Supply Voltage 2 (1.8V)	DVDD18	[Note 1]	1.65	1.8	1.95	V
	PLLVDD					
Operating Ambient Temperature	T_a		−40	25	85	°C

[Note 1] All ground pins are at 0V.

5.3 Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption Normal Operation State		[Notes 1, 2]		102		mW
IOVDD current Normal Operation State		[Note 1]		8		mA
IOVDD current Power-down State		[Note 1]		2		μA
DVDD18+PLLVDD current Normal Operation State		[Note 1]		42		mA
DVDD18+PLLVDD current Power-down State		[Note 1]		0.057		mA

[Note 1] The typical and maximum values are those under typical and maximum recommended operating conditions. High level input voltage at input pins: IOVDD, Low level input voltage: DVSS.

[Note 2] DVSS=0V, IOVDD=3.0V to 3.6V, DVDD18=1.65V to 1.95V, Ta=-40°C to 85°C unless otherwise specified.

5.4 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage 1	V_{IH1}	[Note 1]	2.0		5.25	V
Low Level Input Voltage 1	V_{IL1}	[Note 1]			0.8	V
High Level Input Voltage 2	V_{IH2}	[Note 2]	0.7 × IOVDD			V
Low Level Input Voltage 2	V_{IL2}	[Note 2]			0.3 × IOVDD	V
High Level Output Voltage	V_{OH}	[Note 3]	2.4			V
Low Level Output Voltage 1	V_{OL1}	[Note 3]			0.4	V
Low Level Output Voltage 2	V_{OL2}	[Note 4]			0.4	V
Schmitt Width	I_{SH}	[Note 5]		0.05 × IOVDD		V
Input Leakage Current	I_I				±10	μA
Input Pin Capacitance	C_I			5		pF

[Note 1] GPIO11-0 and IC_N pins.

[Note 2] SDA, SCL, and XIN pins.

[Note 3] GPIO11-3 pin; however, I_{OH}= −1.0mA, I_{OL}=1.0mA.

[Note 4] SDA pin; however, I_{OL}=3.0mA.

[Note 5] SDA and SCL pins

5.5 AC Characteristics

The AC characteristic is measured under the following conditions:

Power supply pins (IOVDD, DVDD18 and PLLVDD): Min (Recommended Operating Conditions).

Input conditions: V_{IH} = 2.0 V, V_{IL} = 0.8 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-On Turn-Off Skew Time	t_{VSKEW}	[Notes 1, 2]	0		5	s
Power Supply Rise Time	t_{VRISE}		0		100	ms
Power Supply Shutdown Time	t_{VDDSD}		0			ms
XIN Clock Frequency	f_{XIN}			22.5792, 24.576		MHz
XIN Clock Duty Ratio	d_{XIN}		40		60	%
XIN Clock frequency deviation tolerance	–				0.15	%
Internal Clock Frequency	f_{DCLK}			$3 \times f_{XIN}$		–
IC_N Time 1	t_{IC1}	[Notes 3, 4]	10			ms
IC_N Time 2	t_{IC2}	IC_N= “L” [Note 4]	1			µs

[Note 1] Supply voltages of 3.3V and 1.8V must be subsequently turned on/off within five seconds. When only one supplys voltage, this device may get damaged.

[Note 2] The power supply sequencing of 1.8V and 3.3V is not defined.

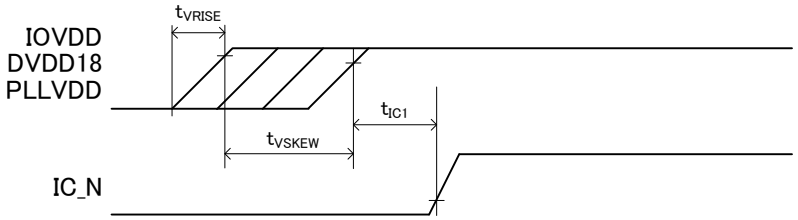
However this device can drive SDA pin when 3.3 V is powered and 1.8 V is not yet powered. When your design turns on 3.3 V before 1.8 V, check the specification and actual operations of I^2C master and slave devices to see if SDA signal being "L" during these periods is not a problem.

SCL/SDA must be pulled up during DVDD (3.3 V supply) ramps up or earlier.
Do not leave SCL/SDA pins open after DVDD (3.3 V supplies) is powered so that no intermediate voltage levels apply to these pins.

[Note 3] This specifies the time required after both 1.8 V and 3.3 V supplies are powered up. The on-chip crystal oscillator and PLL which uses the oscillator output must be up and running within this time.

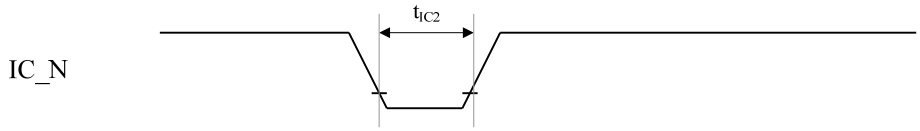
[Note 4] On-chip ROM programs need some initialization period described in *3.7.7 Device Control Examples* after hardware reset.

○ Turn-ON



・ Turn on power supplies while IC_N pin is at "L" level.

○ Normal Operation



・ XIN input and supply voltages need to be stabilized.

○ Turn-OFF

5.5.1 Host processor Interface

The AC characteristics of the host processor interface are measured under the following conditions:

Input Conditions V_{IH} = 0.80 × IOVDD, V_{IL} = 0.20 × IOVDD

Measurement Points V_{IH} = 0.70 × IOVDD, V_{IL} = 0.30 × IOVDD

V_{OH}= 0.70 × IOVDD, V_{OL}= 0.30 × IOVDD

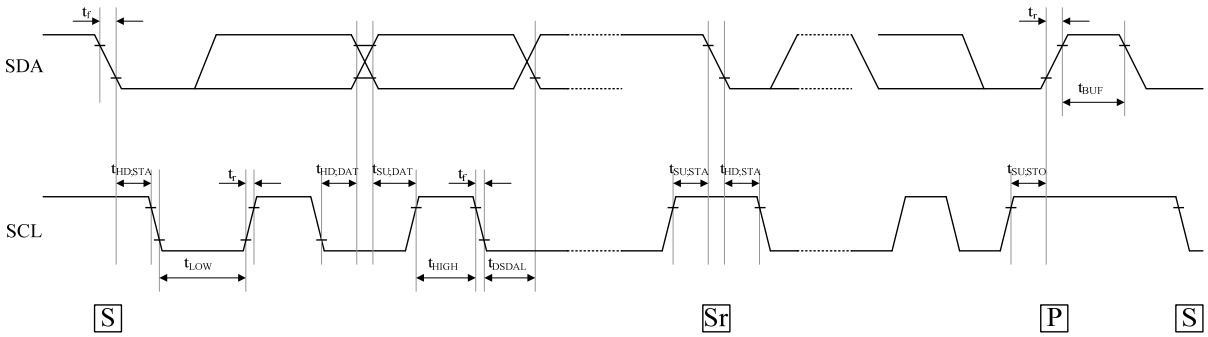
5.5.1.1 Input Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Input Clock Frequency	f_{SCL}		0		400	kHz
"START" Condition Hold Time	$t_{HD;STA}$		0.6			µs
SCL Input Clock "L" Period	t_{LOW}		1.3			µs
SCL Input Clock "H" Period	t_{HIGH}		0.6			µs
Repetitive "START" Condition Setup Time	$t_{SU;STA}$		0.6			µs
Data Input Hold Time	$t_{HD;DAT}$		0			µs
Data Input Setup Time	$t_{SU;DAT}$		100			ns
SDA,SCL Input Rise Time	t_r				300	ns
SDA,SCL Input Fall Time	t_f				300	ns
"STOP" Condition Setup Time	$t_{SU;STO}$		0.6			µs
Bus free time between "STOP" and "START" conditions	t_{BUF}		1.3			µs
Capacitance Load (for each Bus line)	C_b				400	pF

5.5.1.2 Output Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SDA "L" Output Delay Time	t_{DSDAL}				1.15	μs
Data Output Hold Time	$t_{HD;DAT}$		0		0.9	μs

[Note] Capacitor load=400pF, I_{OL}= +3.0mA under the recommended operating conditions.



"S": Start Condition, "Sr": Repetitive Start Condition, "P": Stop Condition

5.5.2 Audio Interface

The AC characteristics of the audio interface are measured under the following conditions:

Input Conditions V_{IH} = 2.4V, V_{IL} = 0.4V

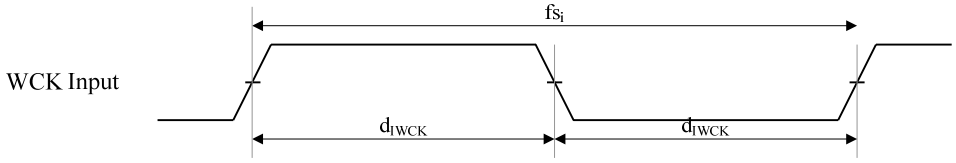
Measurement Points V_{IH} = 2.0V, V_{IL} = 0.8V

V_{OH}= 2.0V, V_{OL}= 0.8V

5.5.2.1 AIFMD[3:0] Register=0x0

5.5.2.1.1 Word Clock Input

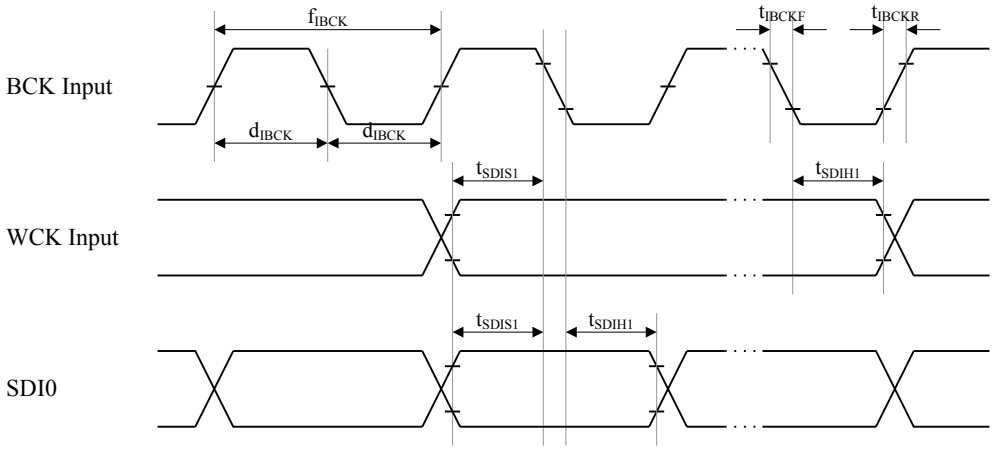
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
WCK Input Frequency	fs_i	f_{XIN}=22.5792MHz, 24.576MHz	8		192	kHz
WCK Input Duty Ratio	d_{IWCK}			50		%



5.5.2.1.2 Audio Input 1

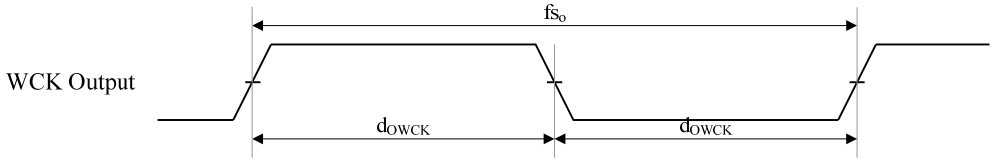
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BCK Input Frequency	f_{IBCK}			64 × fs_i		–
BCK Input Duty Ratio	d_{IBCK}			50		%
BCK Input Rise Time	t_{IBCKR}				15	ns
BCK Input Fall Time	t_{IBCKF}				15	ns
WCK Input, SDI0 Setup Time	t_{SDIS1}		10			ns
WCK Input, SDI0 Hold Time	t_{SDIH1}		10			ns

[Note] The polarity of BCK input signal can be changed with SDIBCKP register. The signal in diagram below is shown in polarity when SDIBCKP is set to 0x0.



5.5.2.1.3 Word Clock Output

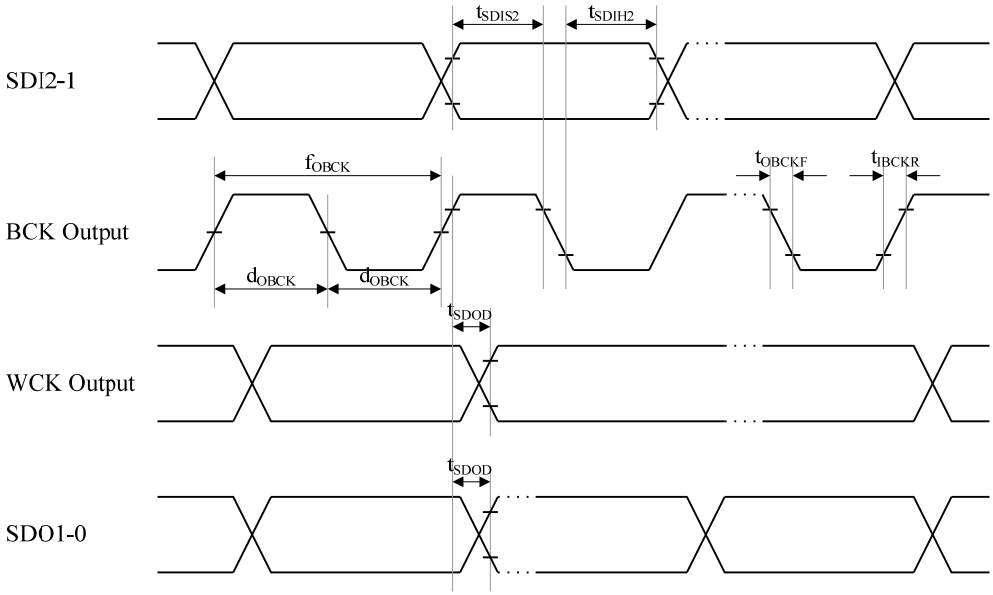
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
WCK Output Frequency	fs_o			44.1, 48		kHz
WCK Output Duty Ratio	d_{OWCK}			50		%



5.5.2.1.4 Audio Input 2 Audio Output

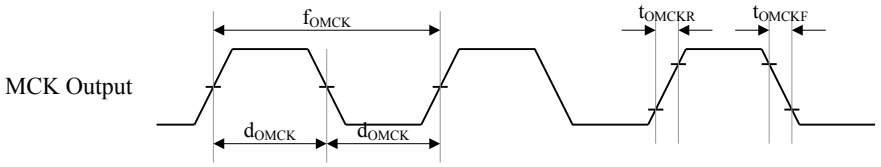
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SDI2-1 Setup Time	t_{SDIS2}		65			ns
SDI2-1 Hold Time	t_{SDIH2}		10			ns
BCK Output Frequency	f_{OBCK}			64 × fs_o		–
BCK Output Duty Ratio	d_{OBCK}			50		%
BCK Output Rise Time	t_{OBCKR}	C_L=20pF			15	ns
BCK Output Fall Time	t_{OBCKF}	C_L=20pF			15	ns
WCK, SDO1-0 Output Delay Time	t_{SDOD}	C_L=20pF	−45		45	ns

[Note] The polarity of the BCK output signal can be changed with the SDOBCKP register. The signal in diagram below is shown in polarity when SDIBCKP is set to 0x0.



5.5.2.1.5 Master Clock Output

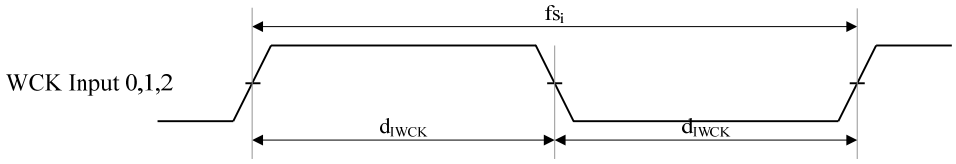
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MCK Output Frequency	f_{OMCK}			256 × fs_o		–
MCK Output Duty Ratio	d_{OMCK}			50		%
MCK Output Rise Time	t_{OMCKR}	C_L=20pF			10	ns
MCK Output Fall Time	t_{OMCKF}	C_L=20pF			10	ns



5.5.2.2 AIFMD[3:0] Register=0x1,0x2,0x3

5.5.2.2.1 Word Clock Input

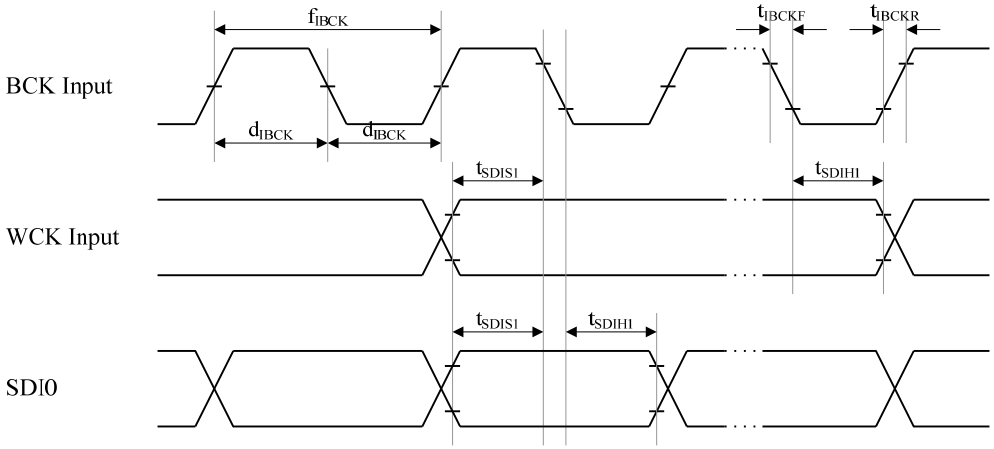
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
WCK Input 0, 1, 2 Frequency	fs_i	f_{XIN}=22.5792MHz, 24.576MHz	8		192	kHz
WCK Input 0, 1, 2 Duty Ratio	d_{IWCK}			50		%



5.5.2.2.2 Audio Input

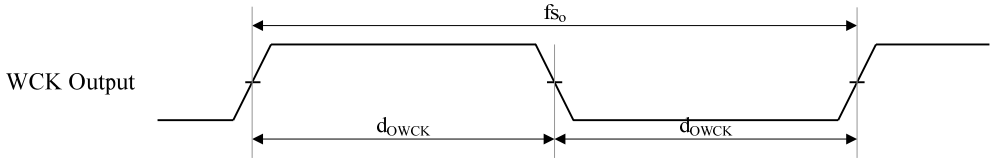
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BCK Input 0, 1, 2 Frequency	f_{IBCK}			64 × fs_i		–
BCK Input 0, 1, 2 Duty Ratio	d_{IBCK}			50		%
BCK Input 0, 1, 2 Rise Time	t_{IBCKR}				15	ns
BCK Input 0, 1, 2 Fall Time	t_{IBCKF}				15	ns
WCK Input 0, 1, 2, SDI0, 1, 2 Setup Time	t_{SDIS1}		10			ns
WCK Input 0, 1, 2, SDI0, 1, 2 Hold Time	t_{SDIH1}		10			ns

[Note] The polarity of the BCK input signal can be changed with the SDIBCKP register. The signal in diagram below is shown in polarity when SDIBCKP is set to 0x0.



5.5.2.2.3 Word Clock Output

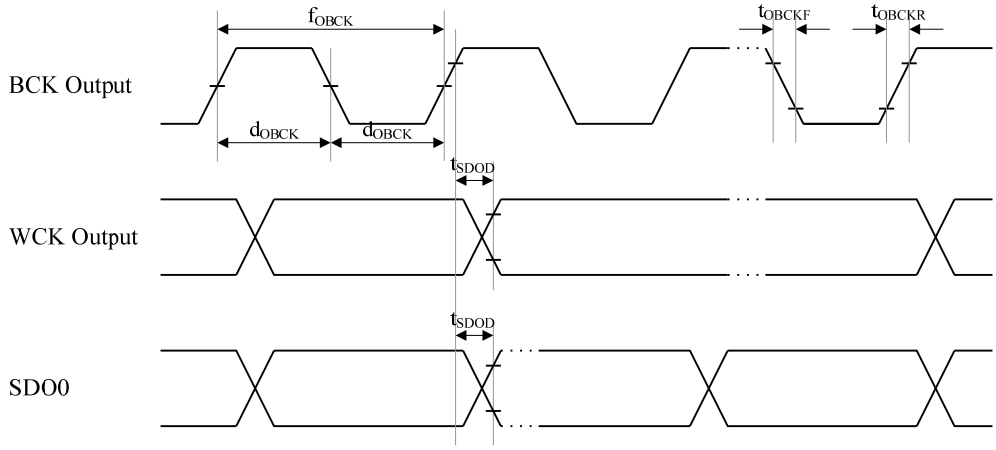
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
WCK Output Frequency	fs_o			44.1, 48		kHz
WCK Output Duty Ratio	d_{OWCK}			50		%



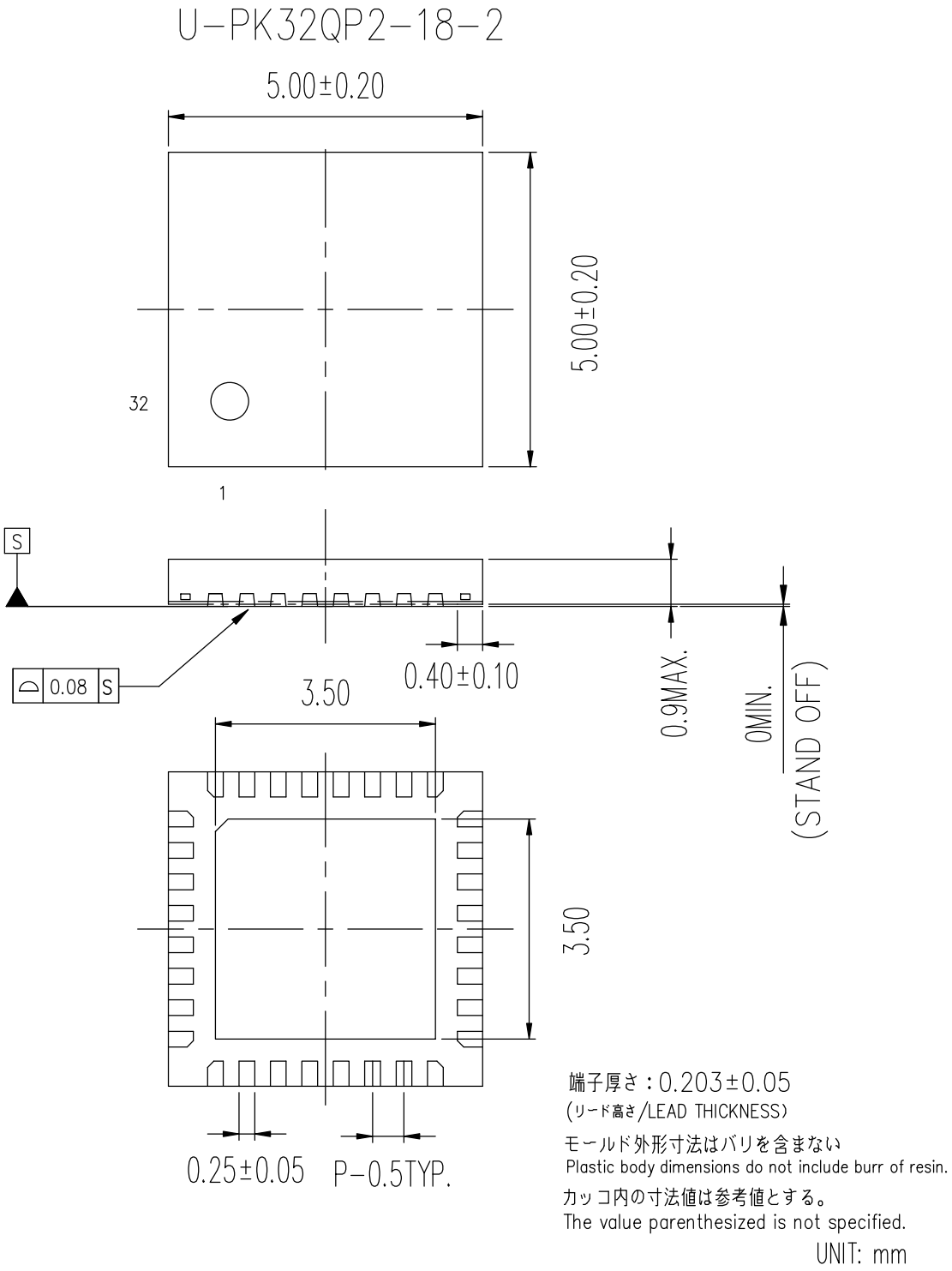
5.5.2.2.4 Audio Output

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BCK Output Frequency	f_{OBCK}			64 × fs_o		–
BCK Output Duty Ratio	d_{OBCK}			50		%
BCK Output Rise Time	t_{OBCKR}	C_L=20pF			15	ns
BCK Output Fall Time	t_{OBCKF}	C_L=20pF			15	ns
WCK Output, SDO0 Delay Time	t_{SDOD}	C_L=20pF	−45		45	ns

[Note] The polarity of the BCK output signal can be changed with the SDOBCKP register. The signal in diagram below is shown in polarity when SDIBCKP is set to 0x0.



6 Package Information



注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

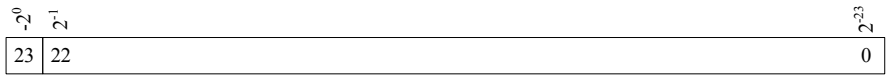
Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

7 Appendix

7.1DATA FORMATS

7.1.1 24-bit fixed-point format

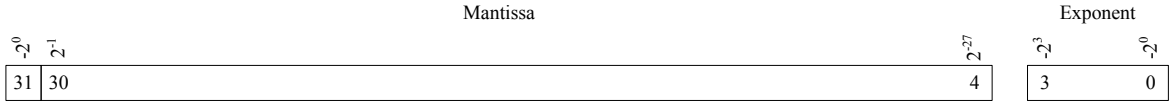
This data format is used for SDSP.



Value	Hexadecimal	Decimal
Maximum positive value	0x7FFFFF	+0.9999998808
+0.5	0x400000	+0.5
Minimum positive value	0x000001	+1.1920928955E-07
Zero	0x000000	0
Minimum negative value	0xFFFFFF	−1.1920928955E-07
−0.5	0xC00000	−0.5
Maximum negative value	0x800000	−1

7.1.2 32-bit floating-point format

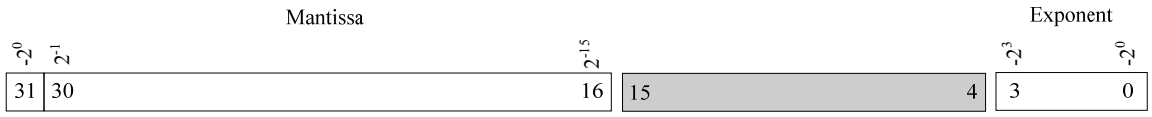
This data format is used for MDSP2.



Value	Hexadecimal	Decimal
Maximum positive value	0x7FFFFFF0	+0.9999999926
+0.5	0x40000000	+0.5
Minimum positive value	0x0000001F	+2.2737367544E-13
Zero	0x0000000F	0
Minimum negative value	0xFFFFFFFF	−2.2737367544E-13
−0.5	0xC0000000	−0.5
Maximum negative value	0x80000000	−1

7.1.3 20-bit floating-point format

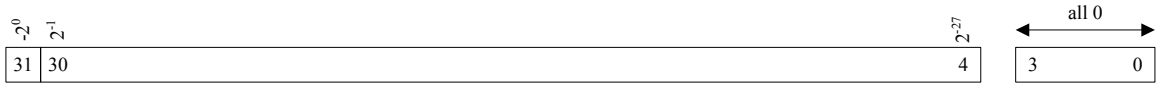
This data format is used for MDSP2.



Value	Hexadecimal	Decimal
Maximum positive value	0x7FFF0000	+0.9999694824
+0.5	0x40000000	+0.5
Minimum positive value	0x0001000F	+9.313225E-10
Zero	0x00000000	0
Minimum negative value	0xFFFF000F	−9.313225E-10
−0.5	0xC0000000	−0.5
Maximum negative value	0x80000000	−1

7.1.4 28-bit fixed-point format

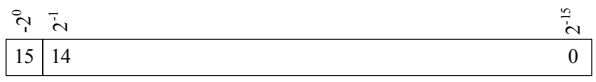
This data format is used for MDSP2.



Value	Hexadecimal	Decimal
Maximum positive value	0x7FFFFFF0	+0.9999999926
+0.5	0x40000000	+0.5
Minimum positive value	0x00000010	+7.4505805969E-09
Zero	0x00000000	0
Minimum negative value	0xFFFFFFF0	−7.4505805969E-09
−0.5	0xC0000000	−0.5
Maximum negative value	0x80000000	−1

7.1.5 16-bit fixed-point format

This data format is used for MDSP2.



Value	Hexadecimal	Decimal
Maximum positive value	0x7FFF	+0.9999694824
+0.5	0x4000	+0.5
Minimum positive value	0x0001	+3.0517578125E-05
Zero	0x0000	0
Minimum negative value	0xFFFF	−3.0517578125E-05
−0.5	0xC000	−0.5
Maximum negative value	0x8000	−1

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

YAMAHA CORPORATION

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