



2. General Description

B116XTN04.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B116XTN04.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.8			
Active Area	[mm]	256.125 X 144.0			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1875 x 0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m ²]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.65 max. (Include Logic and BLU power)			
Weight	[Grams]	235 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	277.5	278.0	278.5
		Width	167.5	168.0	168.5
		Thickness	-	-	3.6
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		262K colors (RGB 6-bit)			



Product Specification

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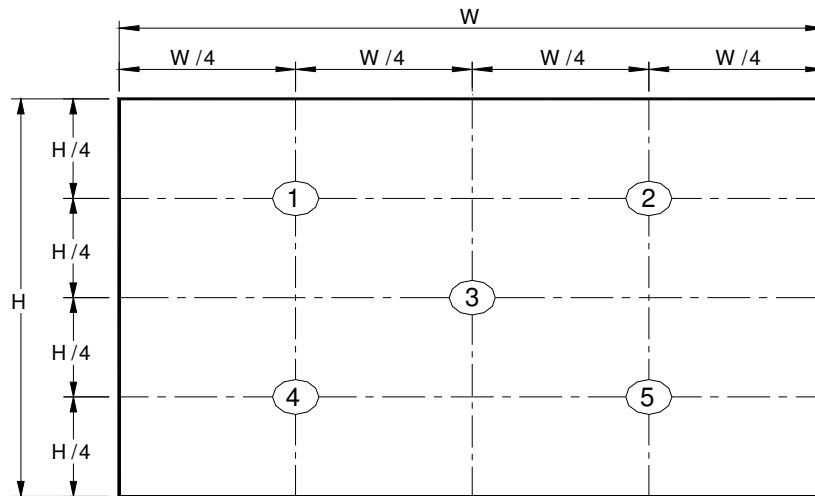
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

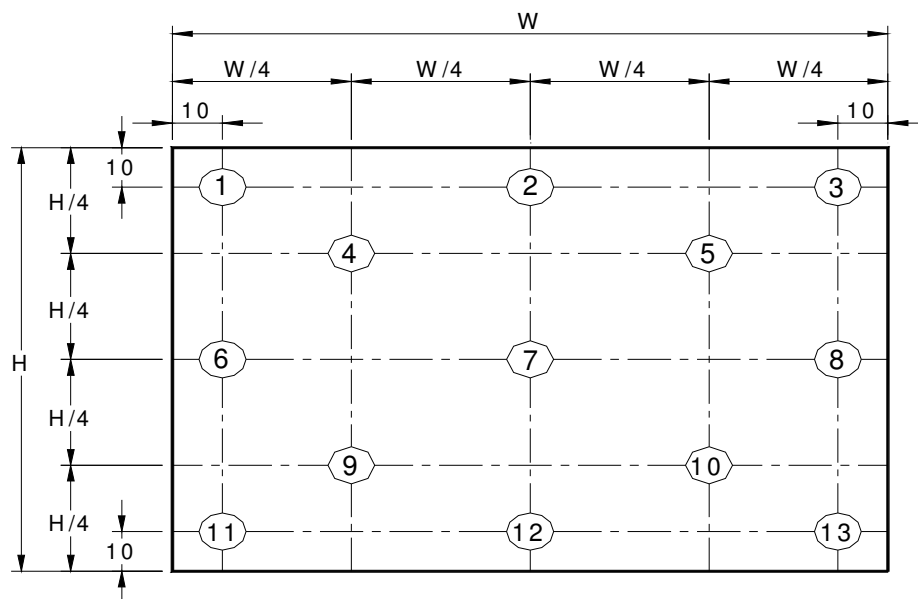
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED=20mA}$		5 points average	170	200	-	cd/m ²	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9
	θ_L		40	45	-		
	ϕ_H	Vertical (Upper) CR = 10 (Lower)	10	15	-		
	ϕ_L		30	35	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		300	400	-		4, 6
Cross talk	%				4		4, 7
Response Time	T_{RT}	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coordinates	Red	Rx	CIE 1931	0.550	0.580	0.610	4
		Ry		0.315	0.345	0.375	
	Green	Gx		0.295	0.325	0.355	
		Gy		0.520	0.550	0.580	
	Blue	Bx		0.125	0.155	0.185	
		By		0.110	0.140	0.170	
	White	Wx		0.283	0.313	0.343	
		Wy		0.299	0.329	0.359	
	NTSC	%			-	45	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

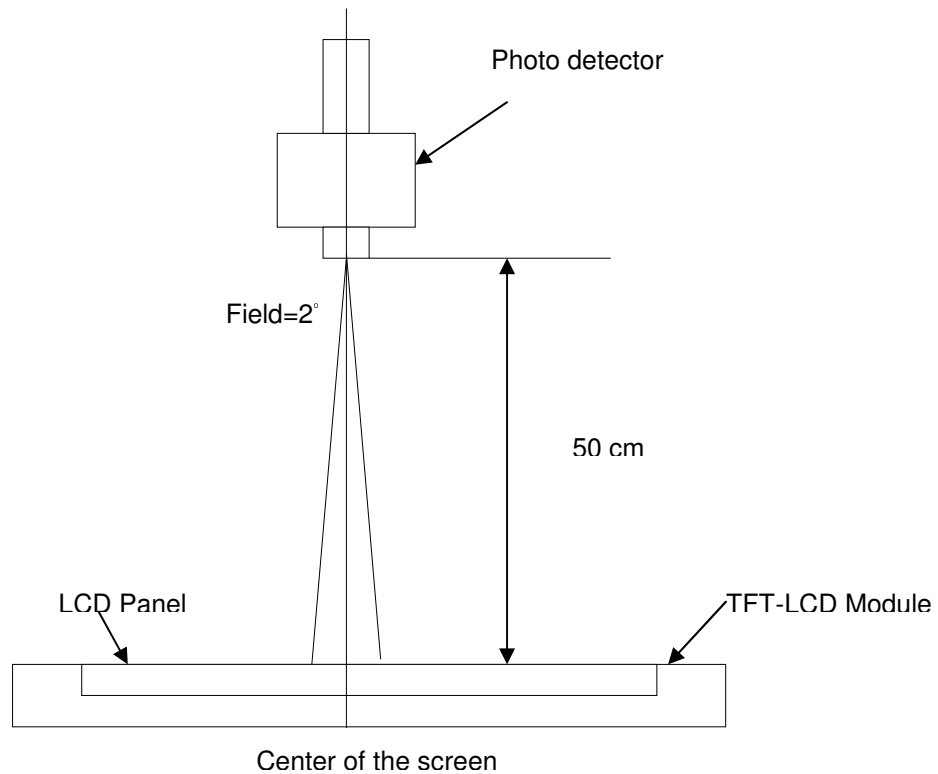
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, measurement should be executed in the center of

screen unless otherwise noted.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

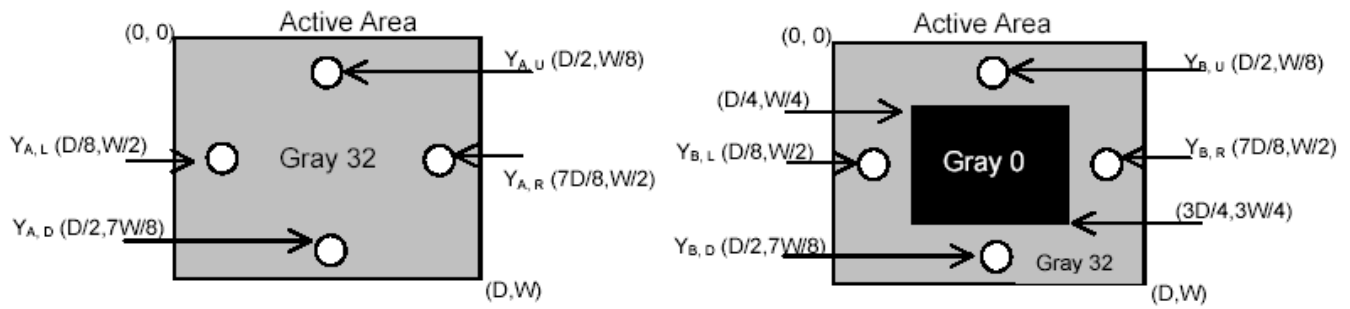
Note 7 : Definition of Cross Talk (CT)

$$\text{CT} = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

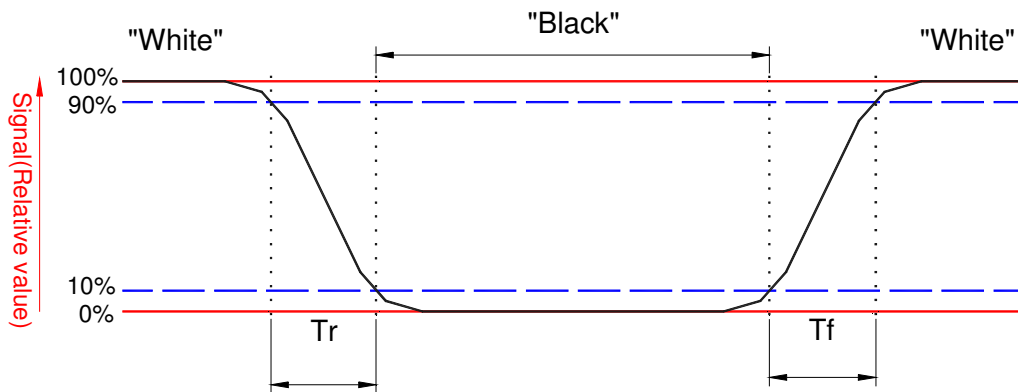
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



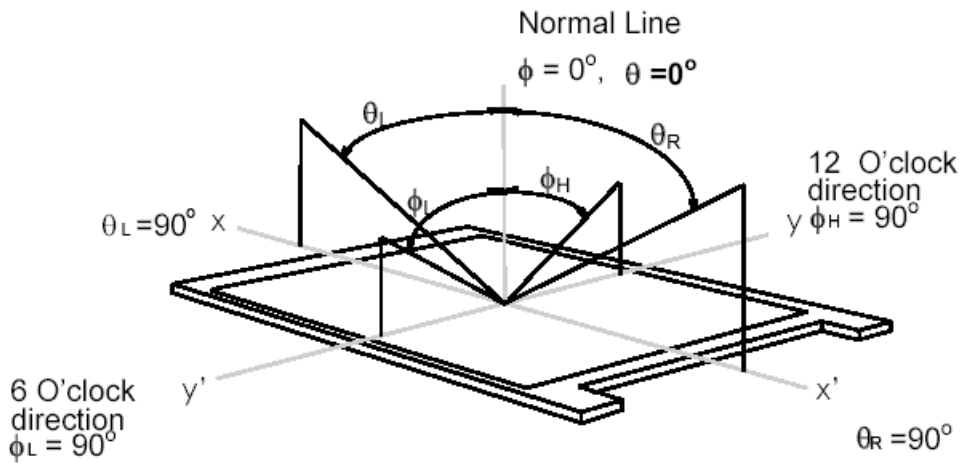
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time is interval between the 10% and 90% of amplitudes. Refer to figure as below.



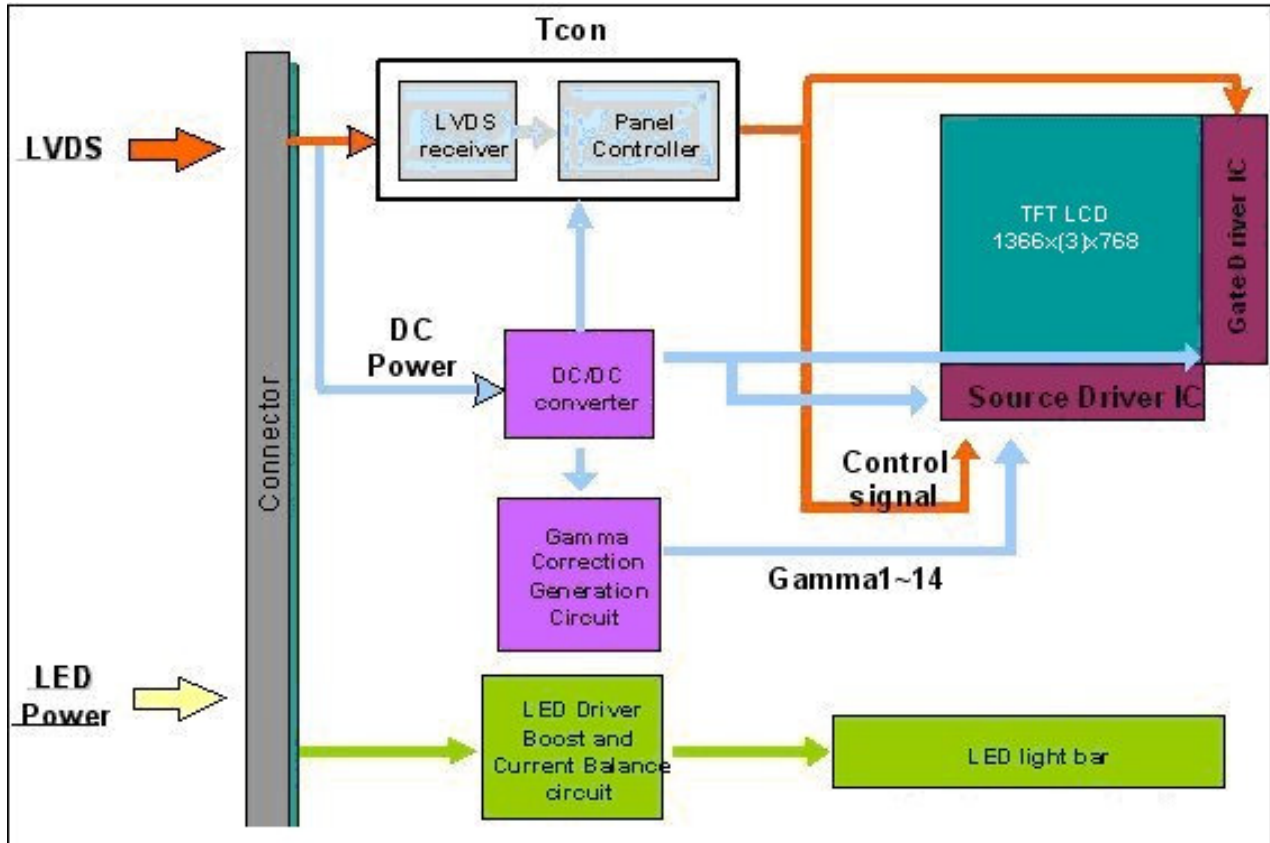
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (ϕ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

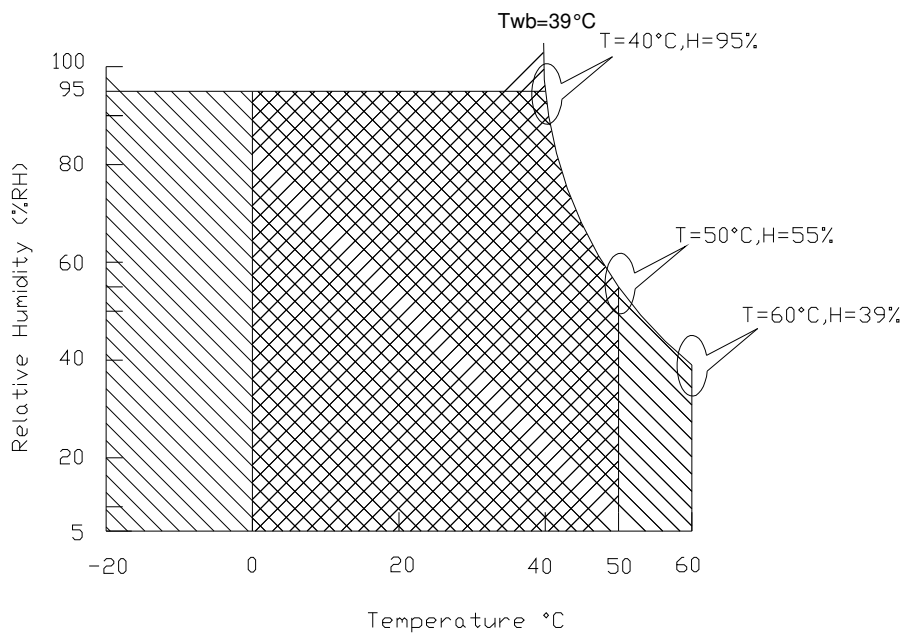
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

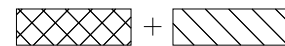
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range



5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

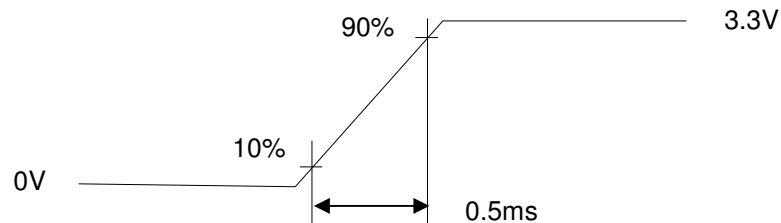
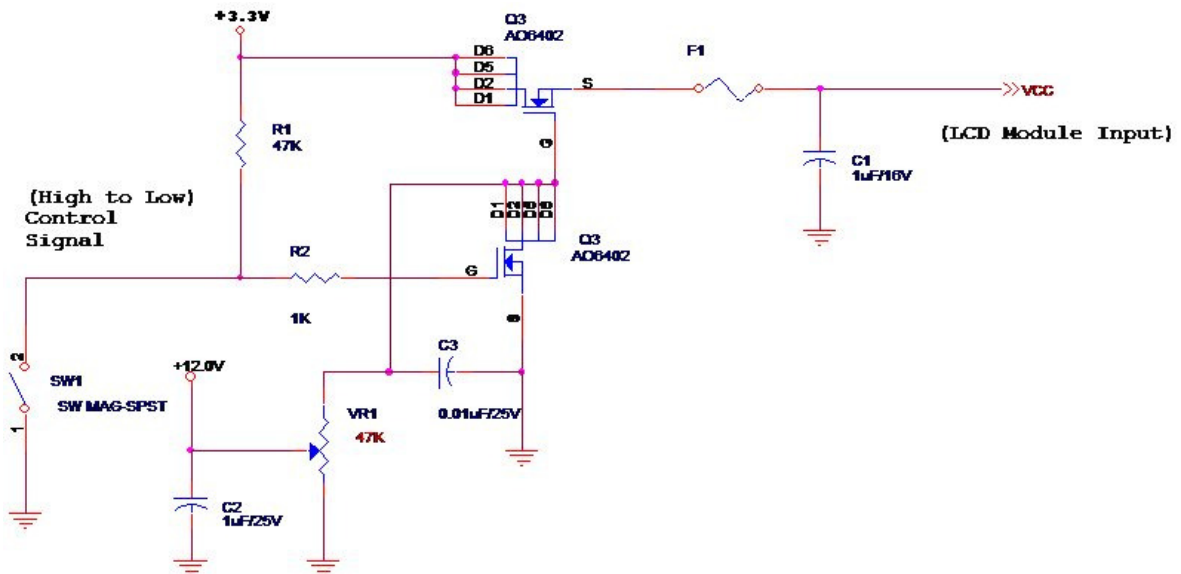
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max} = V_{3.3} \times I_{black}$)

Note 2 : Measure Condition



Vin rising time

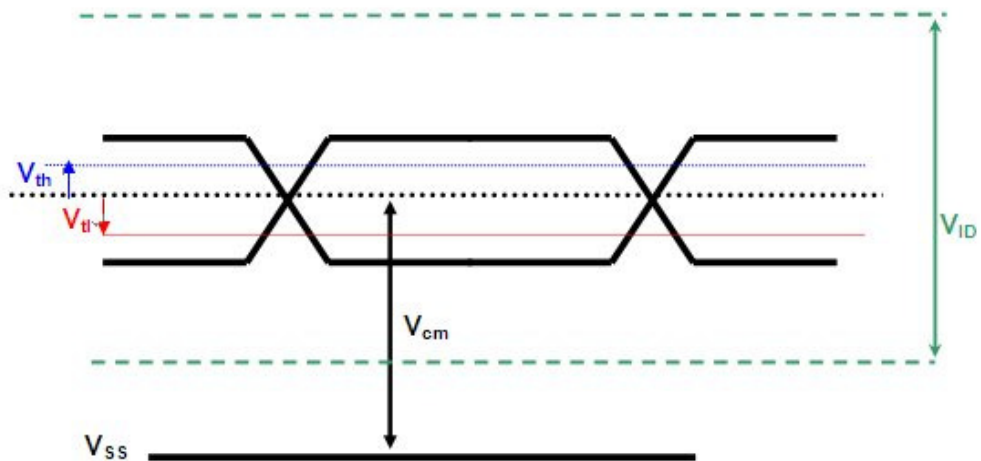
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold ($V_{cm}=+1.2V$)		100	[mV]
V_{tl}	Differential Input Low Threshold ($V_{cm}=+1.2V$)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.9	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 IF=20 mA

Note 1: Calculator value for reference $P_{LED} = VF$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency, and PLED include driving circuit loss.

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.0	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.0	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	180	1K	10K	Hz	
PWM Duty Ratio	Duty	1	--	100	%	

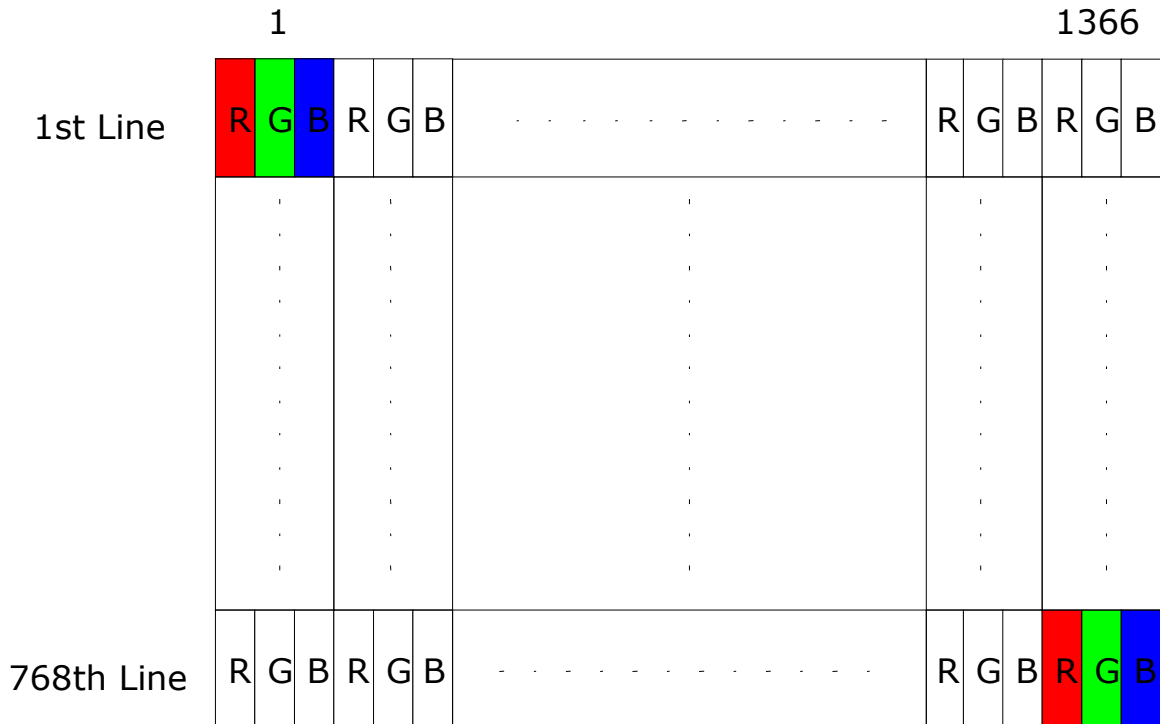
Note 1: Recommend system pull up/down resistor no bigger than 10kohm

Note 2: Minimum PWM Duty Ratio (Duty) is 1%, when FPWM is low Hz er than 5KHz. Otherwise, minimum PWM duty ratio (duty) is limited to 5%

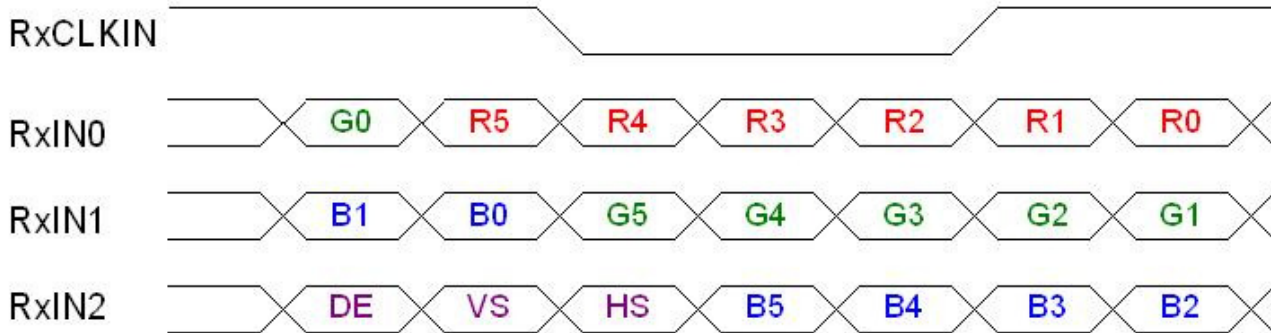
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

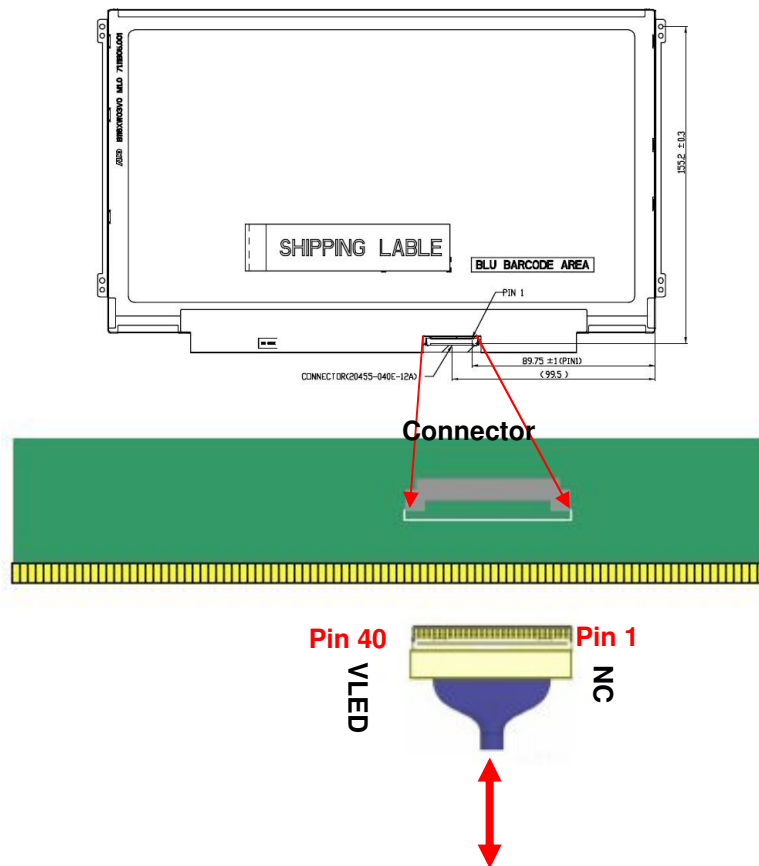
Connector Name / Designation	For Signal Connector
Manufacturer	STM or compatible
Type / Part Number	STM MSAK24025P40 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VEDID	EDID 3.3V Power
5	BIST	Panel self test
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	RxOIN0-	-LVDS Differential Data INPUT(Odd R0-R5,G0)
9	RxOIN0+	+LVDS Differential Data INPUT(Odd R0-R5,G0)
10	VSS	Ground
11	RxOIN1-	-LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
12	RxOIN1+	+LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
13	VSS	Ground
14	RxOIN2-	-LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
15	RxOIN2+	+LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
16	VSS	Ground
17	RxOCKIN-	-LVDS Odd Differential Clock INPUT
18	RxOCKIN+	+LVDS Odd Differential Clock INPUT
19	NC	No connection (Disable)
20	NC	No connection
21	NC	No connection
22	VSS	Ground

23	NC	No connection
24	NC	No connection
25	VSS	Ground
26	NC	No connection
27	NC	No connection
28	VSS	Ground
29	NC	No connection
30	NC	No connection
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_IN	PWM logic input level
36	VLED_EN	LED enable input level
37	DCR_EN	DCR function enable
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

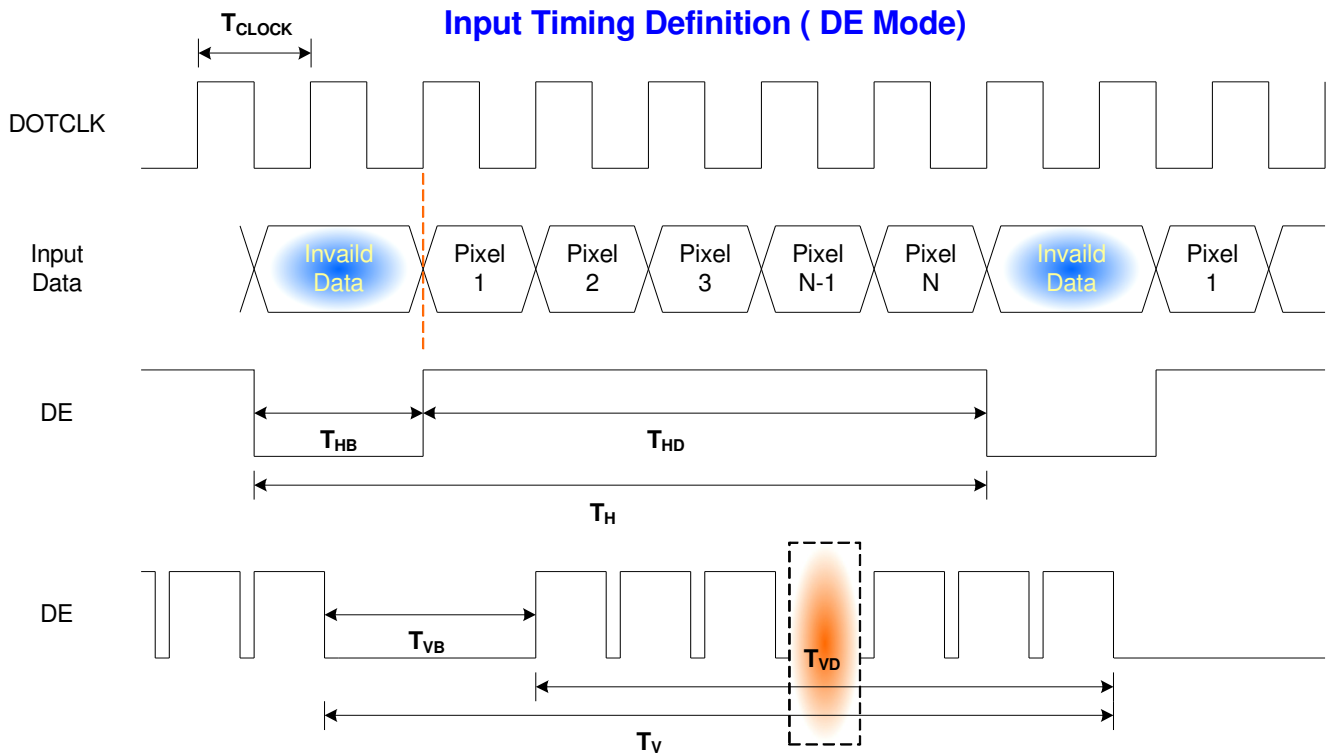
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	40	60	-	Hz	
Clock frequency	$1/T_{Clock}$	65	70.5	80	MHz	
Vertical Section	Period	T_V	776	793	1000	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	8	25	180	
Horizontal Section	Period	T_H	1396	1456	2000	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	30	90	634	

Note1: The above is as optimized setting

Note2: DE mode only

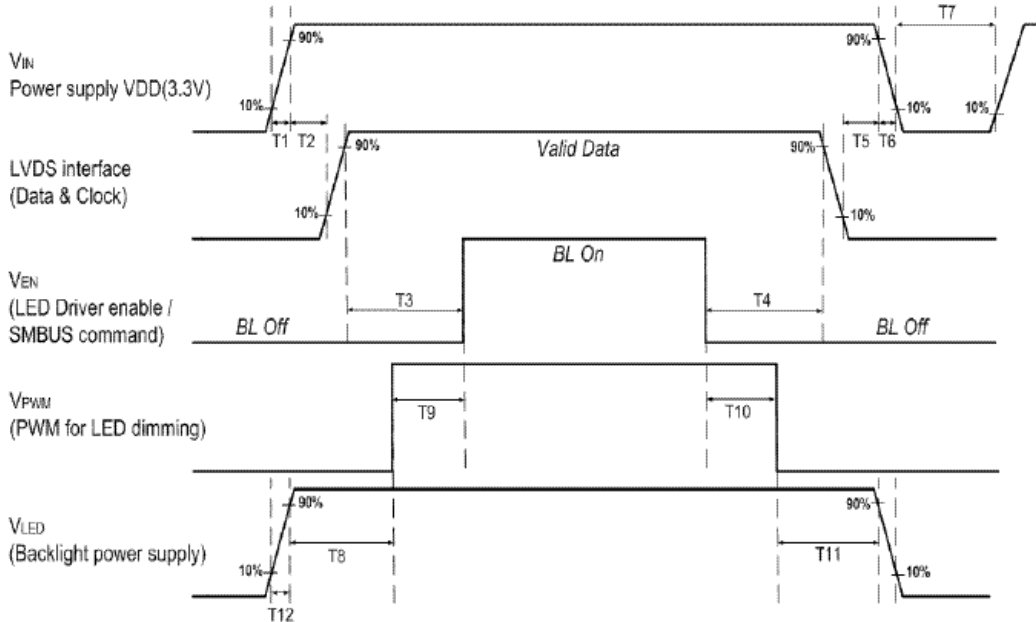
The maximum clock frequency = $(1366+B)*(768+A)*60 < 80\text{MHz}$

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

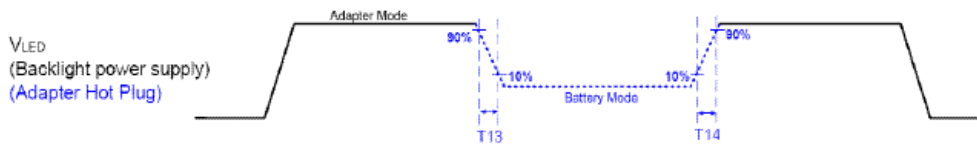


	Min (ms)	Max (ms)
T1	0.5	10
T2	0	50
T3	200	-
T4	200	-
T5	0	50
T6	0	10
T7	500	-
T8	10	-
T9	10	-
T10	10	-
T11	10	-
T12	0.5	10
T13	1*	-
T14	1*	-

Seamless change: $T_{13}/T_{14} = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/\text{PWM Frequency}$

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



Note 1 : If T₃<200ms, the display garbage may occur. (T₃>200ms is recommended)

Note 2 : If T₁ or T₁₂<0.5ms, the inrush current may cause the damage of fuse. If T₁ or T₁₂<0.5ms, the inrush current I²t is under typical melt of fuse Spec, there is no mentioned problem.

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

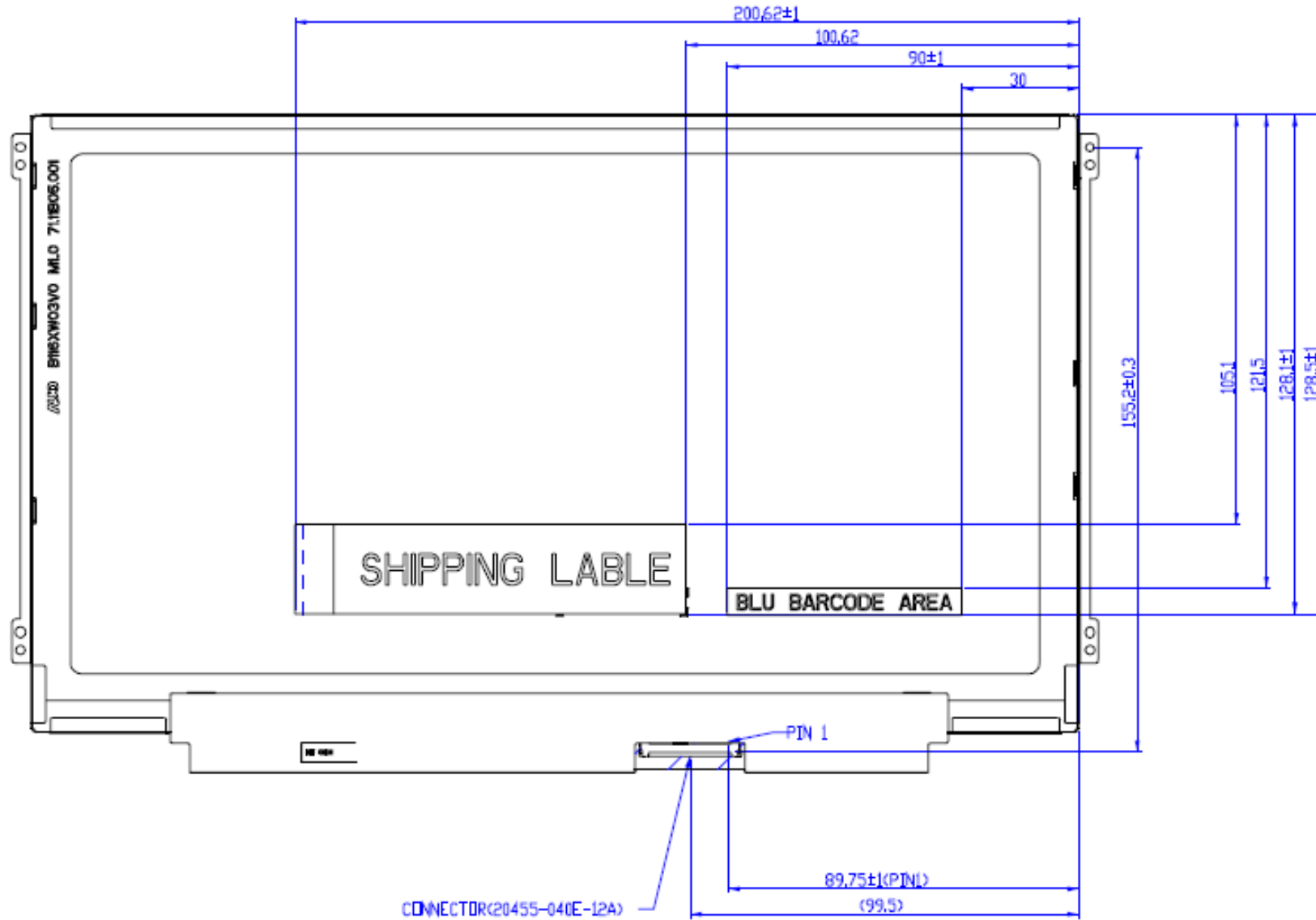
- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

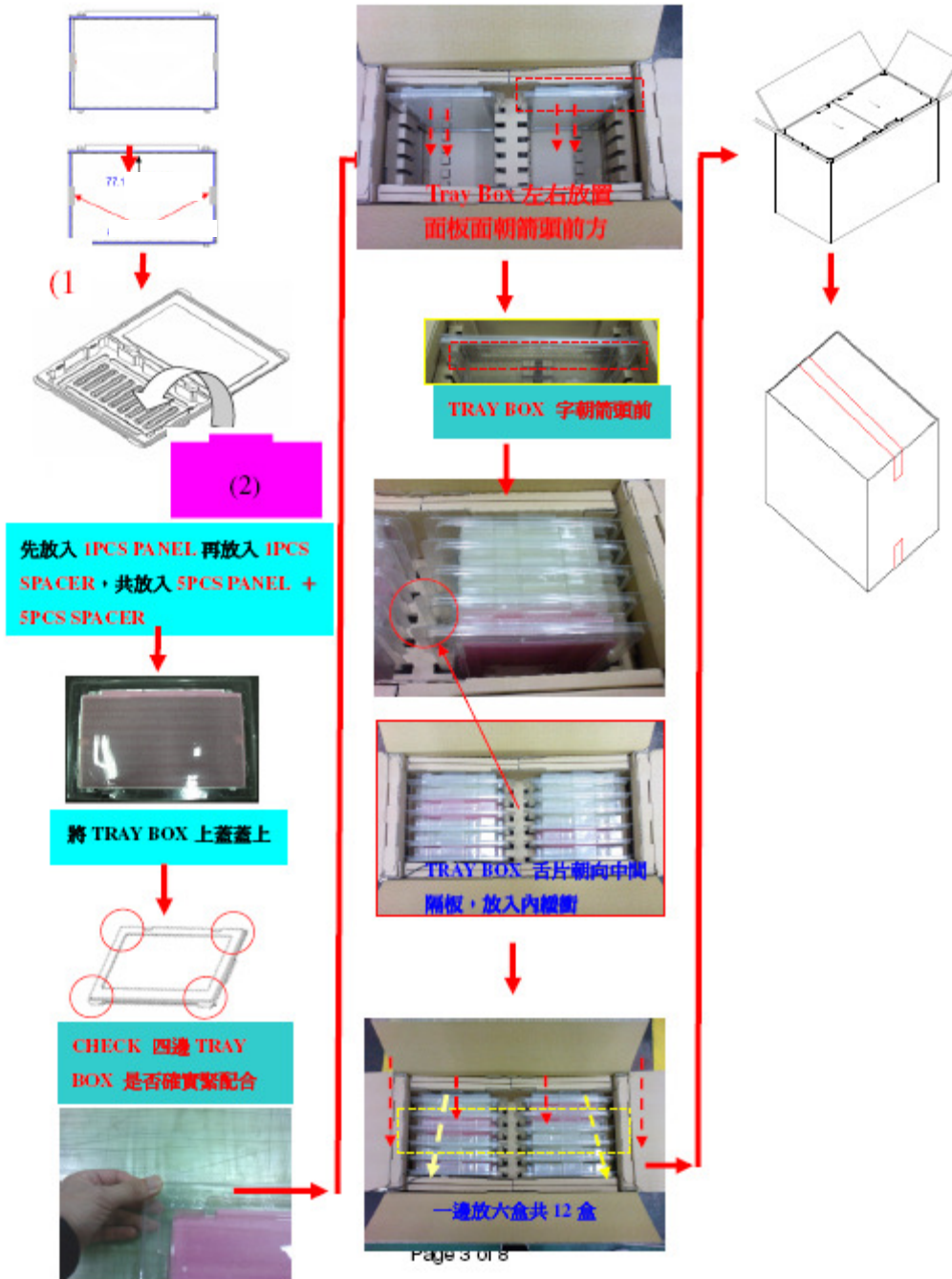
9.1 Shipping Label Format

[Z30]

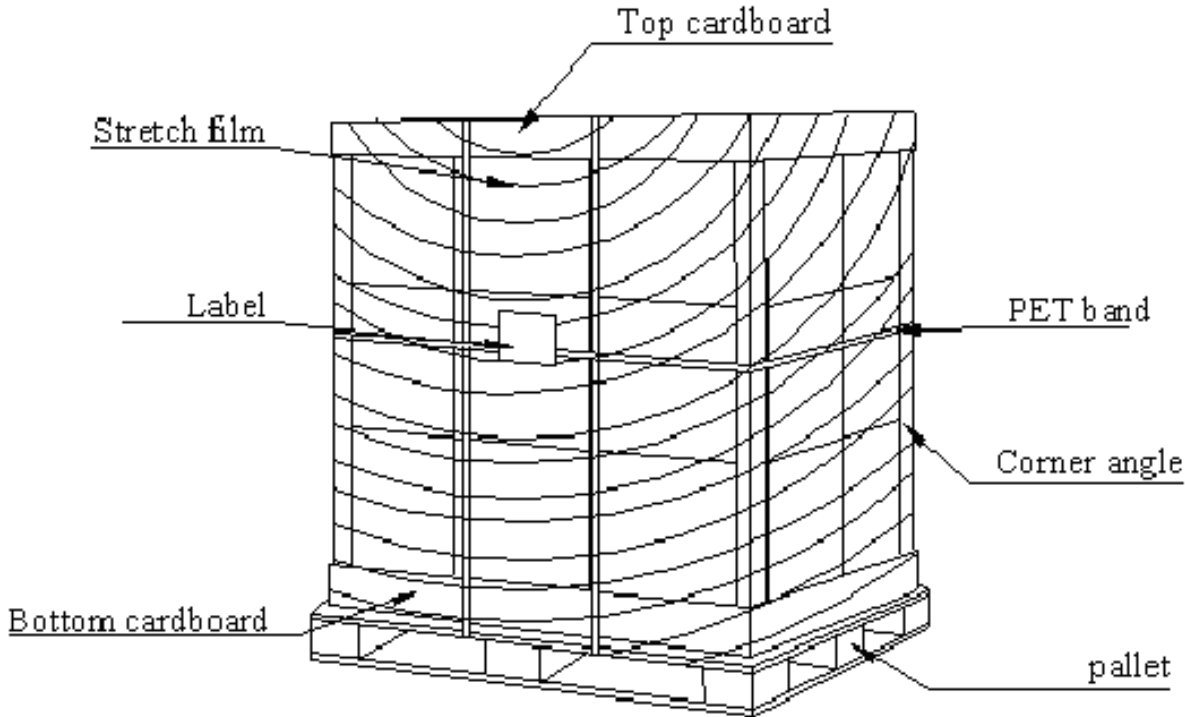
	Manufactured YY/WW Model No: B116XTN04.0 AU Optronics Made in China (Z30)	
*XXXXXXXXXXXX-XXXXXX		
	H/W: 1A F/W:2	
B116XTN04.0		

9.2 Carton Package

The outside dimension of carton is 553(L)mm* 275(W)mm* 379(H)mm



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

	Byte	Field Name and Comments	Value	Value	Value
	(hex)		(hex)	(binary)	(DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	5C	01011100	92
	0B	Panel Supplier Reserved – Product Code	40	01000000	64
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	10	Week of manufacture	00	00000000	0



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	11	Year of manufacture	17	00010111	23
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 4	04	00000100	4
Display Parameters	14	Video I/P definition	90	10010000	144
	15	Max H image size = 25.6 cm(Rounded to cm)	1A	00011010	26
	16	Max V image size = 14.4 cm(Rounded to cm)	0E	00001110	14
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support	02	00000010	2
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	99	10011001	153
	1A	Blue/White Low bit (BxBw/WxWy)	85	10000101	133
	1B	Red X Rx = 0.584	95	10010101	149
	1C	Red Y Ry = 0.333	55	01010101	85
	1D	Green X Rx = 0.338	56	01010110	86
	1E	Green Y Ry = 0.571	92	10010010	146
	1F	Blue X Rx = 0.158	28	00101000	40
	20	Blue Y Ry = 0.133	22	00100010	34
	21	White X Rx = 0.313	50	01010000	80
	22	White Y Ry = 0.329	54	01010100	84
Established Timings	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer's timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descriptor #1	36	Pixel Clock/10,000 (LSB)	70	01110000	112
	37	Pixel Clock/10,000 (MSB)	1C	00011100	28
	38	Horizontal Active = 1366 pixels (lower 8 bits)	56	01010110	86



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	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	A2	10100010	162	
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80	
	3B	Vertical Active = 768 lines	00	00000000	0	
	3C	Vertical Blanking (Tvbp) = 25 lines (DE Blanking typ. for DE only panels)	19	00011001	25	
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48	
	3E	Horizontal Sync, Offset (Thfp) = 48 pixels	30	00110000	48	
	3F	Horizontal Sync, Pulse Width = 32 pixels	20	00100000	32	
	40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 6 lines	36	00110110	54	
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
	42	Horizontal Image Size = 256 mm	00	00000000	0	
	43	Vertical image Size = 144 mm	90	10010000	144	
	44	Horizontal Image Size / Vertical image size	10	00010000	16	
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0	
	Timing Descriptor #2 (=Timing Descriptor #1)	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
		48	Pixel Clock/10,000 (LSB)	20	00100000	32
49		Pixel Clock/10,000 (MSB)	17	00010111	23	
4A		Horizontal Active = 1366 pixels (lower 8 bits)	56	01010110	86	
4B		Horizontal Blanking (Thbp) = 188 pixels (lower 8 bits)	BC	10111100	188	
4C		Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80	
4D		Vertical Active = 768 lines	00	00000000	0	
4E		Vertical Blanking (Tvbp) = 25 lines (DE Blanking typ. for DE only panels)	19	00011001	25	
4F		Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48	
50		Horizontal Sync, Offset (Thfp) = 48 pixels	30	00110000	48	
51		Horizontal Sync, Pulse Width = 32 pixels	20	00100000	32	
52		Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 6 lines	36	00110110	54	
53		Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
54		Horizontal Image Size = 256 mm	00	00000000	0	
55		Vertical image Size = 144 mm	90	10010000	144	
56		Horizontal Image Size / Vertical image size	10	00010000	16	
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0		
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0		



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		Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A			
	59		1A	00011010	26
Timing Descriptor #3 Dell specific information	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1 st Character	30	00110000	48
	60	Dell P/N 2 nd Character	4D	01001101	77
	61	Dell P/N 3 rd Character	4D	01001101	77
	62	Dell P/N 4 th Character	57	01010111	87
	63	Dell P/N 5 th Character	4E	01001110	78
	64	EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	31	00110001	49
	68	Manufacturer P/N	36	00110110	54
	69	Manufacturer P/N	58	01011000	88
6A	Manufacturer P/N	54	01010100	84	
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78	
Timing Descriptor #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
	70	Flag	00	00000000	0
	71	Color Management	00	00000000	0
	72	Panel Structure	41	01000001	65
	73	Frame Rate	02	00000010	2
	74	Light Controller Interface and Luminance	97	10010111	151
	75	Outdoor Features	00	00000000	0
	76	Multi-Media Features	10	00010000	16
	77	Multi-Media Features	00	00000000	0
78	Special Features #1	00	00000000	0	



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	79	Special Features #2	01	00000001	1
	7A	Special Features #3	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	03	00000011	3