SLSV4T244

4-Bit Dual-Supply Non-Inverting Level Translator

The SLSV4T244 is a 4−bit configurable dual−supply voltage level translator. The input A_n and output B_n ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low−voltage translation from the input A_n to the output B_n port.

Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 4.5 V
- High−Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non−preferential V_{CCA} and V_{CCB} Sequencing
- Outputs at 3−State until Active V_{CC} is Reached
- Power−Off Protection
- Outputs Switch to 3−State with V_{CCB} at GND
- Ultra−Small Packaging: 1.7 mm x 2.0 mm UQFN12
- These are Pb−Free Devices

Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

Important Information

- ESD Protection for All Pins:
  HBM (Human Body Model) > 1500 V

ON Semiconductor®

MARKING DIAGRAMS

UQFN12
MU SUFFIX
CASE 523AE

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URM■
○   ■

UR = Specific Device Code
M = Date Code
■ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping[†]
SLSV4T244MUTAG	UQFN12 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
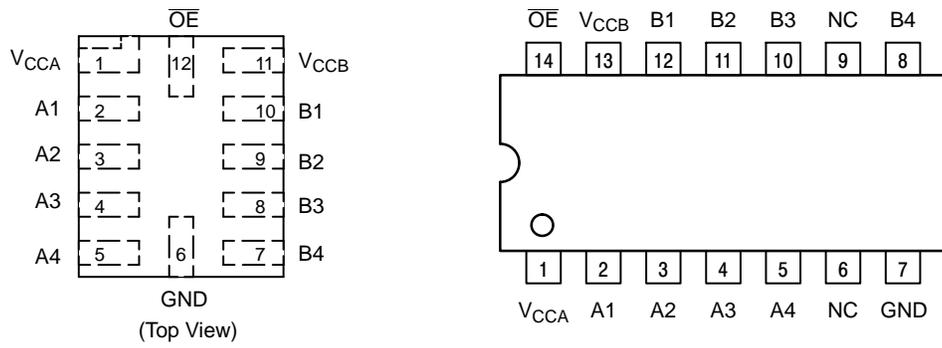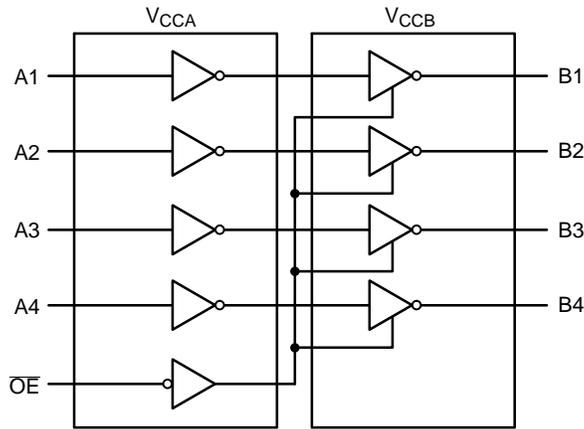
SLSV4T244

Figure 1. Pin Assignments

Figure 2. Logic Diagram

PIN ASSIGNMENT

PIN	FUNCTION
V_{CCA}	Input Port DC Power Supply
V_{CCB}	Output Port DC Power Supply
GND	Ground
A_n	Input Port
B_n	Output Port
$\overline{OE}$	Output Enable

TRUTH TABLE

Inputs		Outputs
$\overline{OE}$	A_n	B_n
L	L	L
L	H	H
H	X	3–State

SLSV4T244

MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +5.5		V
V_I	DC Input Voltage	A_n	−0.5 to +5.5		V
V_C	Control Input	$\overline{OE}$	−0.5 to +5.5		V
V_O	DC Output Voltage (Power Down)	B_n	−0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode)	B_n	−0.5 to +5.5		V
	(Tri−State Mode)	B_n	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current		−20	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current		−50	$V_O <$ GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CCA}, I_{CCB}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	4.5	V
V_I	Bus Input Voltage		GND	4.5	V
V_C	Control Input	$\overline{OE}$	GND	4.5	V
V_{IO}	Bus Output Voltage (Power Down Mode)	B_n	GND	4.5	V
	(Active Mode)	B_n	GND	V_{CCB}	V
	(Tri−State Mode)	B_n	GND	4.5	V
T_A	Operating Temperature Range		−40	+85	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate V_I, from 30% to 70% of V_{CC}; $V_{CC} = 3.3$ V ±0.3 V		0	10	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	−40°C to +85°C		Unit
					Min	Max	
V_{IH}	Input HIGH Voltage (An, $\overline{OE}$)		3.6 – 4.5	0.9 – 4.5	2.2	–	V
			2.7 – 3.6		2.0	–	
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 * V_{CCA}	–	
			0.9 – 1.4		0.9 * V_{CCA}	–	
V_{IL}	Input LOW Voltage (An, $\overline{OE}$)		3.6 – 4.5	0.9 – 4.5	–	0.8	V
			2.7 – 3.6		–	0.8	
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 * V_{CCA}	
			0.9 – 1.4		–	0.1 * V_{CCA}	
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA; $V_I = V_{IH}$	0.9 – 4.5	0.9 – 4.5	V_{CCB} − 0.2	–	V
		I_{OH} = −0.5 mA; $V_I = V_{IH}$	0.9	0.9	0.75 * V_{CCB}	–	
		I_{OH} = −2 mA; $V_I = V_{IH}$	1.4	1.4	1.05	–	
		I_{OH} = −6 mA; $V_I = V_{IH}$	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I_{OH} = −12 mA; $V_I = V_{IH}$	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I_{OH} = −18 mA; $V_I = V_{IH}$	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
		I_{OH} = −24 mA; $V_I = V_{IH}$	3.0	3.0	2.2	–	
V_{OL}	Output LOW Voltage	I_{OL} = 100 μA; $V_I = V_{IL}$	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I_{OL} = 0.5 mA; $V_I = V_{IL}$	1.1	1.1	–	0.3	
		I_{OL} = 2 mA; $V_I = V_{IL}$	1.4	1.4	–	0.35	
		I_{OL} = 6 mA; $V_I = V_{IL}$	1.65	1.65	–	0.3	
		I_{OL} = 12 mA; $V_I = V_{IL}$	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I_{OL} = 18 mA; $V_I = V_{IL}$	2.3	2.3	–	0.6	
			3.0	3.0	–	0.45	
		I_{OL} = 24 mA; $V_I = V_{IL}$	3.0	3.0	–	0.6	
I_I	Input Leakage Current	$V_I = V_{CCA}$ or GND	0.9 – 4.5	0.9 – 4.5	−1.0	1.0	μA
I_{OFF}	Power–Off Leakage Current	$\overline{OE}$ = 0 V	0 / 0.9 – 4.5	0.9 – 4.5 / 0	−1.0 / −1.0	1.0 / 1.0	μA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; I_O = 0, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; I_O = 0, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
$I_{CCA} + I_{CCB}$	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; I_O = 0, $V_{CCA} = V_{CCB}$	0.9 – 4.5	0.9 – 4.5	–	4.0	μA
ΔI_{CCA}	Increase in I_{CC} per Input Voltage, Other Inputs at V_{CCA} or GND	$V_I = V_{CCA}$ − 0.6 V; $V_I = V_{CCA}$ or GND	4.5	4.5	–	10	μA
ΔI_{CCB}	Increase in I_{CC} per Input Voltage, Other Inputs at V_{CCA} or GND	$V_I = V_{CCA}$ − 0.6 V; $V_I = V_{CCA}$ or GND	4.5	4.5	–	10	μA
I_{OZ}	I/O Tri–State Output Leakage Current	T_A = 25°C, $\overline{OE} = V_{CCA}$	0.9 – 4.5	0.9 – 4.5	−1.0	1.0	μA

TOTAL STATIC POWER CONSUMPTION ($I_{CCA} + I_{CCB}$)

	−40°C to +85°C										
	V_{CCB} (V)										
	4.5		3.3		2.8		1.8		0.9		
V_{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
4.5		2		2		2		2		< 1.5	μA
3.3		2		2		2		2		< 1.5	μA
2.8		< 2		< 1		< 1		< 0.5		< 0.5	μA
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	μA
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	μA

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power−up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS

			−40°C to +85°C										
			V_{CCB} (V)										
			4.5		3.3		2.8		1.8		1.2		
Symbol	Parameter	V_{CCA} (V)	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PLH}, t_{PHL} (Note 1)	Propagation Delay, A_n to B_n	4.5		1.6		1.8		2.0		2.1		2.3	ns
		3.3		1.7		1.9		2.1		2.3		2.6	
		2.8		1.9		2.1		2.3		2.5		2.8	
		1.8		2.1		2.4		2.5		2.7		3.0	
		1.2		2.4		2.7		2.8		3.0		3.3	
t_{PZH}, t_{PZL} (Note 1)	Output Enable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	ns
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{PHZ}, t_{PLZ} (Note 1)	Output Disable, $\overline{OE}$ to B_n	4.5		2.6		3.8		4.0		4.1		4.3	ns
		3.3		3.7		3.9		4.1		4.3		4.6	
		2.5		3.9		4.1		4.3		4.5		4.8	
		1.8		4.1		4.4		4.5		4.7		5.0	
		1.2		4.4		4.7		4.8		5.0		5.3	
t_{OSHL}, t_{OSLH} (Note 1)	Output to Output Skew, Time	4.5		0.15		0.15		0.15		0.15		0.15	ns
		3.3		0.15		0.15		0.15		0.15		0.15	
		2.5		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figure 3.

CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or V_{CCA}, f = 10 MHz	20	pF

2. Typical values are at $T_A = +25°C$.
3. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:
$I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

MAXIMUM TRANSLATION FREQUENCY $(C_L = 15 \text{ pF}, T_A = -40°C \text{ to } +85°C)$

V_{CCA} (V)	V_{CCB} (V)	Maximum Frequency (MHz)
1.2	1.2	90
1.8	3.0	300
1.8	4.5	300
3.0	3.0	420
4.5	1.8	380
4.5	3.0	425
4.5	4.5	425
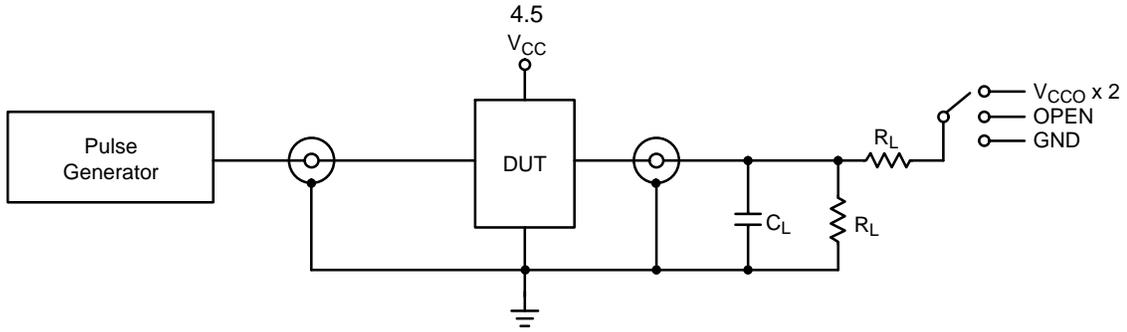
Figure 3. AC (Propagation Delay) Test Circuit

Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2
t_{PHZ}, t_{PZH}	GND
C_L = 15 pF or equivalent (includes probe and jig capacitance) R_L = 2 kΩ or equivalent Z_{OUT} of pulse generator = 50 Ω	
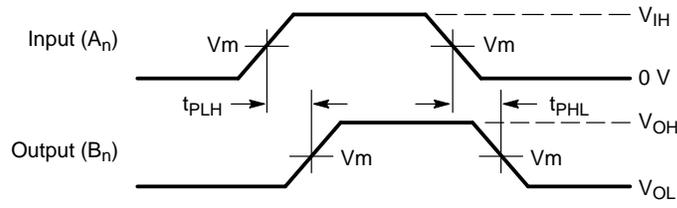
Waveform 1 – Propagation Delays

$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns
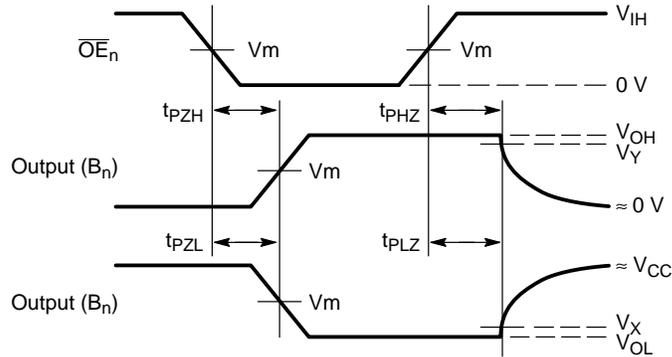
Waveform 2 – Output Enable and Disable Times

$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

Symbol	V_{CC}				
	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V
V_{mA}	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
V_{mB}	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
V_X	V_{OL} + 10% V_{OH}	V_{OL} + 10% V_{OH}	V_{OL} + 10% V_{OH}	V_{OL} + 10% V_{OH}	V_{OL} + 10% V_{OH}
V_Y	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9	V_{OH} x 0.9

SLSV4T244

PACKAGE DIMENSIONS

UQFN12 1.7x2.0, 0.4P
CASE 523AE
ISSUE A

TOP VIEW

DETAIL A
NOTE 5

DETAIL B
OPTIONAL
CONSTRUCTION

SIDE VIEW

BOTTOM VIEW
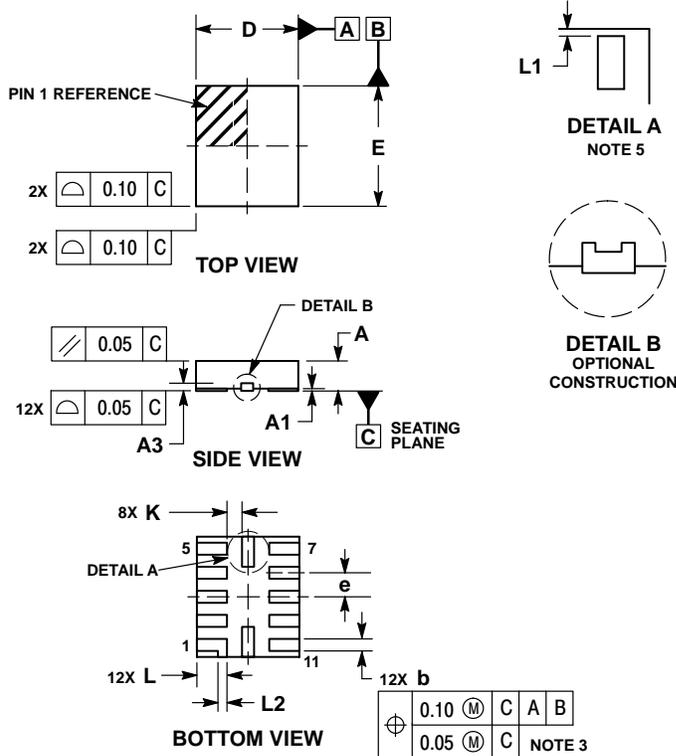
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

MOUNTING FOOTPRINT
SOLDERMASK DEFINED
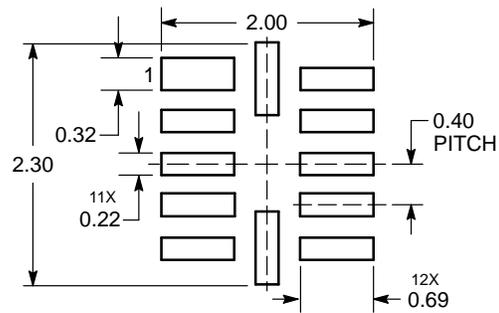
DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SLSV4T244/D