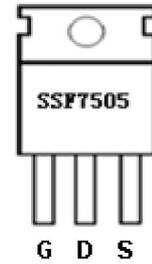
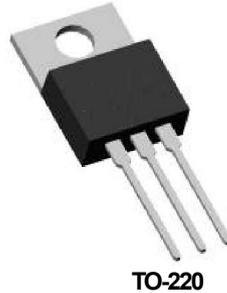
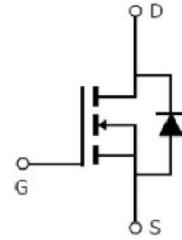


Main Product Characteristics

V_{DSS}	75V
$R_{DS(on)}$	3.3mohm(typ.)
I_D	170A



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature
- Lead free product



Description

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	170	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	110	
I_{DM}	Pulsed Drain Current②	670	
$P_D @ TC = 25^\circ C$	Power Dissipation③	272	W
	Linear Derating Factor	2.0	W/°C
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ $L=0.3mH$ ②	960	mJ
I_{AR}	Avalanche Current @ $L=0.3mH$ ②	80	A
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

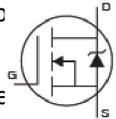
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ^③	—	0.55	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ^④	—	62	$^{\circ}C/W$
	Junction-to-Ambient (PCB mounted, steady-state) ^④	—	40	$^{\circ}C/W$

Electrical Characteristics @ $T_A=25^{\circ}C$ unless otherwise specified

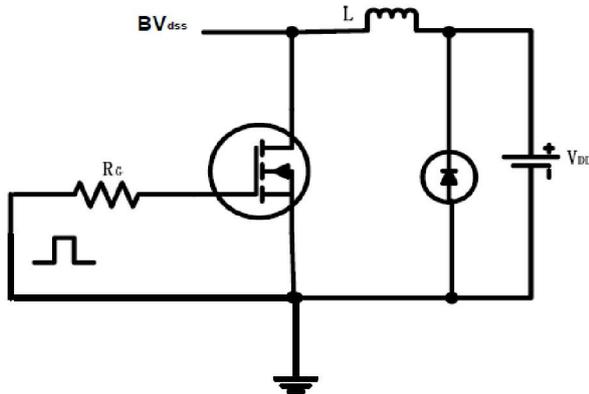
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	3.3	5	m Ω	$V_{GS}=10V, I_D = 30A$
		—	6.25	—		$T_J = 125^{\circ}C$
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.0	—		$T_J = 125^{\circ}C$
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	50		$T_J = 125^{\circ}C$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		-100	—	—		$V_{GS} = -20V$
Q_g	Total gate charge	—	221	—	nC	$I_D = 30A,$ $V_{DS}=30V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	42	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	70	—		
$t_{d(on)}$	Turn-on delay time	—	25	—	ns	$V_{GS}=10V, V_{DS}=30V,$ $R_L=15\Omega,$ $R_{GEN}=2.55\Omega$
t_r	Rise time	—	24	—		
$t_{d(off)}$	Turn-Off delay time	—	125	—		
t_f	Fall time	—	53	—		
C_{iss}	Input capacitance	—	9139	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 600KHz$
C_{oss}	Output capacitance	—	757	—		
C_{rss}	Reverse transfer capacitance	—	669	—		

Source-Drain Ratings and Characteristics

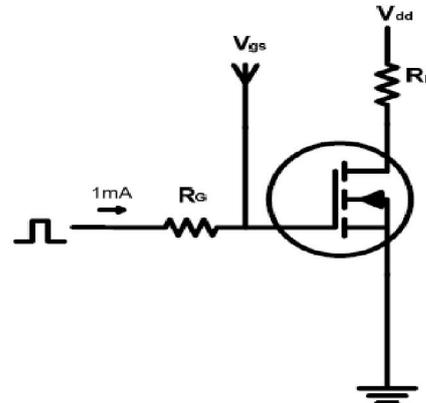
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	170	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	670	A	
V_{SD}	Diode Forward Voltage	—	0.84	1.3	V	$I_S=30A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	47	—	ns	$T_J = 25^{\circ}C, I_F = 75A, di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	97	—	nC	

Test Circuits and Waveforms

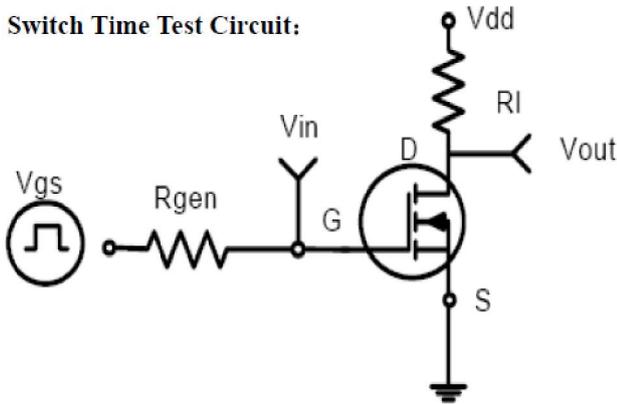
EAS test circuits:



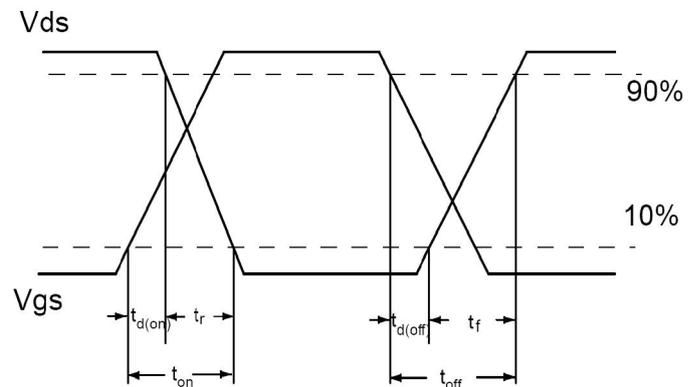
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ C$.
- ⑥ The maximum current rating is limited by bond-wires.

Typical Electrical and Thermal Characteristics

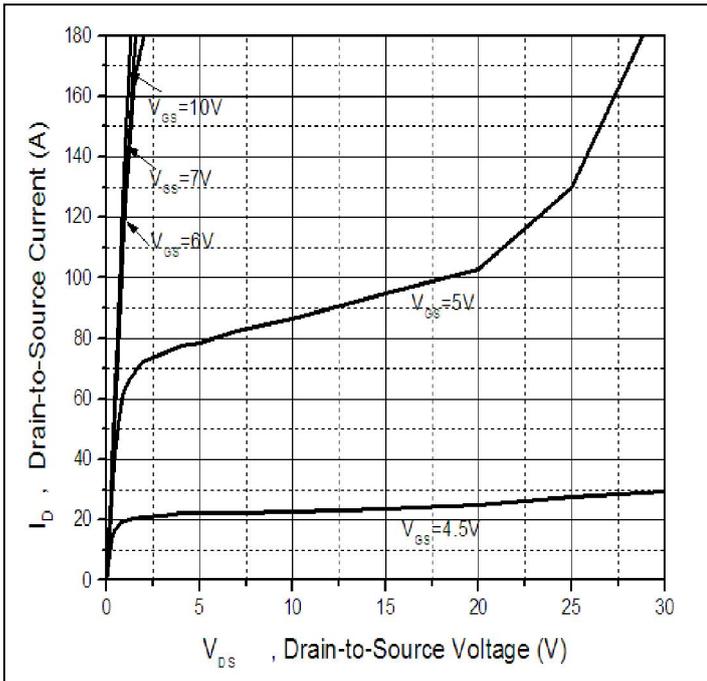


Figure 1: Typical Output Characteristics

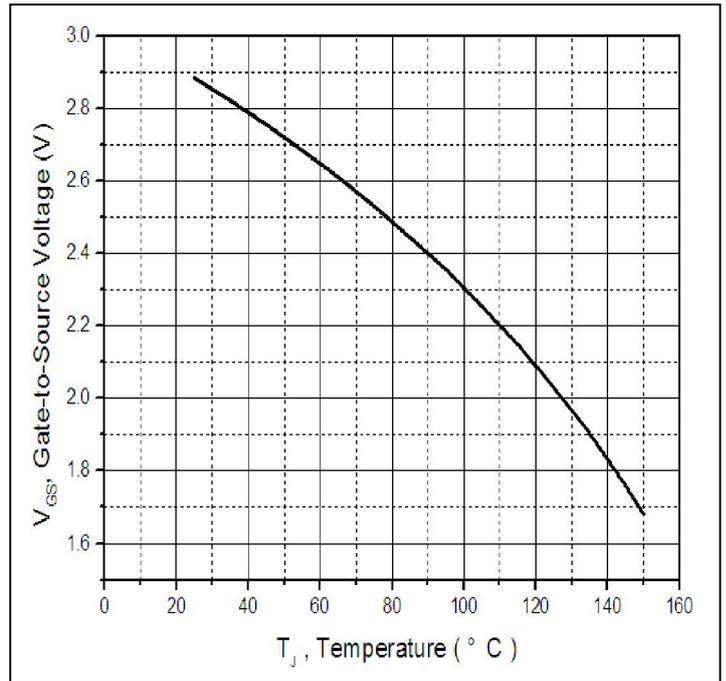


Figure 2. Gate to source cut-off voltage

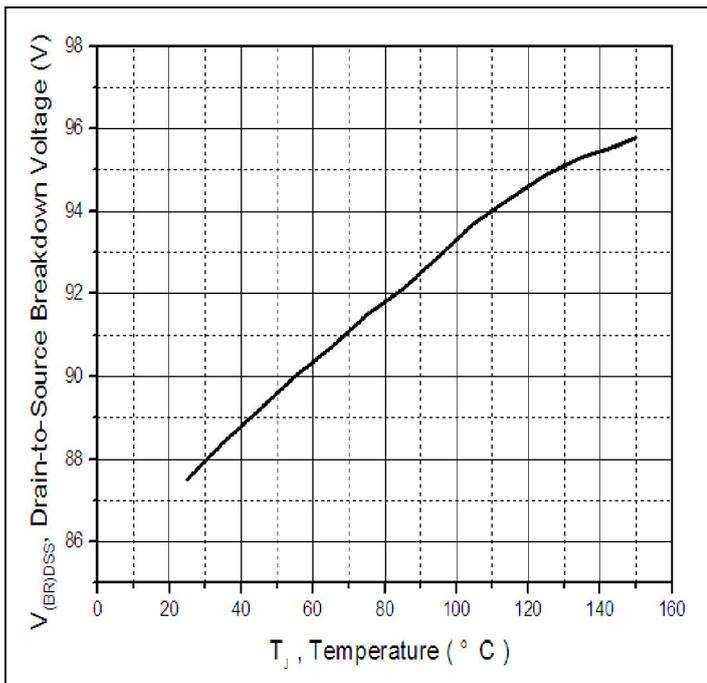


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

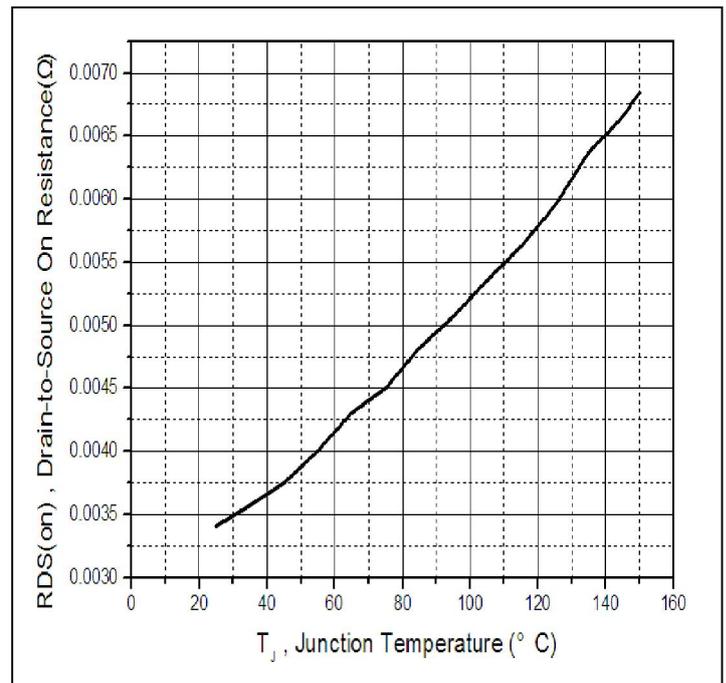


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

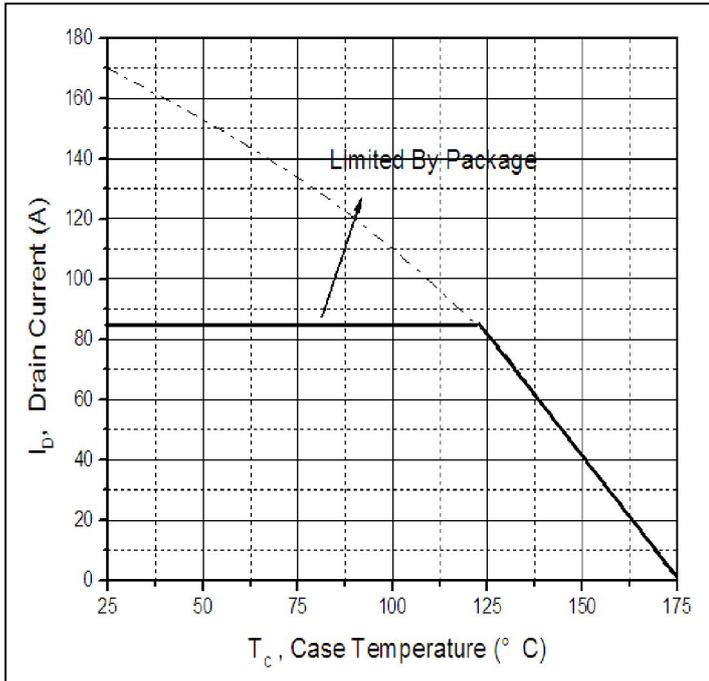


Figure 5. Maximum Drain Current Vs. Case Temperature

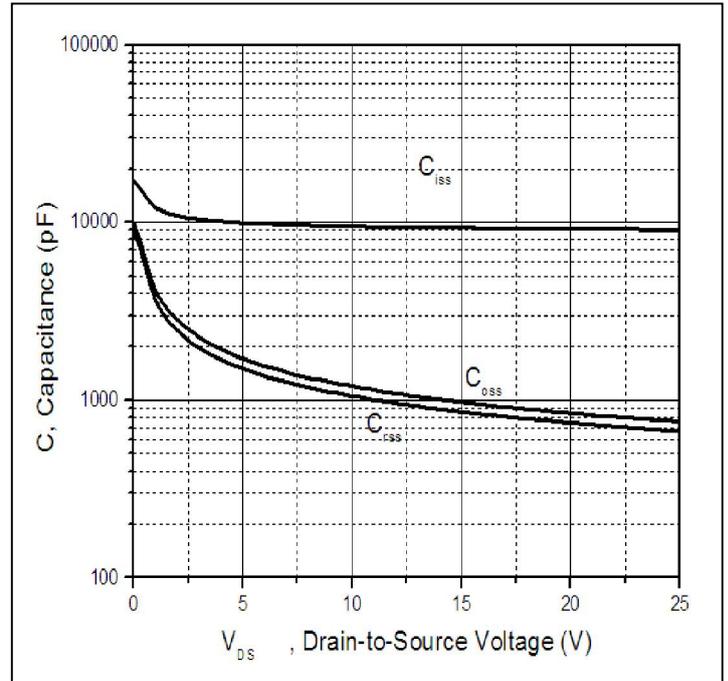


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

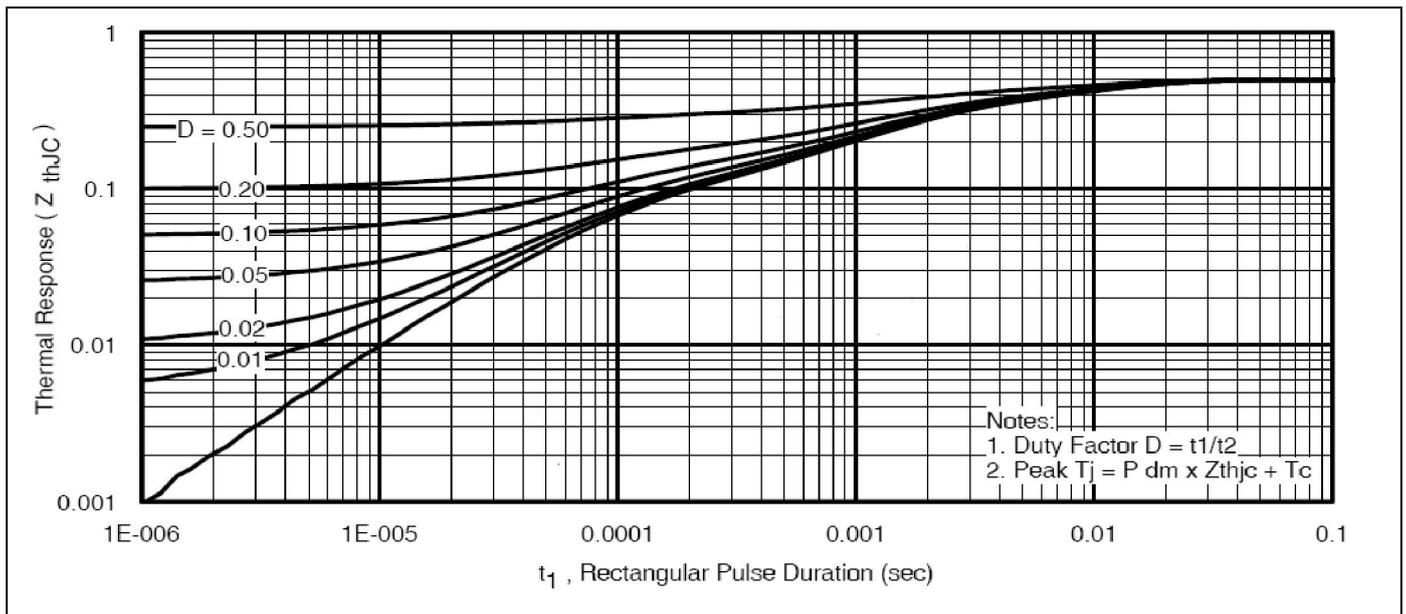
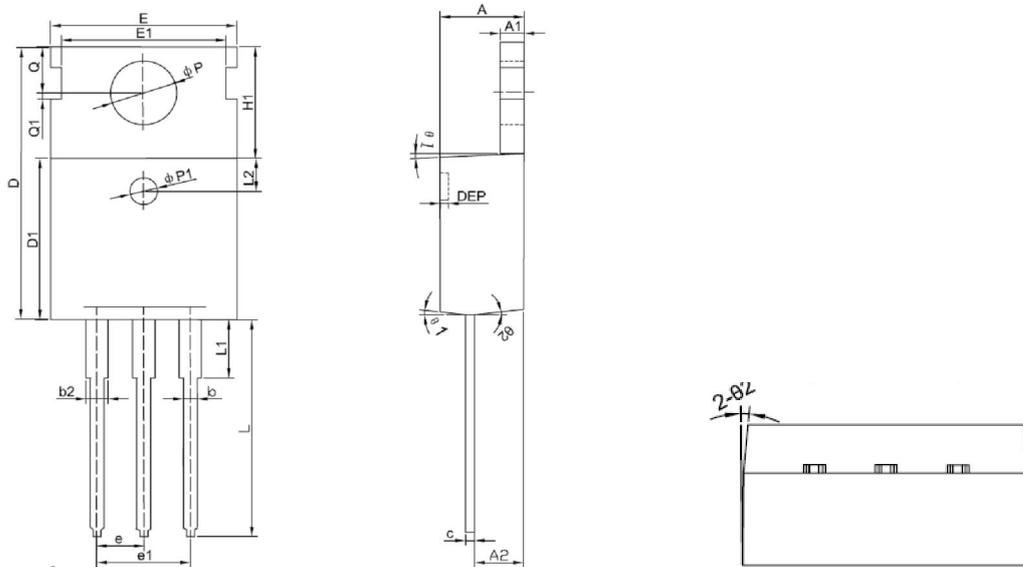


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO220 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
$\Phi P1$	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
$\square 1$	5 ⁰	7 ⁰	9 ⁰	5 ⁰	7 ⁰	9 ⁰
$\square 2$	1 ⁰	3 ⁰	5 ⁰	1 ⁰	3 ⁰	5 ⁰



Ordering and Marking Information

Device Marking: SSF7505

Package (Available)
TO-220
Operating Temperature Range
C : -55 to 175 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices