

MOSFET – Power, N-Channel, Dual ECH8

30 V, 8 A, 20.5 mΩ

ECH8663R

Features

- Low ON-resistance
- 2.5 V Drive
- Common-drain Type
- Protection Diode in
- Built-in Gate Protection Resistor
- Best Suited for LiB Charging and Discharging Switch
- Halogen Free Compliance

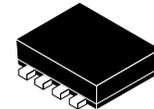
Specifications

ABSOLUTE MAXIMUM RATINGS (at Ta = 25°C)

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|------------------|---|-------------|------|
| Drain-to-Source Voltage | V _{DSS} | | 30 | V |
| Gate-to-Source Voltage | V _{GSS} | | ±12 | V |
| Drain Current (DC) | I _D | | 8 | A |
| Drain Current (Pulse) | I _{DP} | PW ≤ 10 μs, duty cycle ≤ 1% | 60 | A |
| Allowable Power Dissipation | P _D | When mounted on ceramic substrate (900 mm ² × 0.8 mm) 1 unit | 1.4 | W |
| Total Power Dissipation | P _T | When mounted on ceramic substrate (900 mm ² × 0.8 mm) | 1.5 | W |
| Channel Temperature | T _{ch} | | 150 | °C |
| Storage Temperature | T _{stg} | | -55 to +150 | °C |

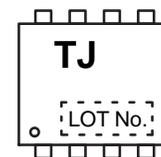
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

| V _{DSS} | R _{Ds(on)} MAX | I _D MAX |
|------------------|-------------------------|--------------------|
| 30 V | 20.5 mΩ @ 4.5 V | 8 A |
| | 21 mΩ @ 4.0 V | |
| | 23 mΩ @ 3.1 V | |
| | 28 mΩ @ 2.5 V | |

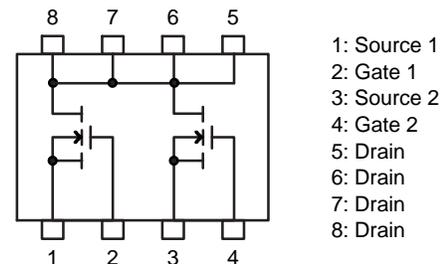


SOT-28FL / ECH8
CASE 318BF

MARKING DIAGRAM



ELECTRICAL CONNECTION



ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|---|--------------------|
| ECH8663R-TL-H | SOT-28FL / ECH8 (Pb-Free and Halide Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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ELECTRICAL CHARACTERISTICS (at $T_a = 25^\circ\text{C}$)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|---------------|--|---------|------|----------|------------------|
| | | | Min | Typ | Max | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$ | 30 | - | - | V |
| Zero-Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ | - | - | 1 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$ | - | - | ± 10 | μA |
| Cutoff Voltage | $V_{GS(off)}$ | $V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$ | 0.5 | - | 1.3 | V |
| Forward Transfer Admittance | $ y_{fs} $ | $V_{DS} = 10 \text{ V}, I_D = 4 \text{ A}$ | 5 | 8.5 | - | S |
| Static Drain-to-Source On-State Resistance | $R_{DS(on)1}$ | $I_D = 4 \text{ A}, V_{GS} = 4.5 \text{ V}$ | 10.5 | 15.5 | 20.5 | $\text{m}\Omega$ |
| | $R_{DS(on)2}$ | $I_D = 4 \text{ A}, V_{GS} = 4.0 \text{ V}$ | 11 | 16 | 21 | $\text{m}\Omega$ |
| | $R_{DS(on)3}$ | $I_D = 2 \text{ A}, V_{GS} = 3.1 \text{ V}$ | 12 | 17.5 | 23 | $\text{m}\Omega$ |
| | $R_{DS(on)4}$ | $I_D = 2 \text{ A}, V_{GS} = 2.5 \text{ V}$ | 12 | 20 | 28 | $\text{m}\Omega$ |
| Turn-ON Delay Time | $t_{d(on)}$ | See specified Test Circuit. | - | 320 | - | ns |
| Rise Time | t_r | | - | 850 | - | ns |
| Turn-OFF Delay Time | $t_{d(off)}$ | | - | 4200 | - | ns |
| Fall Time | t_f | | - | 1800 | - | ns |
| Total Gate Charge | Q_g | $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$ | - | 12.3 | - | nC |
| Gate-to-Source Charge | Q_{gs} | | - | 2.4 | - | nC |
| Gate-to-Drain "Miller" Charge | Q_{gd} | | - | 2.8 | - | nC |
| Diode Forward Voltage | V_{SD} | $I_S = 8 \text{ A}, V_{GS} = 0 \text{ V}$ | - | 0.75 | 1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Switching Time Test Circuit

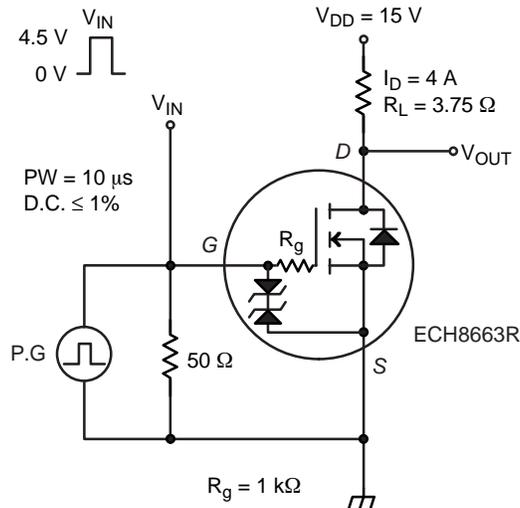


Figure 1. Switching Time Test Circuit

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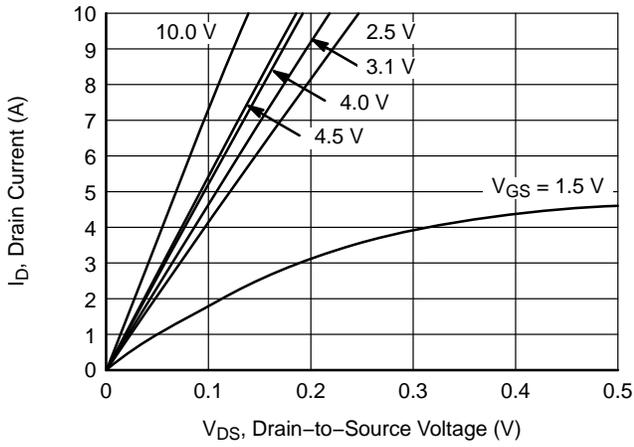


Figure 2. $I_D - V_{DS}$

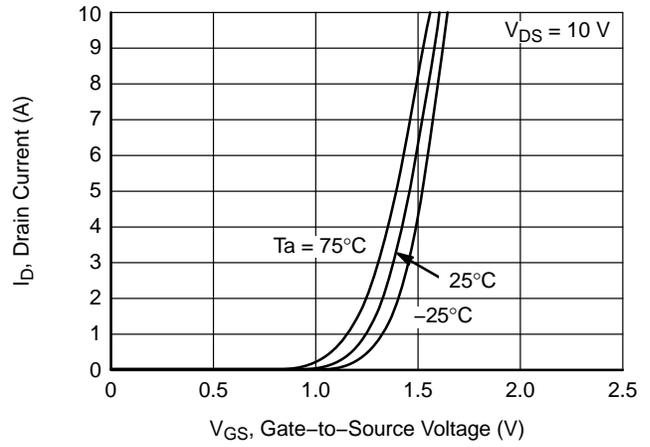


Figure 3. $I_D - V_{GS}$

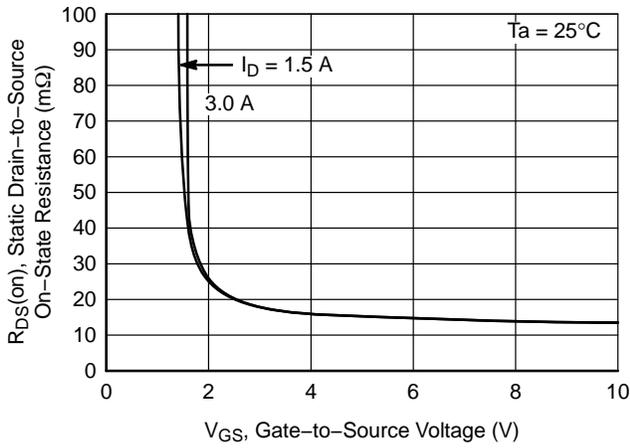


Figure 4. $R_{DS(on)} - V_{GS}$

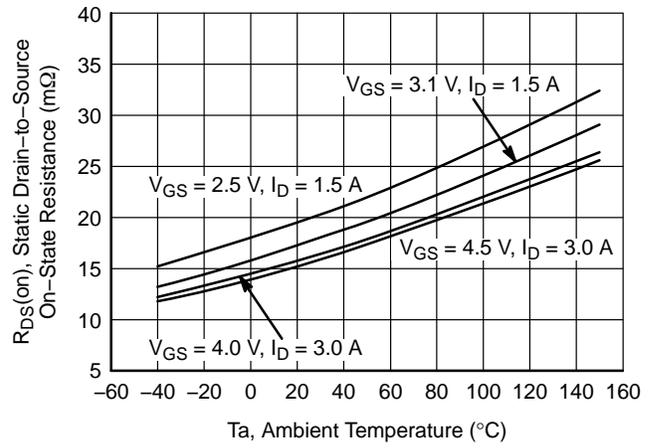


Figure 5. $R_{DS(on)} - T_a$

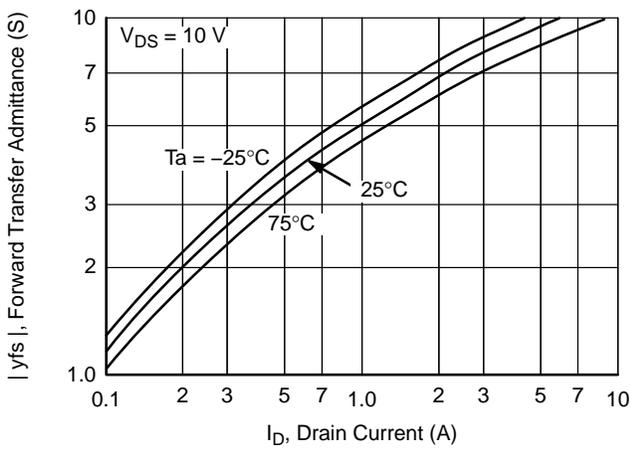


Figure 6. $|y_{fs}| - I_D$

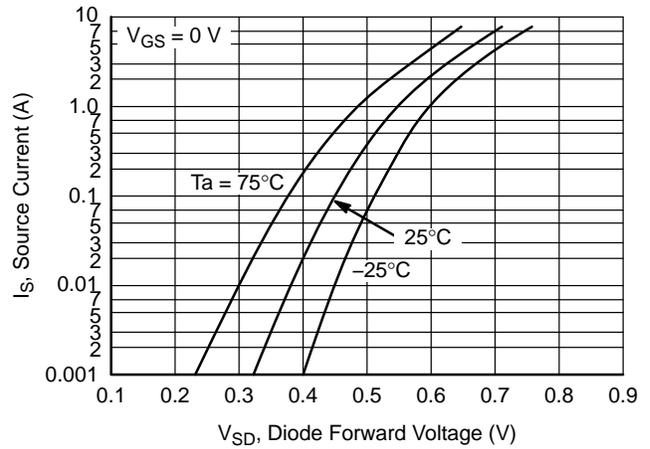


Figure 7. $I_S - V_{SD}$

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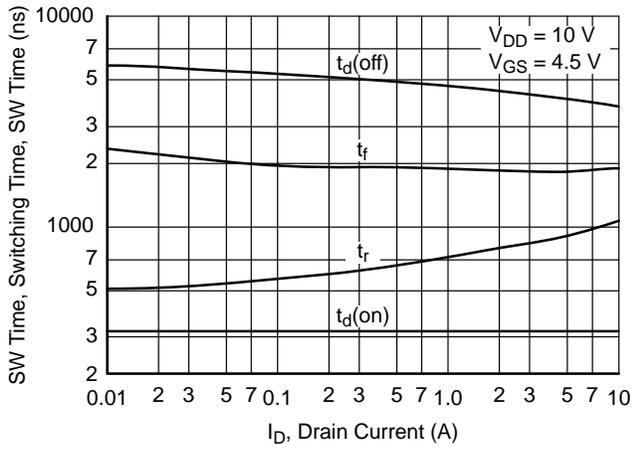


Figure 8. SW Time – I_D

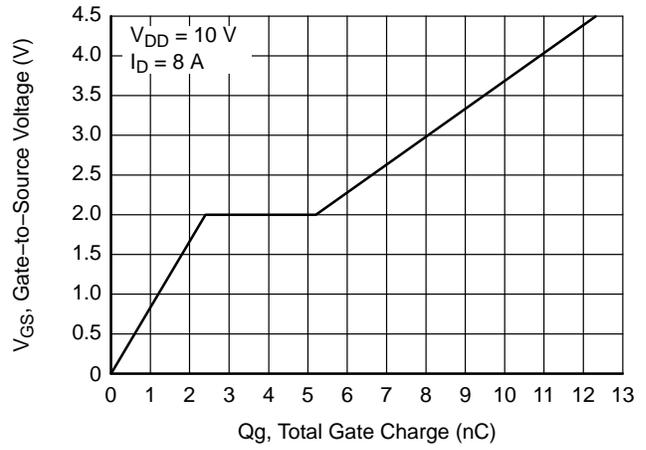


Figure 9. $V_{GS} - Q_g$

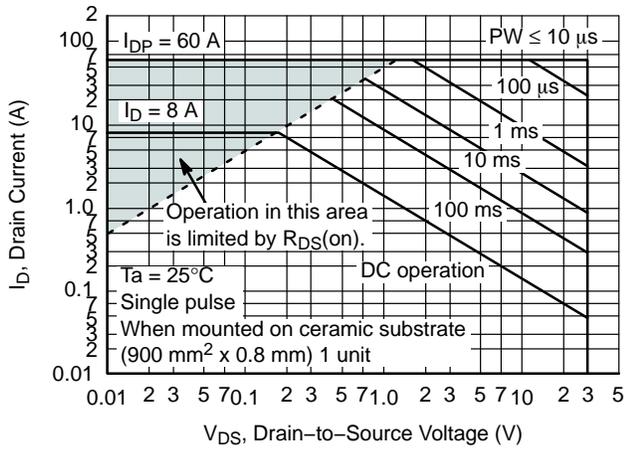


Figure 10. ASO

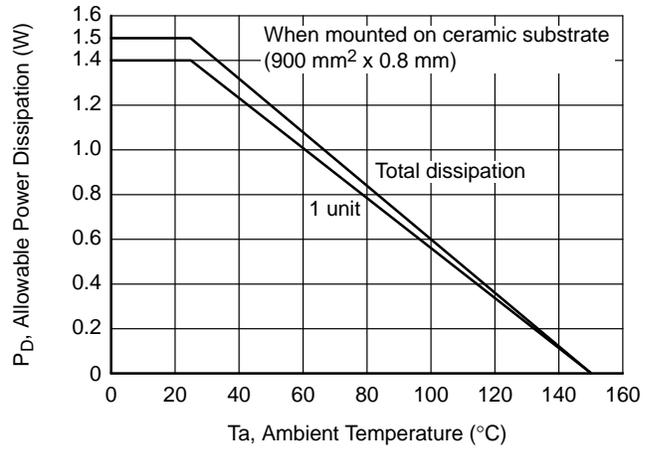
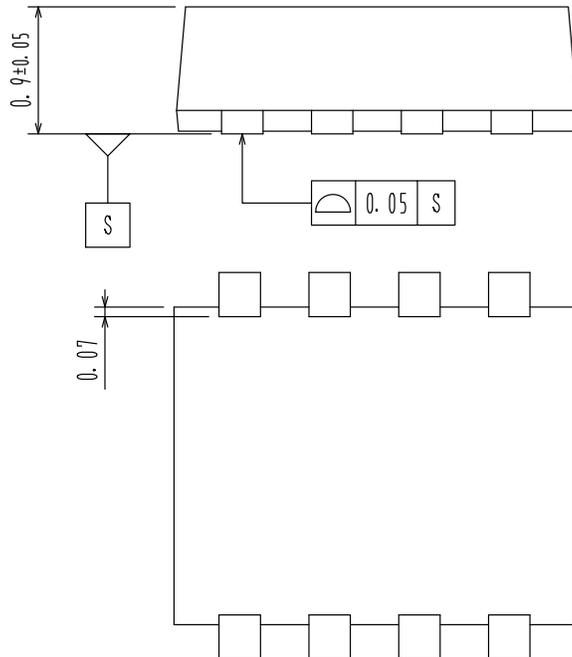
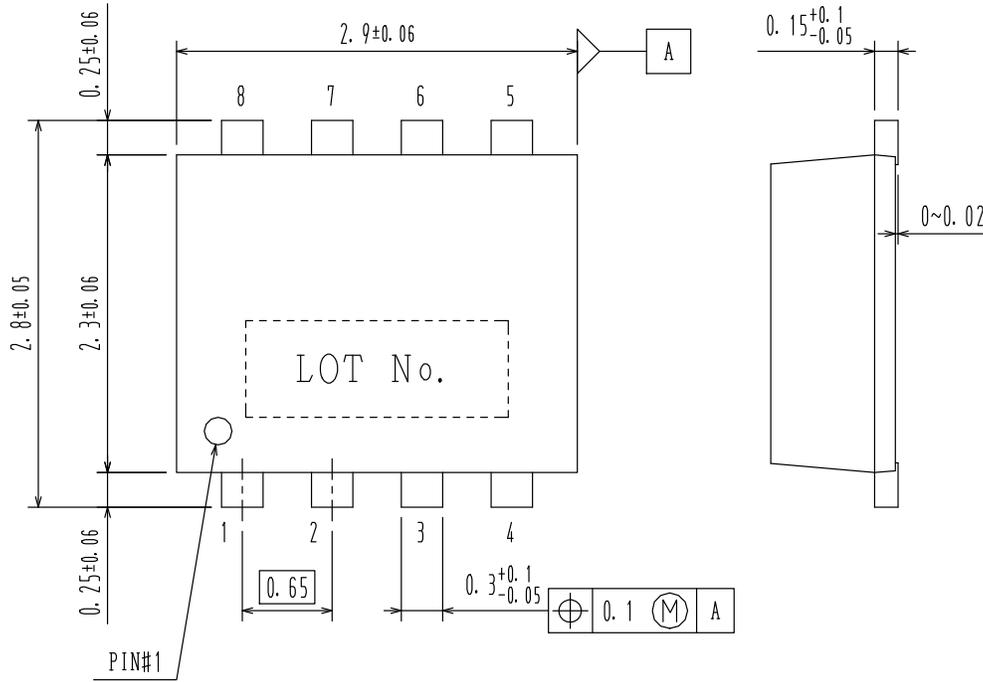


Figure 11. $P_D - T_a$

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DATE 31 MAR 2012



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