

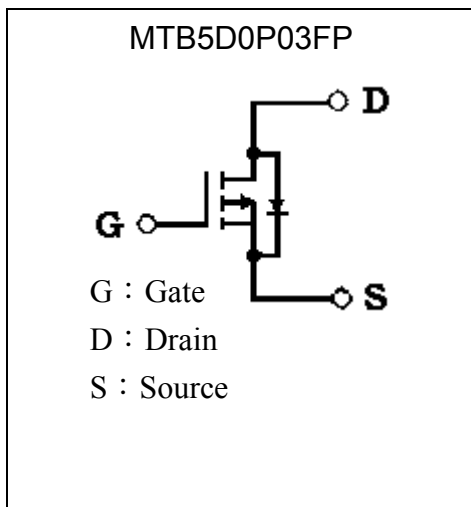
P-Channel Enhancement Mode Power MOSFET
MTB5D0P03FP

BV_{DSS}	-30V
I_D @ V_{GS}=-10V, T_C=25°C	-56A
R_{DS(ON)}@ V_{GS}=-10V, I_D=-25A	4.2m Ω (typ)
R_{DS(ON)}@ V_{GS}=-4.5V, I_D=-10A	4.8m Ω (typ)

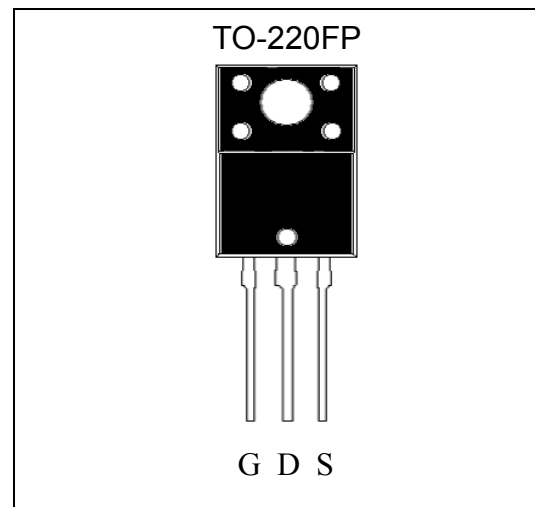
Features

- Single Drive Requirement
- Low On-resistance
- Fast switching Characteristic
- Pb-free lead plating package

Symbol

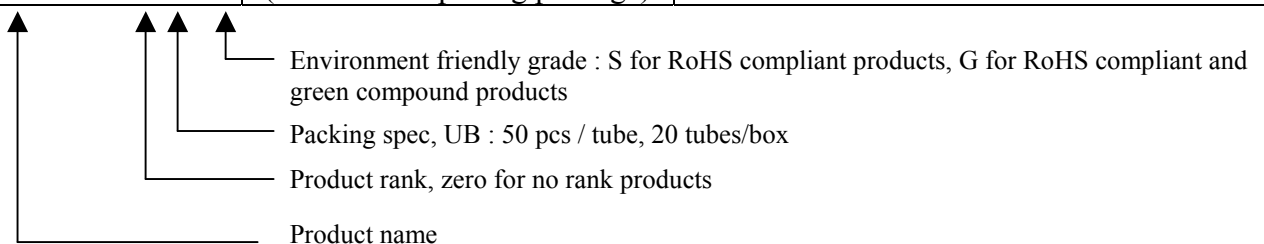


Outline



Ordering Information

Device	Package	Shipping
MTB5D0P03FP-0-UB-S	TO-220FP (Pb-free lead plating package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



**Absolute Maximum Ratings** (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V _{DS}	-30	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current @V _{GS} =-10V, T _C =25°C (Package limited)		I _D	-56	A
Continuous Drain Current @V _{GS} =-10V, T _C =25°C (Silicon limited)			-72	
Continuous Drain Current @V _{GS} =-10V, T _C =100°C			-45.5	
Continuous Drain Current @V _{GS} =-10V, T _A =25°C (Note 2)		I _{DSM}	-12.9	
Continuous Drain Current @V _{GS} =-10V, T _A =70°C (Note 2)			-10.3	
Pulsed Drain Current (Note 4)		I _{DM}	-288	
Power Dissipation	T _C =25°C (Note 1)	P _D	62.5	W
	T _C =100°C (Note 1)		25	
	T _A =25°C (Note 2)	P _{DSM}	2	
	T _A =70°C (Note 2)		1.3	
Single Pulse Avalanche Energy @L=0.5mH, I _{AS} =-30A (Note 3)		E _{AS}	225 *	mJ
Single Pulse Avalanche Current (Note 3)		I _{AS}	-30	A
Operating Junction and Storage Temperature		T _j , T _{stg}	-55~+150	°C

* 100% UIS testing in condition of V_D=-15V, L=0.5mH, V_G=10V, I_{AS}=-20A, Rated V_{DS}=-30V

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	2	°C/W
Thermal Resistance, Junction-to-ambient, max, t≤10s (Note 1)	R _{th,j-a}	15	
Thermal Resistance, Junction-to-ambient, max (Note 1)		62.5	

- Note : 1. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature T_{J(MAX)}=150°C.
4. Pulse width ≤300μs pulses and duty cycle ≤0.5%.
5. The R_{θJA} is the sum of thermal resistance from junction to case R_{θJC} and case to ambient.



Characteristics (Tj=25°C, unless otherwise specified)

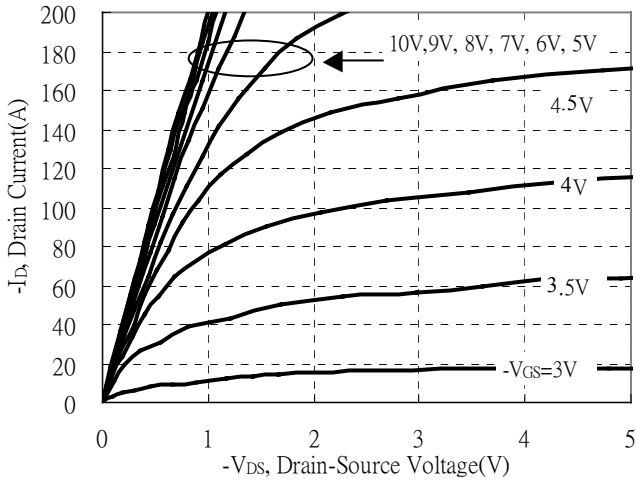
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-30	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1.0	-	-2.5		V _{DS} = V _{GS} , I _D =-250μA
G _{FS}	-	62	-	S	V _{DS} = -5V, I _D =-25A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V
I _{DSS}	-	-	-1	μA	V _{DS} = -30V, V _{GS} = 0V
	-	-	-25		V _{DS} = -30V, V _{GS} = 0V, Tj=70°C
*R _{DS(ON)}	-	4.2	5.5	mΩ	V _{GS} = -10V, I _D =-25A
	-	4.8	7.5		V _{GS} = -4.5V, I _D =-10A
Dynamic					
*Q _g	-	121	181	nC	I _D =-25A, V _{DS} =-24V, V _{GS} =-10V
*Q _{gs}	-	18.6	-		
*Q _{gd}	-	24.5	-		
*t _{d(ON)}	-	19.4	29	ns	V _{DS} =-15V, V _{GS} =-10V, R _G =2.7Ω, I _D =-25A
*t _r	-	21.6	32		
*t _{d(OFF)}	-	133	200		
*t _f	-	49.2	74		
C _{iss}	-	6290	-	pF	V _{GS} =0V, V _{DS} =-25V, f=1MHz
C _{oss}	-	761	-		
C _{rss}	-	375	-		
Source-Drain Diode					
*I _S	-	-	-56	A	
*V _{SD}	-	-0.83	-1.2	V	I _S =-25A, V _{GS} =0V
*t _{rr}	-	26	40	ns	I _F =-25A, V _{GS} =0V, dI _F /dt=100A/μs
*Q _{rr}	-	17	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

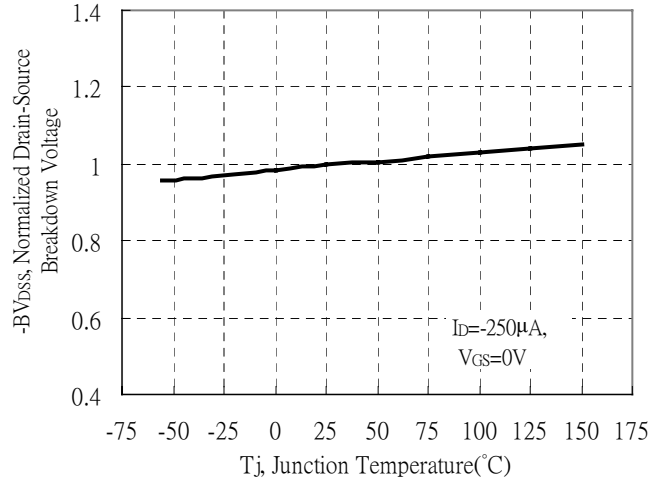


Typical Characteristics

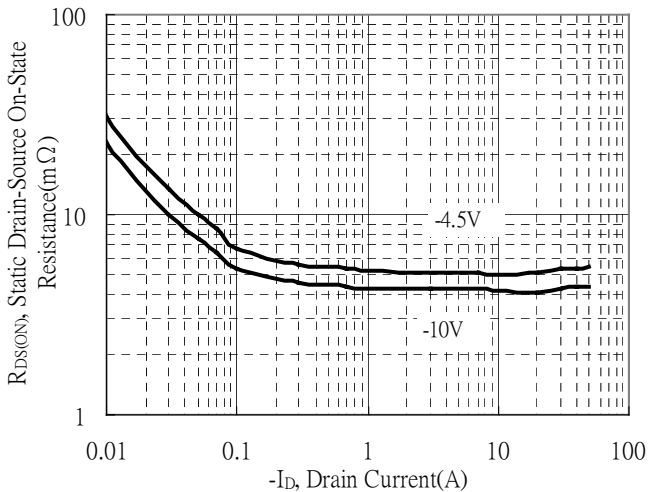
Typical Output Characteristics



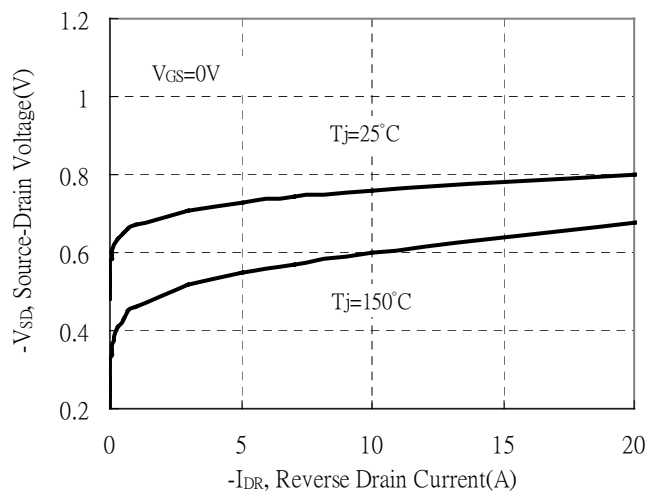
Brekdown Voltage vs Ambient Temperature



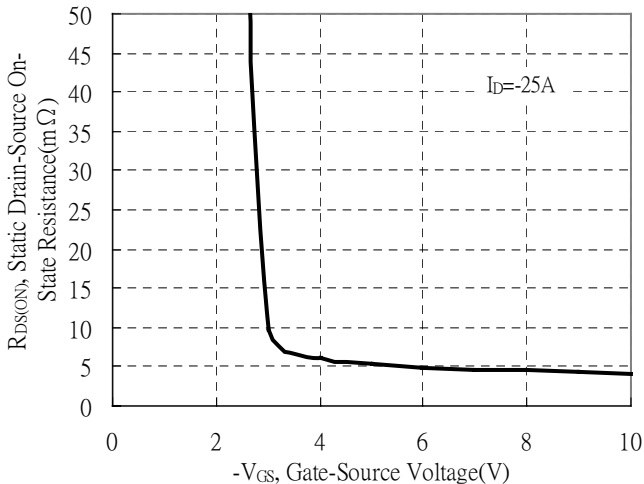
Static Drain-Source On-State resistance vs Drain Current



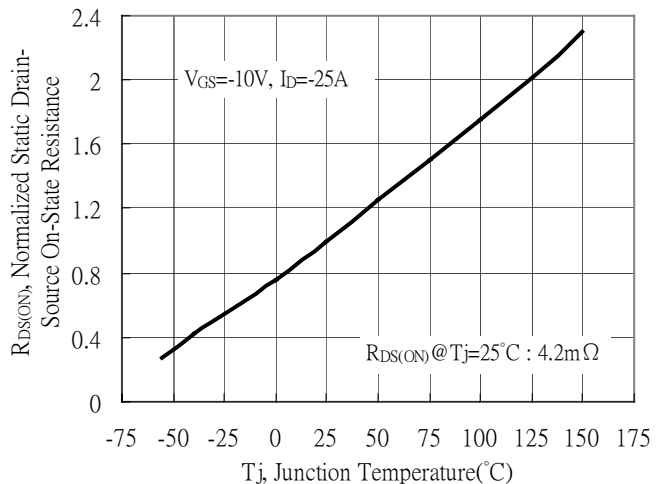
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



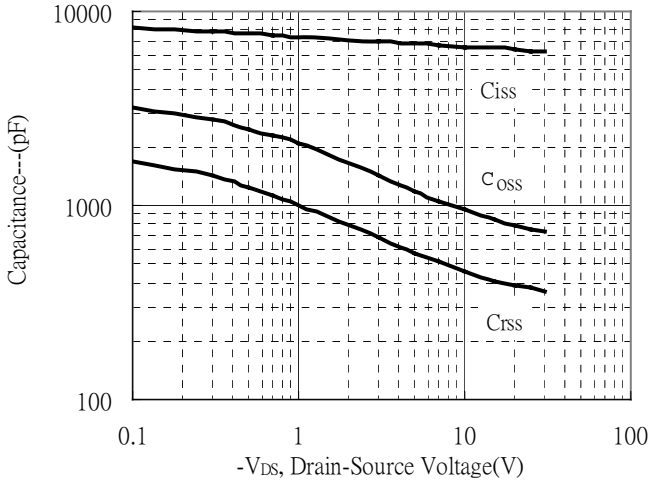
Drain-Source On-State Resistance vs Junction Temperature



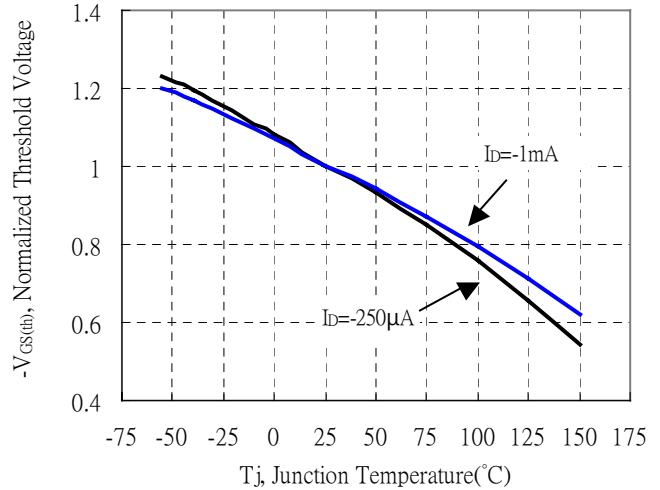


Typical Characteristics(Cont.)

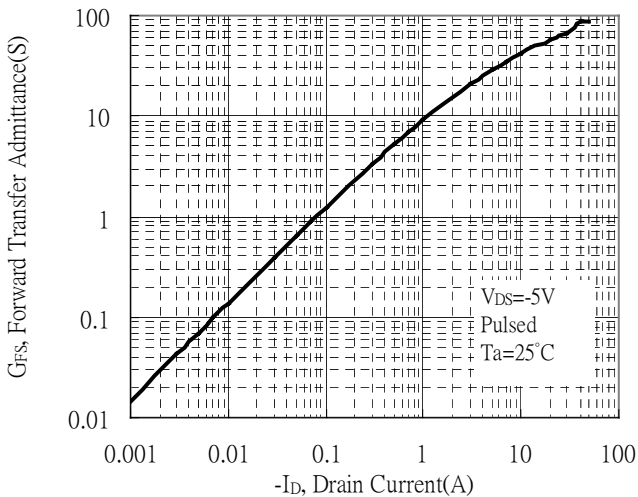
Capacitance vs Drain-to-Source Voltage



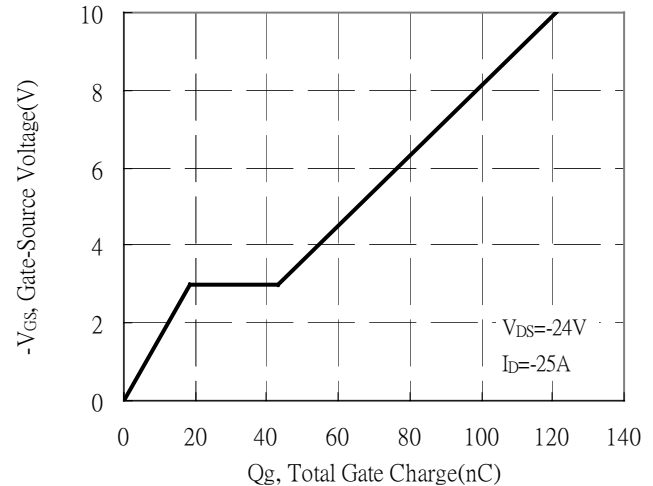
Threshold Voltage vs Junction Temperature



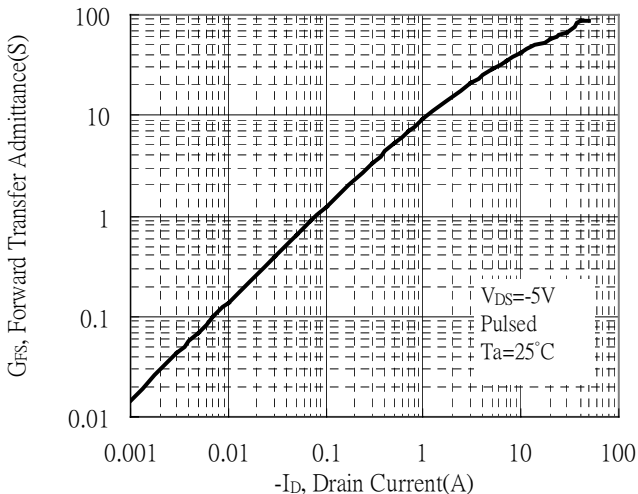
Forward Transfer Admittance vs Drain Current



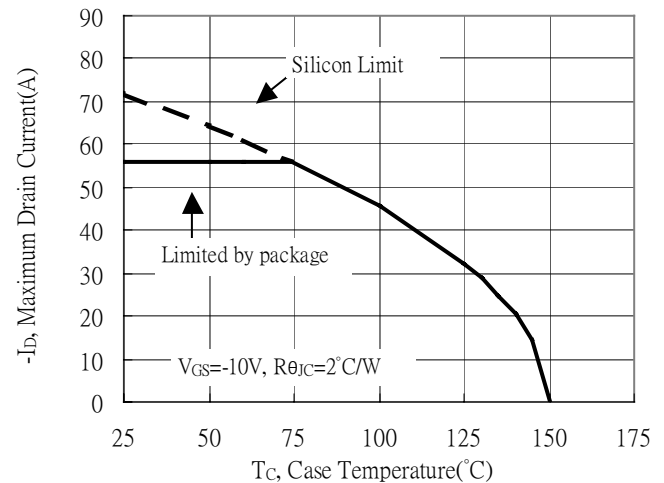
Gate Charge Characteristics



Forward Transfer Admittance vs Drain Current



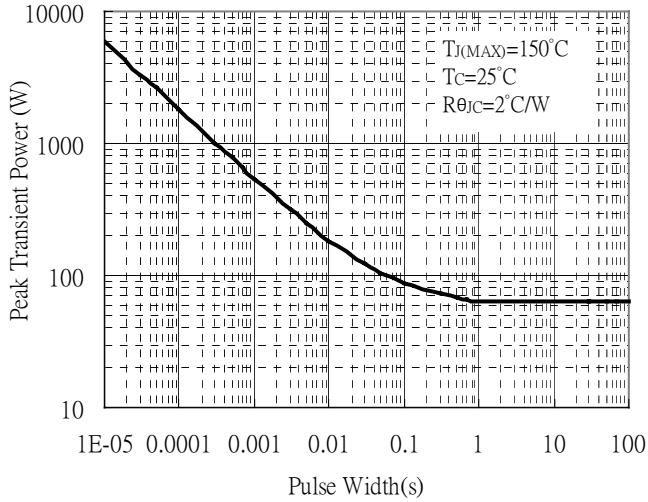
Maximum Drain Current vs Case Temperature



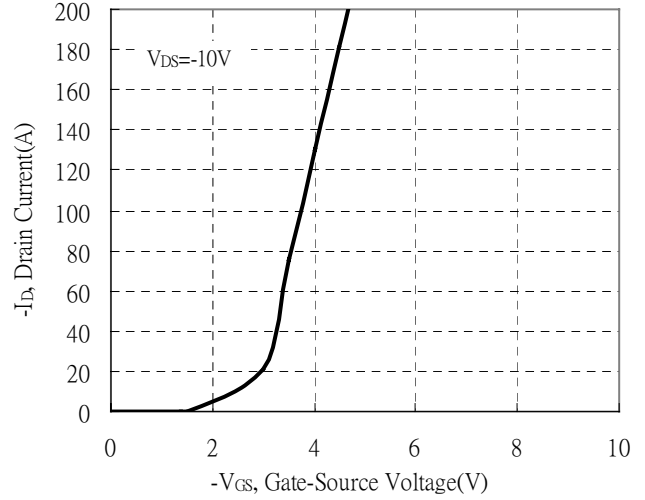


Typical Characteristics(Cont.)

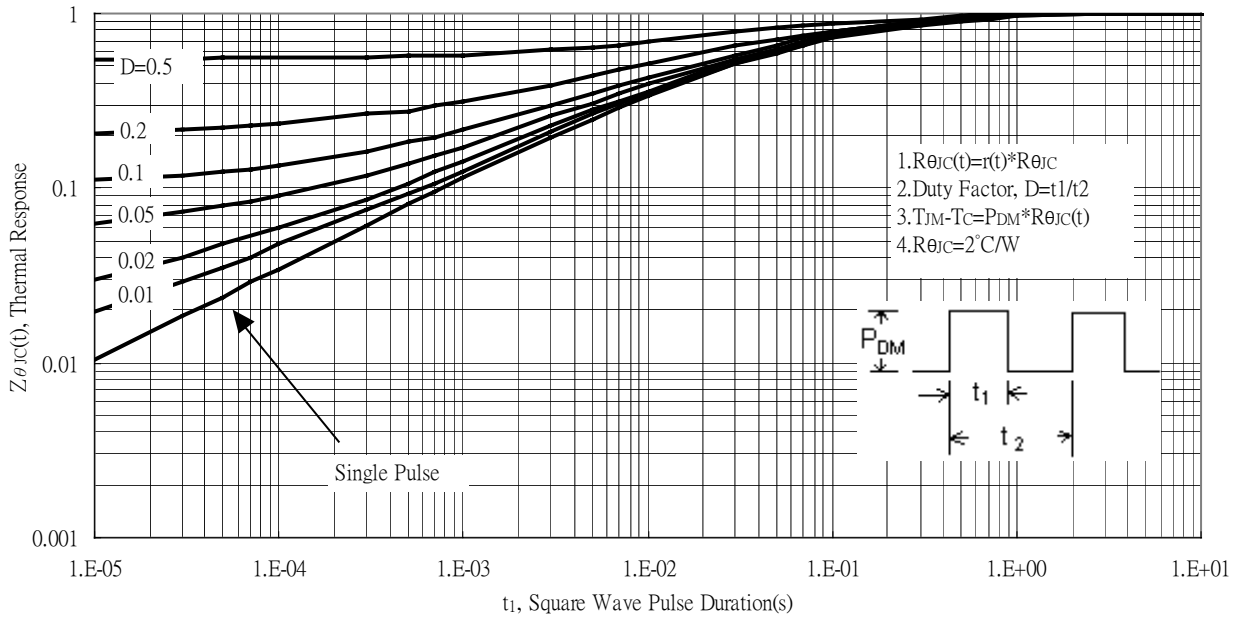
Single Pulse Maximum Power Dissipation



Typical Transfer Characteristics



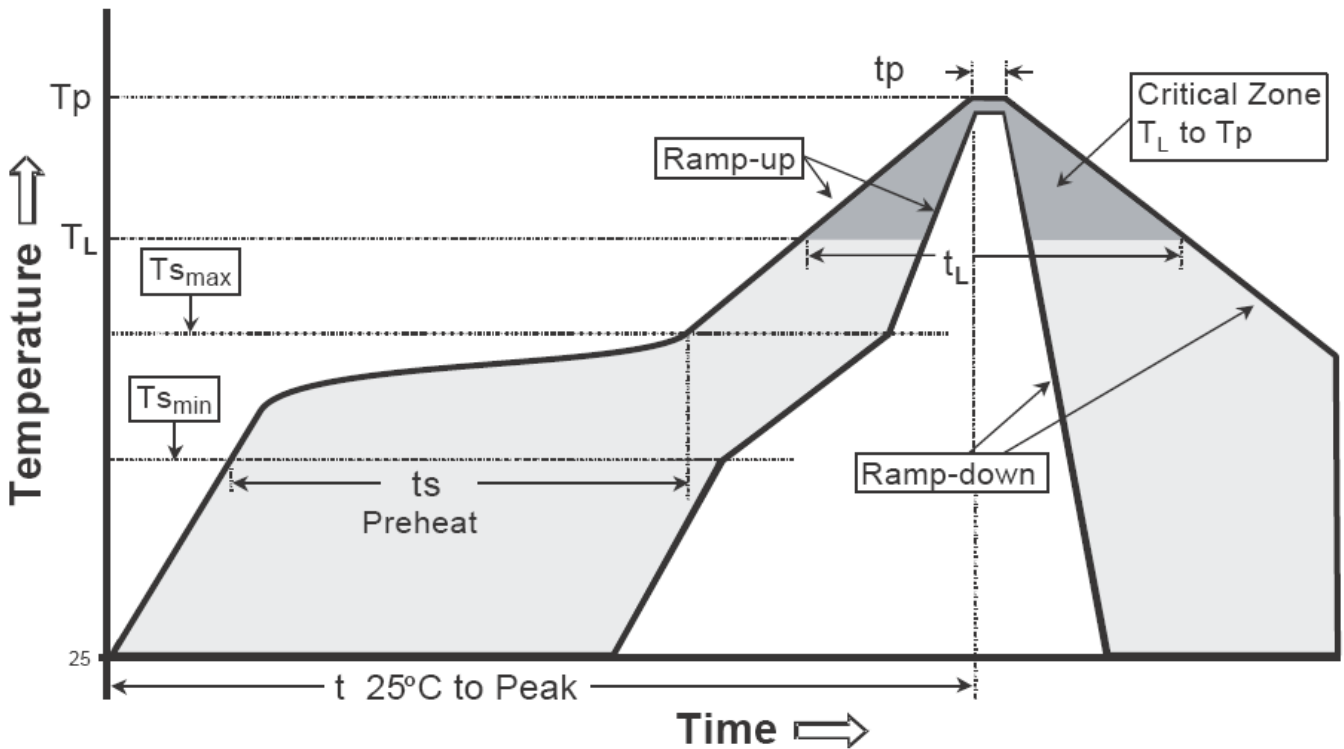
Transient Thermal Response Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

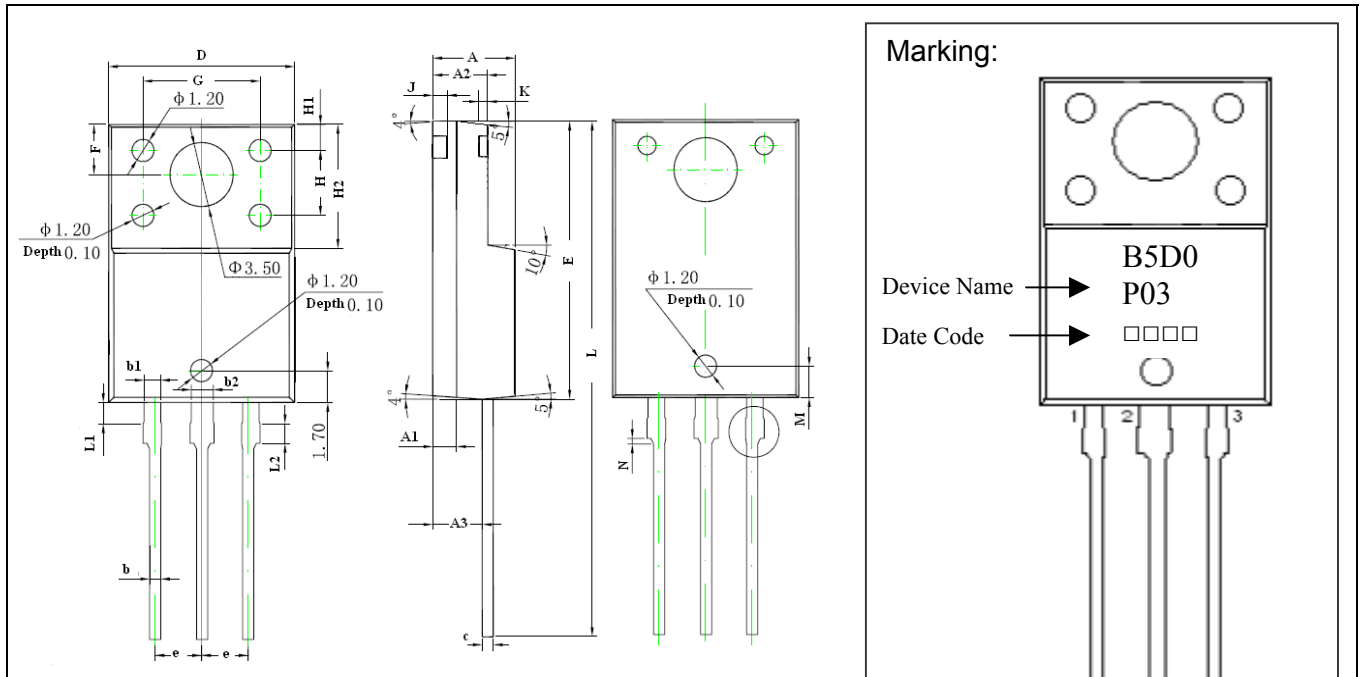
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
 CYStek Package Code: FP

Marking:
 Device Name → B5D0
 P03
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

- Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.