CH7035B DVI Transmitter

FEATURES

- DVI encoder support up to 1080p
- SPDIF audio interface supports either 16-bit or 20-bit stereo data for up to 192kHz/2ch
- Support 2 channel I2S digital audio input for up to 24-bit data stream (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHzand 192kHz)
- DDC master for reading EDID
- Hot plug detection for DVI
- On-chip frame buffer supports frame rate conversion provides the graphic controller the flexibility of video timing output
- Advanced scaling engine to upsize/downsize input resolution for DVI display up to 1080p
- Supports 8/12/16/18/24-bit parallel interface input for either RGB format (RGB-565, RGB-666 or RGB-888 and etc.) or YCrCb format (ITU-R 656 or ITU-R 601). 80/86 MPU interface and DE only mode are also supported.
- Wide range of input resolutions support for up to 1366x768 (i.e. 640x480, 720x480, 720x576, 800x600, 1024x600, 1024x768, 1280x800, and etc.)
- Image display rotation support at 90/180/270 degree or flipped in horizontal/vertical position
- Pixel clock input frequency support for up to 165 MHz
- IO Supply Voltages from 1.2V to 3.3V and SPC/SPD Supply Voltages from 1.8V to 3.3V.
- Programmable power management
- Device fully programmable through serial port or can automatically load firmware from Chrontel Boot ROM (CH9904)
- Offered in a 88-pin QFN package

APPLICATION

- Mobile Phones / Tablet Devices
- Smartbooks / Ultrabooks
- Digital Cameras
- DVD Players or Recorders
- Portable Media Players

GENERAL DESCRIPTION

The Chrontel CH7035B is specifically designed for consumer electronics device and PC markets which multiple high definition content display formats are required. With its advanced video encoder, flexible scaling engine and easy-to-configure audio interface, the CH7035B satisfies manufactures' products display requirements and reduce their costs of development and time-to-market.

The CH7035B's 24-bit parallel bus accepts a wide range of input data formats from the graphic controller. The built-in video port supports 8/12/16/18/24-bit data interface as well as 80/86 MPU interface. The video format conversion module is capable of translating digital RGB-565, RGB-666, RGB-888 or YCrCb (ITU-R 656, ITU-R 601) signal to the DVI signal, combining with the audio stream. The device's video capture block supports input display resolution for up to 1366x768 which can be either interlaced or non-interlaced timing.

The CH7035B has incorporated a high speed SDRAM to help manufactures design their product to achieve simultaneous LCD and DVI display. A sophisticated frame rate conversion technology in the device's scaler retrieves LCD data from the SDRAM frame buffer, and increases the native display resolution up to 1080p DVI display. Furthermore, the CH7035B provides additional image manipulation features including image rotation, which can be implemented through programming internal registers.

The device supports both SPDIF and 2-channel I²S digital audio input. Its high fidelity audio decoder engine has the capability of sampling audio frequency for up to 192k/2ch. The SPIDF supports PCM encoded data and compressed audio including Dolby Digital and DTS.

The CH7035B has an image enhancement function that can fine tune brightness, contrast, hue and saturation down to the pixel-level.

When the HPD signal is asserted, the CH7035B will automatically generate an interrupt to the processor. A build-in DDC port can read the EDID data from DVI monitor through programming. registers by the processor.

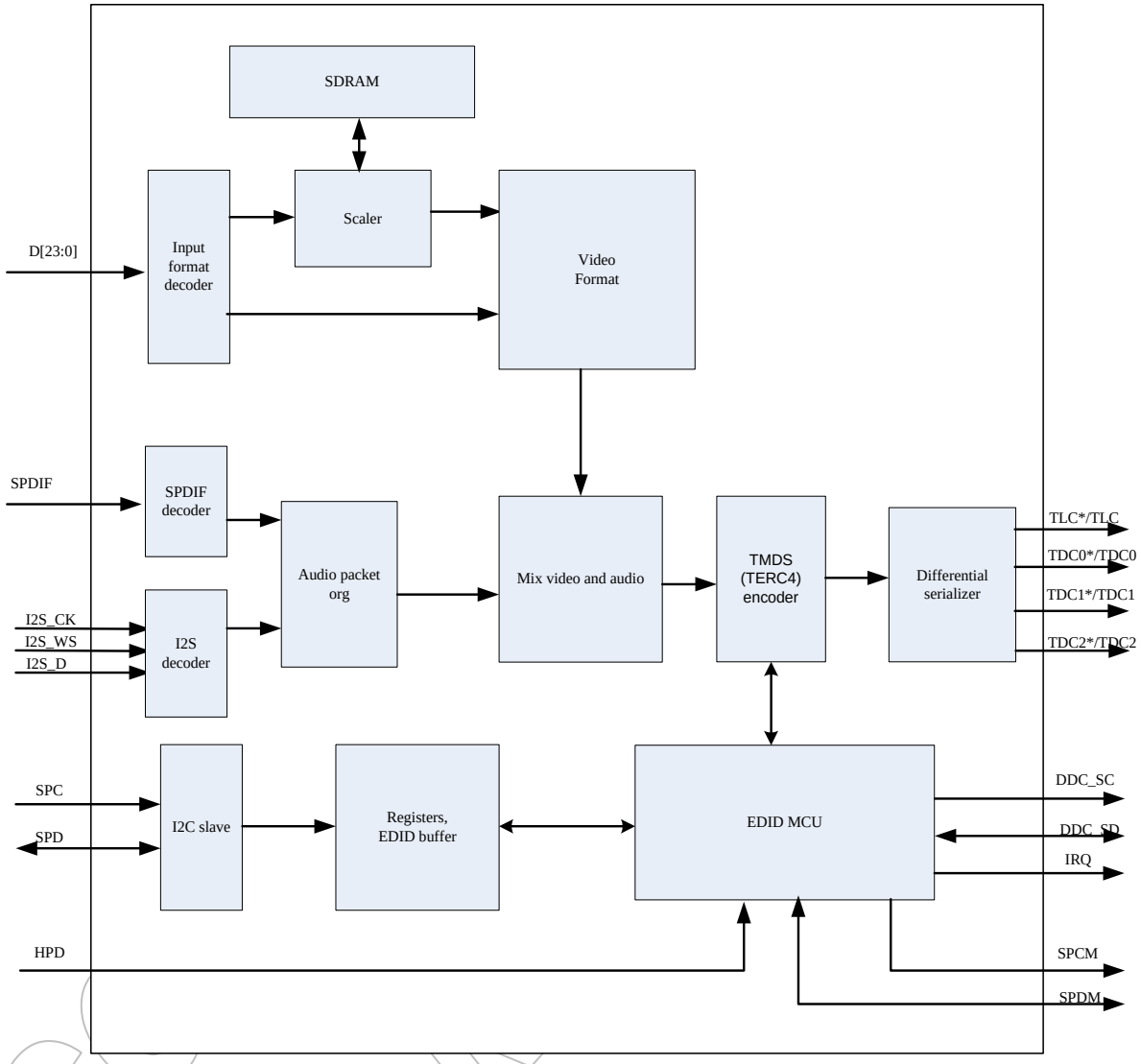

Figure 1: Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

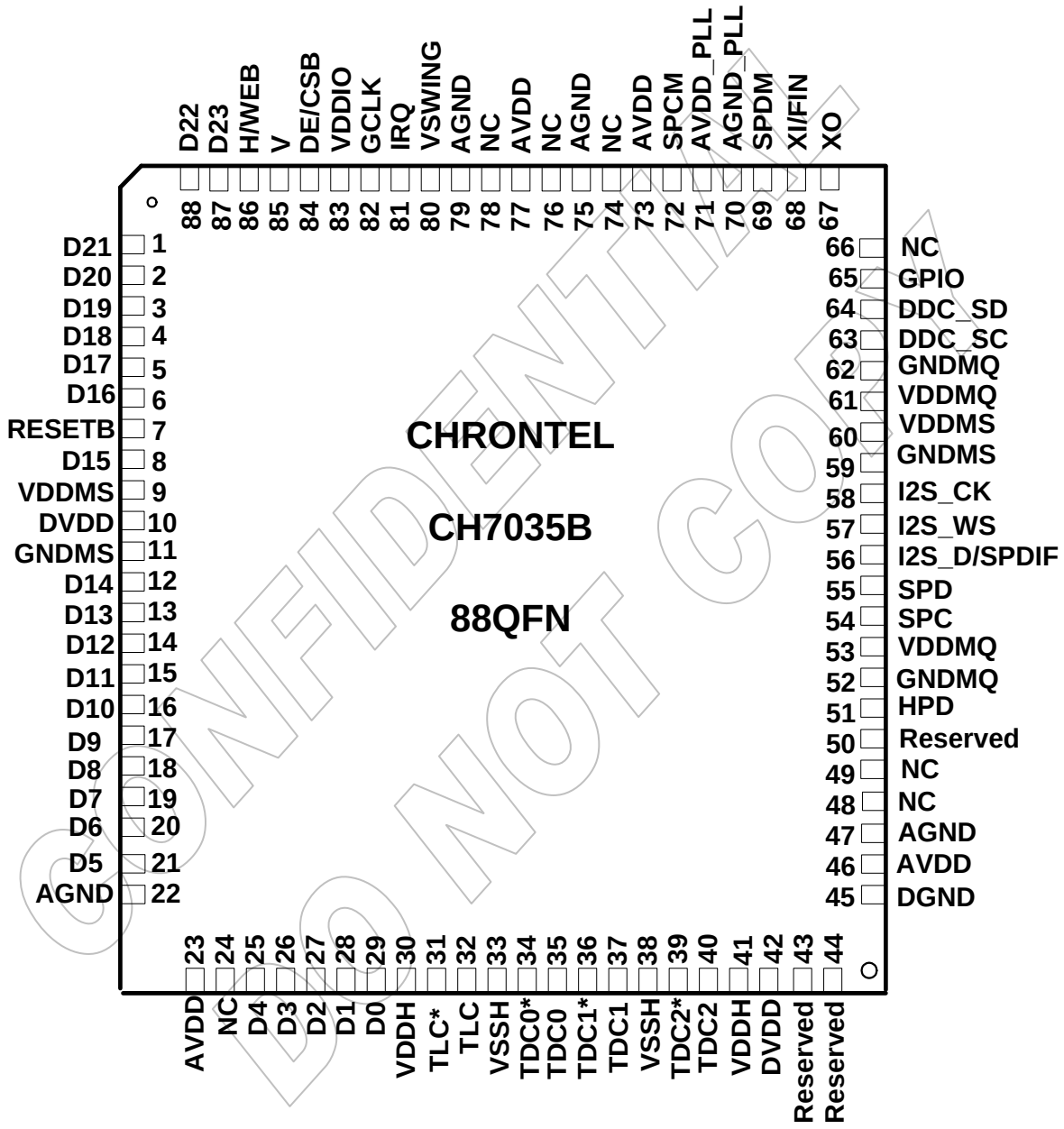

Figure 2: 88 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions (QFN88 Package)

Pin #	Type	Symbol	Description
1~6,8, 12~21, 25~29, 87~88,	In	D[23:0]	**Data Input** These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. All the unused Data input pins should be pulled low with 10KΩ resistors or shorted to Ground directly.
7	In	RESETB	**Reset Input** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
31,32	Out	TLC*,TLC	**DVI Clock Outputs** These pins provide the differential clock output for the DVI .
34,35	Out	TDC0*,TDC0	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0
36,37	Out	TDC1*,TDC1	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1
39,40	Out	TDC2*,TDC2	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2
43	N/A	Reserved	**Reserved** This pin should connect to DVDD directly
44	N/A	Reserved	**Reserved** This pin should connect to DGND directly
50	N/A	Reserved	**Reserved** This pin should be left open or pulled low with a 10 KΩ resistor in the application.
51	In	HPD	**Hot Plug Detect** This input pin determines whether the DVI output driver is connected to a DVI monitor. This pin should be pull low with 47 KΩ Resistor.
54	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required.
55	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required.
56	In	I2S_D/SPDIF	**I2S Data input or SPDIF Audio Signal Input** In default, this pin is configured to SPDIF audio signal input. The signal level is 0-2.5V. I2S audio input can be configured through programming CH7035B registers.
57	In	I2S_WS	**I2S Channel Select Signal**
58	In	I2S_CK	**I2S Clock Signal**
63	Out	DDC_SC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up 1.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
64	In/out	DDC_SD	**Routed Serial Port Data to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up 1.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused
65	In/out	GPIO	**General Purpose Input Output**
67	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and

Pin #	Type	Symbol	Description
			XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
68	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
69	In/Out	SPDM	**Routed Serial Port Data to CH9904 BOOT ROM** This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if unused.
72	Out	SPCM	**Routed Serial Port Clock Output to CH9904 BOOT ROM** This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
80	In	VSWING	**VSWING** This pin sets the swing level of the DVI outputs. A 1.2 KW (1 %) resistor should be connected between this pin and AGND using short and wide traces.
81	Out	IRQ	**Programmed Interrupt output.**
82	In	GCLK	**External Clock Inputs** The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
84	In	DE/CSB	**Data Input Indicator** When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.
85	In/out	V	**Vertical Sync Input/Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
86	In/out	H/WEB	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.
24, 48, 49, 66, 74, 76, 78	N/A	NC	**Not Connect** These pins should be left open.
9,60	Power	VDDMS	**SDRAM Power Supply (3.3V)**
59,11	Power	GNDMS	**SDRAM Ground**
10,42	Power	DVDD	**Digital Power Supply (1.8V)**
45	Power	DGND	**Digital Ground**
23, 46, 73, 77	Power	AVDD	**Analog Power Supply (3.3V)**
22, 47, 75, 79	Power	AGND	**Analog Ground**
30,41	Power	VDDH	**DVI Power Supply (3.3V)**

Pin #	Type	Symbol	Description
33,38	Power	VSSH	**DVI Ground**
53,61	Power	VDDMQ	**SDRAM output buffer Power Supply (3.3V)**
52,62	Power	GNDMQ	**SDRAM output buffer Ground**
71	Power	AVDD_PLL	**PLL Power Supply (1.8V)**
70	Power	AGND_PLL	**PLL Ground**
83	Power	VDDIO	**IO Power Supply (1.2-3.3V)**

2.0 PACKAGE DIMENSIONS

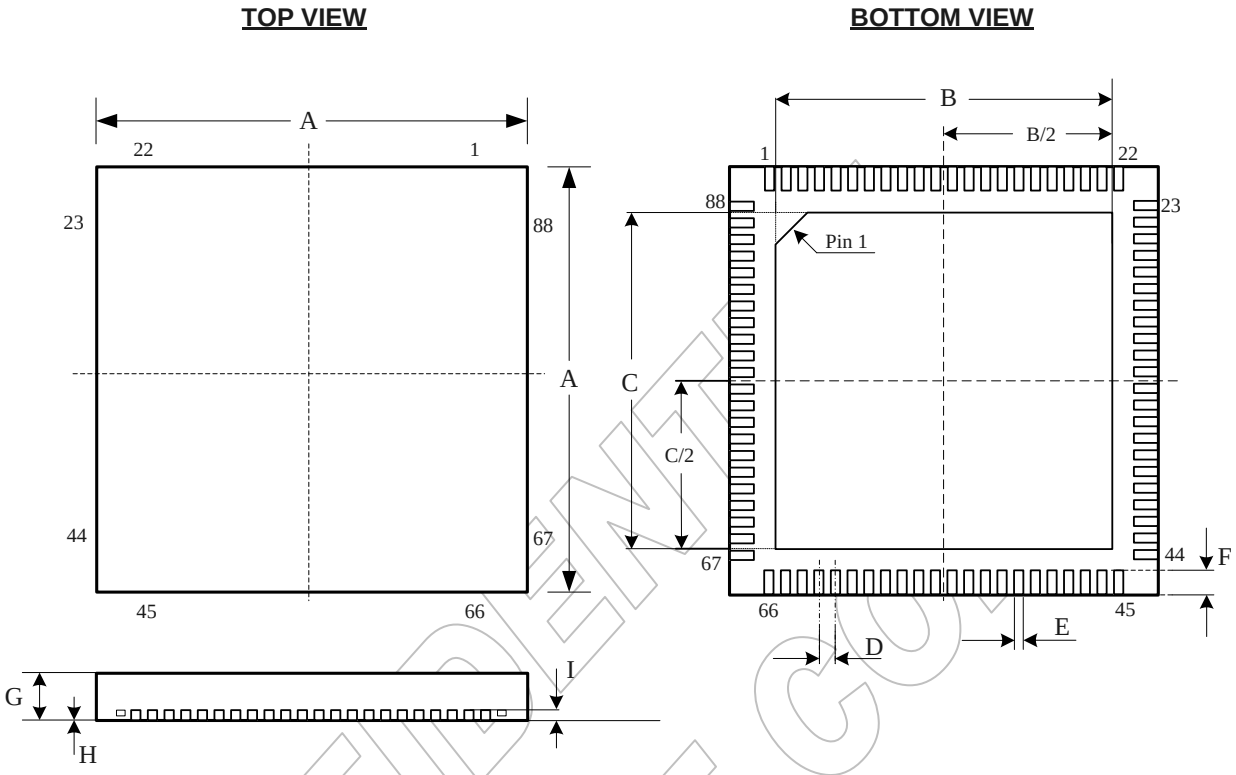

Figure 3: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		SYMBOL								
88 (10 X 10 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	9.90	6.65	6.65	0.30	0.15	0.40	0.80	0	0.20
	NOM	10.00	6.75	6.75	0.40	0.20	0.50	0.85	-	
	MAX	10.10	6.85	6.85	0.50	0.25	0.60	0.90	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7035B-BF	88QFN, Lead-free	Commercial : -20 to 70°C	168/Tray
CH7035B-BFI	88QFN, Lead-free	Industrial : -40 to 85°C	168/Tray

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