

Automotive P-Channel 40 V (D-S) 175 °C MOSFET

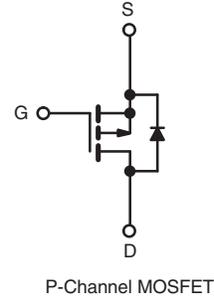
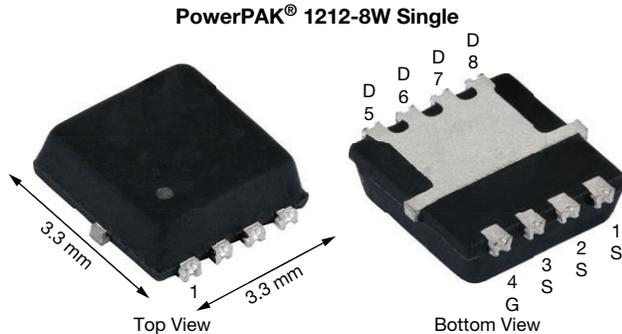
 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	-40
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.029
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.047
I_D (A)	-16
Configuration	Single
Package	PowerPAK 1212-8W

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912


Marking Code: Q023

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25$ °C	I_D	-16	A
	$T_C = 125$ °C		-16	
Continuous Source Current (Diode Conduction) ^a		I_S	-16	
Pulsed Drain Current ^b		I_{DM}	-64	
Single Pulse Avalanche Current	$L = 0.1$ mH	I_{AS}	-26	mJ
Single Pulse Avalanche Energy			E_{AS}	
Maximum Power Dissipation ^b	$T_C = 25$ °C	P_D	62.5	W
	$T_C = 125$ °C		20	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	81	°C/W
Junction-to-Case (Drain)			R_{thJC}	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



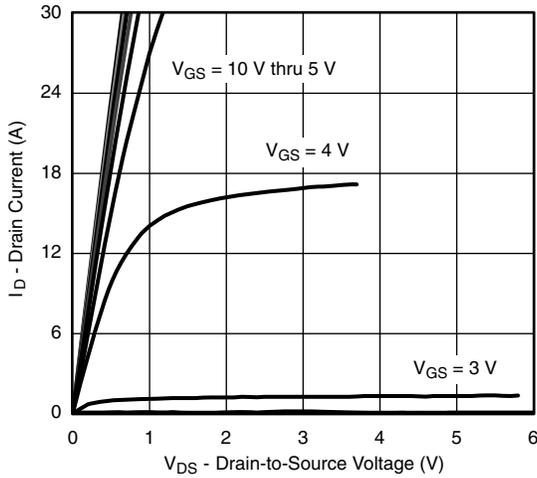
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-1.5	-2.0	-2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -40 V	-	-	-1	μA
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 125 °C	-	-	-50	
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 175 °C	-	-	-150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≥ 5 V	-20	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V	I _D = -12 A	-	0.020	0.029	Ω
		V _{GS} = -10 V	I _D = -12 A, T _J = 125 °C	-	0.030	0.043	
		V _{GS} = -10 V	I _D = -12 A, T _J = 175 °C	-	0.040	0.051	
		V _{GS} = -4.5 V	I _D = -9 A	-	0.035	0.047	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -7 A		-	12	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = -20 V, f = 1 MHz	-	1565	1875	pF
Output Capacitance	C _{oss}			-	245	295	
Reverse Transfer Capacitance	C _{rss}			-	170	205	
Total Gate Charge ^c	Q _g	V _{GS} = -4.5 V	V _{DS} = -20 V, I _D = -9.3 A	-	17.7	21.2	nC
Gate-Source Charge ^c	Q _{gs}			-	5.6	6.6	
Gate-Drain Charge ^c	Q _{gd}			-	8.1	9.7	
Gate Resistance	R _g	f = 1 MHz		1.1	1.95	2.8	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -20 V, R _L = 14.2 Ω I _D ≅ -1.4 A, V _{GEN} = -10 V, R _g = 1 Ω	-	11	14	ns	
Rise Time ^c	t _r		-	10	13		
Turn-Off Delay Time ^c	t _{d(off)}		-	36.5	44		
Fall Time ^c	t _f		-	10.2	13		
Source-Drain Diode Ratings and Characteristic ^b							
Pulsed Current ^a	I _{SM}			-	-	-64	A
Forward Voltage	V _{SD}	I _F = -8.8 A, V _{GS} = 0 V		-	-0.8	-1.1	V

Notes

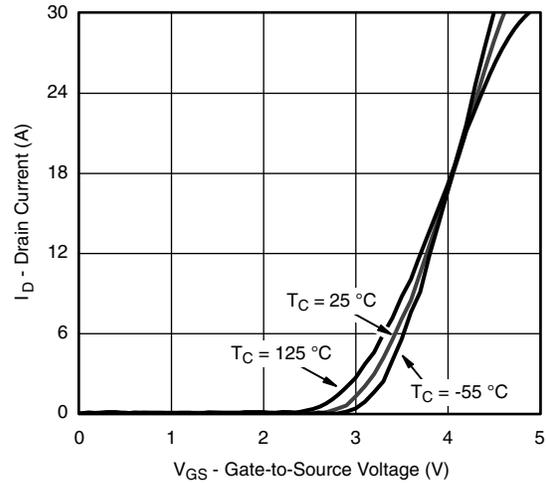
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

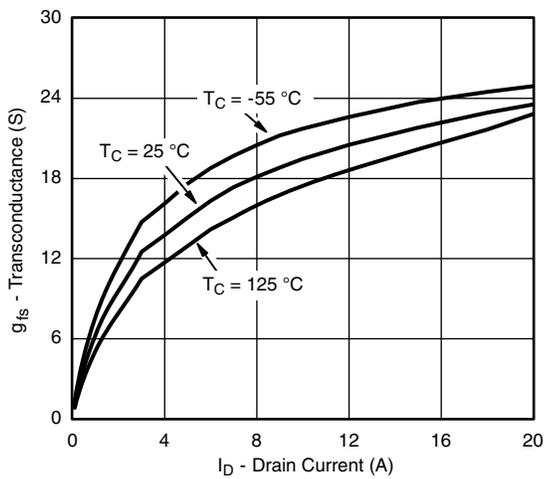
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



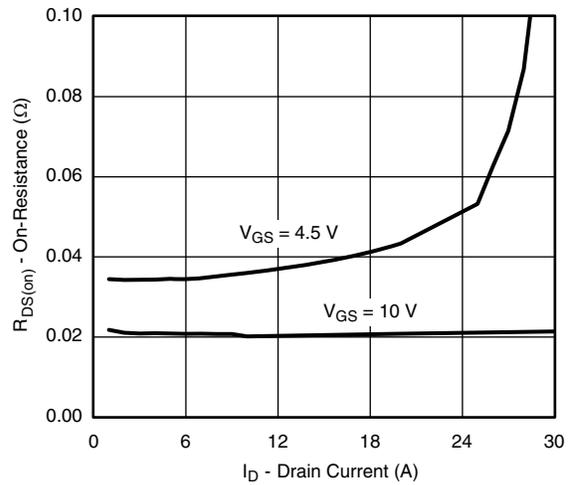
Output Characteristics



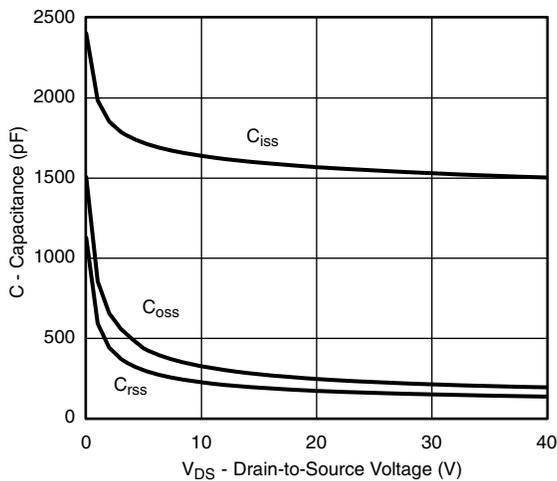
Transfer Characteristics



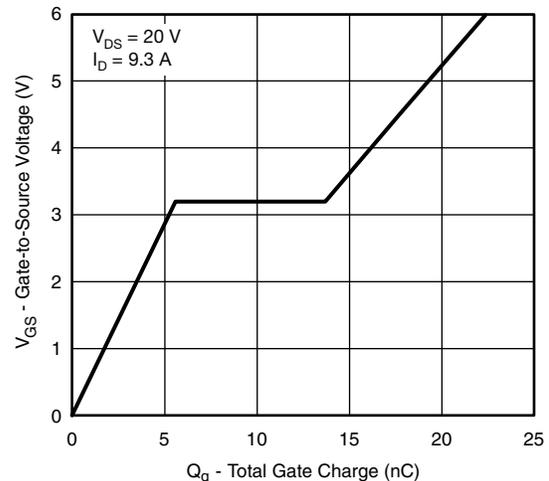
Transconductance



On-Resistance vs. Drain Current



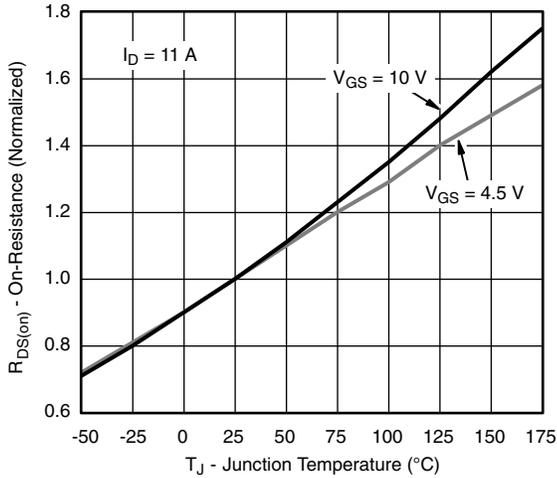
Capacitance



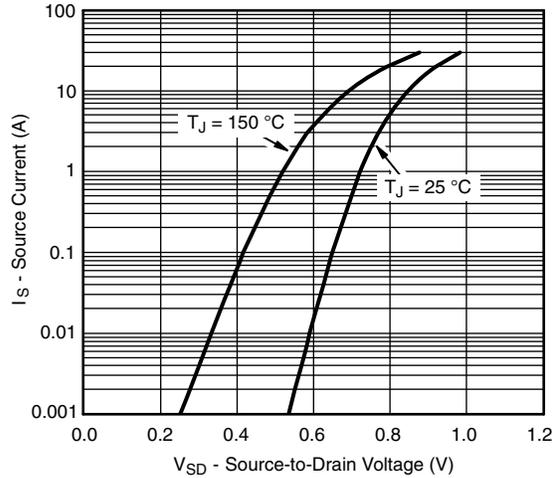
Gate Charge



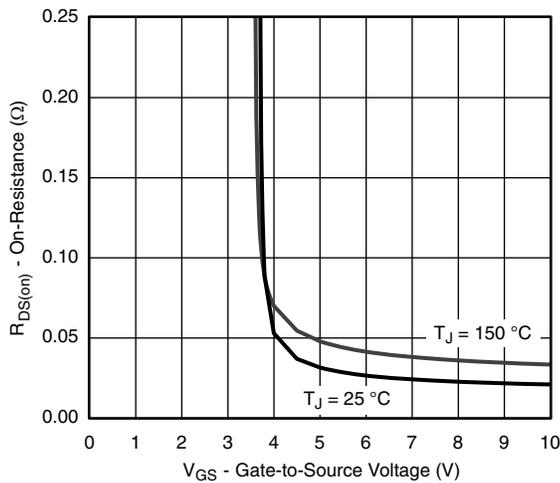
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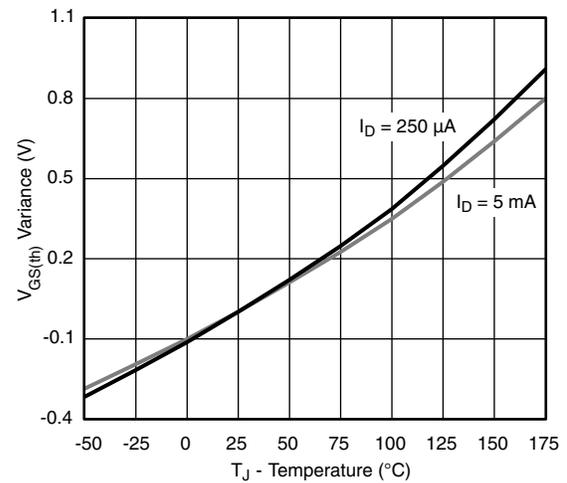
On-Resistance vs. Junction Temperature



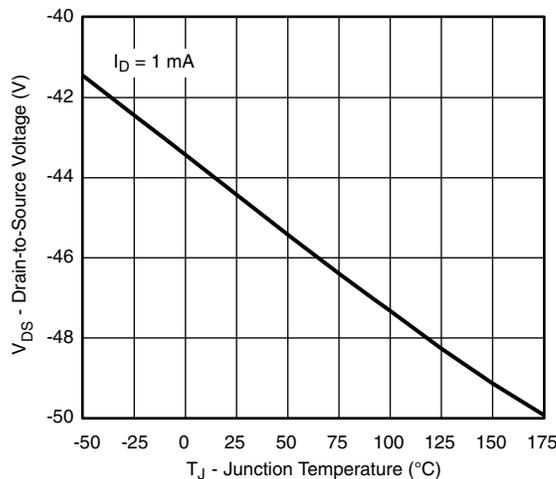
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



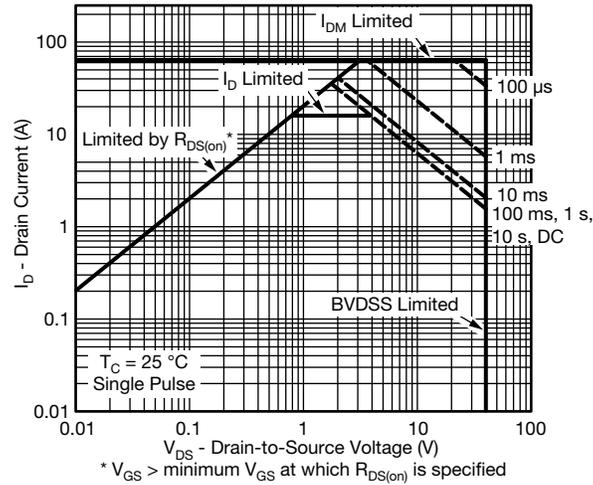
Threshold Voltage



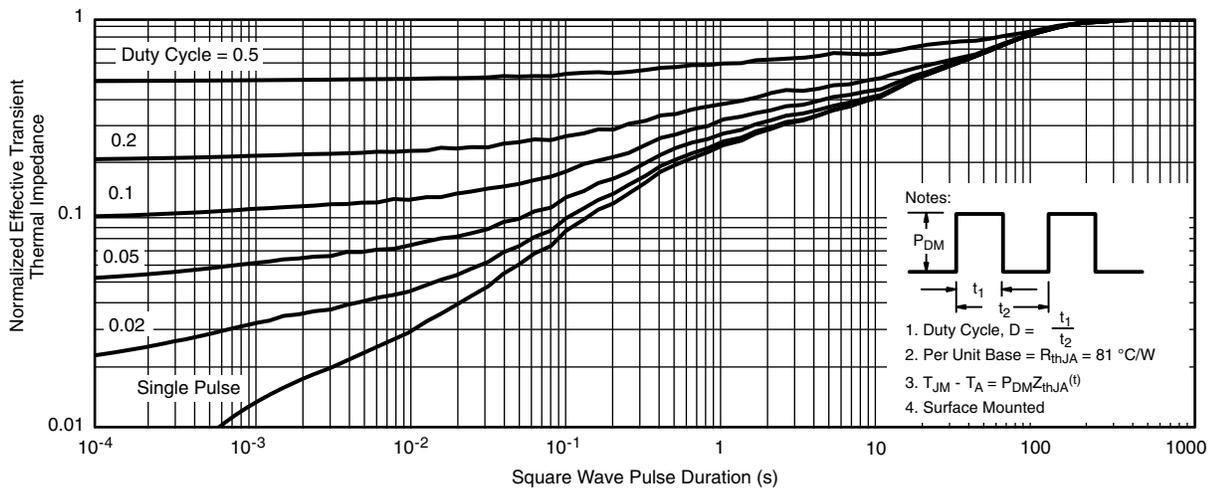
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



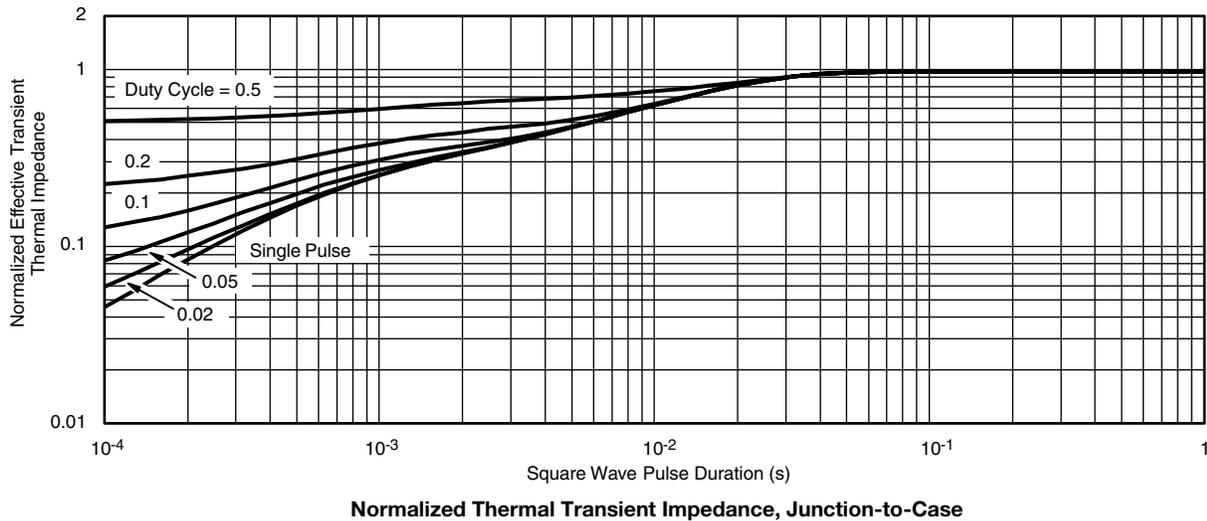
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67977.



PowerPAK® 1212-8 and PowerPAK 1212-8W

Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK 1212-8 and PowerPAK 1212-8W packages:

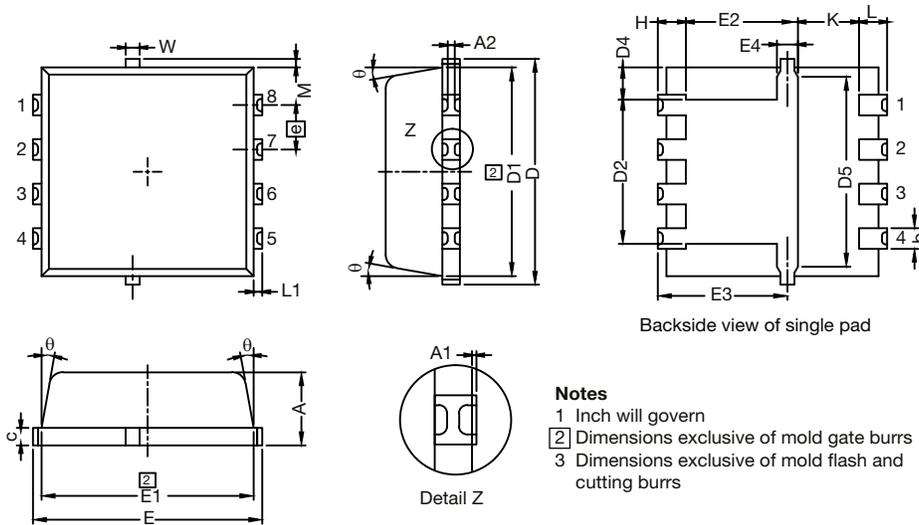
DATASHEET PART NUMBER	OLD ORDERING CODE ^a	NEW ORDERING CODE
SQ7414AEN	SQ7414AEN-T1-GE3	SQ7414AEN-T1_GE3
SQ7414AENW	-	SQ7414AENW-T1_GE3
SQ7415AEN	SQ7415AEN-T1-GE3	SQ7415AEN-T1_GE3
SQ7415AENW	-	SQ7415AENW-T1_GE3
SQS401EN	SQS401EN-T1-GE3	SQS401EN-T1_GE3
SQS401ENW	-	SQS401ENW-T1_GE3
SQS405EN	SQS405EN-T1-GE3	SQS405EN-T1_GE3
SQS405ENW	-	SQS405ENW-T1_GE3
SQS420EN	SQS420EN-T1-GE3	SQS420EN-T1_GE3
SQS423EN	SQS423EN-T1-GE3	SQS423EN-T1_GE3
SQS460EN	SQS460EN-T1-GE3	SQS460EN-T1_GE3
SQS462EN	SQS462EN-T1-GE3	SQS462EN-T1_GE3
SQS482EN	SQS482EN-T1-GE3	SQS482EN-T1_GE3
SQS484EN	SQS484EN-T1-GE3	SQS484EN-T1_GE3
SQS490EN	SQS490EN-T1-GE3	SQS490EN-T1_GE3
SQS840EN	SQS840EN-T1-GE3	SQS840EN-T1_GE3
SQS850EN	SQS850EN-T1-GE3	SQS850EN-T1_GE3

Note

a. Old ordering code is obsolete and no longer valid for new orders



PowerPAK® 1212-8W Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
A2	0	-	0.13	0	-	0.005
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D4	0.47 typ.			0.0185 typ.		
D5	2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 typ.			0.013 typ.		
e	0.65 BSC.			0.026 BSC		
K	0.86 typ.			0.034 typ.		
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: C15-1530-Rev. B, 16-Nov-15
 DWG: 6032



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