



# SPP7001K

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP7001K is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

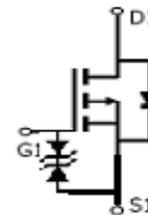
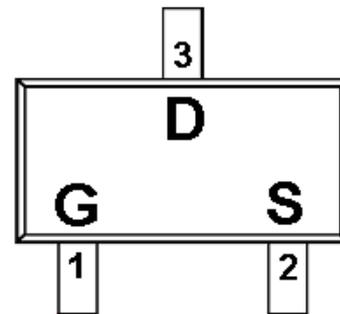
### FEATURES

- ◆ -60V/-0.5A, $R_{DS(ON)}=6\Omega@V_{GS}=-10V$
- ◆ -60V/-0.25A, $R_{DS(ON)}=10\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ ESD protected
- ◆ SOT-23 package design

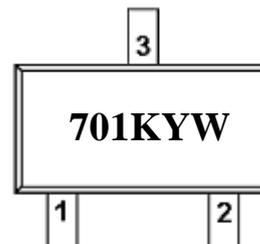
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOT-23)



### PART MARKING



Y : Year Code  
W : Week Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP7001KS23RGB	SOT-23	701K

※ Week Code : A ~ Z ( 1 ~ 26 ) ; a ~ z ( 27 ~ 52 )

※ SPP7001KS23RGB : Tape Reel ; Pb – Free; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-60	V	
Gate –Source Voltage	V <sub>GSS</sub>	±30	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-0.5	A
		TA=70°C	-0.3	
Pulsed Drain Current	I <sub>DM</sub>	-1	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-0.5	A	
Power Dissipation	P <sub>D</sub>	TA=25°C	1.25	W
		TA=70°C	0.8	
Operating Junction Temperature	T <sub>J</sub>	150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	375	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 10$	$\mu A$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$			-1	$\mu A$
		$V_{DS}=-60V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-10V$	-1			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-0.5A$			6	$\Omega$
		$V_{GS}=-4.5V, I_D=-0.25A$			10	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-0.5A$		1		S
Diode Forward Voltage	$V_{SD}$	$I_S=-0.2A, V_{GS}=0V$			-1.5	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-30V, V_{GS}=-15V$ $I_D=-0.5A$		2		nC
Gate-Source Charge	$Q_{gs}$			0.53		
Gate-Drain Charge	$Q_{gd}$			0.72		
Input Capacitance	$C_{iss}$	$V_{DS}=-25V, V_{GS}=0V$ $f=1MHz$		25		pF
Output Capacitance	$C_{oss}$			13		
Reverse Transfer Capacitance	$C_{rss}$			7.3		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-25V, I_D=-200mA,$ $V_{GEN}=-10V$		20		nS
Turn-Off Time	$t_{d(off)}$			35		

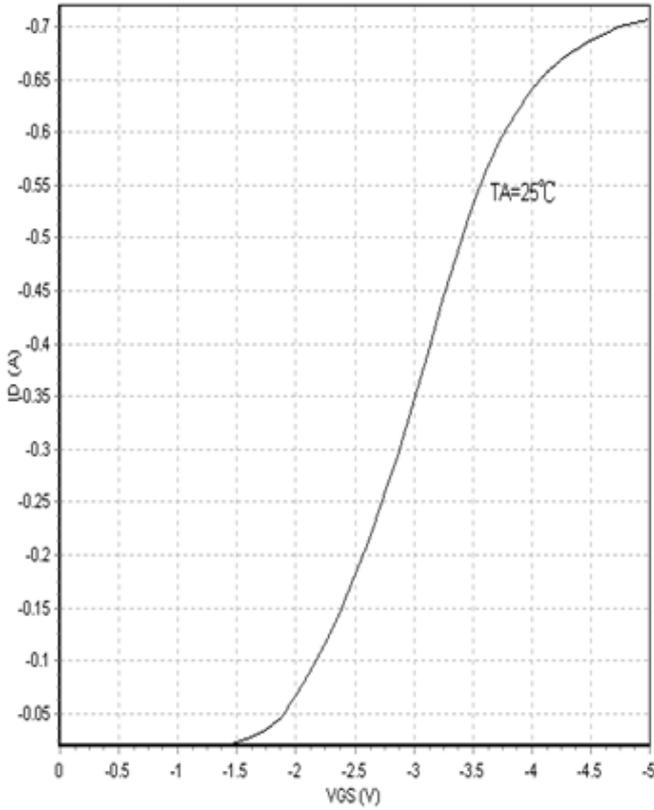


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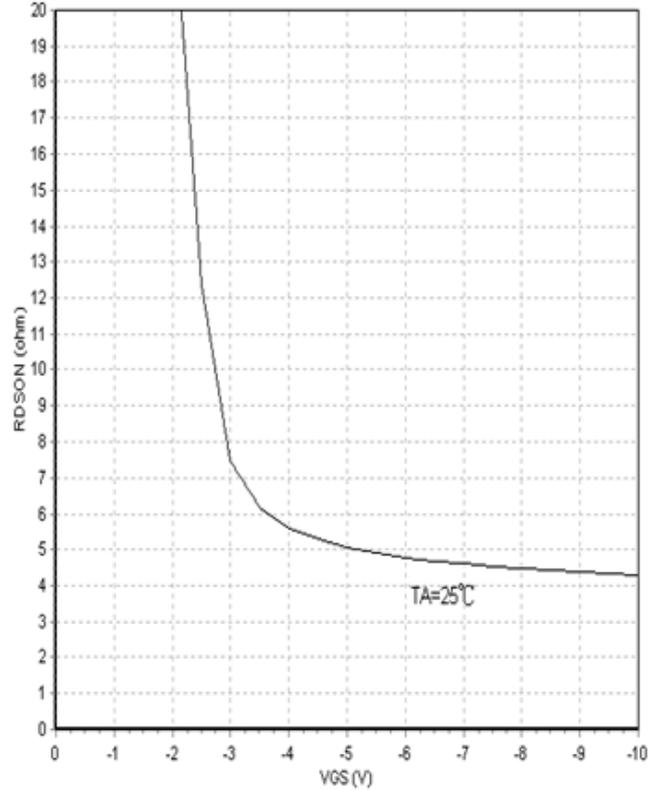
## P-Channel Enhancement Mode MOSFET

### TYPICAL CHARACTERISTICS

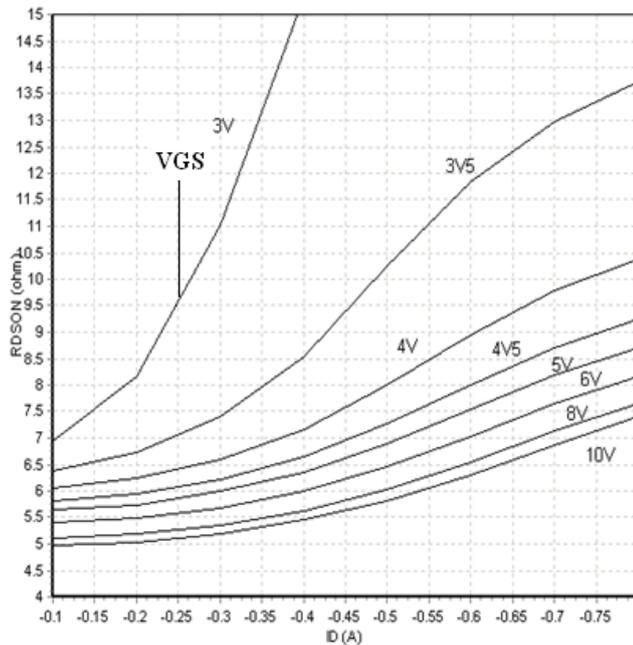
#### Drain-Current vs. Gate-Source Voltage



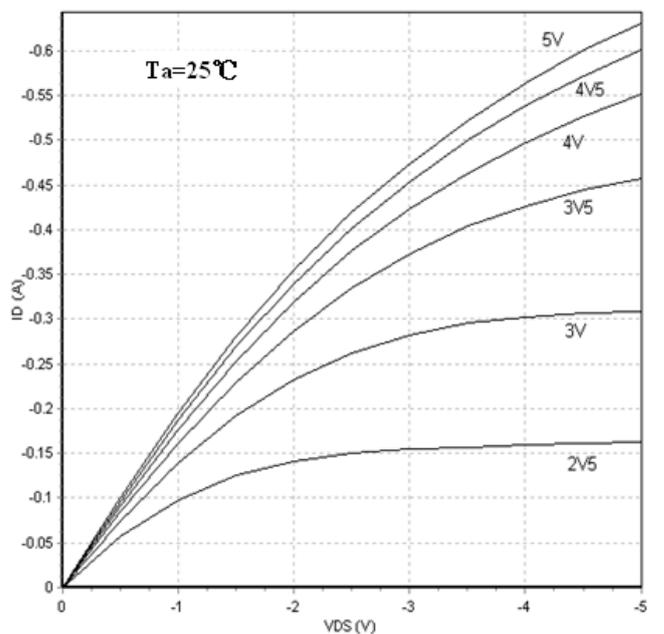
#### On-Resistance vs. Gate-Source Voltage



#### On-Resistance vs. Drain-Current



#### Drain-Source Current vs. Drain-Source Voltage



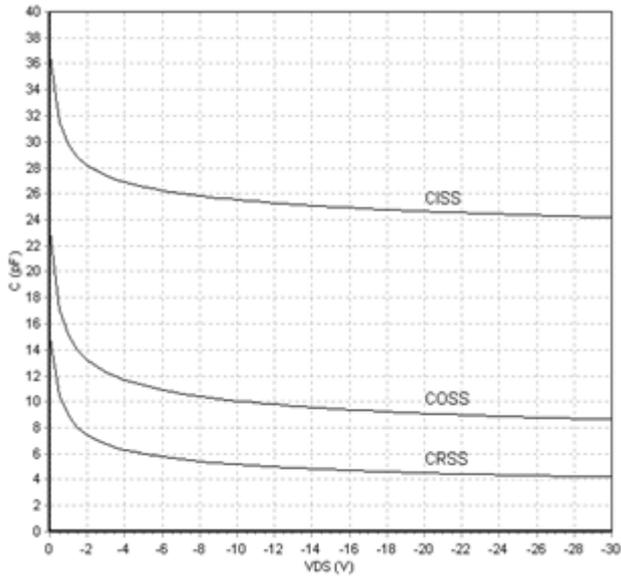


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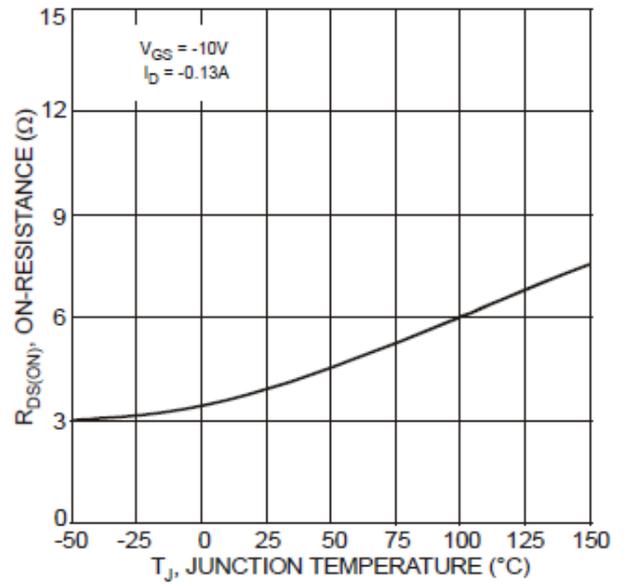
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### TYPICAL CHARACTERISTICS

Capacitance vs. Drain-Source Voltage



On-Resistance vs. Drain-Current





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