



4N40

Power MOSFET

4A, 400V N-CHANNEL POWER MOSFET

DESCRIPTION

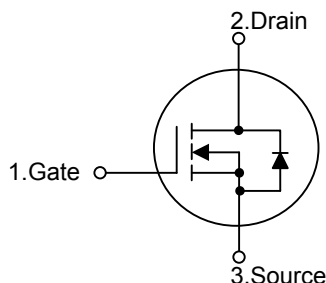
The UTC **4N40** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **4N40** is universally applied in electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

FEATURES

- * High switching speed
- * $R_{DS(ON)} < 1.5\Omega$ @ $V_{GS}=10V$, $I_D=2A$
- * 100% avalanche tested

SYMBOL

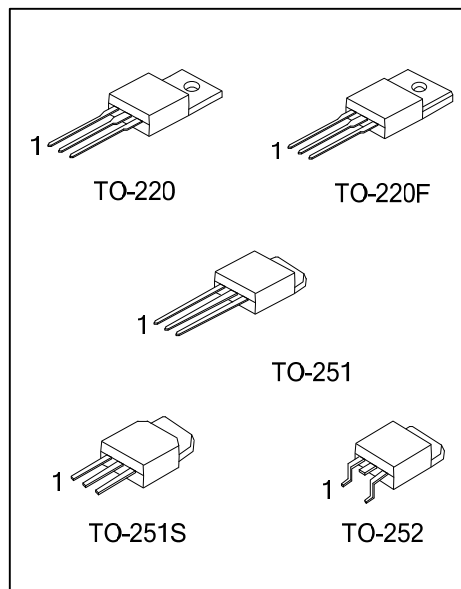


ORDERING INFORMATION

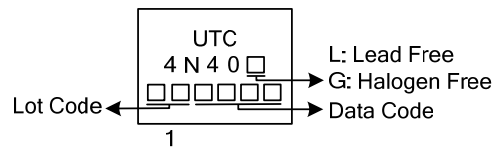
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N40L-TA3-T	4N40G-TA3-T	TO-220	G	D	S	Tube
4N40L-TF3-T	4N40G-TF3-T	TO-220F	G	D	S	Tube
4N40L-TM3-T	4N40G-TM3-T	TO-251	G	D	S	Tube
4N40L-TMS-T	4N40G-TMS-T	TO-251S	G	D	S	Tube
4N40L-TN3-R	4N40G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

4N40L-TA3-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF3: TO-220F, TM3: TO-251 TMS: TO-251S, TN3: TO-252 (3) L: Lead Free, G: Halogen Free and Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	400	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^{\circ}\text{C}$)	I_D	4	A
	Pulsed (Note 1)	I_{DM}	8	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	140	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation	TO-220	P_D	60	W
	TO-220F		27	W
	TO-251/TO-251S/TO-252		52	W
Derate above 25°C	TO-220		0.48	W/ $^{\circ}\text{C}$
	TO-220F		0.22	W/ $^{\circ}\text{C}$
	TO-251/TO-252		0.41	W/ $^{\circ}\text{C}$
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. $L=18\text{mH}$, $I_{AS}=4\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F	θ_{JA}	62.5	$^{\circ}\text{C/W}$
	TO-251/TO-251S/TO-252		110	
Junction to Case	TO-220	θ_{JC}	2.08	$^{\circ}\text{C/W}$
	TO-220F		4.5	
	TO-251/TO-251S/TO-252		2.4	

■ ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$, unless otherwise specified)

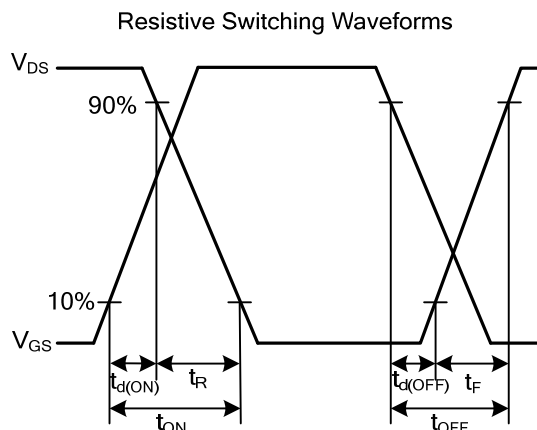
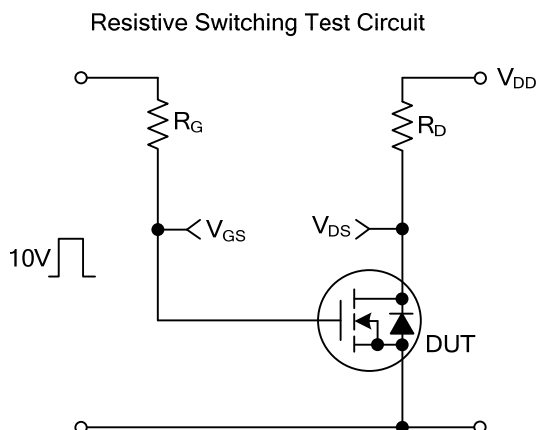
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	400			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =400V, V _{GS} =0V			1	μA
			V _{DS} =320V, T _C =125°C			100	μA
Gate- Source Leakage Current	Forward	I _{GSS}	V _{GS} =+30V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-30V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =2A			1.8	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		315		pF
Output Capacitance		C _{OSS}			120		pF
Reverse Transfer Capacitance		C _{RSS}			40		pF
SWITCHING PARAMETERS							
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =30V, I _D =0.5A, R _G =25Ω (Note 2, 3)		30		ns
Rise Time		t _R			60		ns
Turn-OFF Delay Time		t _{D(OFF)}			100		ns
Fall-Time		t _F			68		ns
Total Gate Charge		Q _G	V _{DD} =50V, I _D =1.3A, V _{GS} =10V, I _G =100μA		18.5	30	nC
Gate-Source Charge		Q _{GS}			4.5		nC
Gate-Drain Charge		Q _{GD}			5.5		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V _{SD}	I _S =4A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =4A, V _{GS} =0V, dI _F /dt=100A/μs(Note 2)		800		ns

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

3. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS



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