ISOFACE™

ISO2H823V2.5

Galvanic Isolated 8 Channel High-Side Switch

Datasheet

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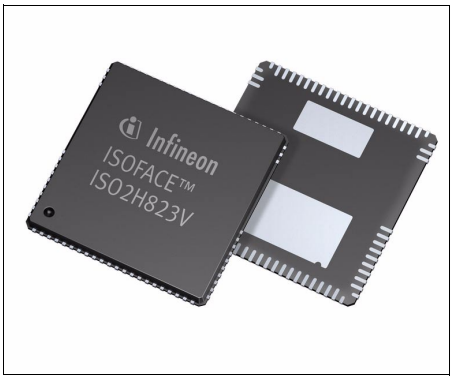
1 Overview



PG-VQFN-70-2

Infineon Technologies 2nd generation ISOFACE™ 8-channel high-side driver IC ISO2H823V2.5 offers integrated 2.5kV galvanic isolation, thus meets the IEC 61131-2 requirements for reinforced isolation. Concurrently, the ISO2H823V2.5 sets a new standard for system-level diagnostics. Each of the 8 channels is equipped with 5-fold diagnostic monitoring capabilities: Open Load (Active Mode - Driver On and Inactive Mode - Driver Off) , Short-to-Vbb, Overcurrent (= Short-to-GND), Overtemperature.
With the ever increasing level of complexity and integration in industrial control systems comprehensive diagnostic monitoring is highly valuable in a vast range of industrial applications, both for preventive maintenance as well as to shorten costly un-scheduled down-times

Product Highlights

- 2.5 kV Galvanic isolation integrated (UL508 & CSA22.2 certified)
  Meets IEC 61131-2 requirements for reinforced isolation
- 8 - channel high-side switches of 0.6 A each
- 5 different types of diagnostic feedback for each channel
- µController compatible 8-bit parallel/serial interface
- 12 mm x 12 mm PG-VQFN-70-2 package

Key Features

- Interface 3.3V CMOS operation compatible
- Parallel/Serial µC interface
- High common mode transient immunity
- Integrated Diagnostics:
  – 5 different types for diagnostic feedback per output channel
  – 5 types of diagnostic feedback on global level
- Common output disable pin
- Common error indication pin
- Resynchronization to achieve a low-jitter switching on and off of high-side switches
- Active output current limitation for short circuit protection
- Reverse Output Voltage protection
- Undervoltage shutdown with autorestart and hysteresis
- Integrated clamping to switch inductive loads up to 150 mJ energy per channel
- Thermal shutdown and diagnostics per channel with auto-restart
- V_{BB} range from 11 V to 35 V designed for 24 V systems

Type	Package
ISO2H823V2.5	PG-VQFN-70-2

- ESD protection
- RoHS compliant

Typical Application

- Isolated switch for industrial applications:
  PLC, distributed control systems, industial PCs, robotics, etc.
- All types of resistive, inductive and capacitive loads
- µController compatible power switch for 24 V DC applications
- Driver for solenoid, relays and resistive loads

Description

The ISO2H823V2.5 is a galvanically isolated 8-bit data interface in PG-VQFN-70-2 package that provides 8 fully protected high-side power switches that are able to handle currents up to 730 mA per channel.

An 8-bit parallel µController compatible interface or a serial SPI-interface allows to connect the IC directly to a µController system. The input interface supports also a direct control mode for writing driver information and is designed to operate with 3.3 V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.

This product is the second generation of isolated 8 channel digital output device (ISO2H823V2.5) and provides a robust integrated diagnosis for switches with low R_{DSon} as well as an upgraded µController interface.

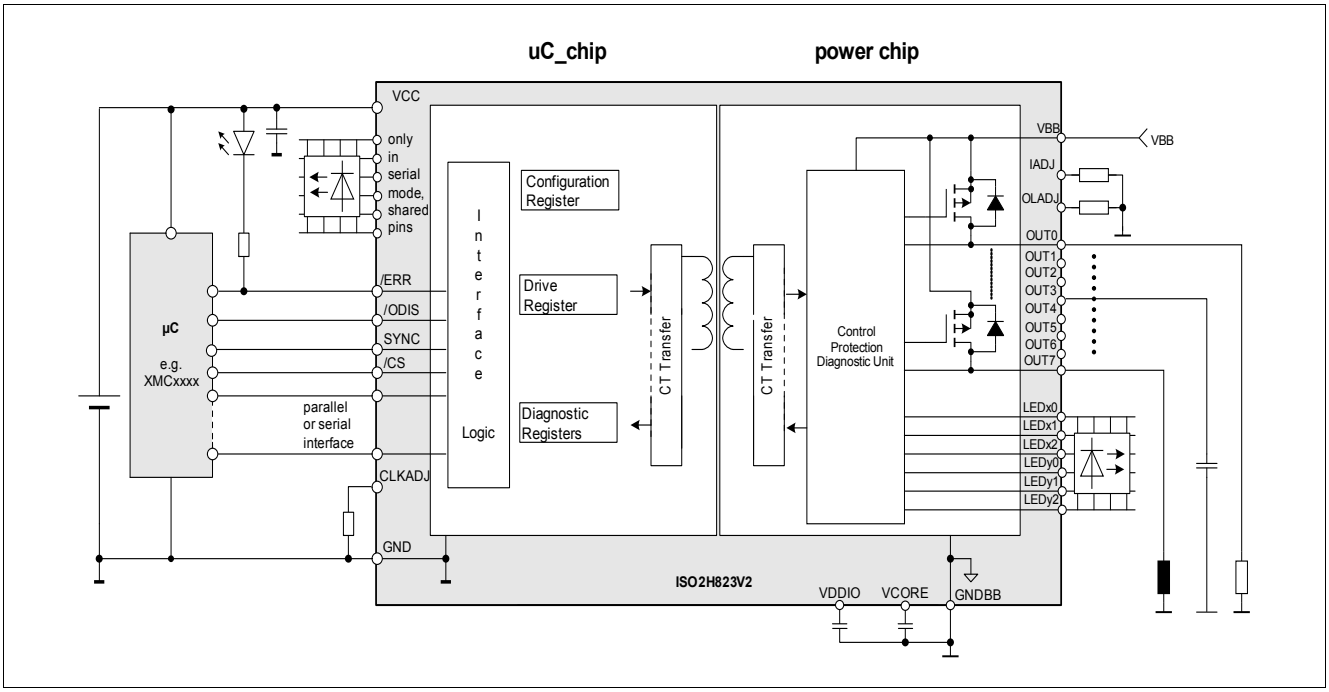


Figure 1 Typical Application

Infineon Ordering Code :

SP001225470

2 Pin Configuration and Functionality

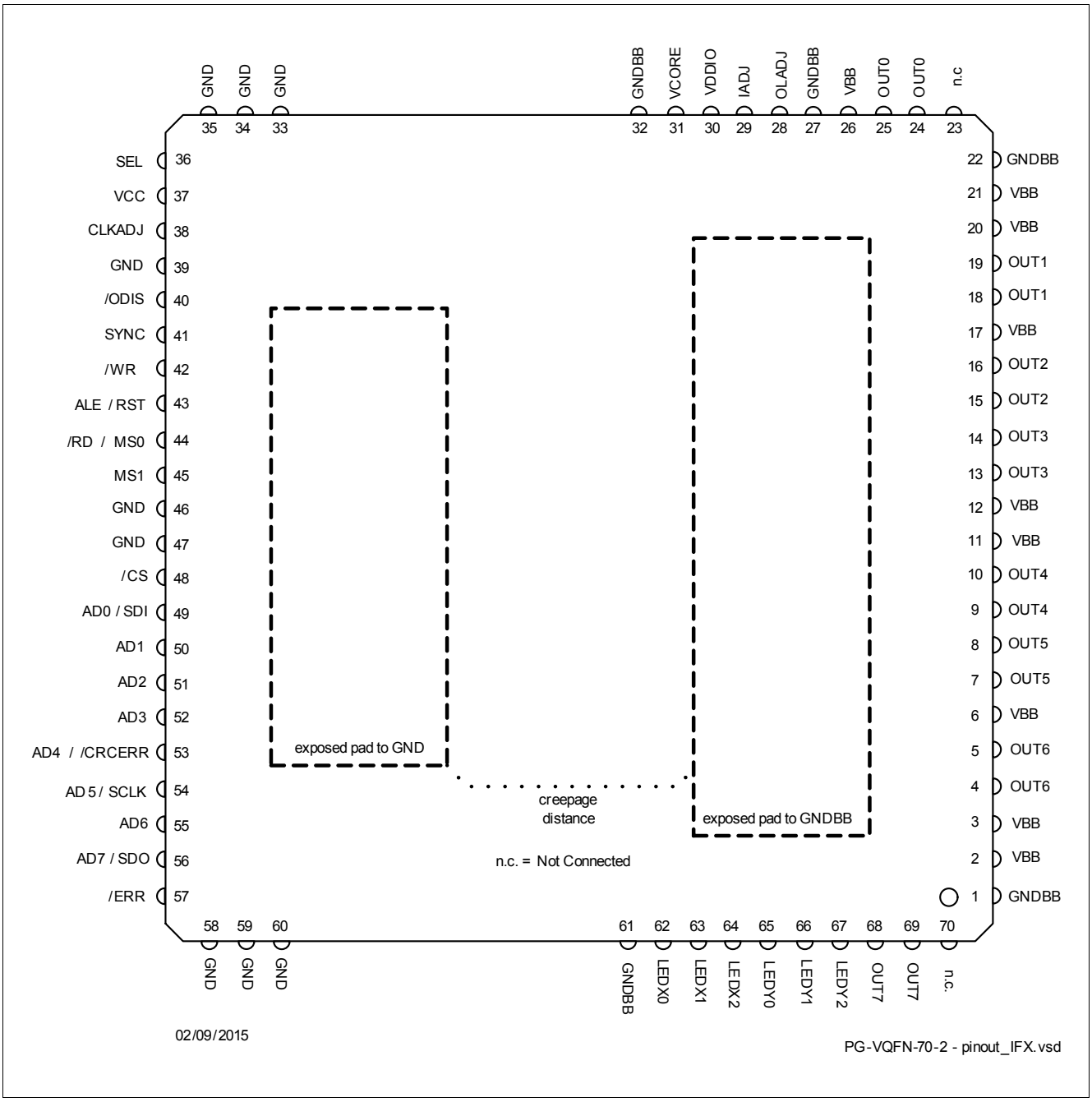


Figure 2 Power PG-VQFN-70-2 (430 mil)

Table 1 Pin Configuration

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
top side pins								
1	GNDBB		A	Output Stage Ground	GNDBB			
2	VBB		A	Output Stage Positive Supply	VBB			
3	VBB		A	Output Stage Positive Supply	VBB			
4	OUT6		A	Switch Output 6	OUT6			
5	OUT6		A	Switch Output 6	OUT6			
6	VBB		A	Output Stage Positive Supply	VBB			
7	OUT5		A	Switch Output 5	OUT5			
8	OUT5		A	Switch Output 5	OUT5			
9	OUT4		A	Switch Output 4	OUT4			
10	OUT4		A	Switch Output 4	OUT4			
11	VBB		A	Output Stage Positive Supply	VBB			
12	VBB		A	Output Stage Positive Supply	VBB			
13	OUT3		A	Switch Output 3	OUT3			
14	OUT3		A	Switch Output 3	OUT3			
15	OUT2		A	Switch Output 2	OUT2			
16	OUT2		A	Switch Output 2	OUT2			
17	VBB		A	Output Stage Positive Supply	VBB			
18	OUT1		A	Switch Output 1	OUT1			
19	OUT1		A	Switch Output 1	OUT1			
20	VBB		A	Output Stage Positive Supply	VBB			
21	VBB		A	Output Stage Positive Supply	VBB			
22	GNDBB		A	Output Stage Ground	GNDBB			
23	n.c.	not connected			n.c.	not connected		
24	OUT0		A	Switch Output 0	OUT0			
25	OUT0		A	Switch Output 0	OUT0			
26	VBB		A	Output Stage Positive Supply, Supply of Reference Voltages	VBB			
27	GNDBB		A	Output Stage Ground	GNDBB			

Table 1 Pin Configuration (cont'd)

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
28	OLADJ		A	Open Load Adjust	OLADJ			
29	IADJ		A	Current Reference Adjust	IADJ			
30	VDDIO		A	CT Blocking Capacitor	VDDIO			
31	VCORE		A	Digital Core Supply	VCORE			
32	GNDBB		A	Output Stage Ground	GNDBB			
gap used for creepage distance								
33	GND		A	Logic Ground	GND			
34	GND		A	Logic Ground	GND			
35	GND		A	Logic Ground	GND			
36	SEL	I	PD	Serial / Parallel Mode Select	SEL			
37	VCC		A	Positive 3.3 V logic supply	VCC			
38	CLKADJ		A	Clock Frequency Adjustment	CLKADJ			
39	GND		A	Logic Ground	GND			
40	$\overline{\text{ODIS}}$	I	PD	Output Disable	$\overline{\text{ODIS}}$			
41	SYNC	I	PU	Synchronize and Freeze Diagnostics	SYNC			
42	$\overline{\text{WR}}$	I	PU	Data Write Input	n.c.	high impedance "Z"		
43	ALE/RST	I	PD	Address Latch Enable / Reset	RST	I	PD	Reset
44	$\overline{\text{RD}}$	I	PU	Data Read Input	MS0	I	PD	SPI Mode Select bit 0
45	n.c.			not connected	MS1	I	PD	SPI Mode Select bit 1
46	GND		A	Logic Ground	GND			
47	GND		A	Logic Ground	GND			
48	$\overline{\text{CS}}$	I	PU	Chip Select	$\overline{\text{CS}}$			
49	AD0	IO	PPZ	Addr-Data in/output bit0	SDI	I	PD	SPI Data input
50	AD1	IO	PPZ	Addr-Data in/output bit1	n.c.			high impedance "Z"
51	AD2	IO	PPZ	Addr-Data in/output bit2	n.c.			high impedance "Z"
52	AD3	IO	PPZ	Addr-Data in/output bit3	n.c.			high impedance "Z"
53	AD4	IO	PPZ	Addr-Data in/output bit4	$\overline{\text{CRCERR}}$	OD	PU	CRC Error output
54	AD5	IO	PPZ	Addr-Data in/output bit5	SCLK	I	PD	SPI Shift Clock input
55	AD6	IO	PPZ	Addr-Data in/output bit6	n.c.			high impedance "Z"
56	AD7	IO	PPZ	Addr-Data in/output bit7	SDO	O	PPZ	SPI Data Output
57	$\overline{\text{ERR}}$	OD	PU	Fault indication	$\overline{\text{ERR}}$			
58	GND		A	Logic Ground	GND			
59	GND		A	Logic Ground	GND			
60	GND		A	Logic Ground	GND			
gap used for creepage distance								

Table 1 Pin Configuration (cont'd)

Pin	Parallel Interface Mode				Serial Interface Mode			
	Symbol	Ctrl [1]	Type [2]	Function	Symbol	Ctrl	Type	Function
61	GNDBB		A	Output Stage Ground	GNDBB			
62	LEDX0		A	LED Output Row 0	LEDX0			
63	LEDX1		A	LED Output Row 1	LEDX1			
64	LEDX2		A	LED Output Row 2	LEDX2			
65	LEDY0		A	LED Output Column 0	LEDY0			
66	LEDY1		A	LED Output Column 1	LEDY1			
67	LEDY2		A	LED Output Column 2	LEDY2			
68	OUT7		A	Switch Output 7	OUT7			
69	OUT7		A	Switch Output 7	OUT7			
70	n.c.	not connected			n.c.	not connected		

1) Direction of the digital pins : I = input, O = output, IO = Input/Output

2) Type of the pin: A = analog, OD = Open-Drain, PU = internal Pull-Up resistor, PD = internal Pull-Down resistor, PPZ = Push-Pull pin with High-Impedance functionality

In case of serial mode six pins can be used to drive a LED-matrix on the uC-side (**Table 2**). For this purpose the bit LEDON in register GLCFG has to be set to "1".

Table 2 Pin Configuration for LED-Application on the uC-Side

Pin	Serial Interface Mode			
	Symbol	Ctrl	Type	Function
top side pins				
55	AD6		OD	LEDR0
52	AD3		OD	LEDR1
51	AD2		OD	LEDR2
42	$\overline{WR}$		OD	LEDC0
43	ALE/RST		OD	LEDC1
50	AD1		OD	LEDC2

2.1 Pin Functionality

This section describes the pins of the µController Interface as well as the Process Interface.

2.1.1 Pins of Power Interface

VBB (Positive supply 11-35 V output stage)

V_{BB} supplies the output stage. An external circuitry for reverse polarity protection is required (see Electrical Characteristics).

A ceramic capacitor of minimum 2.2 µF must be connected between VBB and GNDBB.

GNDBB (Ground for VBB domain)

This pin acts as the ground reference for the output stage that is supplied by V_{BB}.

OUT0... OUT7 (Output channel 0 ... 7)

Due to EMI-requirements (Radio-Frequency-Common-Mode and burst-application) a capacitor of min.10 nF (±10%, recommended value 12 nF ± 10%) for each output pin has to be connected to GNDBB.

LEDX0... LEDX2 (LED Row output channel 0 ... 2)

Low side switches

LEDY0... LEDY2 (LED Column output channel 0 ... 2)

High side drivers

IADJ (Current Adjust)

Reference current input, must be connected to GNDBB through a reference resistor of typ. 6.81 KΩ (E96 series). The DC-level V_{IADJ} is 1.215 V.

OLADJ (Open Load Adjust)

The current for the Open load detection can be adjusted by connecting a resistor between this pin and GNDBB (from the E96 series : 25 kΩ - 2.3 kΩ).The DC-level V_{OLADJ} is 1.215 V.

VDDIO (3.3 V Supply Blocking Capacitor)

A 1 µF ceramic capacitor must be connected between VDDIO and GNDBB.

VCORE (Blocking Capacitor for 1.5 V Digital Core)

A 470 nF ceramic capacitor must be connected between VCORE and GNDBB.

2.1.2 Pins of Serial and Parallel Logic Interface

Some pins are common for both interface types, some others are specific for the parallel or serial access.

VCC (Positive 3.3 V logic supply)

V_{CC} supplies the output interface that is electrically isolated from the output power stage. The interface can be supplied with 3.3 V. A ceramic capacitor of minimum 2.2 µF must be connected between VCC and GND.

GND (Ground for VCC domain)

This pin acts as the ground reference for the uC-interface that is supplied by V_{CC}.

CLKADJ (Clock Adjust)

A high precision resistor of 10 KΩ has to be connected between CLKADJ and GND. The DC-level V_{CLKADJ} is 0.5 V.

$\overline{\text{ERR}}$ (Fault Indication)

The low active $\overline{\text{ERR}}$ signal contains the OR-wired diagnostic information depending on choosen serial or parallel mode (VBB undervoltage or missing voltage detection, the internal data transmission failure detection unit and the fault(s) of the output switch).The output pin $\overline{\text{ERR}}$ provides an open drain functionality.This pin has an internal Pull-Up resistor. In normal operation the signal $\overline{\text{ERR}}$ is high.

$\overline{\text{ODIS}}$ (Output Disable)

The low active $\overline{\text{ODIS}}$ signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal $\overline{\text{ODIS}}$ is high. Setting $\overline{\text{ODIS}}$ to Low clears the **DRIVE** register as well. The minimum width of the $\overline{\text{ODIS}}$ signal is 5 µs.

SEL (Serial or Parallel Mode Select)

When this pin is in a logic Low state, the IC operates in Parallel Mode. For Serial Mode operation the pin has to be pulled into logic High state. During Start Up the IC is operating in Parallel Mode. This pin has an internal Pull-Down resistor and a 200 ns blanking time[1)].

SYNC

In isochronous mode (clock-sync-mode) the transfer of the latched output data register into the output-stages is controlled by the SYNC signal. When the SYNC-signal is in low state, the output-stage won't be updated any longer, the last value is frozen. With the rising edge of SYNC the information of the latched output data registers will be transferred to the output stages. It can be choosen by a configuration bit whether all the channel diagnostic bits will be latched into the DIAG channel register every data cycle or only when the SYNC-signal is in high state. In the last case when the SYNC-signal is in low state, the DIAG channel register wouldn't be updated any longer, the last value would be frozen. SYNC is also used for resynchronization of the data transmission with the target to achieve a low jitter. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

$\overline{\text{CS}}$ (Chip Select)

When this pin is in a logic Low state, the IC interface is enabled and data can be transferred. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

When the $\overline{\text{CS}}$ pin is held Low whereas the ALE pin is High for at least 100 µs, the device is reset.

The following pins are provided in the parallel interface mode

AD7:AD0 (AddressData input / output bit7 ... bit0)

The pins AD0 .. AD7 are the bidirectional input / outputs for data write and read. Depending on the state of the ALE pin and the AD7 pin, register addresses or data can be transferred between the internal registers and e.g. the micro-controller. By connecting $\overline{\text{CS}}$ and $\overline{\text{WR}}$ and ALE/RST pins to GND and $\overline{\text{RD}}$ to VCC, the parallel direct mode is activated.

$\overline{\text{WR}}$ (Write)

By pulling this pin down, a write transaction is initiated on the AddressData bus and the data has to be valid on the rising edge of $\overline{\text{WR}}$. The AD7-bit of the register address has to be set to '1'. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

$\overline{\text{RD}}$ (Read)

By pulling this pin down, a read transaction is initiated on the AddressData bus and the data becomes valid on the rising edge of $\overline{\text{RD}}$. The AD7-bit of the register address has to be set to '0'. This pin has an internal Pull-Up resistor and a 20 ns blanking time[1)].

ALE (Address Latch Enable)/RST

The pin ALE is used to select between address (ALE is in a logic High state) or data (ALE is in a logic Low state). Furthermore, a read or write transaction can be selected with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pin. When ALE is pulled high, address is transferred and latched over the bit AD0 to AD7. During the time interval where ALE = High $\overline{\text{RD}}$ or $\overline{\text{WR}}$ has to be pulled to High. During the Low State of ALE all transactions hit the same address. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)]. For the reset-function see comment under the item: $\overline{\text{CS}}$.

1) the signal must be stable for the duration of the blanking time before it is accepted as valid

The following pins are provided in the serial interface mode

MS0, MS1 (Serial Mode Select)

By driving these pins to Logic High or Low the Serial Interface Mode (number of bits - 8, 16, 24 - to be transferred, CRC) can be selected. These pins have both an internal Pull-Down resistor and a 200 ns blanking time[1)].

SCLK (Serial Interface Shift Clock)

Input data are sampled with rising edge and output data are updated with the falling edge of this input clock signal. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)].

SDI (Serial Interface Input Data)

SDI is put into a dedicated FIFO (clocked by SCLK) to program the DRIVE register and the internal address and the write data. This pin has an internal Pull-Down resistor and a 20 ns blanking time[1)].

SDO (Serial Interface Data Output)

SDO provides the serial output data bits

$\overline{\text{CRCERR}}$ (CRC Error Output)

This pin is in a logic Low state when CRC errors or Shift-Clock errors are detected internally. This pin has an open drain functionality and an internal Pull-Up resistor.

3 Block Diagram

The IC is divided into an uC_chip and into a power chip due to the galvanical isolation.The uC_chip contains the uC-interface and the power chip the power switches.

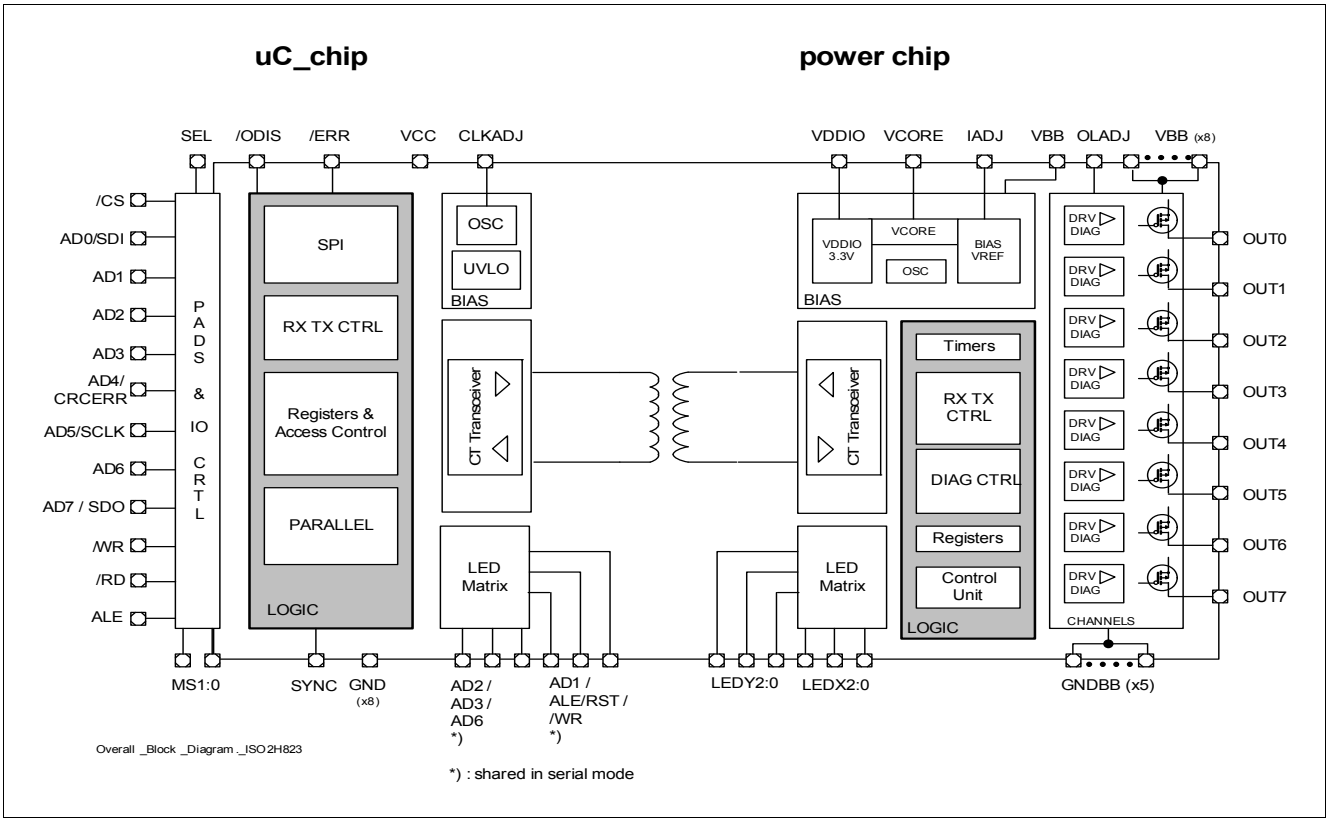


Figure 3 Block Diagram

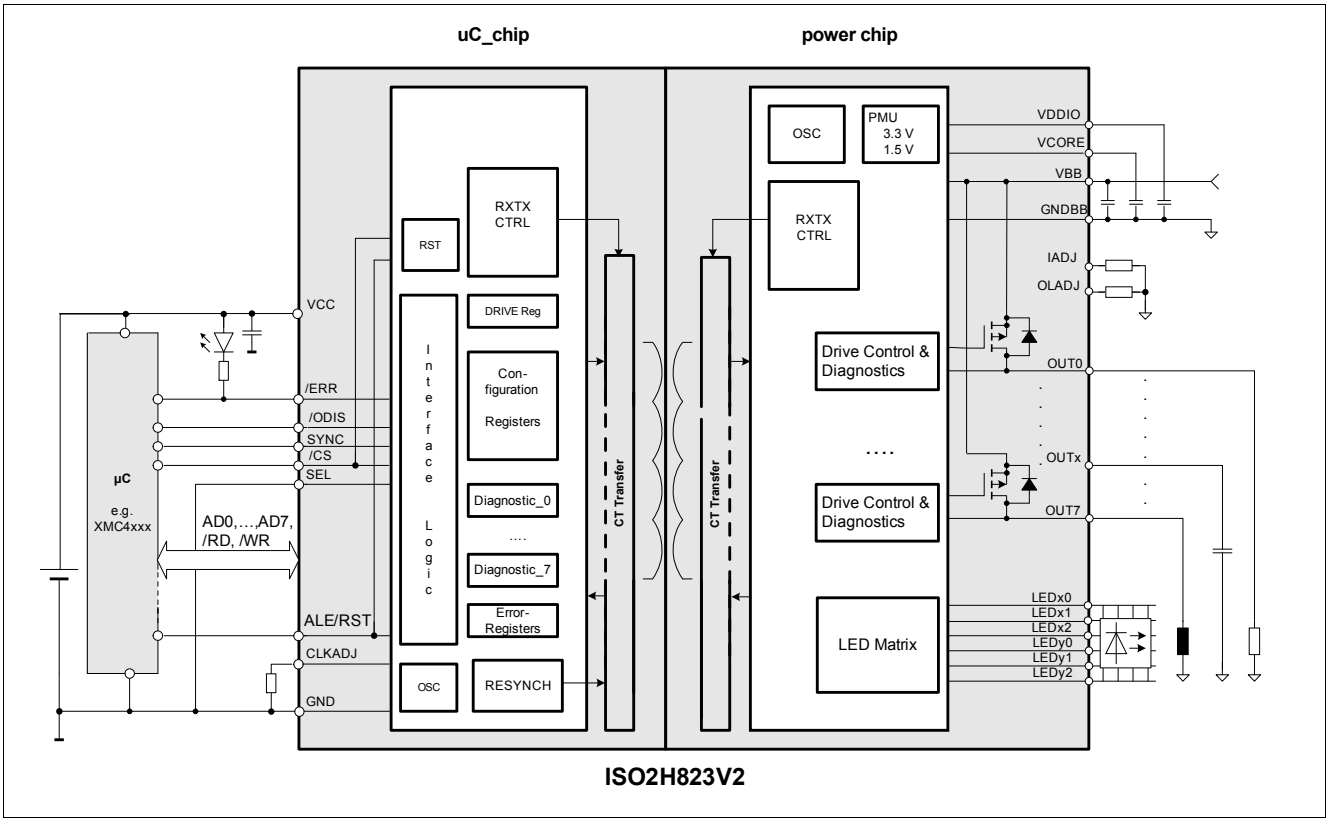


Figure 4 Application with Parallel Interface

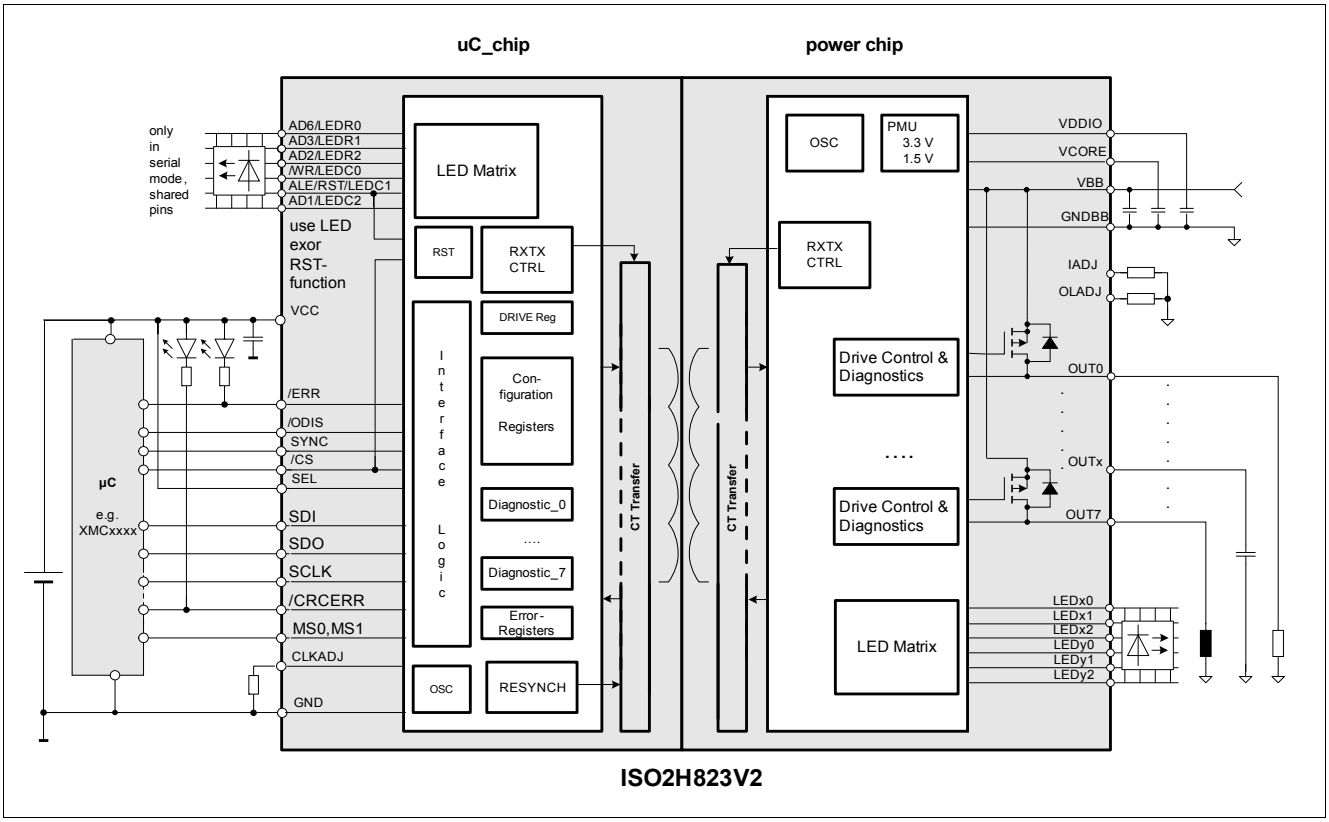


Figure 5 Application with Serial Interface

4 Functional Description

4.1 Introduction

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface (µC-chip) is supplied at V_{CC} and the output stage (power chip) is supplied at V_{BB}. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state. The power chip generates out of V_{BB} two internal voltages V_{DDIO} = 3.3 V (± 10 %) and V_{CORE} = 1.5 V (± 10%) which have to be buffered externally.

The ISOFACE ISO2H823V2.5 includes 8 high-side power switches that are controlled by means of the integrated parallel/serial interface. The interface is 8-bit µController compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0 … OUT7 (power chip) by means of the inputs AD0 … AD7 (µC-chip) without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µController compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against overload, overtemperature and against overvoltage by an active zener clamp.

4.2 Microcontroller Interface

The microcontroller interface can be configured as a parallel or serial interface via the SEL pin.

4.2.1 Parallel Interface Mode

The ISO2H823V2.5 device contains a parallel interface that can be selected by pulling the SEL Pin to logic Low state. The interface can be directly controlled by the µController output ports (see **Figure 6**). The output pins AD7:AD0 are in state “Z” as long as $\overline{CS}$=1, $\overline{RD}$=1 and $\overline{WR}$=1.

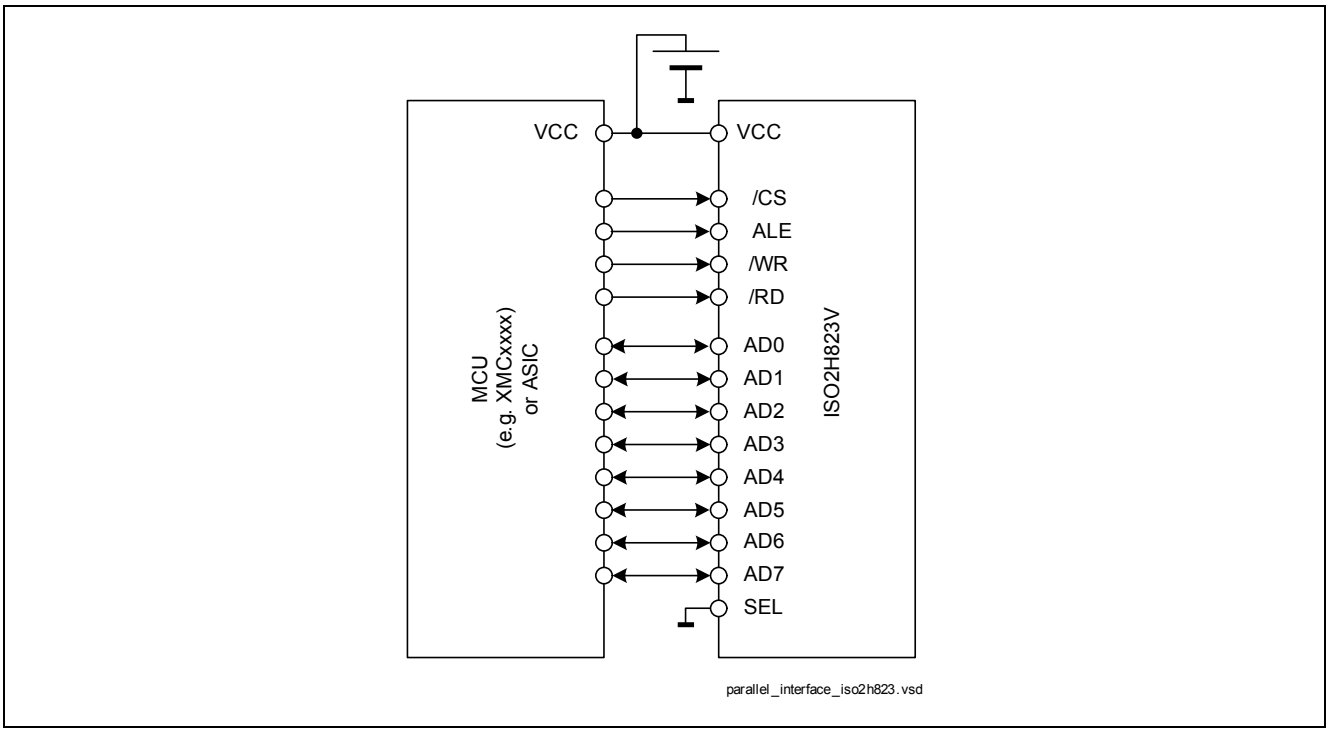


Figure 6 Bus Configuration for Parallel Mode

The timing requirements for the parallel interface are shown in **Figure 7** (Read), **Figure 8** (Write) and **Table 23**.

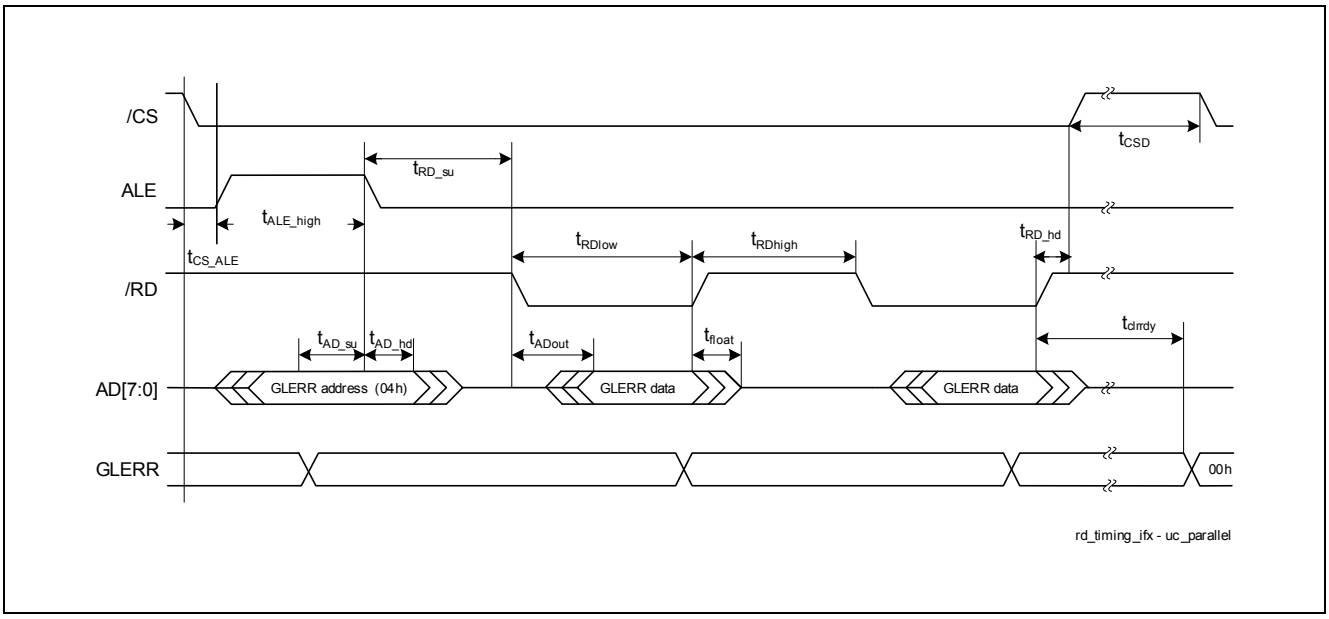


Figure 7 Timing by Parallel Read Access (e.g. GLERR Register)

For a reading access to internal registers the MSB of the address register has to be set to “0”.

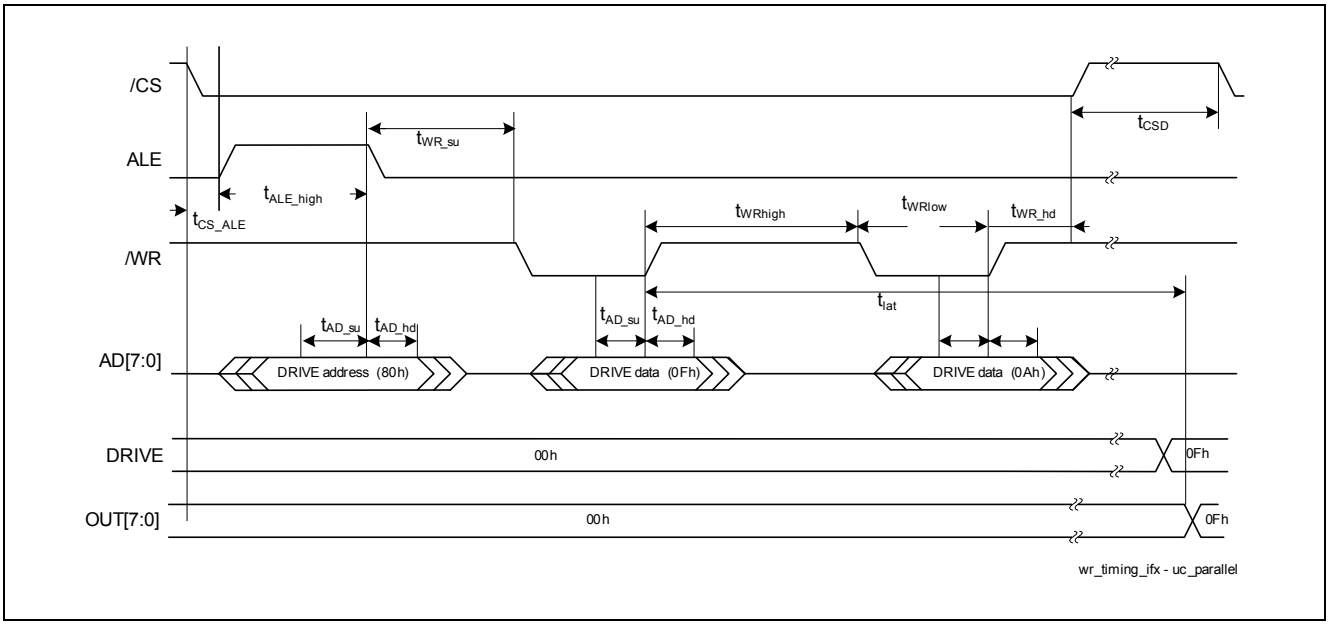


Figure 8 Timing by Parallel Write Access (e.g. DRIVE Register)

For a writing access to internal registers the MSB of the address register has to be set to “1”.

4.2.1.1 Parallel Direct Mode

The parallel interface can be also used in a direct mode that allows direct changes of the output OUT0...OUT7 by means of the corresponding inputs D0-D7 without additional logic signals. To activate the parallel direct mode $\overline{CS}$, $\overline{WR}$ and ALE pins have to be wired to ground and $\overline{RD}$ has to be wired to V_{CC} as shown in the **Figure 9**. Although the diagnostics cannot be read in this operation mode, the faults as specified in **Table 3** are still reported at the $\overline{ERR}$ pin (volatile).

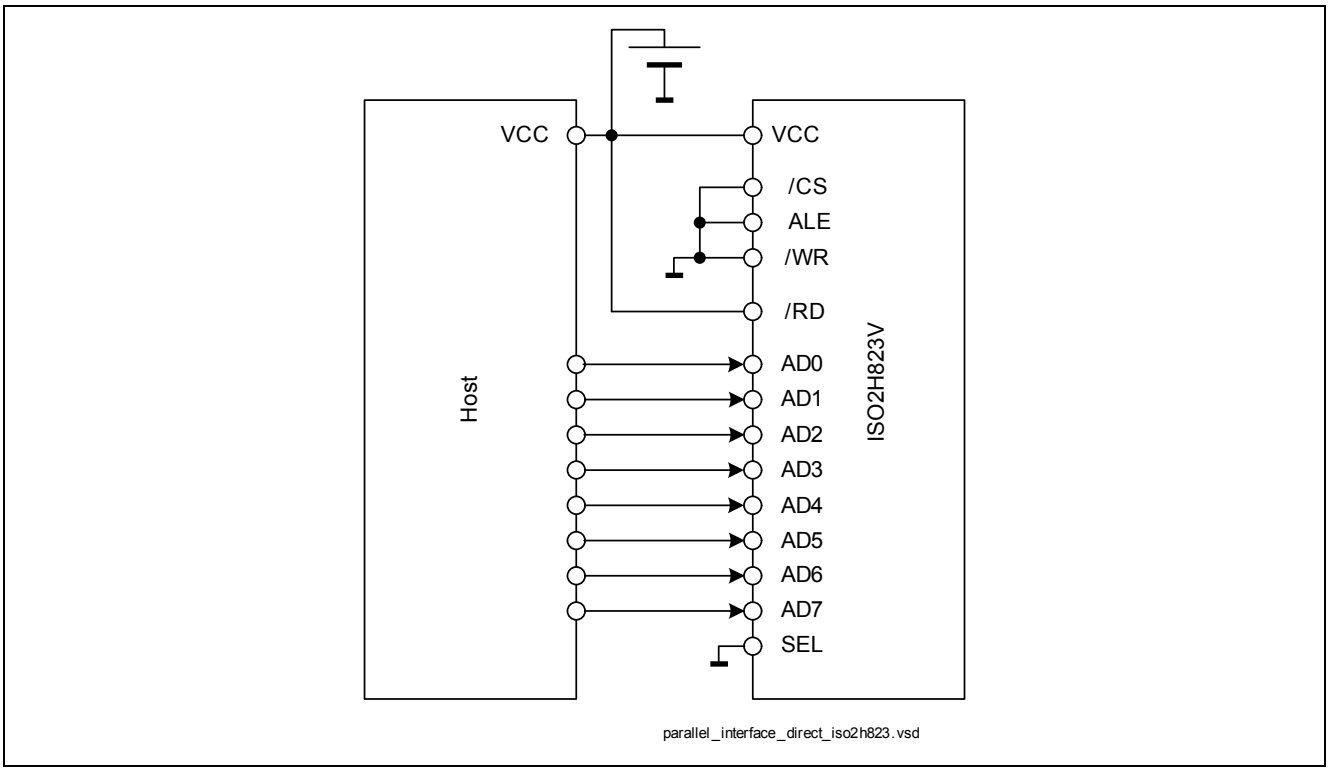


Figure 9 Parallel Direct Mode

The direct mode is intended to be an additional parallel mode which is invoked directly after reset. In this case internal settings have already been realized (f.e. MSB of the address register is set to “1”).

4.2.2 Serial Interface Mode

The ISO2H823V2.5 device contains a serial interface that can be activated by pulling the SEL pin to logic High state. The interface can be directly controlled by the µController output ports. The output pin SDO is in state “Z” as long as $\overline{CS}$=1. Otherwise, the bits at the SDI input are sampled with the rising edge of SCLK and registered into the input FIFO buffer of length dependent on the selected SPI-mode (8, 16, 24 bits, **Figure 12**, **Figure 13**, **Figure 14**, **Figure 15**). With every falling edge of SCLK the bits to be read are provided serially to the pin SDO.

The timing requirements for the serial interface are shown in **Figure 10** and in **Table 24**.

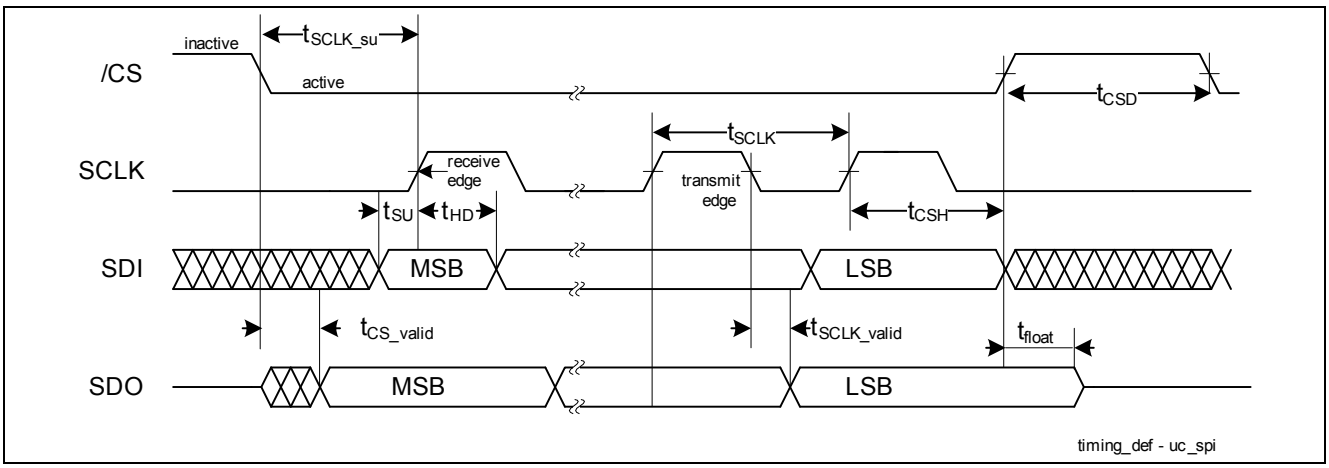


Figure 10 Serial Bus Timing

Several SPI topologies are supported: pure bus topology, daisy chain and any combinations (**Figure 11**). Of course independent individual control with a dedicated SPI controller interfaces for each slave IC is possible, as well.

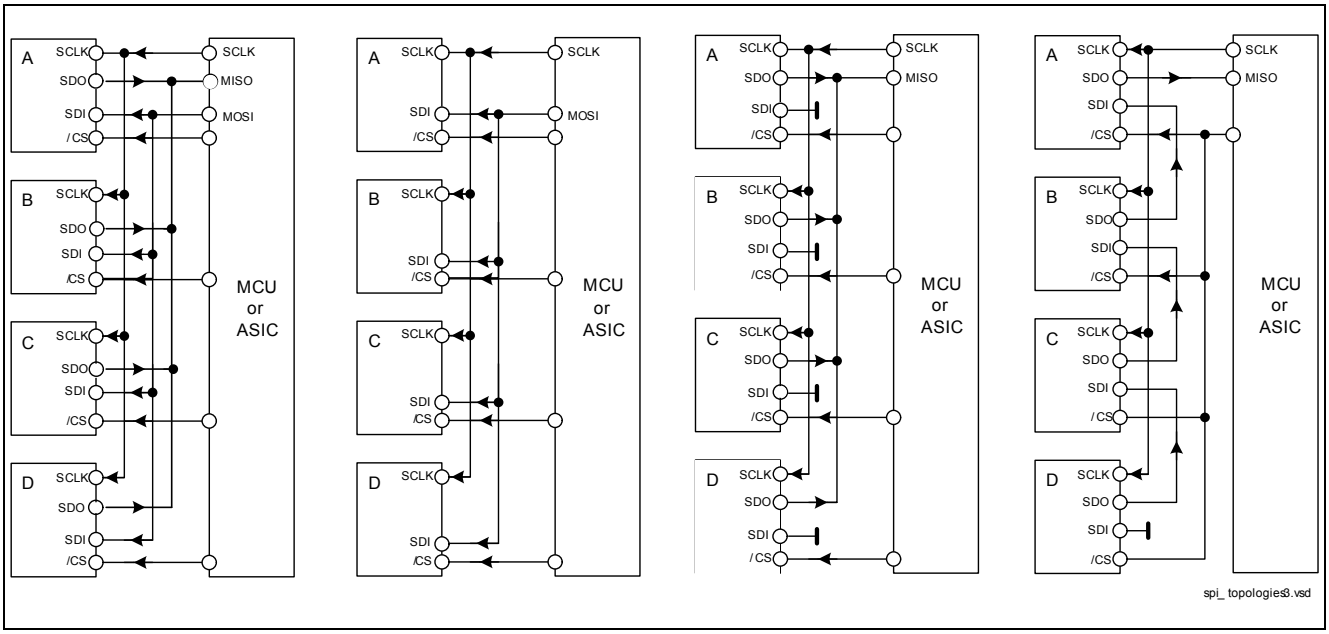


Figure 11 Example SPI Topologies

4.2.2.1 SPI Modes

Four different SPI-modes can be distinguished (**Figure 12** - **Figure 15**).

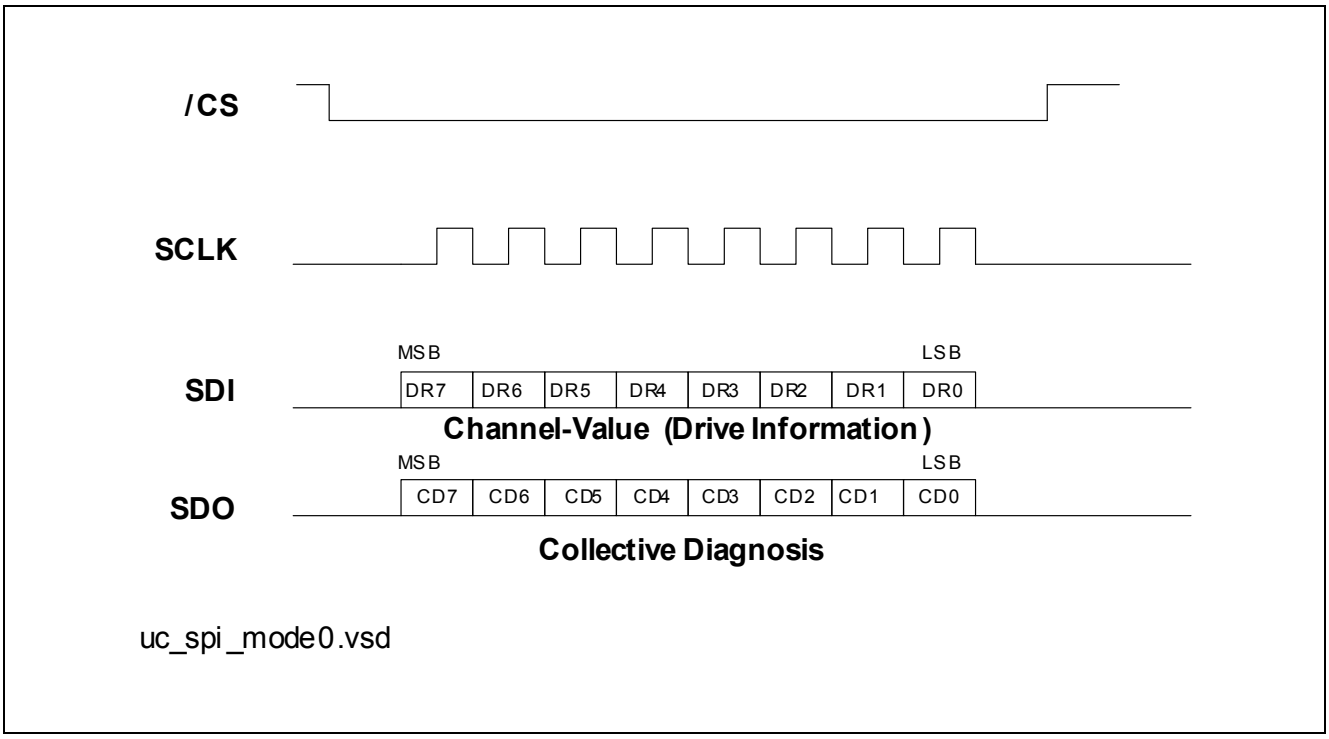


Figure 12 SPI Mode 0, MS0 = 0, MS1 = 0, Daisy Chain Supported

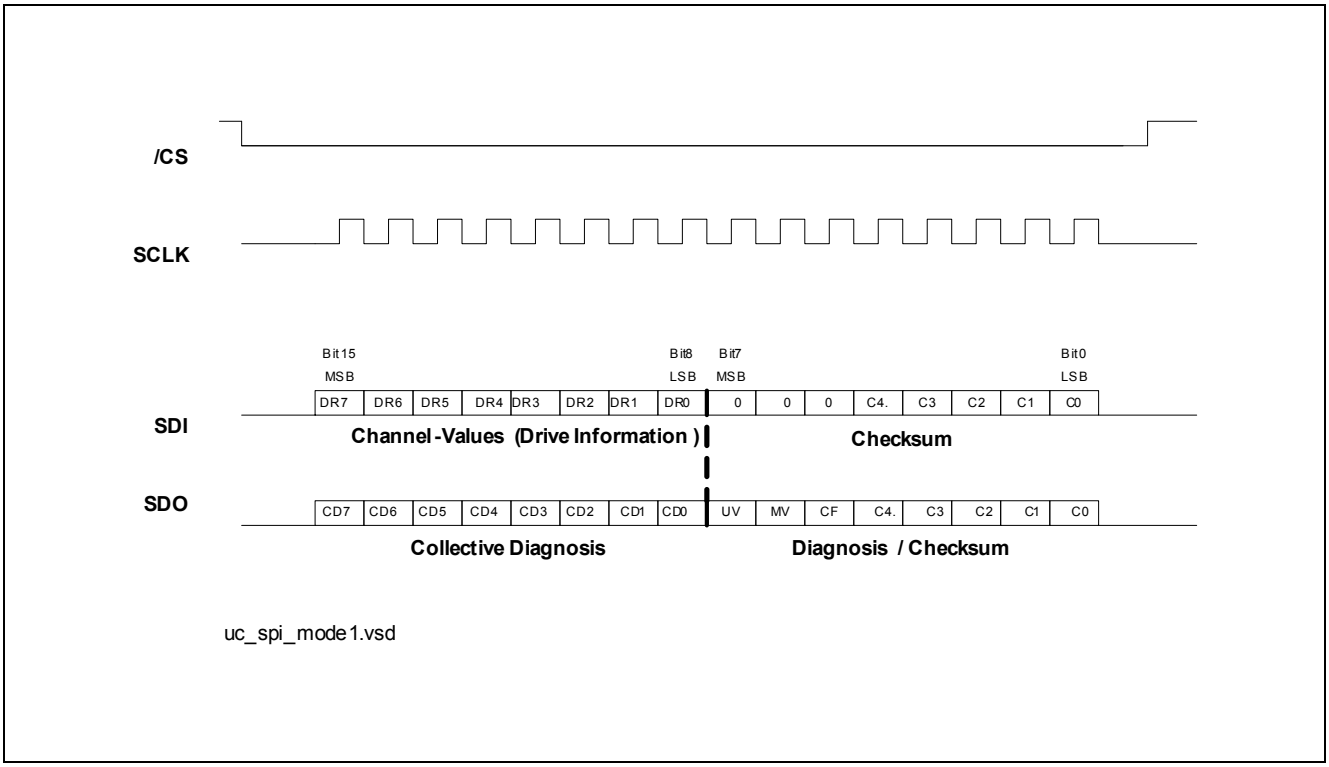


Figure 13 SPI Mode 1, MS0 = 1, MS1 = 0, Daisy Chain Supported

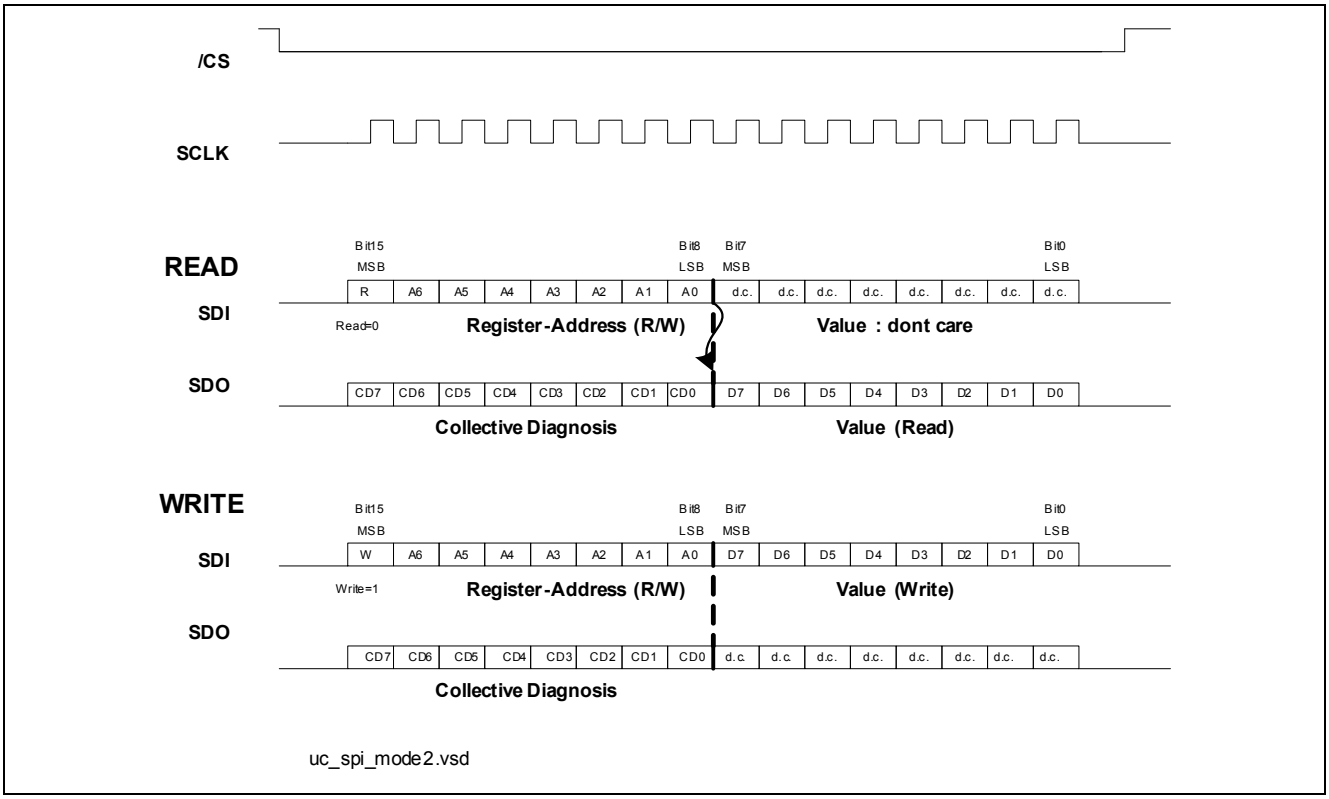


Figure 14 SPI Mode 2, MS0 = 0, MS1 = 1

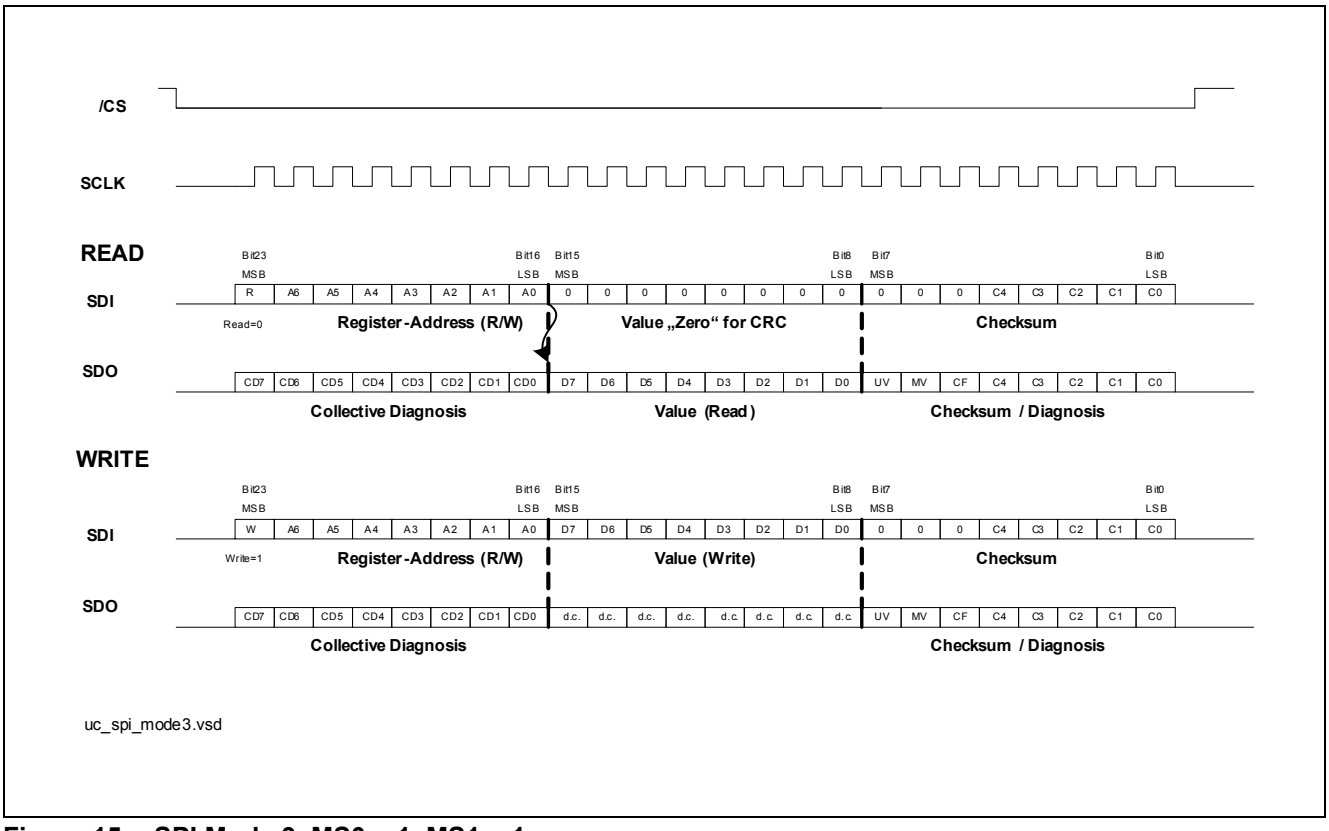


Figure 15 SPI Mode 3, MS0 = 1, MS1 = 1

4.2.2.2 Daisy Chain Mode

Up to 4 devices can be connected together as shown in the **Figure 16** to operate in the daisy chain mode. Serial modes 0 and 1 can be operated in daisy chain mode. In this case, the SDO output of one device is directly connected to the SDI input of the next device. The SPI chain has to be connected to the µC or Bus ASIC (MOSI, MISO and common SCLK and $\overline{CS}$ signals). If the received SCLK pulses are not fulfilling the modulo(8)-condition the $\overline{CRCERR}$ pin will be activated.

In the serial mode 1 the CRC-generation has to be reset after 16 SCLK-cycles. At the rising edge of $\overline{CS}$ each connected daisy-chain-device checks its related 16 bit-stream concerning CRC-consistency.

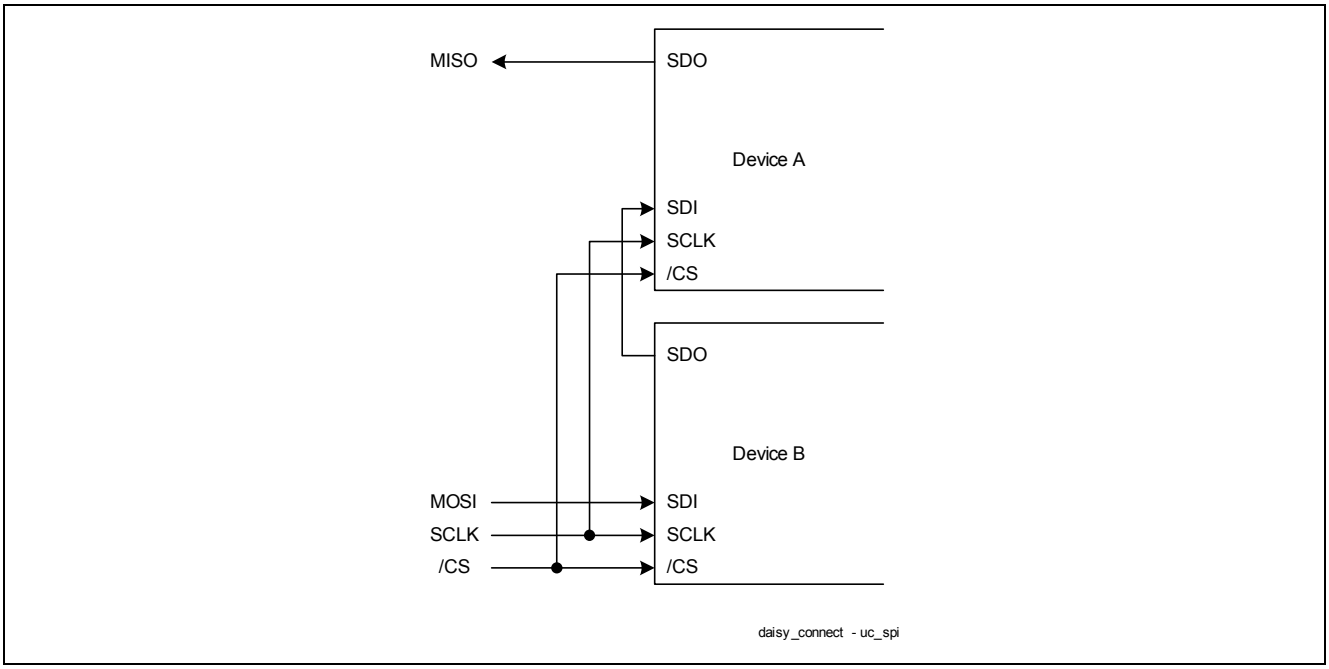


Figure 16 Connecting Two Devices for Daisy Chain Mode

The data shifted in the first device SDI input is shifted out at the SDO output after the first byte for the serial mode 0 (after the second byte for the mode 1) while $\overline{CS}$ remains Low as shown in the **Figure 17**.

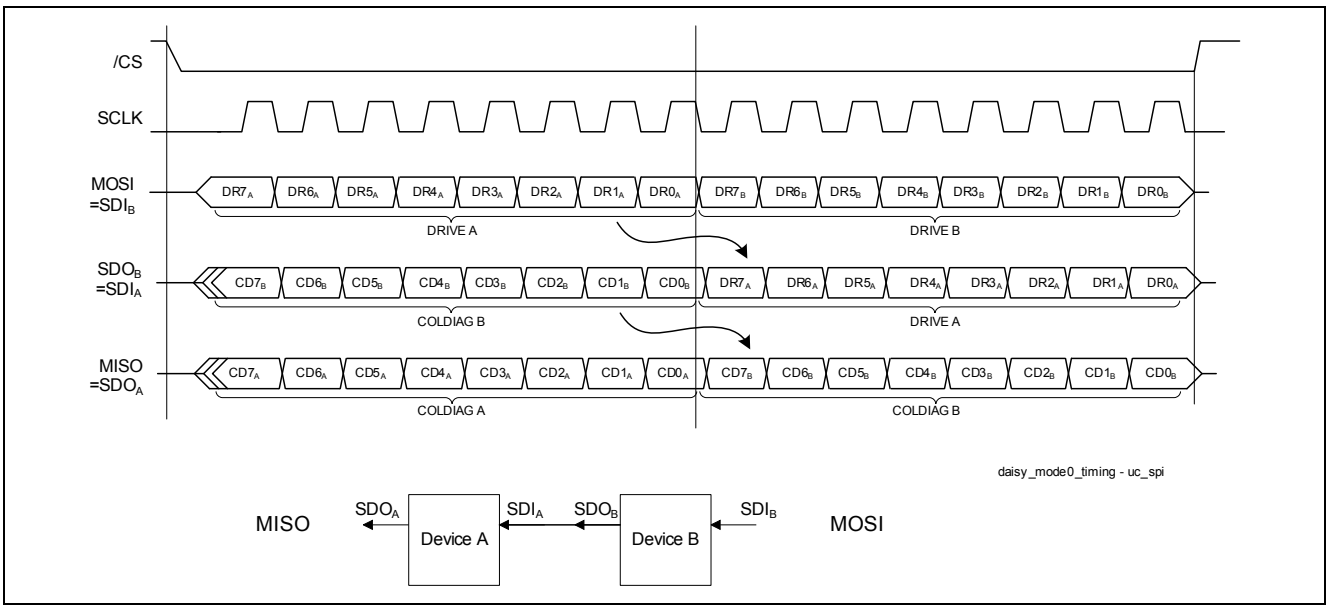


Figure 17 Typical Timing Diagram of Daisy Chain Operation (Serial Mode 0)

4.2.2.3 Cyclic Redundancy Check CRC

To detect errors inside SPI data transmission two SPI-Modes are provided with integrated Cyclic Redundancy Check.

The 5-Bit-CRC checksum will be calculated with the polynom $X^5+X^4+X^2+1$. The bit length used for the calculation is 11 bits for SPI-mode 1 and 19 bits for SPI-mode 3. The internal CRC-working register is loaded with “11111” before start of the CRC-calculation.

The SPI-mode 1 supports only the write procedure for the **DRIVE** register (SPI-mode 1, MS1, MS0 = 01). Eight bits of drive-information plus 3 dummy bits and the related CRC-information (5 bits based on the fed-in 11 bits) are delivered to the CRC-engine. At the same time the **COLDIAG**-information in combination with the **UV**,**MV**,**CF**-bits and the related CRC-information (based on these 11bits: **COLDIAG**, **UV**,**MV**,**CF**) are fed out of SDO. The bit stream format is shown in **Figure 13**.

SPI-mode 3 provides register based access to the ISO2H823V2.5 with implemented CRC. The bit stream for a write access to a register consists of the register address (8 bits), register data (8 bits), 3 dummy bits and the CRC signature (5 bits) as shown in **Figure 15**. The total bitstream is fed into the CRC-input engines and processed according to the underlying CRC-algorithm serially. At the same time the **COLDIAG**-information in combination with the **UV**,**MV**,**CF**-bits and the related CRC-information (based on these 19 bits: **COLDIAG**, 8 dummy bits,**UV**,**MV**,**CF**) are fed out of SDO.

The bit stream for a read access to a register consists of the register address (8 bits), 11 dummy bits and the CRC signature (5 bits) as shown in **Figure 15**.The total bitstream is fed into the CRC-input engines and processed according to the underlying CRC-algorithm serially. At the same time the **COLDIAG**-information, register data in combination with the **UV**,**MV**,**CF**-bits and the related CRC-information (based on these 19 bits: **COLDIAG**,8 bits register data, **UV**,**MV**,**CF**) are fed out of SDO.

After processing the 24 in-bits (including the CRC-signature) the result of the CRC-algorithm processing has to be zero. In the case of another result different from zero the delivered signature is not consistent with the delivered bit stream. This will be indicated by driving the $\overline{\text{CRCERR}}$ Pin to Low.

In both cases (SPI-mode 1 and SPI-mode 3) the status of the CRCERR pin is evaluated not at the end of the bit sequence but with rising edge of $\overline{\text{CS}}$. The procedure is consistent with the daisy-chain application where each partner of the daisy chain checks its own contribution with the rising edge of $\overline{\text{CS}}$ when it is confirmed that the chain is completely filled.

$\overline{\text{CRCERR}}$ reflects both the modulo-8-condition of the number of SCLK-signals and the correctness of the CRC-signature. Both kinds of information are evaluated only during $\overline{\text{CS}}$ is Low and reported with the rising edge of $\overline{\text{CS}}$. Therefore it is assured that non-active ICs ($\overline{\text{CS}}$ = High) does not report a $\overline{\text{CRCERR}}$ = Low signal in case of toggling of SCLK.

The signal $\overline{\text{CRCERR}}$ has an internal pull-up-resistor of 50 kΩ. When releasing $\overline{\text{CRCERR}}$ the internal pull-up resistor determines the rise time, which is about 3 µs. It is possible to reduce the rise time to around 1 µs by adding an external pull-up resistor of 10kΩ at the $\overline{\text{CRCERR}}$ pin.

4.2.3 Common Error Indication Output

The dedicated $\overline{\text{ERR}}$ pin signalizes a common fault. This low-active pin has an open drain functionality with a pull-up resistor.

Depending on the µController-interface mode in use, several internal status signals are OR-wired to drive the $\overline{\text{ERR}}$ pin:

- In direct mode, the **OTC** flag (**LEDGx**-bit-field of CT-transmission, OR-wired, volatile) and the volatile **W4P**-information are routed to the $\overline{\text{ERR}}$ pin.
- The output stage undervoltage (**UV**) and missing voltage (**MV**) of the power-chip which are transmitted via the integrated coreless transformer are provided at the $\overline{\text{ERR}}$ pin.
- The internal data transmission error (**TE**) over the galvanic isolation is available as well at the $\overline{\text{ERR}}$ pin.
- The signal Wait-for-Power chip (**W4P**) is also provided. It detects that a continuous transmission error over a longer time has occurred e.g. when the process side is not supplied properly and that no diagnostic data are received on the µController-interface side.
- The common fault error signal (**CF**) is routed out to the $\overline{\text{ERR}}$ pin in parallel mode. This signal is the OR-combination of the **COLDIAG** register bits (sticky).
- **CF** is not routed out to the ERR pin in any serial mode. In serial modes 1 and 3 the **CF**-bit is contained in the serial telegram

The **Table 3** provides the overview of the signals provided at the $\overline{\text{ERR}}$ pin and the behaviour of the bits used. The prefix “S” specifies the bits as sticky.

During UVLO, all status signals and register bits are reset. The flags **UV**, **MV**, **TE** and **W4P** have a reset value of 1, so that by default these errors are active. As a consequence after power-up the $\overline{\text{ERR}}$ pin is by default driven Low. The $\overline{\text{ERR}}$ pin returns to High logic level once all the signals OR-wired at this pin are Low i.e. once all the fault conditions are not detected anymore and the bits have been cleared. This behaviour requires the external controller to read the **GLERR** and **INTERR** to “clear” the $\overline{\text{ERR}}$ pin (except in parallel direct mode where the error bit is simply **OTC** of type: volatile bit generated by oring the volatile gated-**LEDGx**-information of each channel and **W4P**). In some operation modes the update and the clearing of the status bits are done automatically after every access (serial mode 0 and 1). For the other operation modes, the error bits need to be read with direct addressing to be updated and cleared (parallel mode and serial modes 2,3).

The $\overline{\text{ERR}}$ signal differs between serial modes and parallel modes since in serial modes 1 and 3 the **CF** bit is already shifted out when CRC is used. The serial or parallel mode is selected with the SEL signal whereas the serial submodes are controlled with the SPI_MODE 2-bit signal.

Table 3 Bits composing the $\overline{\text{ERR}}$ signal

Status Bits	Serial Communication				Parallel Communication		
	Mode-0	Mode-1	Mode-2	Mode-3	Single Access	Repeated Read	Direct Mode
SUV	X	X	X	X	X	X	
SMV	X	X	X	X	X	X	
CF					X	X	
STE	X	X	X	X	X	X	
SW4P	X	X	X	X	X	X	X[1)]
OTC							X

1) Bit is volatile in direct mode

Upon reset most of the bits used in the $\overline{\text{ERR}}$ generation are reset to High, the $\overline{\text{ERR}}$ pin is pulled down on startup and will remain Low as long as the external controller does not clear the corresponding bits (and as long as the fault exists).

4.2.4 Update of the Diagnostic Registers

The following list describes the handling of appearing and disappearing failures and therefore the diagnostics.

- Appearing diagnostic/failure: appearing diagnostics are stored internally within sticky registers and are OR-ed into the register **COLDIAG** (except **LEDGx**). Therefore the appearing diagnostic/failure bit can be seen immediately. After reading **COLDIAG** the diagnostic bits are transferred from the internal sticky registers to **DIAG0**,...,**DIAG7** from which these can be read now in detail.
- Disappearing diagnostic/failure : the diagnostic bits are stored internally as sticky bits and therefore also (ored) in **COLDIAG**. In the case the source for the diagnostic bits has disappeared the diagnostic bits are still available internally and in **COLDIAG** until the user has read **COLDIAG**. Therefore the diagnostic bits never disappear with vanishing of the source for setting the bits alone. Both conditions have to be fulfilled: vanishing of the source of the occurence and reading of **COLDIAG**.
- In the case the isochronous mode for the channel diagnostic values is activated with the bit **FRZSC** in register **GLCFG** (see **Chapter 4.2.5.2**) the diagnostic bits are transferred from the internal sticky registers to **DIAG0**,...,**DIAG7** with each edge of the SYNC-signal.

4.2.5 SYNC Operation

The Isochronous Mode enables the synchronization of several devices (e.g. to provide 32 channels 4 devices are grouped in parallel). In this way the update of all the output channels as well as their diagnostics can be synchronized and held such that the Bus ASIC or microcontroller can program a new control word of the output channels and read the diagnostics status. In continuous mode, each device with its own built-in oscillator is updated independently.

The Isochronous Mode is controlled by the SYNC pin and independent of the selected serial or parallel interface (with the SEL pin). It concerns only the update of user registers in the system.

4.2.5.1 SYNC-Signal for Drive-Signals

Figure 18 explains in detail the mechanism for SYNC = High, SYNC = Low and the rising and falling edges of SYNC for transferring the drive-information from the uC-Chip to the Power Chip.

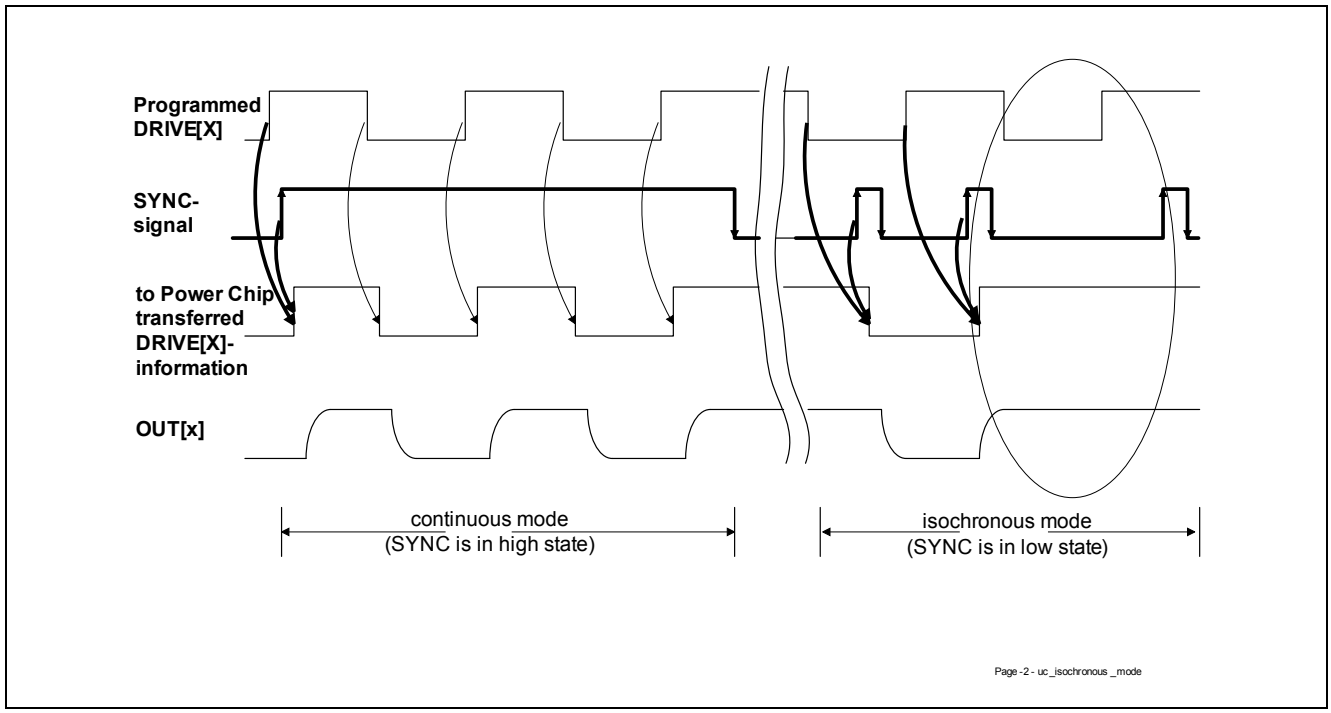


Figure 18 SYNC Operation Timing

SYNC = High, Normal Mode:

The **DRIVE**-register can be written with new data and the contents of it is also transferred to the power chip.

SYNC = Low, Isochronous-Mode:

In isochronous mode the user can write the **DRIVE**-register but this value will not be transferred to the Power Chip. Therefore the driver configuration (activation of drivers in the Power Chip) is frozen. In **Figure 18** it can be clearly seen that the toggling of the **DRIVE**[x]-information (SPI-data-cycle) at the right side had not been transferred to the process side (see oval area in **Figure 18**).

4.2.5.2 SYNC-Signal for Diagnostics

Independent from the level of the SYNC-signal always the same reading-sequence of the diagnostics shall be obeyed : read **COLDIAG**, check which channel x (in the following examples of **Table 4** and **Table 5** : channel 0) shows the setting of diagnostic bits and read the related **DIAG0**,...,**DIAG7** for checking in detail which diagnostic

has been reported. Reading of **COLDIAG** first assures that the **DIAG0**,...,**DIAG7**-registers are loaded from the internal sticky registers.

SYNC = High, Continuous Mode:

When the signal SYNC is High (default), the continuous mode is selected and the diagnostic registers **DIAG0**,....**DIAG7** are always updated after read access to **COLDIAG**.

Table 4 shows the typical scenario where an external disturbance (openload or short-circuit-to VBB) cause the setting of the diagnostic registers **DIAG0**,...,**DIAG7** (here **DIAG0**) and the collective diagnostic register **COLDIAG**. After vanishing of the disturbance and reading of **COLDIAG** the internal diagnostic registers are reset. The SYNC-waveform is sketched in red (in **Table 4** for the continuous mode any waveform is allowed), the disturbance in light shaded grey (in this example strictly time limited) and the possible read-access in dark grey.

Table 4 Continuous Mode (GLCFG : FRZSC = 0), Disturbance (to Channel 0) Scenario

Waveform of SYNC **.....”0”.....**	**permanently “High”** **xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx”1”xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx** **or any waveform of SYNC is allowed when GLCFG:FRZSC = 0**									
scenario #										
1	**disturbance**									
1 read results **COLDIAG** **DIAG0**		**read=yes** **0x01** **0xvalue**			**read=yes** 0x00 0x00					
2	**disturbance**									
2 read results **COLDIAG** **DIAG0**		**read=yes** **0x01** **0xvalue**			**read=yes** **0x01** **0xvalue**			**read=yes** 0x00 0x00		

SYNC = Low, Isochronous-Mode:

The isochronous mode for the channel diagnostic values is activated with the bit **FRZSC** in register **GLCFG**. If **FRZSC** = 1 (**RESYN** = 0) the isochronous mode for diagnostics is enabled.

When SYNC is Low, the **DIAG0**-7 and **COLDIAG** (including **CF**) are not updated anymore (frozen). At the falling edge of SYNC the information of the internal sticky registers is transferred to **DIAG0**,...,**DIAG7**. During SYNC = High the information of the internal sticky registers has been mirrored and ored to **COLDIAG**. When isochronous mode is activated the **DIAG0**,...,**DIAG7**-registers and **COLDIAG** freeze the diagnostic data. But the internal sticky registers collect the diagnostic information independently from SYNC. With rising edge of SYNC the **DIAG0**,...,**DIAG7** registers and **COLDIAG** are updated on base of the contents of the internal sticky registers.

Table 5 shows some scenarios where an external disturbance (openload or short-circuit-to VBB) cause the setting of the diagnostic registers **DIAG0**,...,**DIAG7** (here **DIAG0**) and the collective diagnostic register **COLDIAG**. In all scenarios the same procedure is sketched where a disturbance occurs and the diagnostic registers are read in the following. The SYNC-waveform is sketched in red (in **Table 5** for the isochronous mode with low and high periods), the disturbance in light shaded grey (in this example strictly time limited at different timestamps) and the possible read-access in dark grey. In **Table 5** the occurence of the disturbance relative to the edges of the SYNC-signal is altered. Read procedures can occur during the phase of SYNC = 0 or SYNC = 1. Dependent on the occurence of the disturbance relative to the SYNC-edges and the read-process the diagnostic values have been already set in **COLDIAG** and **DIAG0**,...,**DIAG7** or the old values have been frozen. In the second case the new values will be updated in **COLDIAG** and **DIAG0**,...,**DIAG7** with the next rising edge of SYNC and can be read with the next read-

cycle. Due to the sticky registers no diagnostic value is lost. After vanishing of the disturbance and reading the diagnostic values are reset.

Entries in **COLDIAG** can be reset during SYNC = Low after a reading procedure when the disturbance had been registered before the falling edge of SYNC and is therefore securely delivered. But **DIAG0**,...,**DIAG7** remains unaffected from this reading procedure.

Table 5 Isochronous Mode (GLCFG : FRZSC = 1 (RESYN = 0)), Channel 0 Disturbed, Scenarios

Waveform of SYNC	**xxxx High**	**x x x x**	**xxxxxxx"0"xxxxxxx Low**	**x x x x**	**xxxxxxxxx"1"xxxxxxxx High**	**x x x x**	**xxx"0"xx Low**	**x x x x**	**xxx"1"xx High**
scenario #									
1	**disturbance**								
1 read results **COLDIAG** **DIAG0**			read=yes **0x01** **0xvalue**		read=yes 0x00 0x00				
2	**disturbance**								
2 read results **COLDIAG** **DIAG0**			read=yes **0x01** **0xvalue**	=yes **0x00** **0x** **val**	read=yes 0x00 0x00				
3		**....disturbance.....**							
3 read results **COLDIAG** **DIAG0**			read=yes 0x00 0x00		read=yes **0x01** **0xvalue**	read=yes 0x00 0x00			
4			**.....disturbance.....**						
4 read results **COLDIAG** **DIAG0**			read=yes 0x00 0x00		read=yes **0x01** **0xvalue**	read=yes 0x00 0x00			
5	**disturbance**								
5 read results **COLDIAG** **DIAG0**			read=yes 0x01 0xvalue				read=yes 0x00 0x00		
6		**....disturbance.....**							
6 read results **COLDIAG** **DIAG0**			read=yes 0x00 0x00				read=yes **0x01** **0xvalue**		read=yes 0x00 0x00

Table 5 Isochronous Mode (GLCFG : FRZSC = 1 (RESYN = 0)), Channel 0 Disturbed, Scenarios

Waveform of SYNC	**xxxx High**	**x x x x**	**xxxxxxx"0"xxxxxxx Low**	**x x x x**	**xxxxxxxxx"1"xxxxxxxx High**	**x x x x**	**xxx"0"xx Low**	**x x x x**	**xxx"1"xx High**
7			**.....disturbance.....**						
7 read results **COLDIAG** **DIAG0**			read=yes 0x00 0x00				read=yes **0x01** **0xvalue**		read=yes 0x00 0x00

4.2.6 $\overline{\text{ODIS}}$ Output Disable

The low active $\overline{\text{ODIS}}$ signal immediately switches off the output channels OUT0-OUT7. This pin has an internal Pull-Down resistor. In normal operation the signal $\overline{\text{ODIS}}$ is High. Setting $\overline{\text{ODIS}}$ to Low clears the registers as well. The minimum width of the $\overline{\text{ODIS}}$ signal is 5 µs.

4.2.7 LEDGOFF

The gated-LED-signal **LEDGx**, x=0,...,7 is per default reported in the diagnostic registers **DIAG0**,...,**DIAG7** (not ored in the **COLDIAG**-register). **LEDGx** is updated with a long time constant every 100ms. Therefore the bit **LEDGOFF** in **GLCFG** offers the possibility to suppress the reporting in the diagnostic registers **DIAG0**,...,**DIAG7**.

4.2.8 OLOFF

The bit **OLOFF** in **GLCFG** offers the possibility to suppress the reporting of **OLIx**, **OLAx** in the diagnostic registers **DIAG0**,...,**DIAG7**.

4.2.9 RESET (Hard and Soft)

4.2.9.1 Hardware Reset

The external hardware reset can be enabled or disabled by the bit **RSTOFF** in the register **GLCFG**, by default the external hardware reset function is enabled. The external hardware reset forces the logic asynchronous reset for the uC_chip (acts like a power-on-reset), all register are loaded with the default values. It is triggered when the signal ALE is set High whereas the $\overline{\text{CS}}$ signal is set Low for at least 100 µs. Once an internal timer reaches the end value of 100 µs then the hardware reset condition is fulfilled and "latched". At the point where one of the signals ALE and $\overline{\text{CS}}$ returns to its default value, the reset is processed. With resetting the **DRIVE**-register and restarting the CT-transmission the output switches are shut down.

4.2.9.2 Soft Reset

The soft reset for the uC_chip is triggered by the bit **SWRST** (self clearing after performing the soft reset) in the register **GLCFG**. If the soft reset is triggered the **DRIVE**, **INTERR**, **GLERR**, **DIAG0**,...,**DIAG7**, **COLDIAG**, **DIAGCFG** register are set to their reset values synchronously. In addition the internal flags are cleared. The CT-transmission is restarted. The actual transmission cycle is not disturbed. With resetting the **DRIVE**-register and restarting the CT-transmission the output switches are shut down.

4.2.10 Resynchronization of CT-Transmission

During the CT-transmission the drive-information **DRIVE** for 8 power switches is sent from the uc-Chip to the Power-Chip. Subsequently one of the diagnostic informations (status-information, **OTx**, **OLIx**, **OLAx**, **OCLx**, **SCVx** or **LEDGx**-information for the 8 power switches) is sent back. The duration of a CT-time slot with transmission of drive - information and back-transmission of one of the diagnostic information lasts about 5 us ± 20 %. (internal operating frequency : 10 MHz, resistor at pin CLKADJ : 10 kΩ). When the user programs the drive register a timing uncertainty arises when the specific programed switch is activated or deactivated in the power chip. The data of the drive register can be transferred to the power chip only in the next free CT-time slot.

The goal of resynchronization is to limit the timing uncertainty due to transmission and retransmission to a value below ± 1.5 us but with a fixed latency of minimum 7.0 us . For triggering the transmission the signal SYNC is used when **GLCFG**:**RESYN** = 1. A timing difference between switching on and off of the power transistors exists which is already included in the timing uncertainty value above. Switching off a power transistor is delayed by up of 0.5 us max relative to the SYNC-rising edge compared to switching on a power transistor.

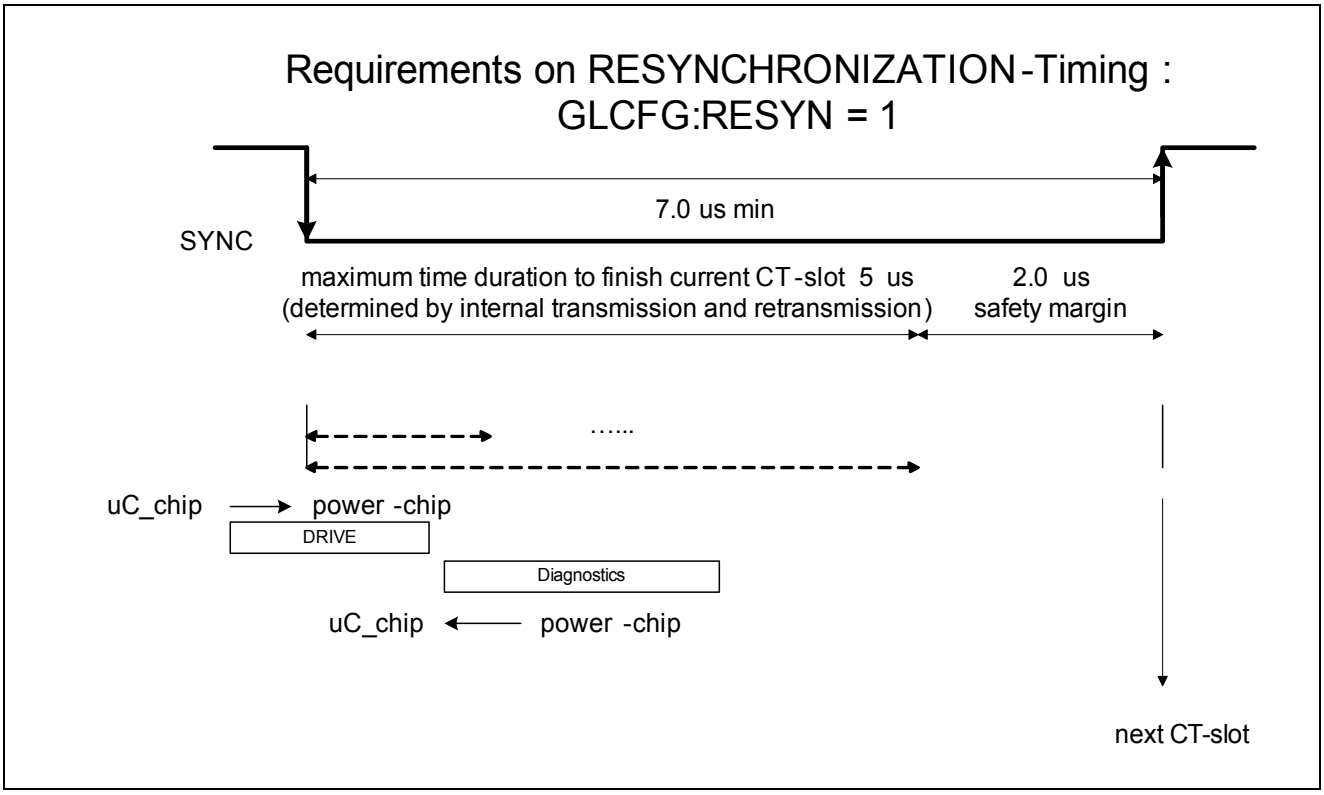


Figure 19 Timing of Resynchronization

Transmission without Resynchronization:

- **GLCFG**:**RESYN** = 0 or 1
- signal SYNC = 1
- write the drive information into **DRIVE**
- the contents of **DRIVE** is transferred via the CT to the power-chip

Transmission with Resynchronization:

- signal SYNC = 1
- **GLCFG**:**RESYN** = 1
- write the drive information into **DRIVE_RESYNCH**
- signal SYNC = 0
- the duration of the signal SYNC = 0 (minimum 7.0 us) determines the time for resynchronization and the time until the next CT-transfer
- In the meantime the pending transmission and retransmission has been finished and the contents of **DRIVE_RESYNCH** has been transferred to **DRIVE**
- set signal SYNC = 1, the CT-transfer is started from **DRIVE** with the rising edge of SYNC

Without any negative pulses on SYNC the CT-transfer is operated permanentely from **DRIVE**; the negative pulses on SYNC are solely used for resynchronization, the isochronous mode for drive-information and for diagnostics is inactive when **GLCFG**:**RESYN** is set to “1”.

Information for the **DRIVE_RESYNCH**-register can be written long before the resynchronzation trigger with falling and rising edge of SYNC.

The user has to obey the timing requirements of the SYNC-signal. For a duration longer than 300 us ± 20% the watchdog in the power chip disables the output drivers. For a shorter duration of the SYNC-signal than recommended the resynchronization is not guaranteed and the normal transmission fed by the register **DRIVE** can be performed.

Figure 20 shows 2 different applications of resynchronization. The timing gap between two synchronizations can be as low as 1 us. In this way the customer can decide between single synchronization steps and permanent synchronized transmission with the drawback of reduced CTthrough put (time for waiting of new transmission).

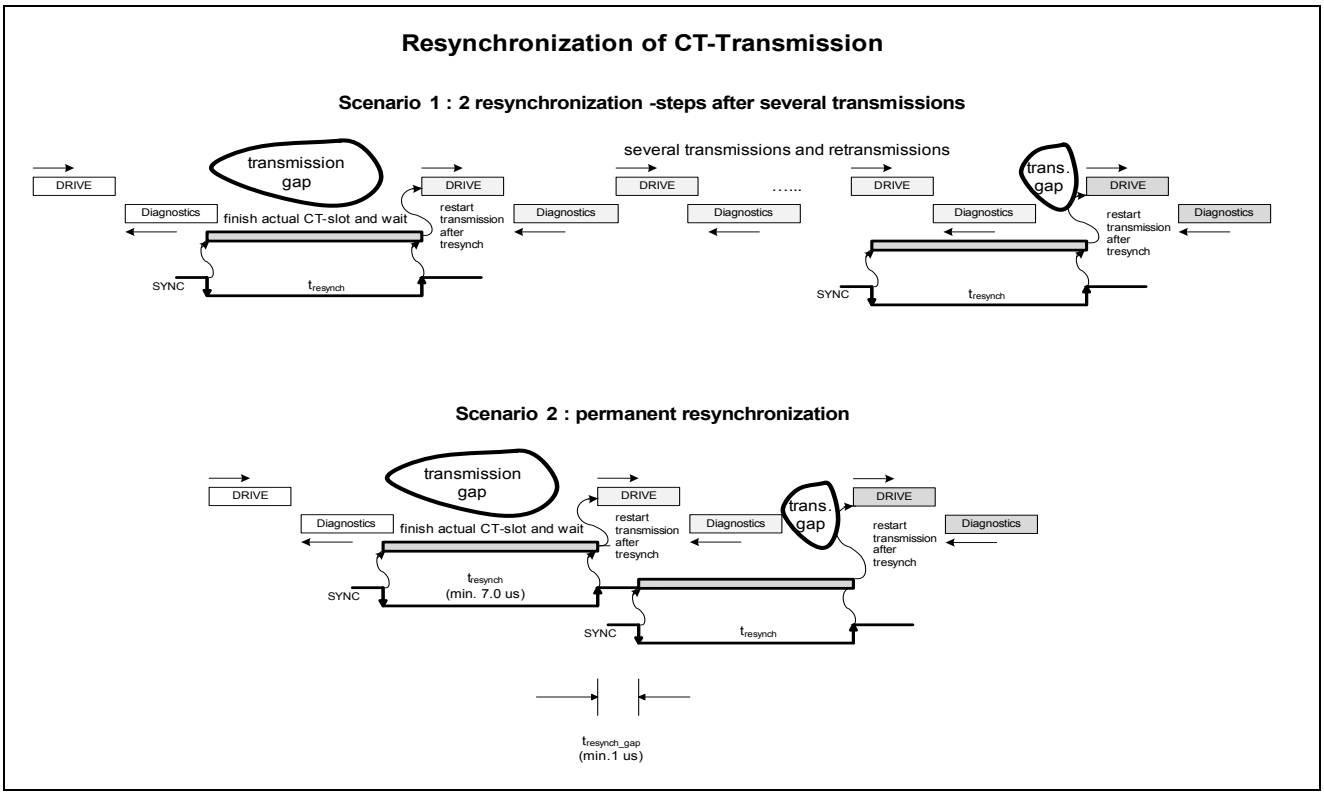


Figure 20 Examples of Application of Resynchronization

Application hint : It is not possible to select **GLCFG**:**RESYN** = 1 and isochronous mode of drive information or/and isochronous mode of diagnostics at the same time. That means resynchronization and isochronous mode of driver information and diagnostics at the same time is not possible. With **GLCFG**:**RESYN** = 1 edges on SYNC are used solely for resynchronization.

4.3 Output Stage

Each channel contains a high-side power FET that is protected by embedded protection functions. The continuous current for each channel is 600 mA nominal, which depends on the cooling conditions and the total power dissipation.

4.3.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin $\overline{\text{ODIS}}$ that disables all eight outputs and resets the latches.

4.3.2 Protection Functionality

4.3.2.1 Power Transistor Overvoltage Protection

Each of the eight output stages has it's own zener clamp that causes a voltage limitation at the power transistor when solenoid loads are switched off. V_{ONCL} is then clamped to 52 V (typ.).

4.3.2.2 Power Transistor Overload Protection

The outputs are provided with a linear current limitation, which regulates the output current to the current limit value in case of overload. The electrical operation point does not lead to a shutdown.

The excess power dissipation in the power transistor during current limitation will lead to a rapid increase of the junction temperature. When the junction temperature exceeds 150 °C (typ.) the output will switch off and will switch on again when the junction temperature has cooled down by a temperature hysteresis of 15 K (typ.). Therefore during overload a thermal on-off toggling may occur.

The thermal hysteresis is reset during inactive mode. Therefore when switching to the active mode the power transistor is first switched on if the junction temperature is below 150 °C.

4.3.2.3 Current Sense and Limitation

To achieve an excellent accuracy for the current limitation and current referred diagnostic (**OCLx**) an external reference resistor is used. The resistor must be connected between the pins IADJ (as close as possible) and GNDBB. The nominal resistor value is 6.81 kΩ (E96; current drawn out of IADJ typ.178 µA) , the tolerance should be within 2% to meet an overall current limit tolerance from 0.73 A to 1.3 A.

Operation with other resistor values than 6.8 kΩ ±5% is not allowed and may lead to insufficient short circuit protection.

To offer open load diagnostics in active mode, a part of the power transistor is driven down when the drain-source-voltage drops below a certain limit (low load condition). The voltage drop across the remaining part is used to evaluate an open load diagnostic.

4.3.3 Diagnostic Functions

For each of the output stages 5 different types of diagnostics are available. **Table 6** specifies the diagnostics.

Some of the diagnostics are available only in active mode, others only in inactive mode. The diagnostics **OLIx**, **OLAx**, **SCVx** can be prolonged within the complementary mode. Overtemperature in inactive mode is not reported (set to zero).

Table 6 Diagnostic

Item	Diagnostic Type	Inactive Mode	Active Mode
OTx	Overtemperature	no	yes (**OTx** Active)
OLIx	Open Load/Wire Break, “inactive”	yes	no
OLAx	Open Load/Wire Break, “active”	no	yes
OCLx	Current Sense, Overload Detection	no	yes
SCVx	Short Circuit to V_{BB}	yes	not distinguishable from **OLAx**

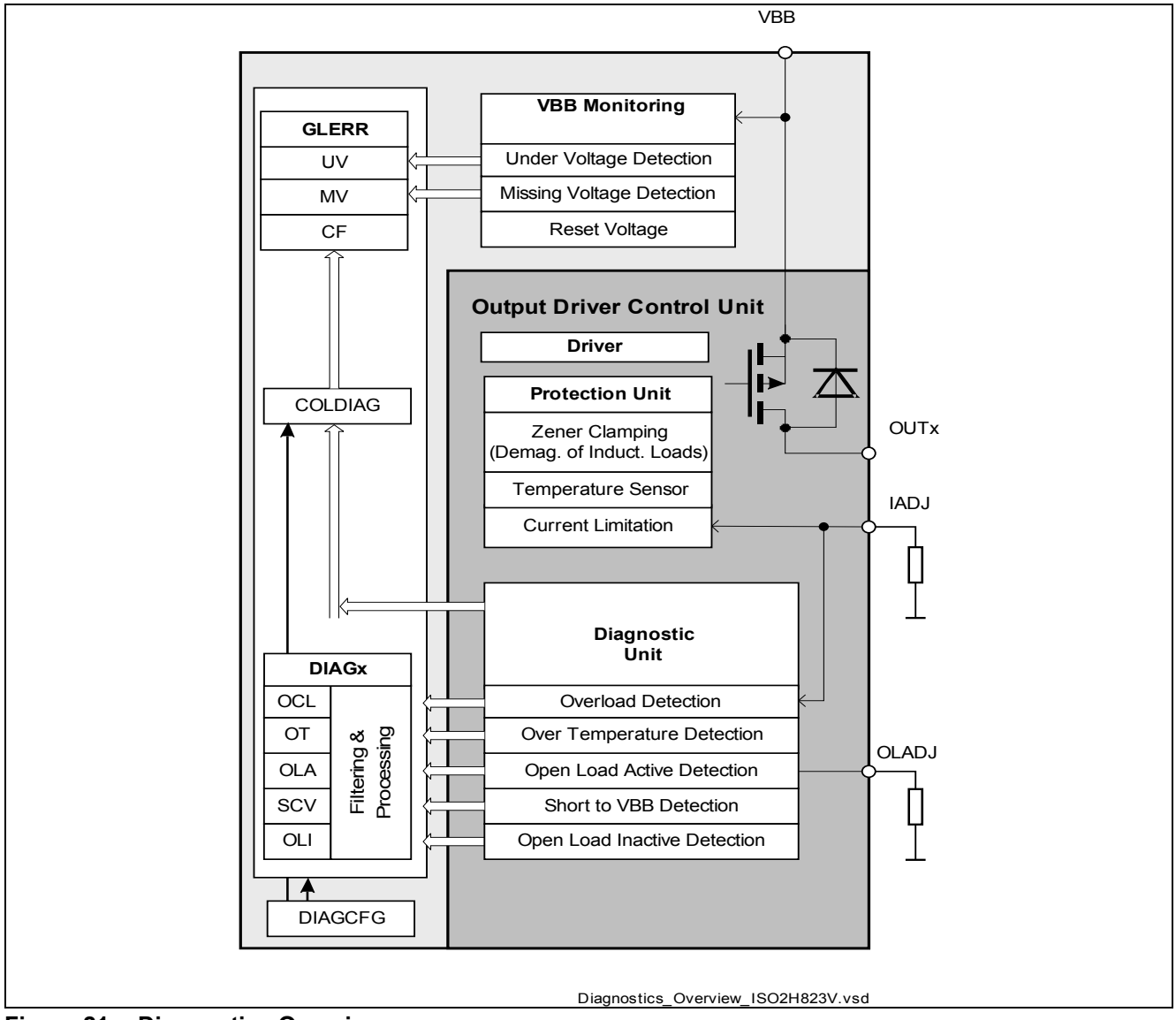


Figure 21 Diagnostics Overview

The diagnostics **OLIx**, **SCVx** are reported in inactive mode and **OLAx** is reported in active mode. When the duration of the disturbance was not sufficient to guarantee a 6 ms blanking/filtering time these diagnostics are at least reported when switching from one mode into the other mode. The diagnostics **OLIx**, **OLAx** and **SCVx**,**OLAx** appear in pairs one component for the inactive mode and one component for the active mode with a delay for the filtering. In order not to allow reporting gaps the diagnostics are prolonged until the complementay part is occurring or until a time out counter has expired (f.e. the diagnostic **OLIx** (**SCVx**) is prolonged also during the active time period until the filter delivers a reliable **OLAx**- (**OLAx**-) diagnostics and vice versa).

4.3.3.1 Diagnostics in Inactive Mode

When the output is in inactive mode a diagnostic current is fed to the output. If the load is connected and the load resistance is less than 12 kΩ, the output voltage will be 300 mV or less.

If no load is connected a voltage drop of 7 V is present at the output. A voltage in the range of 5.5 V up to 9.2 V at the output OUTx is detected and reported as open load inactive (**OLIx**) after filtering.

If the output is shorted to V_{BB} the output voltage will be close to V_{BB} level even in inactive mode, this depends upon the type of the short circuit. A voltage level above 9.2 V at the output is detected and reported as short circuit to V_{BB} (**SCVx**) after filtering.

The window comparator for **OLIx** (5.5 V - 9.2 V) is realized with the analog level comparators for 5.5 V and 9.2 V and the digital filters for **OLIx** and **SCVx**. After filtering **SCVx** has the priority against **OLIx**. By means of the digital filters EMI-contributions shall be filtered before deciding about **OLIx** or **SCVx**.

If a capacitive load with a long RC time constant is connected to the ISO2H823V2.5 (like a 12 kΩ resistor through a long cable with 100 nF capacitance) when switching off, the output voltage sequently passes through the windows of short to VBB detection and broken wire detection. During a blanking time of 6 ms (typ.) the diagnostic signals are ignored to avoid false triggering of diagnostic registers.

If the corresponding channel is switched on again before the end of the blanking time (6 ms) , the state of the diagnostic signals present before switching on is transferred to the diagnostic registers, bypassing the blanking window of 6 ms and filtered instead with a filtering time of 100 us, 0.5 ms, 1 ms depending on the switching frequency.

Table 7 Filter Time in Inactive Mode for OLIx and SCVx

Duration of inactive time t_{OFF} before switching	Filter time
0 ms < t_{OFF} < 1.5 ms	100 us
1.5 ms < t_{OFF} < 3 ms	0.5 ms
3 ms < t_{OFF} < 6 ms	1 ms
t_{OFF} > 6 ms	6 ms (**OLIx**), 2 ms (**SCVx**)

For the largest **SCVx**-filter a filter-length of 2.0 ms is choosen but a setting of **SCVx** is only possible after the blanking window of 6 ms. No single channel over temperature diagnostics is given during inactive mode to avoid false triggering when switching inductive loads.

4.3.3.2 Diagnostics in Active Mode

If during active mode operation the remaining voltage drop of a low load condition is compared to the voltage drop across a reference transistor biased with a reference current. The reference current can be set by the value of a resistor connected between OLADJ and GNDBB defining the threshold for open load diagnostics. The resulting open load threshold is inversely proportional to the connected resistor (25 kΩ - 2.3 kΩ, E96 series; current out of the OLADJ-pin 48.6 µA - 528 µA) and can be set within 0.5 mA to 5 mA.

Like the diagnostics in inactive mode the open load diagnostics in active mode (**OLAx**) is ignored during a 6 ms blanking window after switching on. If the channel is switched off before the end of the blanking window the current state of the open load diagnostics is transferred to the diagnostic registers, bypassing the blanking window of 6 ms and filtered instead with a filtering time of 100 µs, 0.5 ms or 1.0 ms (depending on the switching frequency).

The over load diagnostic (**OCLx**) occurs generally if the output stage limits the load current. Therefore the diagnostic threshold is equal to the current limiting value. An overload may and a short to GNDBB will probably lead to a thermal shutdown. The shutdown is indicated separately by the diagnostics **OTx**. The standard filter time for overload (**OCLx**) and overtemperature (**OTx**) is 50 us (for a thermal shutdown).

Table 8 Filter Time in Active Mode for OLAx

Duration of active time t_{ON} before switching	Filter time
0 ms < t_{ON} < 1.5 ms	100 us
1.5 ms < t_{ON} < 3 ms	0.5 ms
3 ms < t_{ON} < 6 ms	1 ms
t_{ON} > 6 ms	6 ms

Some loads like incandescent lamps or DC motors show an inrush current, which is normal and should not trigger an overload diagnostic. In some cases even a transient thermal shutdown can not be avoided but an **OTx**-message is avoided for the time duration of running up f.e. a cold lamp (max. 200 ms). In this case and only for this short time duration the current limiting threshold can be set to 1.5 A and the temperature threshold to 200°C by the internal finite state machine.

The ISO2H823V2.5 adapts filtering of over load and thermal shutdown diagnostics as well as shutdown temperature and current limit level by evaluating the previous turn off time and the load resistance.

4.3.3.3 Diagnostic Scenarios in Dependence of Switching Frequency

The **Table 9** explains the occurence of diagnostics dependent on the switching frequencies for the disturbance “Short-Circuit-to-VBB”.

Table 9 Occurence of Diagnostics during the Disturbance : Short-Circuit-to-VBB

Stable Switching Frequency : f	**Reported Diagnostic**	**Unwanted Diagnostics at Onset of .....or at Resolving of SCVx-Disturbance**	
permanently “low” : f <= 62,5 Hz	**SCVx**, **OLAx**		**OLIx** [1]
permanently “intermediate” 62,5 Hz < f < 2 kHz	**SCVx**, **OLAx**	**OLIx** [2]	
permanently “high” f >= 2 kHz	**SCVx**, **OLAx**	**OLIx** [2]	
Transitions in the Switching Frequency : f			
permanently “low” --> permanently “high” f <= 62,5 Hz --> f >= 2 kHz	**SCVx**, **OLAx**	**OLIx** [1] [2] : depends on the time of onset and resolving of **SCVx**-disturbance	
permanently “high” --> permanently “low” f >= 2 kHz --> f <= 62,5 Hz	**SCVx**, **OLAx**	**OLIx** [1] [2] : depends on the time of onset and resolving of **SCVx**-disturbance	

1) In **Table 9** an additional **OLIx**-signal can be generated when **1. the SCVx-disturbance has been resolved in the inactive phase** and **2.** the inactive phase is longer than 8 ms (f < 62,5 Hz) and **3.** the **SCVx**-disturbance has been existing for >= 6 ms in the inactive phase. The occurence of the additional **OLIx**-signal depends on the relative duration of the inactive mode and the **SCVx**-disturbance. **It disappears at last after 4 ms or with continued switching of the power transistor.** As the user himself has caused the additional **OLIx**-signal by resolving the **SCVx**-disturbance the user can ignore this signal for the next 4 ms or can continue switching the power transistor.

2) Depending on the onset of the **SCVx**-disturbance in scenarios with high or intermediate switching frequency **one time an unwanted OLIx-reporting can occur which vanishes during further switching**. As in the upper case [1] the user can ignore it as in the sequel the correct signaling occurs.

The **Table 10** explains the occurence of diagnostics dependent on the switching frequencies for the disturbance “Openload”.

Prerequisite : an external capacitor of C = 10 nF (minimum value) for enhancing the EMI-robustness is attached to the output. VBB = 24 V.

In **Table 10** the additional **SCVx**-diagnostic reflects the transition from active to inactive mode when the external C (EMI-robustness) has to be decharged via a high ohmic internal resistor. During the decharging process the output voltage is in the region of reporting **SCVx**.

Table 10 Occurence of Diagnostics during the Disturbance : Wirebreak

Stable Switching Frequency : f	**Reported Diagnostic**	**Comment**
permanently “low” : f <= 50Hz	**OLIx**, **OLAx**, **SCVx**	additionally **SCVx**[1)]
permanently “intermediate” 50 Hz < f < 2 kHz	**SCVx**, **OLAx**	instead of **OLIx** : **SCVx**[2)]
permanently “high” f >= 2 kHz	**SCVx**, **OLAx**	instead of **OLIx** : **SCVx**[2)]
Transitions in the Switching Frequency : f		
permanently “low” --> permanently “high” f <= 50 Hz --> f >= 2 kHz	**OLIx**, **OLAx**, **SCVx** ---> **SCVx**, **OLAx**	additionally **SCVx**[1)]
permanently “high” --> permanently “low” f >= 2 kHz --> f <= 50 Hz	**SCVx**, **OLAx** ----> **OLIx**, **OLAx**, **SCVx**	additionally **SCVx**[1)]

1) **additionally SCVx reported**, diagnostic due to decharging of the external C (EMI-robustness)

2) **instead of OLIx is SCVx reported**,diagnostic due to decharging of the external C (EMI-robustness)

4.3.3.4 Global Diagnostics

The global diagnostics include:

- **UV**: undervoltage supply condition when VBB is below 16 V with 0.5 V hysteresis,
- **MV** : missing voltage supply condition when VBB is below 13 V with 0.5 V hysteresis,
- **OTP**: global over temperature (chip temperature outside the switch area triggers above 125 °C), the global over temperature does not lead to thermal shutdown,
- **ALLOFF**: all drivers in the power chip are disabled (by **DRIVE**-programming, $\overline{\text{ODIS}}$-setting or temperature shutdown of all channels),
- **LAMP**: the load of one of the drivers behaves like a cold lamp

4.3.3.5 Power Supply

The startup procedure of the power chip is explained in **Figure 22**.

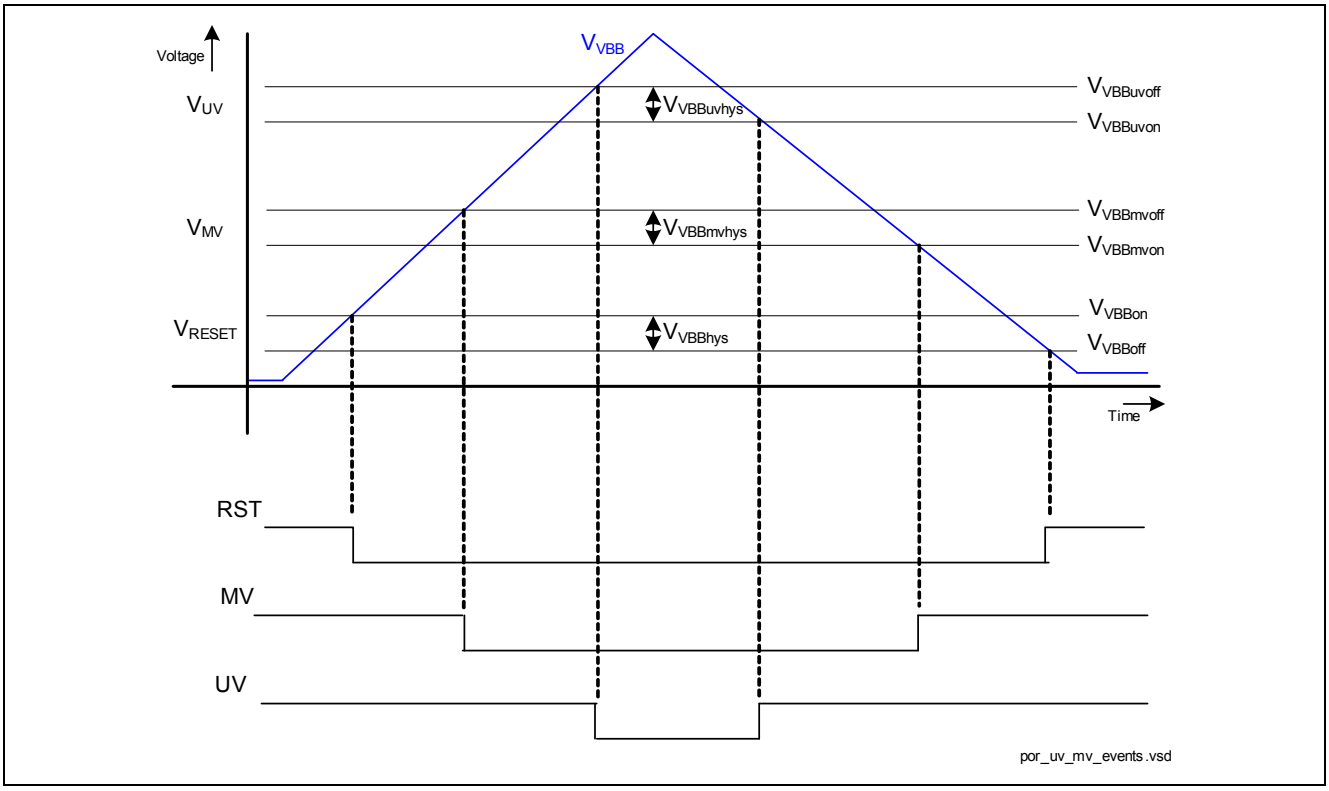


Figure 22 Start Up Procedure of the Power Chip

During UVLO, all registers of the power chip are reset to their reset values as specified in the register description (Chapter 6). As a result, the flags **TE**, **UV** as well as **MV** are High and the $\overline{\text{ERR}}$ pin is Low (error condition). Immediately after the reset is released, the chip is first configured by “reading“ the logic level of the SEL, MS1, MS0 - pins. The IC powers up as a parallel device i.e. the AD0-7 pins are high-impedance until the IC configuration is over.

The supply voltage VBB is monitored during operation by two internal comparators (with typ. 2 ms blanking time) detecting:

- VBB Undervoltage: If the voltage drops below the **UV** threshold, the **UV**-bit in the **GLERR** register is set High. The IC operates normally.
- VBB Missing Voltage: If the voltage further drops below the **MV** threshold, lower than the previous threshold, the **MV**-bit in the **GLERR** register is set, the Power Side of the IC is turned off when reaching the VReset-threshold whereas the Micro-Controller Side remains active.

Note: The driver stage is self protected in overload condition: the internal switches will be turned off as long as the overcurrent condition is detected and the IC will automatically restart once the overload condition disappears.

Important: Since the **UV** and **MV** (as well as the **TE**) bits used for generating the $\overline{\text{ERR}}$ signal are preset to High during UVLO, the $\overline{\text{ERR}}$ pin is Low after power up. Therefore the $\overline{\text{ERR}}$ requires to be explicitly cleared after power up. At least one read access to the **GLERR** and **INTERR** registers or one default read access in certain access-modes (see **Chapter 4.2.3**) is needed to update those status bits and thus release the $\overline{\text{ERR}}$ pin.

4.3.4 LED Matrix

The driving signal for the LED-matrix is the drive-signal of the register DRIVE gated with the signal **LEDGx** of the registers **DIAG0**,...,**DIAG7**. This signal is generated in the power chip and transferred via the CT-interface to the uC-Chip. For suppressing a thermic toggling visible on the LED-matrix **LEDGx** disables the related LED for at least 100ms when an overtemperature (**OTx**) or overcurrent condition (**OCLx**) has occurred.

4.3.4.1 LED Matrix on the Process Side

Eight LEDs arranged in a 3x3 matrix can be driven through the outputs LEDx0 to LEDx2 and LEDy0 to LEDy2 of the Power Chip. Each output channel has a corresponding status LED in the matrix showing the actual status of the channel. When the LED lights up, the corresponding channel is in the active mode and has no thermal shutdown and no overcurrent condition.

Series resistors must be inserted in each column line LEDy0...LEDy2 to set the LED current. The driving level on the column lines is the V_{BB} voltage level. The row lines are driven alternately with 1/3 duty cycle at 1000 Hz. The resulting average current for each LED is 1/3*(V_{BB} minus diode forward voltage)/series resistance.

If the diode matrix is used at all, all 8 LEDs must be connected for correct function of the matrix.

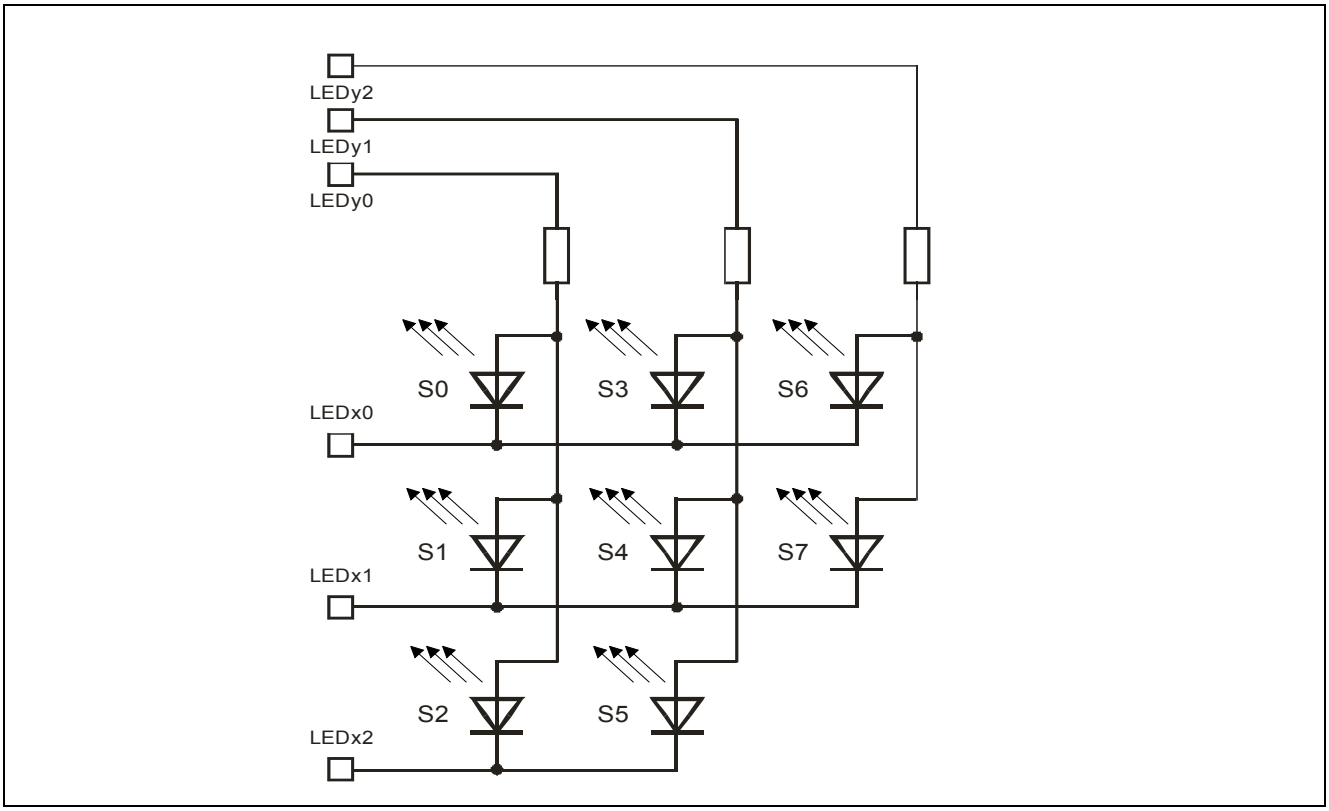


Figure 23 LED Matrix connected to the Power Chip

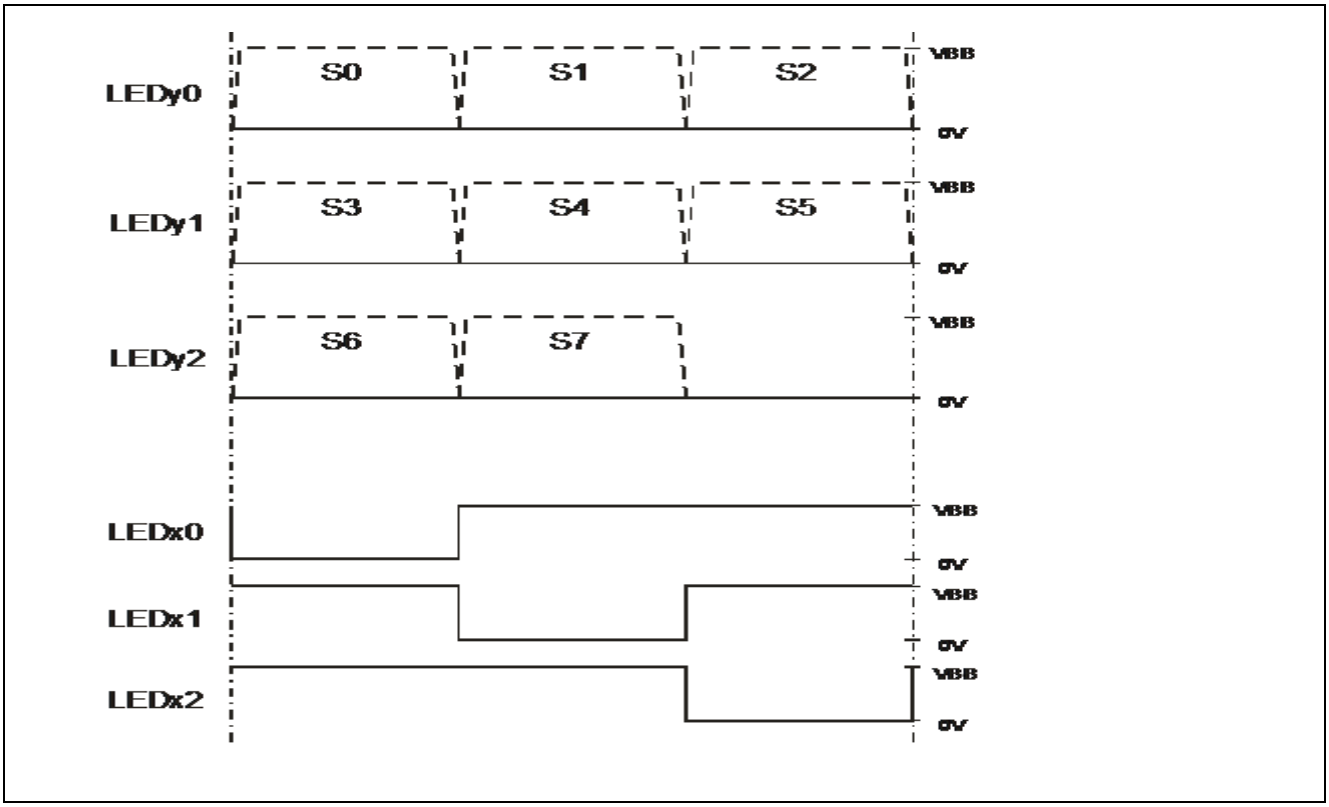


Figure 24 LED Pulse Diagram

If no LEDs are used at all it is possible (by reasons of EMI) to connect all column signals LEDY0,..,2 together and all row-signals LEDx0,..,2 together but a connection among columns and rows is not allowed. In the case of paralleling of channels it is possible to substitute the unused LEDs by resistors which have the only function to dissipate the current which is delivered in case the not existing diode is accessed. If no limiting element is used (f.e. resistor) the voltage at the LEDs of the non-activated rows can rise up to VBB if the non-existing element is activated (the related row activated and the corresponding column activated).

4.3.4.2 LED Matrix on the uController Side (only in Serial Communication Mode)

For the driving signals on the uController-side the following pins are used for the column signals : AD1 / LEDC2, ALE/RST / LEDC1, $\overline{WR}$ / LEDC0 and for the row-signals : AD2 / LEDR2, AD3 / LEDR1, AD6 / LEDR0. For enabling the LED-function on the uC-Chip side the bit **LEDON** in the **GLCFG**-register has to be set. LED-operation is only possible in the serial communication mode. If **LEDON** = 1 the hardware reset function is disabled.

As in the case for the LED on the power chipside a 3x3 matrix can be driven. Each output channel has a corresponding status LED in the matrix showing the actual status of the channel. When the LED lights up, the corresponding channel is in the active mode and has no thermal shutdown and no overcurrent condition. The 9.th LED is connected with the $\overline{ERR}$-signal.

Series resistors must be inserted in each column line LEDC0...LEDC2 to set the LED current. The driving level on the column lines is the V_{CC} voltage level. The row lines are driven alternately with 1/3 duty cycle at 1000 Hz. The resulting average current for each LED is 1/3*(V_{CC} minus diode forward voltage)/series resistance.

If the diode matrix is used (**LEDON** = 1) , all 9 LEDs must be connected for correct function of the matrix.

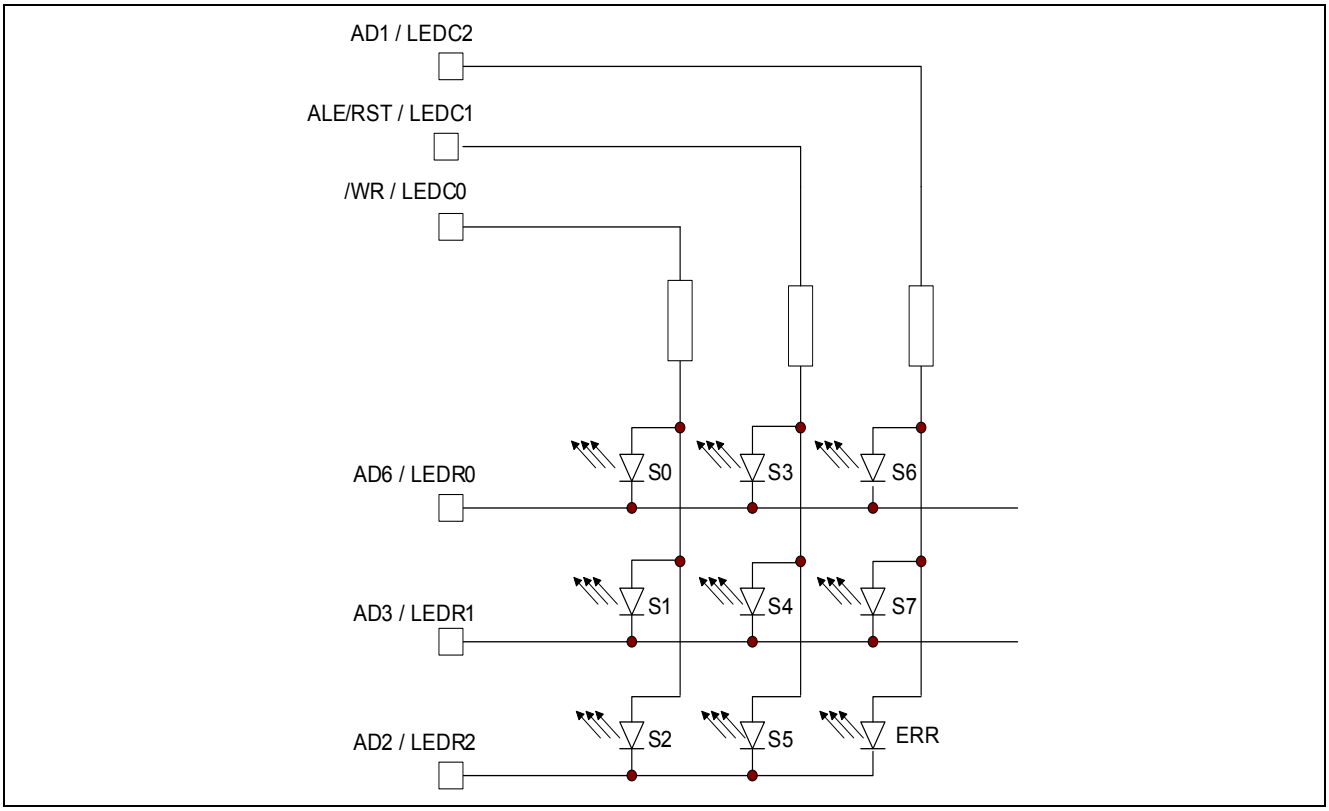


Figure 25 LED Matrix connected to the uC-Chip

In the case of paralleling of channels it is possible to substitute the unused LEDs by resistors which have the only function to dissipate the current which is delivered in case the not existing diode is accessed.

The minimum value of the VCC-voltage is 2.75 V. But this low voltage will limit the choice of the used LEDs (in the worst case only LEDs with a lower forward voltage of around 2.2 V are possible).

4.4 EMI-Robustness

Care has been taken to increase the Burst- and RFCM-robustness according to the standardization requirements referenced in

- DIN EN 61131-2 (Programmable Controllers , Part 2 : Equipment Requirements and Tests)
- IEC 61000 -4-4 (Testing and measurement techniques - electrical fast transient/burst immunity test)
- IEC 61000 -4-6 (Testing and measurement techniques - immunity to conducted disturbances, induced by radio-frequency fields)

respectively.

As the standardization document DIN EN 61131-2 gives a system-requirement we can give only recomendations for the application with ISO2H823V2.5 for improvement the EMI-robustness. Exact values have to be evaluated with the total system including external components and PCB-layout and wiring.

For Burst- and RFCM-robustness we consider only the driver-pins OUTx and VBB as these pins are exposed to external disturbances. Other pins of ISO2H823V2.5 are encapsulated within the housing of the control equipment (f.e. PLC).

The influence of HF-signals is eliminated internally with assistance of the external capacitor of min.10 nF ($\pm$ 10%) at the output OUTx of each power transistor. To increase the safety margin if higher test voltages are applied it is possible to increase the capacitor up to 12 nF $\pm$ 10 %.The purpose is to suppress frequency contributions of the external disturbance greater than 2 MHz.

Investigations have been done with an external load of a high value of 12 kΩ. Other critical loads consisting of a high inductive value combined by a high resistive value (f.e. 0.8 H, 1.4 kΩ) have been also examined.

4.4.1 Burst Robustness

Figure 26 shows the test circuitry for applying burst pulses. The fat drawn equipment symbolizes the burst-generator and the coupling of burst pulses to the OUTx-pins and/or to the VBB-pin (see the different coupling network for OUTx, VBB as specified in IEC 61000).

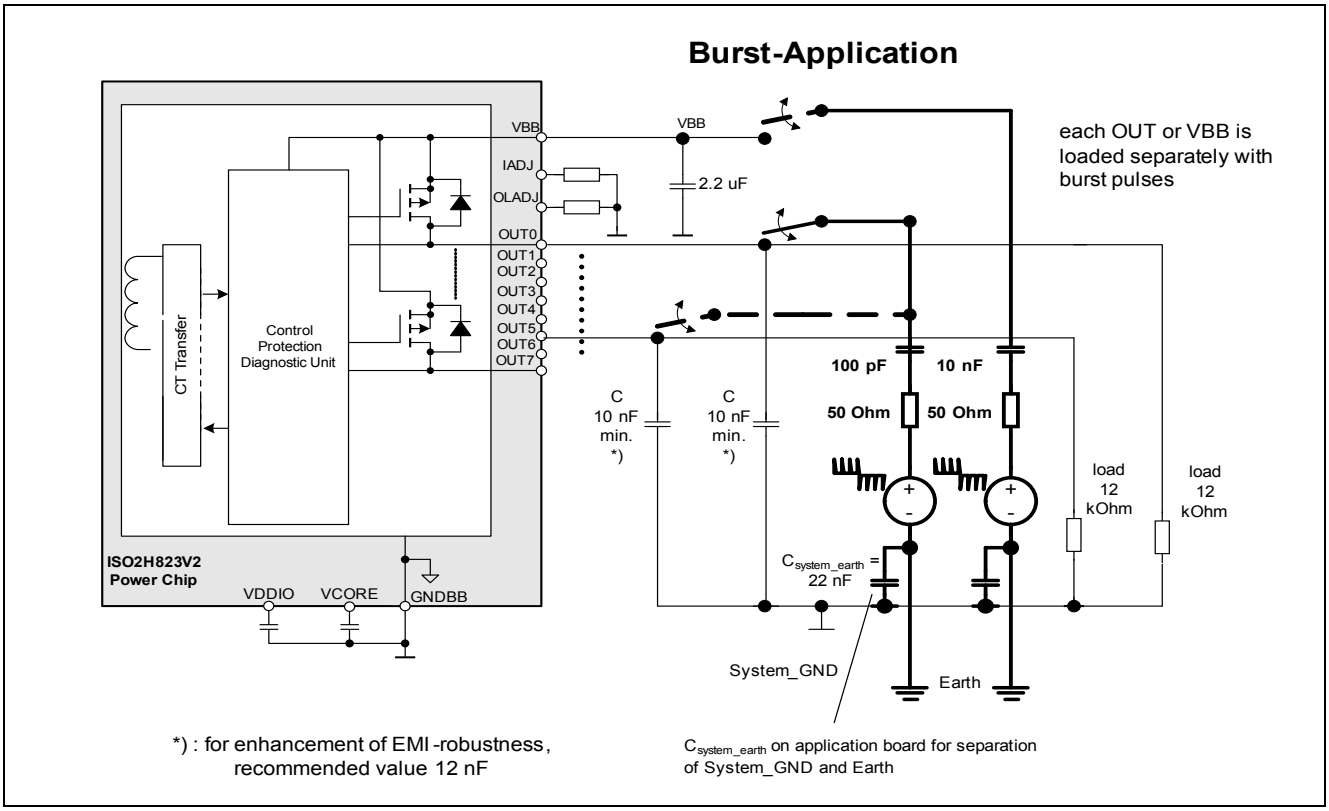


Figure 26 Burst-Application

For burst-disturbance the standard foresees 2 repetition frequencies : 5 kHz and 100 kHz. For the repetition frequency of 5 kHz the target is to achieve a burst-robustness of min .± 2500 V within the system with external elements. For a repetition frequency of 100 kHz it is much harder a give an estimation without the knowledge of external elements. For this case no statement is given here.

4.4.2 RFCM-Robustness

Figure 27 shows the test circuitry for applying RFCM frequencies. The fat drawn equipment symbolizes the HF-generator and the coupling of HF frequencies to the OUTx-pins and/or to the VBB-pin (the drawn coupling network shall symbolize an effective impedance of 150 Ω regardless of the frequency as specified in IEC 61000). The HF-disturbance is an 80%-amplitude modulated signal with the carrier frequency of 10 kHz - 80 MHz and the modulation frequency of 1 kHz.

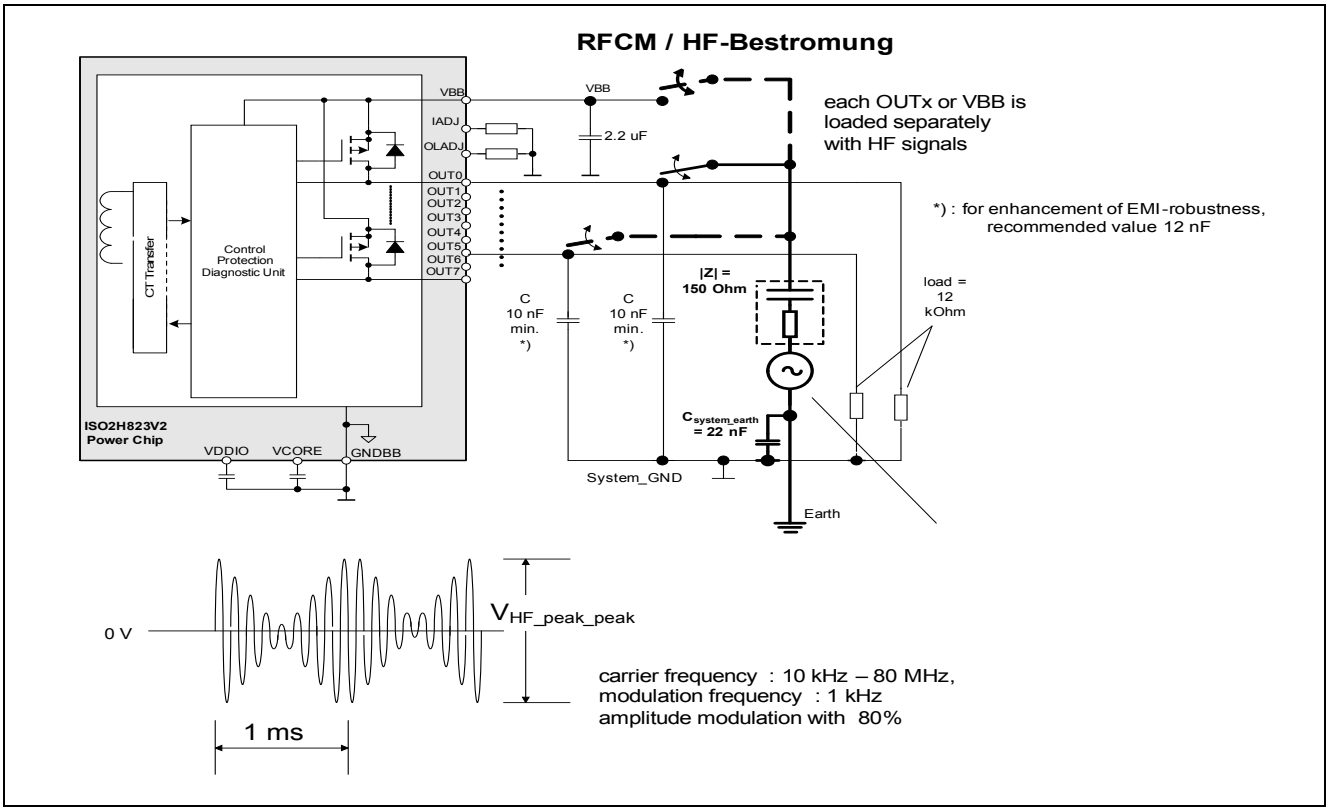


Figure 27 RFCM-Application

The 80 % amplitude modulated signal is shown in **Figure 27** in the lower half. With external elements on the user-PCB-board it is targeted to achieve a RFCM-robustness against the defined HF-signals of $V_{HF\_peak\_peak}$ = ± 25 V.

4.5 Application Hints

4.5.1 Layout Recommendations

The reference resistor for CLKADJ must be placed close to the pin 38 CLKADJ and pin 39 GND. Decoupling capacitors should be close to VCC terminal pin 37 and directly connected to the GND plane on the PCB.

GND and GNDBB must be totally isolated in the PCB layout. A separation distance of min. 3.2mm is recommended.

The reference resistors for OLADJ, IADJ must be placed close to their terminals of the ISO2H823V2.5 and the connection to the referring ground plane should be as short as possible. The capacitors for V_{CORE} and V_{DDIO} must be placed close the pins and directly connected to the GNDBB plane.

5 Electrical Characteristics

Note: All voltages at pins 1 to 32 as well as 61 to 70 are measured with respect to GNDBB. All voltages at pins 33 to 60 are measured with respect to GND. The voltage levels are valid if other ratings are not violated. The two voltage domains V_{CC} and V_{BB} are internally galvanic isolated.

Note: All Typical Values are defined by T_j = 25°C, V_{BB} = 24 V, V_{CC}= 3.3V.

*Note: Electrical Values are defined in the range T_j = -40 ... 125°C, V_{BB} = 11...35 V, V_{CC} = 2.75...3.6 V, unless otherwise specified, **Table 13** to **Table 26**.*

5.1 Absolute Maximum Ratings

(at T_j = -40 … 135 °C, unless otherwise specified)

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 37 (V_{CC}) is discharged before assembling the application circuit. Operating at absolute maximum ratings can lead to a reduced lifetime.
Absolute maximum ratings are not subject to production test.

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage input interface	V_{CC}	-0.5	–	3.6	V	–
Supply voltage output interface	V_{BB}	-1[1)]	–	45	V	–
Continuous voltage at data inputs (AD0 … AD7)	V_{Dx}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{CS}$	V_{CS}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ALE}$	V_{ALE}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{RD}$	V_{RD}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{WR}$	V_{WR}	-0.5	–	3.6	V	–
Continuous voltage at pin SYNC	V_{SYNC}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ODIS}$	V_{ODIS}	-0.5	–	3.6	V	–
Continuous voltage at pin $\overline{ERR}$	V_{ERR}	-0.5	–	3.6	V	–
Continuous voltage at pin SEL	V_{SEL}	-0.5	–	3.6	V	–
Continuous voltage at pin MSx	V_{MSx}	-0.5	–	3.6	V	–
Continuous voltage at pin CLKADJ	V_{CLKADJ}	-0.5	–	3.6	V	–
Continuous voltage at pin VCORE	V_{VCORE}	-0.5	–	1.65	V	–
Continuous voltage at pin VDDIO	V_{VDDIO}	-0.5	–	3.6	V	–
Continuous voltage at pin IADJ	V_{IADJ}	-0.5	–	3.6	V	–
Continuous voltage at pin OLADJ	V_{OLADJ}	-0.5	–	3.6	V	–
Continuous voltage at pin OUTx	V_{OUTx}	V_{BB} -55	–	V_{BB}	V	–
Continuous voltage at pin LEDXx	V_{LEDXx}	-0.5	–	V_{BB}	V	–
Continuous voltage at pin LEDYx	V_{LEDYx}	-0.5	–	V_{BB}	V	–

Table 11 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Load current (short-circuit current)	I_L	–	–	Self limited	A	–
LED matrix driver current	I_{LED}	-20		20	mA	Peak current each LED
Static operating temperature	$T_{j\ stat}$	-40		Internal limited	°C	Static operation
Peak junction temperature	$T_{j\ per}$	–		175	°C	Periodic duty cycle <1%
Peak junction temperature	T_{js}	–		200	°C	Non periodic
Periodic temperature cycling	ΔT_{jper}	–		75	K	f = 2 Hz
Transient thermal impedance all 8 channels	Z_{th}	–	0.375	–	K/W	12 ms sawtooth pulse, all channels equally loaded
Transient thermal impedance single channel	Z_{th}	–	3.5	–	K/W	50 ms sawtooth pulse 1 channel loaded
Storage Temperature	T_{stg}	-50	–	150	°C	–
Power Dissipation[2)]	P_{tot}	–	–	1.5	W	–
Inductive load switch-off energy dissipation for each channel, single pulse[3)], all channels are switching simultaneously, T_j=125°C, I_L = 0.6 A	E_{AS}			150	mJ	
Electrostatic discharge voltage (Human Body Model) according to JESD22-A114	V_{ESD}	–	–	2	kV	–
Electrostatic discharge voltage (Charge Device Model) according to JESD22-C101	V_{ESD}	–	–	0.5	kV	–

1) Defined by P_{tot}.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Single pulse means that the thermal recovery time is sufficient so that an increase of the chip temperature is avoided or at least limited (depends on the thermal connection of chip with PCB-board, **Figure 34**- **Figure 36**) .

5.2 Operating Conditions and Power Supply

For proper operation of the device, absolute maximum rating (Table 11) and the parameter ranges in Table 12 must not be violated. Exceeding the limits of operating condition parameters may result in device malfunction or spec violations. The power supply pins V_{BB} and V_{CC} have the characteristics given in Table 14.

Table 12 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage Logic V_{CC}	V_{VCC}	2.75	–	3.6	V	Related to GND
Supply Voltage Power V_{BB}	V_{VBB}	11	–	35	V	Related to GNDBB
Ambient Temperature	T_A	-40	–	85	°C	–
Junction Temperature	T_J	-40	–	150	°C	
Package Temperature	T_{pack}	-40	–	125	°C	Exposed Pad
Common Mode Transient	dV_{ISO}/dt	-25	–	25	kV/µs	1)
Magnetic Field Immunity	$\|HIM\|$	30	–	–	A/m	IEC61000-4-8 1)
Bias Resistor for Current Limit	R_{IADJ}	6.46	6.81	7.14	kΩ	C_{IADJ} < 25 pF
Bias Resistor for Open Load	R_{OLADJ}	2.3	–	25	kΩ	C_{OLADJ} < 25 pF
Bias Resistor for CLKADJ	R_{CLKADJ}	9.9	10	10.1	kΩ	E96-resistor, C_{CLKADJ} < 25 pF

1) Not subject to production test, specified by design.

Table 13 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - case top 1)	R_{thJC_Top}	–	–	10.5	K/W	Measured on top side
Thermal resistance junction - case bottom 1)	R_{thJC_Bot}	–	–	0.5	K/W	–
Thermal resistance junction - pin 1)	R_{thJP}	–	–	26	K/W	
Thermal resistance 2)1)	$R_{th(JA)}$	–	23	–	K/W	–

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Table 14 Electrical Characteristics of the Power Supply Pins

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{BB} UVLO startup threshold	V_{VBBon}	–	8.9	9.35	V	–
V_{BB} UVLO shutdown threshold	V_{VBBoff}	7.5	7.9	–	V	–
V_{BB} UVLO Hysteresis	V_{VBBhys}	–	1	–	V	–
V_{BB} missing voltage OFF (MV) threshold	$V_{VBBmvoff}$	–	13.3	14.0	V	–
V_{BB} missing voltage ON (MV) threshold	$V_{VBBmvon}$	12.1	12.8	–	V	–
V_{BB} undervoltage OFF (UV) threshold	$V_{VBBuvoff}$	–	16.2	17.0	V	–
V_{BB} undervoltage ON (UV) threshold	$V_{VBBuvon}$	14.9	15.7	–	V	–
Glitch filters for V_{BB} missing voltage and undervoltage[1]	T_{VBBfil}	–	2	–	ms	–
Undervoltage Current for V_{BB}	I_{VBBuv}	–	1.7	–	mA	V_{VBB} < 7.0 V
Quiescent Current V_{BB}	I_{VBBq}	–	9	–	mA	V_{VBB} = 24 V, all channels inactive, V_{CC} = 0 V
Voltage Level of VDDIO	V_{VDDIO}	–	3.3	–	V	V_{VBB} = 24 V
Voltage Level of VCORE	V_{VCORE}	–	1.5	–	V	V_{VBB} = 24 V
Startup Delay (time between V_{BBon}/V_{CCon} and first active mode)[1]	t_{VXXon}	–	0.3	–	ms	–
V_{CC} UVLO startup threshold	V_{VCCoff}	–	–	2.75	V	–
V_{CC} UVLO shutdown threshold[2]	V_{VCCon}	2.5	–	–	V	–
V_{CC} UVLO threshold hysteresis	V_{VCChys}	0.01	–	–	V	–
Quiescent Current V_{CC}	I_{VCCq}	–	1.2	–	mA	V_{VCC} = 2.4 V
Current V_{CC} without SPI-Activity	I_{VCC}	–	5.8	8.5	mA	V_{VCC} = 3.6 V
Current V_{CC} without SPI-Activity	I_{VCC}	–	-	8	mA	V_{VCC} = 3.3 V
Current V_{CC} without SPI-Activity	I_{VCC}	–	-	7	mA	V_{VCC} = 2.75 V

1) Not subject to production test, specified by design.

2) Note that the specified operation of the IC requires V_{VCC} as given in **Table 12**

5.3 Load Switching Capabilities and Characteristics

Table 15 Load Switching Capabilities and Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-state resistance	R_{ON}	–	210	250	mΩ	I_L = 0.6 A T_j = 125 °C VBB = 24 V, Each channel
Leakage output current (included in $I_{BB(off)}$)	$I_{L(off)}$	–	–	35	µA	V_{ADx} = low, each channel, x = 0,...,7, VBB = 24 V
Turn-on time to 90% V_{OUT} [1]	t_{on}	–	–	30	µs	R_L = 48 Ω, V_{ADx} = 0 to 3.3V, V_{BB} = 24 V
Turn-off time to 10% V_{OUT} [1]	t_{off}	–	–	30	µs	R_L = 48 Ω, V_{ADx} = 3.3 to 0V, V_{BB} = 24 V
Slew rate V_{OUT}	dV/dt_{on}	–	2	–	V/µs	R_L = 48 Ω, V_{BB} = 24 V
Slew rate V_{OUT}	$-dV/dt_{off}$	–	2	–	V/µs	R_L = 48 Ω, V_{BB} = 24 V

1) The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a transmission error on the coreless transformer transmission turn-on or turn-off time can increase by up to 20 µs.

5.4 Output Protection Functions

Table 16 Output Protection Functions [1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current limit	I_{OCL}	0.73	1	1.3	A	V_{BB} - V_{out} = 1 V
Short circuit current	I_{SCL}	0.7	1	1.4	A	V_{BB} - V_{out} = 28.8 V [2]
Output clamp (inductive load switch off) [3] at V_{OUT} = V_{BB} - $V_{ON(CL)}$	$V_{ON(CL)}$	45	52	60	V	$I_{ON(CL)}$ = 50 mA
Thermal overload trip temperature [4]	T_{jt}	135	150	–	°C	–
Thermal hysteresis [4]	ΔT_{jt}	–	15	–	K	–

1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.
2) Thermal effects when $T_{jswitch} >> T_{case}$
3) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$.
4) Not subject to production test, specified by design.

5.5 Electrical Characteristics µController Interface

For the Parallel Mode see **Table 17**, **Table 19**, **Table 23** and **Table 25**

For the Serial Mode see **Table 17**, **Table 19**, **Table 24** and **Table 25**

Timing characteristics refer to C_L < 50 pF and R_L > 10 kΩ

Table 17 Setting at the Configuration Pin (CLKADJ)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKADJ Pin Regulated Voltage	$V_{CLKADJreg}$	–	0.5	–	V	–

Table 18 Error Pins ($\overline{ERR}$, $\overline{CRCERR}$)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Error Voltage ($\overline{ERR}$, $\overline{CRCERR}$=0)	V_{ERR_CRCERR}	–	–	0.25 V_{CC}	V	I_{ERR_CRCERR} = 5 mA[1]
Error Pin Pull-Up Resistance ($\overline{ERR}$, $\overline{CRCERR}$ = 1)	$R_{ERR\_CRCERR\ pu}$	–	50	–	kΩ	–
Maximum Switching Frequency ($\overline{ERR}$, $\overline{CRCERR}$)[2]	f_{SW}	–	200	–	kHz	10 kΩ external Pull-Up Resistor

1) Spikes on $\overline{CRCERR}$ due to f.e. cross coupling between SCLK and $\overline{CRCERR}$ are not expected to violate this figure V_{ERR_CRCERR}, because cross coupling pulses are very small (10 nsec), V_{ERR_CRCERR} is evaluated after the rising edge of $\overline{CS}$ (and not during any edges of SCLK) and with a lower I_{ERR_CRCERR} (f.e. 1 mA) V_{ERR_CRCERR} is also lowered (in the example by a factor of 5).

2) Not subject to production test, specified by design; worst case is the reading in serial mode 2 with a frequency of 500 kHz $\overline{CRCERR}$ can toggle with 500 kHz

Table 19 Logical Pins ($\overline{RD}$, $\overline{WR}$, ALE, MS0/1, $\overline{CS}$, AD7: AD0, SCLK, SDO, SDI, SEL, SYNC, $\overline{ODIS}$)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage High Level	V_{IH}	0.7·V_{VCC}	–	V_{VCC}+0.3	V	–
Input Voltage Low Level	V_{IL}	-0.3[1]	–	0.3·V_{VCC}	V	–
Input Voltage Hysteresis	V_{Ihys}	–	100		mV	–
Output Voltage High Level	V_{OH}	0.75·V_{VCC}	–	1·V_{VCC}	V	I_{OH} = 5 mA[2]
Output Voltage Low Level	V_{OL}	0	–	0.25·V_{VCC}	V	I_{OL} = 5 mA
Output Voltage High Level	V_{OH}	-	2.65	-	V	V_{VCC} = 2.75V, I_{OH} = 1mA[3]
Output Voltage Low Level	V_{OL}	-	0.1	-	V	V_{VCC} = 2.75V - 3.6V, I_{OL} = 1mA

1) Not subject to production test, specified by design.

2) Maximum source / sink current: I_{OHmax} = I_{OLmin} = 5 mA; external load C_L < 50 pF, R_L > 10 kΩ

3) Same argumentation as for Digital Input Isoface : typical values over temperature derived for I_{OH} = 5 mA and I_{OL} = 5 mA. Extrapolation to I_{OH} = 1mA and I_{OL} = 1mA to possible. Voltage drop scales with a factor of 1/5 with the change of 5 mA to 1 mA. Not subject to production test.

Table 20 SYNC-Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Minimum time interval for µC-Read-Access after falling edge of SYNC-signal	$t_{syncmin}$	400	500		ns	1)
Minimum width of SYNC-signal	t_{syncw}	200			ns	1)
SYNC-period	$t_{syncper}$	500			ns	1)
Minimum time interval for Direct-Write-Access after falling edge of SYNC-signal (to ensure that the new data are not CT-transmitted during SYNC = low)	t_h	400	500		ns	1)

1) not subject of production test, specified by design

Table 21 RESYNCH-Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Minimum width of SYNC-low-phase during resynchronization	$t_{resynch}$	7.0	--	240	us	1)
Minimum time interval between two resynchronization processes (minimum width of SYNC-high-phase)	t_{resync_gap}	1.0			us	1)
Timing jitter of transmission of drive-data over CT	$t_{resynch\_jitter}$	-0.75	--	0.75	us	1)

1) not subject of production test, specified by design

Table 22 Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{CS}$ Disable time ($\overline{CS}$ high time between two read accesses on different registers)	t_{CSD}		400		ns	1)
Read-Period for two read accesses on the same register (especially for COLDIAG, GLERR, INTERR)	t_{RD_PER}		2000		ns	1)
$\overline{CS}$ Disable time ($\overline{CS}$ high time between a write access and a read access for reading back the written value)	t_{CSD_WRRD}		400		ns	1)

1) not subject of production test, specified by design

Table 23 Parallel Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$)	R_{PU}	–	50	–	kΩ	–
Input Pull Down Resistance (ALE)	R_{PD}	–	50	–	kΩ	–
$\overline{CS}$ setup time related to ALE	t_{CS_ALE}	14			ns	
ALE high duration (for addressing)	t_{ALE_high}	200			ns	
$\overline{WR}$ Low duration (for Write Data)	t_{WRlow}	100			ns	
$\overline{WR}$ High duration (for Write Data)	t_{WRhigh}	100			ns	
Read Request Frequency	f_{RD}	0.033[1]	–	2.5	MHz	repeated read access during $\overline{CS}$ = 0
Read Request Period (1/f$\overline{RD}$)	t_{RD}	400	–	30000[2]	ns	repeated read access during $\overline{CS}$ = 0
$\overline{RD}$ Low duration (by Read)	t_{RDlow}	200			ns	
AD7:AD0 Output disable time	t_{float}	20		80	ns	
AD0-7 Output Valid (by Read)	t_{ADout}			180	ns	
$\overline{RD}$ setup time	t_{RD_su}	50			ns	
$\overline{WR}$ setup time	t_{WR_su}	50			ns	
$\overline{RD}$ hold time	t_{RD_hd}	20			ns	
$\overline{WR}$ hold time	t_{WR_hd}	20			ns	
$\overline{WR}$ latency time	t_{lat}[3]		300		ns	
$\overline{RD}$ Pad to COLDIAG, GLERR and INTERR Registers Update (Bits Clearing)	t_{clrrdy}[4]		300		ns	
AD0-7 Data bus setup time	t_{AD_su}	20			ns	
AD0-7 Data bus hold time	t_{AD_hd}	60			ns	
Time for $\overline{CS}$ = $\overline{WR}$ = ALE = 0, $\overline{RD}$ = 1 until direct mode is entered	t_{direct}		30		us	

1) Minimum value to guarantee that the direct control mode is not entered, see also t_{RD} and t_{direct}

2) After 30 us the interface may enter the direct control mode, see also t_{direct}

3) not subject to production test, t_{lat} determined by internal synchronization cycles (internal clock 10 MHz) and propagation over CT (5 us)

4) not subject to production test, t_{clrrdy} determined by internal synchronization cycles (internal clock 10 MHz)

Table 24 Serial Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ($\overline{CS}$)	R_{PU}	–	50	–	kΩ	–
Input Pull Down Resistance (SCLK, SDI)	R_{PD}	–	50	–	kΩ	–
Serial Clock Frequency	f_{SCLK}	0.06	–	6	MHz	–
Serial Clock Period (1/fSCLK)	t_{SCLK}	166	–	–	ns	–
Serial Clock High Period	t_{SCLKH}	83	–	–	ns	–
Serial Clock Low Period	t_{SCLKL}	83	–	–	ns	–
$\overline{CS}$ Hold time (rising edge of SCLK to rising edge of $\overline{CS}$)	t_{CSH}	100			ns	
Data setup time (required time SDI to rising edge of SCLK)	t_{SU}	20			ns	
Data hold time (rising edge of SCLK to SDI)	t_{HD}	20			ns	
$\overline{CS}$ falling edge to SDO output valid time	t_{CS_valid}			150	ns	
$\overline{CS}$ falling edge to first rising SCLK edge	t_{SCLK_su}	200			ns	
SCLK falling edge to SDO output valid time	t_{SCLK_valid}			80	ns	
Minimum SDO Output disable time	t_{float}			90	ns	
New serial mode activation time (MS0/MS1 change to earliest interface access)	t_{MS_rdy}		400		ns	no µController access allowed during the change[1] ($\overline{CS}$ = 1)

1) not subject to production test, specified by design

Table 25 $\overline{ODIS}$, ALE/RST Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Pull Up Resistance ($\overline{ODIS}$)	R_{PU}	–	50	–	kΩ	–
Minimum width of $\overline{ODIS}$-signal	t_{ODISW}	5	–		µs	–
Minimal Duration for triggering Reset	t_{RSTW}	100	–	–	µs	ALE/RST = V_{CC} and $\overline{CS}$ = GND

5.6 Diagnostics

Table 26 Channel Specific Diagnostics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload threshold	ITH_{OCL}	0.73	1	1.3	A	R_{IADJ} = 6.81 kΩ
Active open load threshold	ITH_{OLA1}	0.1	0.35	0.55	mA	R_{OLADJ} = 24,3 kΩ
Active open load threshold	ITH_{OLA2}	1.8	2.4	2.9	mA	R_{OLADJ} = 3.48 kΩ
Active open load threshold	ITH_{OLA3}	0.9	1.4	1.9	mA	I_{OLADJ} = 200 µA[1]
Inactive bypass current	I_{OLI}	10.0	21	32	µA	Including switch leakage
Inactive open load voltage	V_{OLI}	5.75	6.7	7.8	V	–
Inactive open load detection, On-threshold	VTH_{OLI}	5	5.4	5.75	V	–
Inactive short to V_{BB} detection, On-threshold	VTH_{SCV}	8.4	9.2	10	V	take care when V_{VBB} = V_{VBBmin} = 11 V for stability of VBB (good buffering)
Overload filtering normal mode[2]	t_{FILT_OCL}	–	0.5	–	ms	for the thermal shutdown other value 50 us
Overload filtering cold lamp mode[2]	t_{FILT_COL}	–	200	–	ms	–
Active open load blanking[2]	t_{blank_OLA}	–	6	–	ms	blanking time = filter length, other values 100us,0.5ms, 1.0ms[3]
Inactive open load blanking[2]	t_{blank_OLI}	–	6	–	ms	blanking time = filter length, values 100us,0.5ms, 1.0ms
Inactive short to V_{BB} blanking[2]	t_{blank_SCV}	–	6	–	ms	the blanking time for SCV is 6 ms but the internal filterlength is 2 ms , other values 100us, 0.5ms, 1.0ms
LEDy matrix driver on resistance	R_{ON_LEDy}	–	–	70	Ω	Load current 10 mA, VBB = 24V
LEDx matrix driver on resistance	R_{ON_LEDx}	–	–	30	Ω	Load current 30 mA,VBB=24V

1) A current of 200 µA is forced out of the OLADJ Pin, this is equivalent to an nominal R_{OLADJ} of 6 kΩ.
R_{OLADJ} = V_{OLADJ} / I_{OLADJ} = 1.2 V / 200 µA

2) all timing values defined and checked by design; test in production: structural test by SCAN-pattern plus test of internal oscillator frequency (24 MHz ± 17,5 %)

3) other values 100us, 0.5ms, 1.0ms are dynamically adapted to the switching frequency of the user

5.7 Isolation and Safety-Related Specification

Measured from input terminals to output terminals, unless otherwise specified

Table 27 Isolation and Safety-Related Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rated dielectric isolation voltage[1]	V_{ISO}	2500	---	–	VAC	1 - minute duration[2]
Short term temporary overvoltage	V_{IOTM}	4250	---	–	Vpk	1s
Minimum external air gap (clearance)		–	3.5	–	mm	Shortest distance through air
Minimum external tracking (creepage)		–	3.5	–	mm	Shortest distance path along body
Minimum Internal Gap		–	0.01	–	mm	Isolation distance through insulation

1) The dielectric withstand voltage class (Nennisolationsklasse) is : 500 V.
2) The parameter is not subject to production test, verified by characterization.

Approvals

UL508, CSA C22.2 NO. 14
Certificate Number: 20090514-E329661

5.8 Reliability

For Qualification Report please contact your local Infineon Technologies office!

5.9 Typical Performance Characteristics

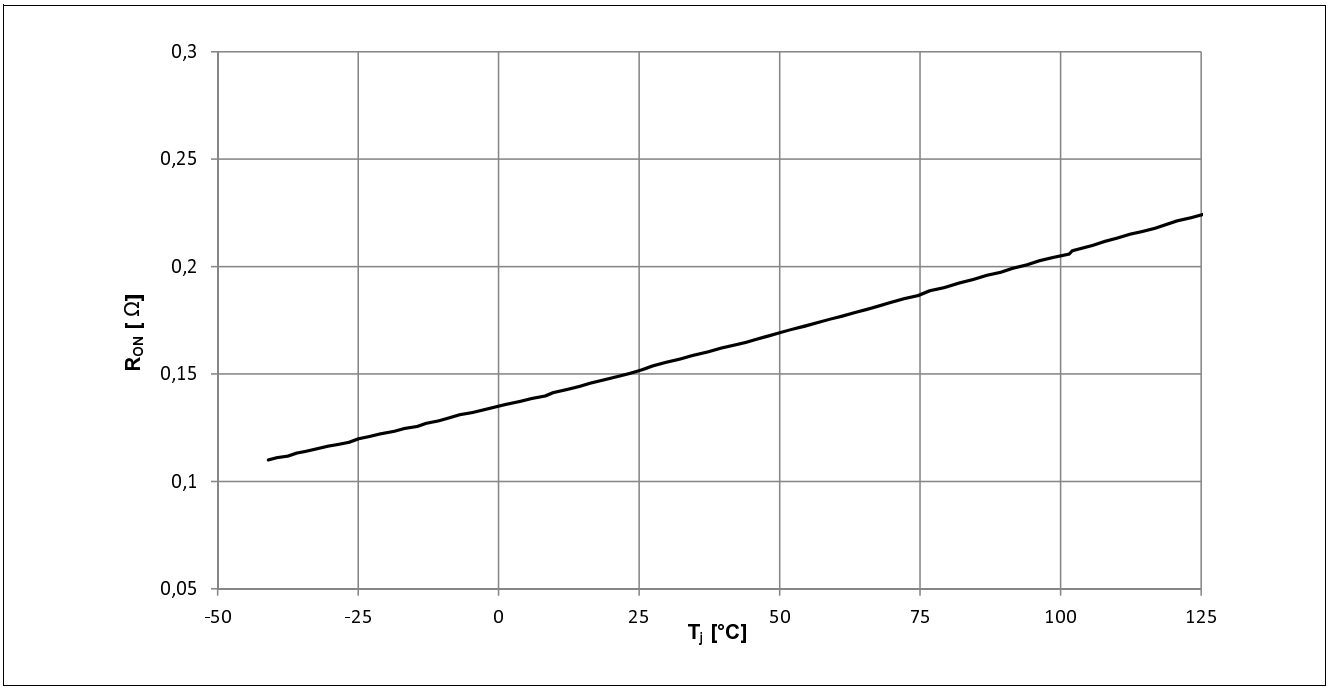


Figure 28 Typ. On-State Resistance

$R_{ON} = f(T_j)$, I_L = 0.6A, V_{BB} = 24V, V_{in} = high

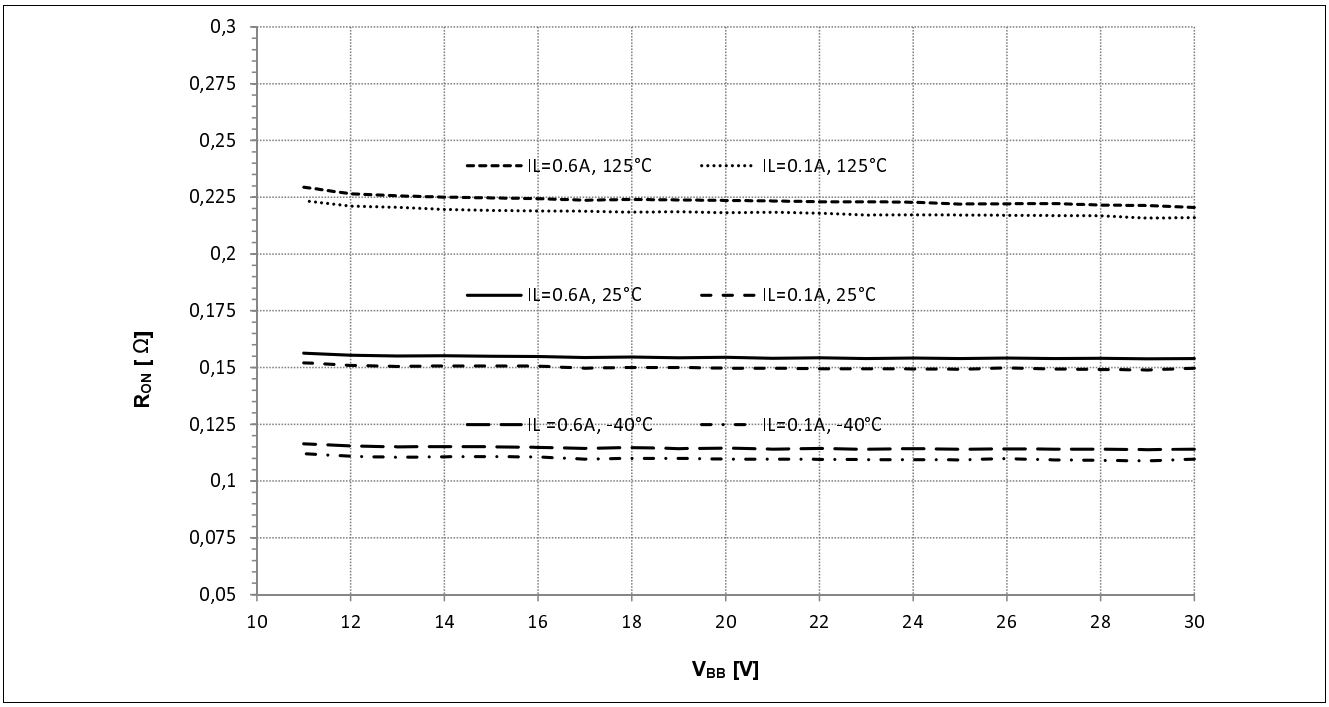


Figure 29 Typ. On-State Resistance

$R_{ON} = f(V_{BB})$, I_L = 0.6 A, I_L = 0.1 A, V_{in} = high

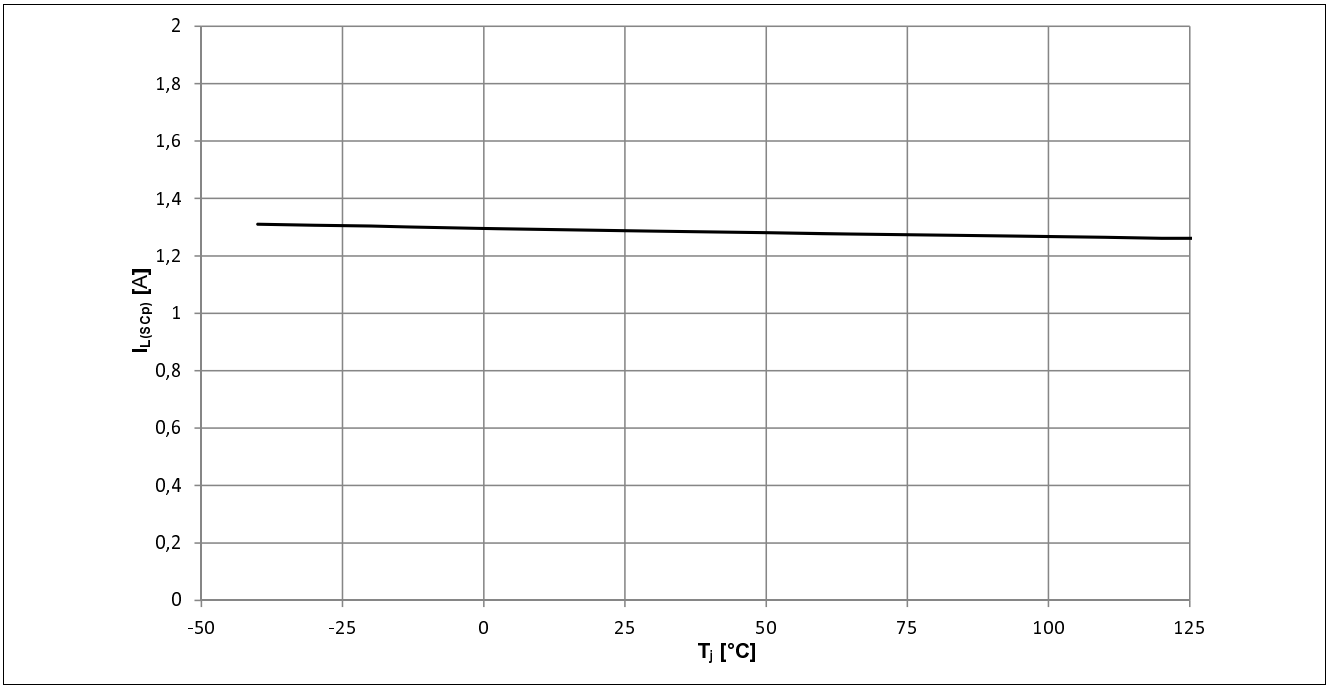


Figure 30 Typical Initial Peak Short Circuit Current Limit vs T_j

$I_{L(SCp)} = f(T_j)$, V_{BB} = 24 V, output switched on with a short circuit present at the output

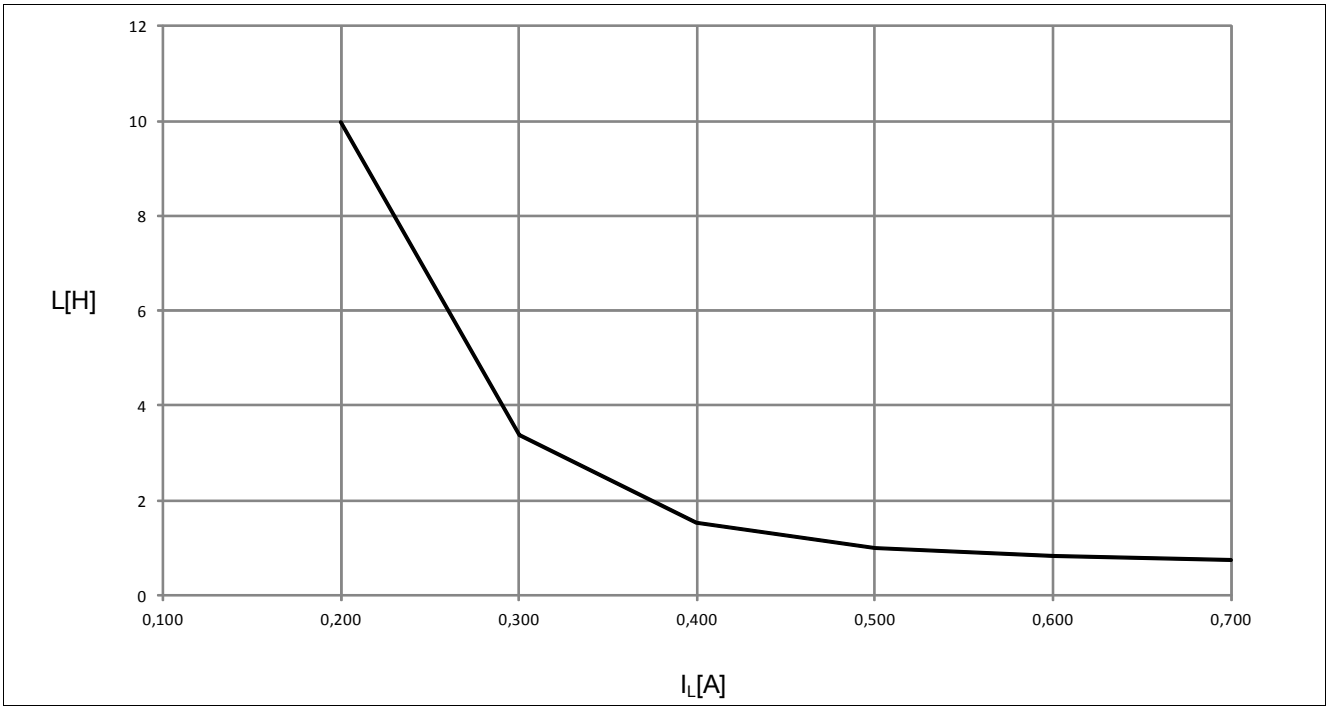


Figure 31 Maximum Allowable Load Inductance for a Single Switch Off of Each Channel, Calculated

$L = f(I_L)$, T_{jstart} = 125 °C, V_{BB} = 24 V, R_L = 48 Ω, all channels are switching simultaneously

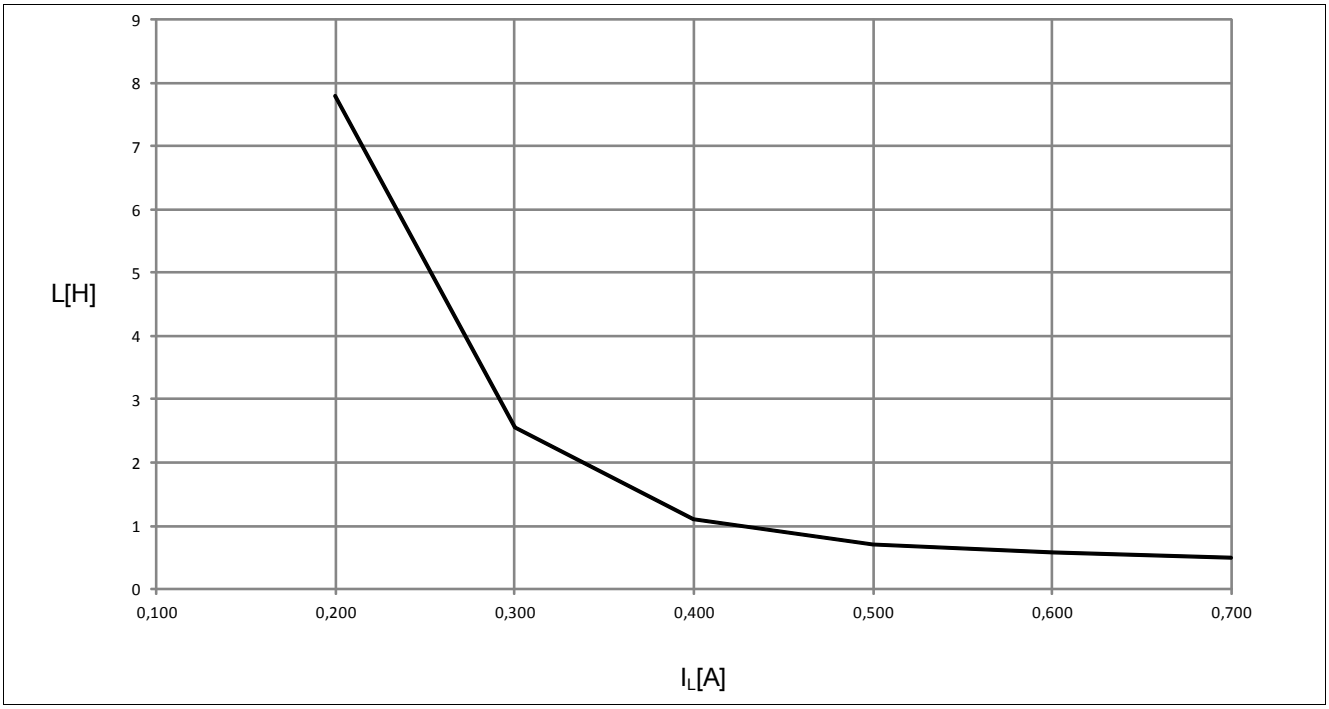


Figure 32 Maximum Allowable Load Inductance for a Single Switch Off of Each Channel, Calculated

$L = f(I_L)$, T_{jstart} = 125 °C, V_{BB} = 24 V, R_L = 0 Ω, all channels are switching simultaneously

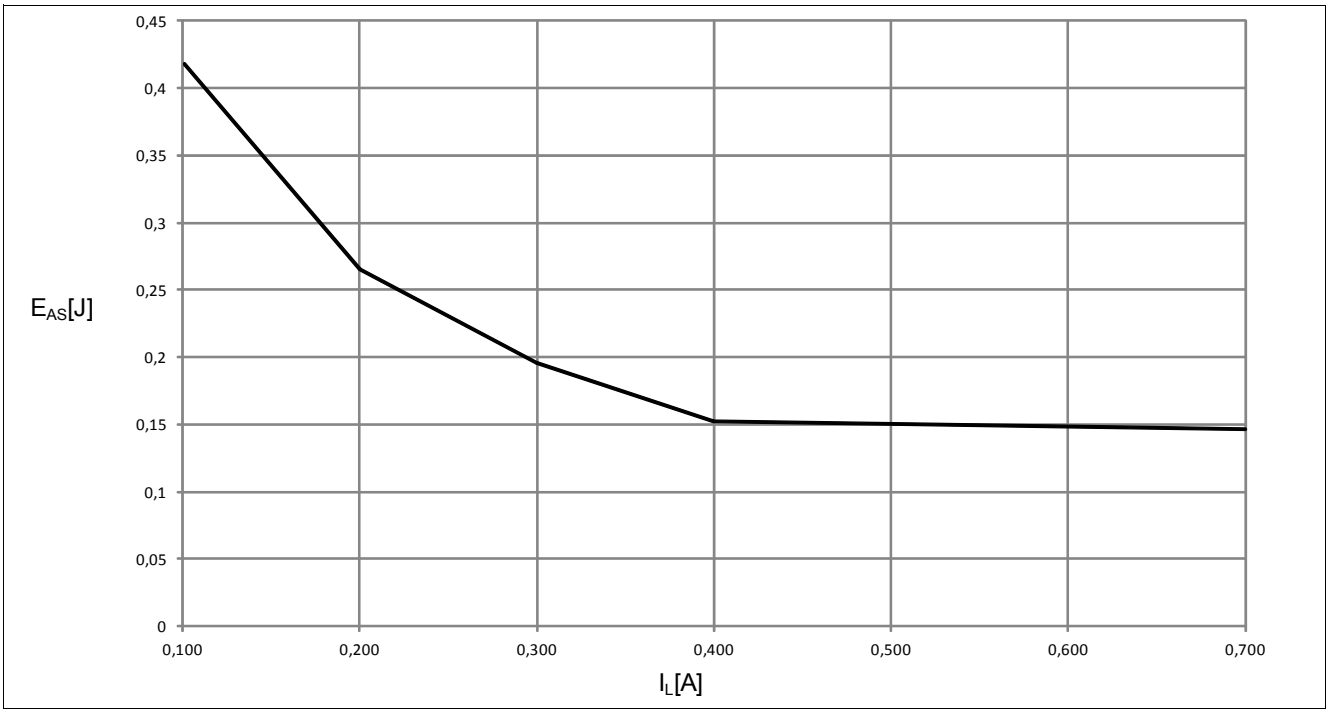


Figure 33 Maximum Allowable Inductive Switch Off Energy, Single Pulse for Each Channel

$E_{AS} = f(I_L)$, T_{jstart} = 125 °C, V_{BB} = 24 V, all channels are switching simultaneously

Single pulse means that the thermal recovery time is sufficient so that an increase of the chip temperature is avoided or at least limited (depends on the thermal connection of chip with PCB-board, **Figure 34** -**Figure 36**) .

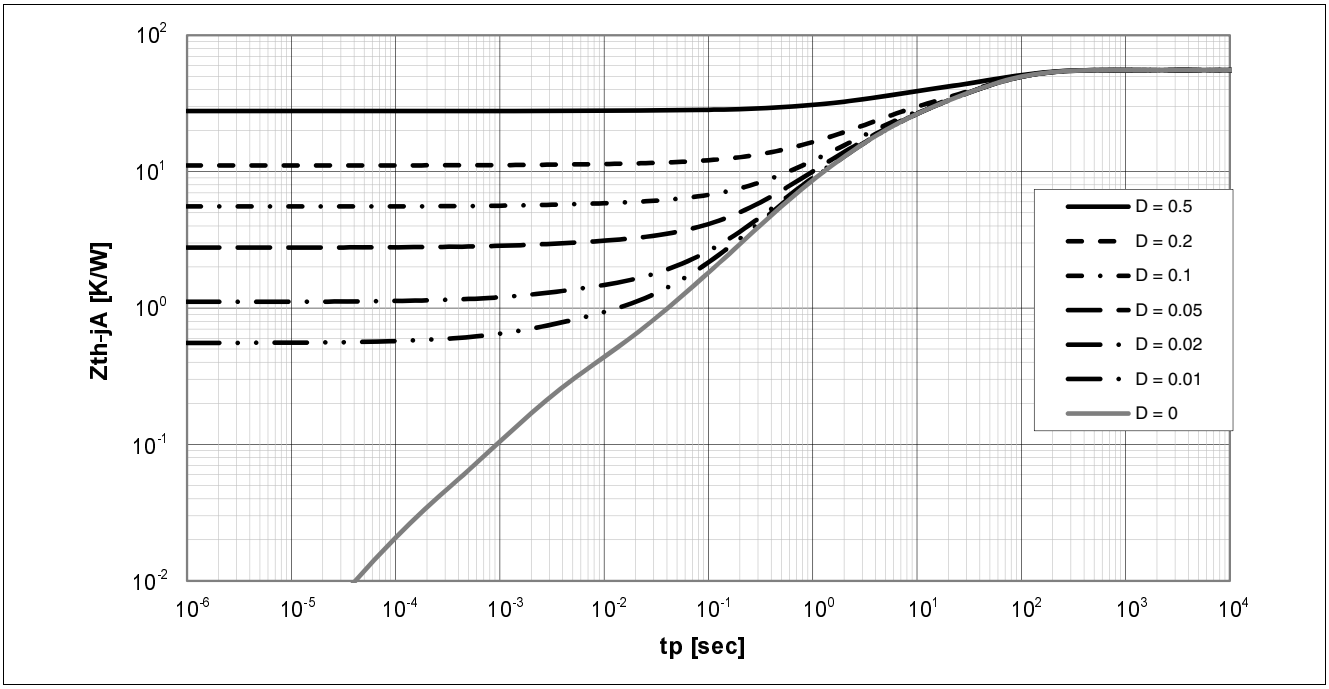


Figure 34 Typ. Transient Thermal Impedance 1s0p

$Z_{thJA} = f(t_p)$, Parameter: $D = t_p/T$

Product simulated on a 76.2 x 114.3 x 1.5 mm 1s0p board according JEDEC JESD 51-3.

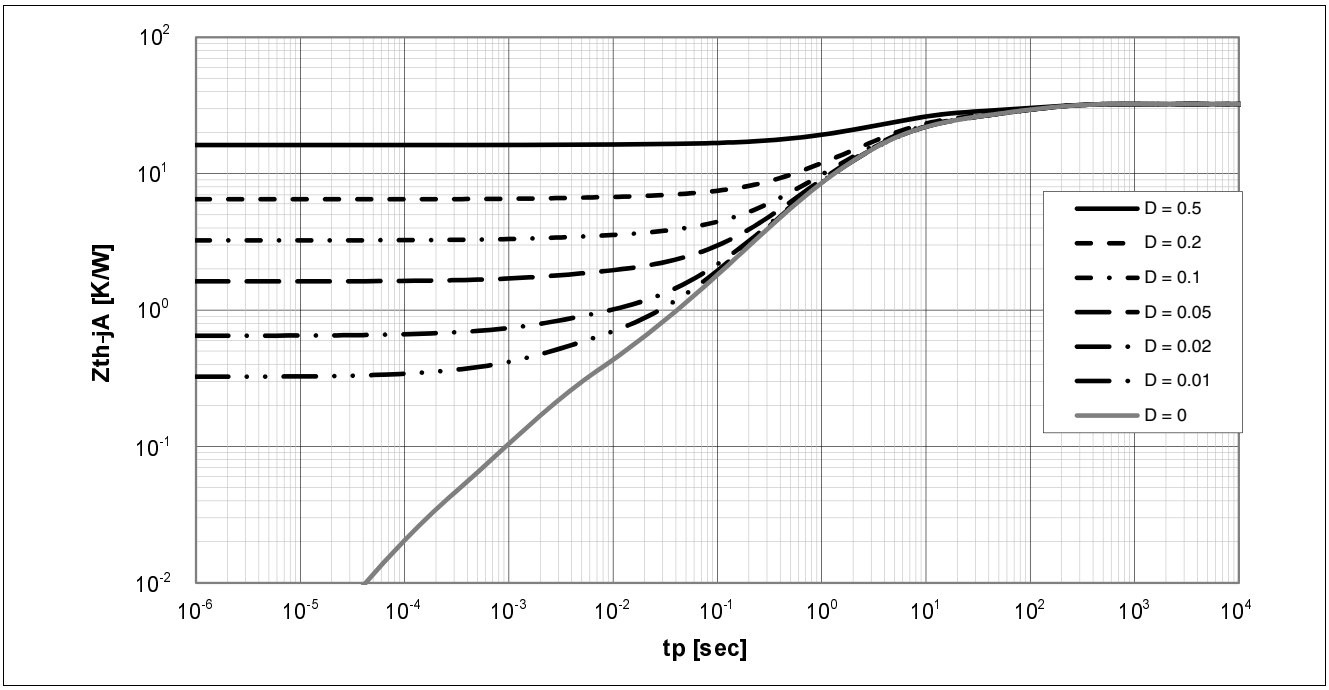


Figure 35 Typ. Transient Thermal Impedance 2s2p no vias

$Z_{thJA} = f(t_p)$, Parameter: $D = t_p/T$

Product simulated on a 76.2 x 114.3 x 1.5 mm 2s2p board without thermal vias used in the exposed pad area according JEDEC JESD 51-5,7.

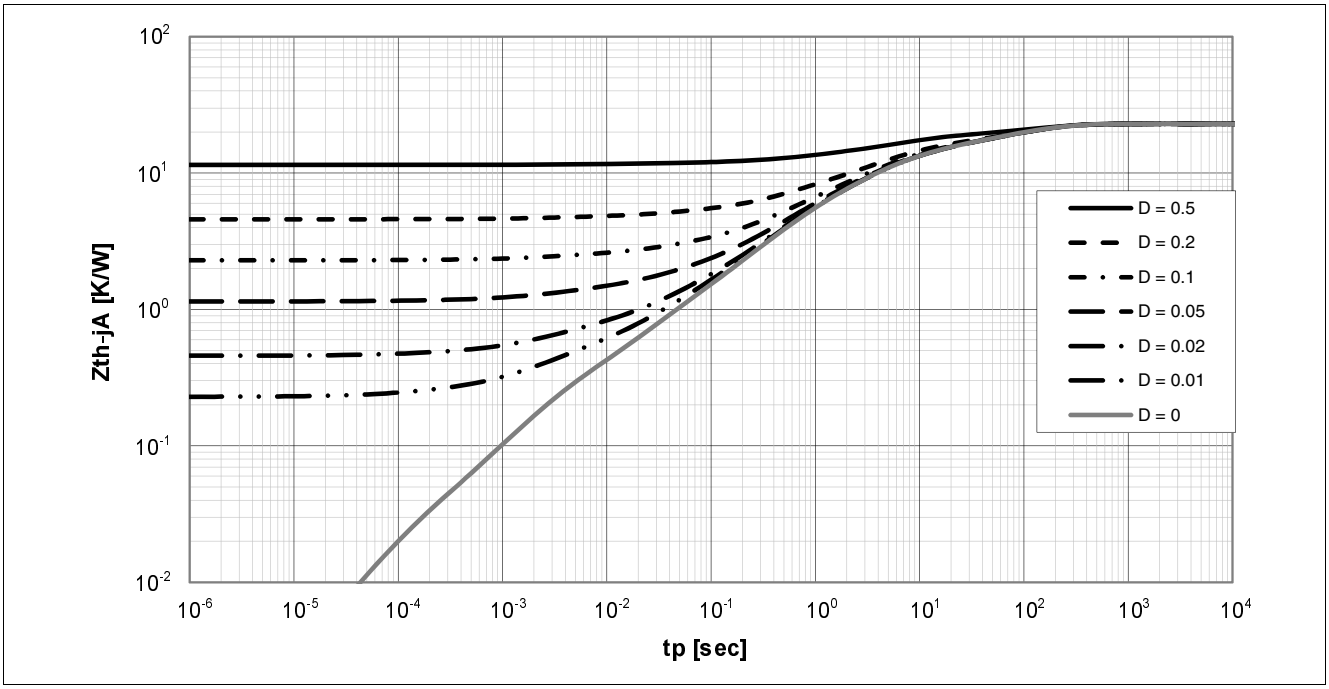


Figure 36 Typ. Transient Thermal Impedance 2s2p

$Z_{thJA} = f(t_p)$, Parameter: $D = t_p/T$

Product simulated on a 76.2 x 114.3 x 1.5 mm 2s2p board with thermal vias connected to the first inner copper layer in the exposed pad area according JEDEC JESD 51-5,7.

6 µController Interface Registers

This section presents the user registers.

Access Conventions

Table 28 Register Access Definition

Type	Symbol	Description
Read	r	The bit can be read
Read only, updated by hardware	h	The bit is updated by the device itself (for instance: sticky bit)
Write	w	The bit can be written

Presentation

The User Registers are 8-bit wide and can be accessed over either the serial or the parallel interface. The **Table 29** lists the registers of the chip. The address is 8-bit whereby the MSB is used to indicate whether it is a write access (MSB=1) or Read access (MSB=0). The address is even i.e. the LSB is ignored (for addressing). The default selected register is the **DRIVE** register for write access.

Table 29 Register Overview

Register Short Name	Register Long Name	Offset Address	Page Number
µController Interface Registers, User Registers			
DRIVE	Output Driver Register (rw)	00_H	**66**
DRIVE_RESYNCH	Output Driver Register for Resynchronization (rw)	$1C_H$	**66**
COLDIAG	Collective Diagnostics Register (rh)	02_H	**69**
GLERR	Global Error Register (rh)	04_H	**71**
DIAGCFG	Channel Diagnostics Configuration Register (rw)	06_H	**72**
DIAG0	Diagnostics Register for Channel-0 (rh)	08_H	**74**
DIAG1	Diagnostics Register for Channel-1 (rh)	$0A_H$	**75**
DIAG2	Diagnostics Register for Channel-2 (rh)	$0C_H$	**75**
DIAG3	Diagnostics Register for Channel-3 (rh)	$0E_H$	**75**
DIAG4	Diagnostics Register for Channel-4 (rh)	10_H	**75**
DIAG5	Diagnostics Register for Channel-5 (rh)	12_H	**75**
DIAG6	Diagnostics Register for Channel-6 (rh)	14_H	**75**
DIAG7	Diagnostics Register for Channel-7 (rh)	16_H	**75**
INTERR	Internal Error Register (rh)	18_H	**76**
GLCFG	Global Configuration Register (rwh)	$1A_H$	**78**

The registers are addressed wordwise.

6.1 User Registers

These registers can be accessed via the serial or parallel interface. The default selected register is the **DRIVE** register for write access.

Update of the Diagnostics Registers

The different faults monitored at each output channel are filtered with blanking time units. They are then stored in registers and sent over the Coreless Transformer to the µController-Interface chip with an update rate of 35 µs.

On the µController-Interface side, the diagnostics are stored in an intermediate register bank to be processed as sticky bits: once a fault is detected (and received) the corresponding bit is set and remains set even if the fault disappears. The bit can only be cleared once the fault is not detected anymore and a clear was requested by a serial or parallel access (see **Figure 37**).

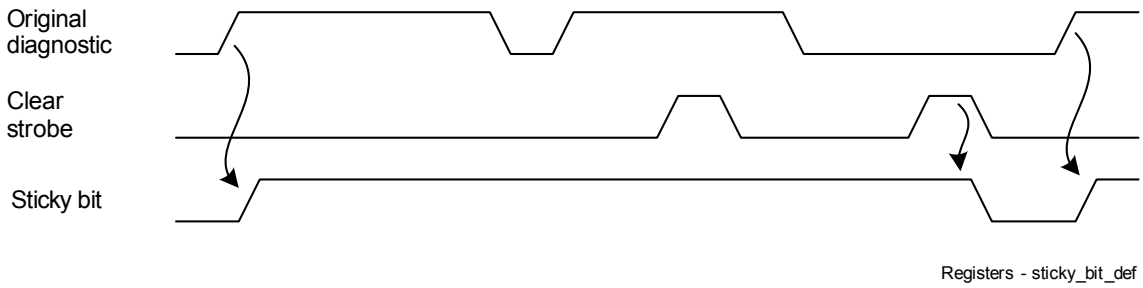


Figure 37 Sticky Bit Operation

Output Driver Register

This register contains the command for the 8 output channels. When the pin $\overline{ODIS}$ is High, the output channels are controlled as set by this register. When the $\overline{ODIS}$ is Low, the output channels are immediately turned off and the contents of the **DRIVE** register is cleared.

DRIVE	Offset	Reset Value
Output Driver Register (rw)	00_H	00_H

7	6	5	4	3	2	1	0
SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SW7	7	rw	**Output Driver Control for Channel 7** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW6	6	rw	**Output Driver Control for Channel 6** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.

Field	Bits	Type	Description
SW5	5	rw	**Output Driver Control for Channel 5** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW4	4	rw	**Output Driver Control for Channel 4** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW3	3	rw	**Output Driver Control for Channel 3** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW2	2	rw	**Output Driver Control for Channel 2** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW1	1	rw	**Output Driver Control for Channel 1** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
SW0	0	rw	**Output Driver Control for Channel 0** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.

Output Driver Register for Resynchronization

This register contains the command for the 8 output channels for resynchronization. It has to be written in case a resynchronization of the CT-transmission is desired. Then the contents of **DRIVE_RESYNCH** is used for the CT-transmission instead of the contents of **DRIVE**.

DRIVE_RESYNCH	Offset	Reset Value
Output Driver Register (rw)	$1C_H$	00_H

7	6	5	4	3	2	1	0
RW7	RW6	RW5	RW4	RW3	RW2	RW1	RW0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RW7	7	rw	**Output Driver Resynchronization Control for Channel 7** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.

Field	Bits	Type	Description
RW6	6	rw	**Output Driver Resynchronization Control for Channel 6** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW5	5	rw	**Output Driver Resynchronization Control for Channel 5** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW4	4	rw	**Output Driver Resynchronization Control for Channel 4** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW3	3	rw	**Output Driver Resynchronization Control for Channel 3** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW2	2	rw	**Output Driver Resynchronization Control for Channel 2** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW1	1	rw	**Output Driver Resynchronization Control for Channel 1** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.
RW0	0	rw	**Output Driver Resynchronization Control for Channel 0** This bit field controls the state of the output driver. 0_B The channel output is inactive. 1_B The channel output is driven.

Collective Diagnostics Register

This register contains the overall diagnostics for each of the 8 output channels. Each channel-bit corresponds to the OR-combination of the **SCVx**, **OCLx**, **OLIx**, **OLAx** and **OTx**-bits of the enabled diagnostic function. This register contains the state of the channel diagnostics. On read access the internal diagnostics data is cleared and the **DIAG0**,...,**DIAG7** registers are updated (see **Update of the Diagnostics Registers**). In serial modes 0 and 1 the update of the **DIAG0**,...,**DIAG7** is generated automatically after every access whereas in serial modes 2 and 3 as well as in parallel mode the **DIAG0**,...,**DIAG7** registers are updated after each direct access to the **COLDIAG** register.

COLDIAG	Offset	Reset Value
Collective Diagnostics Register (rh)	02_H	00_H

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CH7	7	rh	**Overall Diagnostics for Channel 7** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH6	6	rh	**Overall Diagnostics for Channel 6** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH5	5	rh	**Overall Diagnostics for Channel 5** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH4	4	rh	**Overall Diagnostics for Channel 4** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH3	3	rh	**Overall Diagnostics for Channel 3** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH2	2	rh	**Overall Diagnostics for Channel 2** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.
CH1	1	rh	**Overall Diagnostics for Channel 1** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.

Field	Bits	Type	Description
CH0	0	rh	**Overall Diagnostics for Channel 0** This bit field indicates the overall diagnostics. 0_B No fault is detected. 1_B At least one failure is detected.

Global Error Register

This register contains the overall status of the IC parameters monitored during system operation. The bits are routed to the $\overline{ERR}$ pin as well (see Table 3). The **UV** and **MV** bits are reset to High during UVLO. In some operation modes, the register needs to be read to clear these bits and release the $\overline{ERR}$ pin (see “Update of GLERR, INTERR-Reg”). The **CF**-bit is the OR-combination of **COLDIAG** bits.

GLERR	**Offset**	**Reset Value**
Global Error Register (rh)	**04_H**	**16_H**

7	6	5	4	3	2	1	0
Vers_3	**Vers_2**	**Vers_1**	**Vers_0**	**RES**	**UV**	**MV**	**CF**
r	r	r	r	r	rh	rh	rh

Field	Bits	Type	Description
Vers_3	7	r	**Actual :”0”**
Vers_2	6	r	**Actual :”1”**
Vers_1	5	r	**Actual :”0”**
Vers_0	4	r	**Actual :”0”**
RES	3	r	**Reserved** Returns 0 when read.
UV	2	rh	**VBB Undervoltage** This bit field indicates if an undervoltage condition has been detected at VBB. 0_B No undervoltage detected. 1_B Undervoltage detected.
MV	1	rh	**VBB Missingvoltage** This bit field indicates if a missingvoltage condition has been detected at VBB. 0_B No missingvoltage detected. 1_B Missingvoltage detected.
CF	0	rh	**Common Diagnostics Fault** This bit field is the OR-combination of all bits of the COLDIAG register. 0_B No fault is detected. 1_B At least one failure is detected.

Channel Diagnostics Configuration Register

This register enables the diagnostics for each channel and selects whether the channel collective diagnostic bit is updated in the **COLDIAG** register (and as a consequence in the **CF**-bit field of the **GLERR** register and at the $\overline{\text{ERR}}$ pin).

DIAGCFG	Offset	Reset Value
Channel Diagnostics Configuration Register (rw)	06_H	FF_H

7	6	5	4	3	2	1	0
DIAGEN7	DIAGEN6	DIAGEN5	DIAGEN4	DIAGEN3	DIAGEN2	DIAGEN1	DIAGEN0
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DIAGEN7	7	rw	**Enables Diagnostics for Channel 7** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN6	6	rw	**Enables Diagnostics for Channel 6** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN5	5	rw	**Enables Diagnostics for Channel 5** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN4	4	rw	**Enables Diagnostics for Channel 4** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN3	3	rw	**Enables Diagnostics for Channel 3** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN2	2	rw	**Enables Diagnostics for Channel 2** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.
DIAGEN1	1	rw	**Enables Diagnostics for Channel 1** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.

Field	Bits	Type	Description
DIAGEN0	0	rw	**Enables Diagnostics for Channel 0** This bit field enables all the channel diagnostics. 0_B All the channel diagnostics are disabled. 1_B The channel diagnostics are enabled and updated in the **COLDIAG** register.

Diagnostics Registers for Channel-x

These registers contain the individual diagnostics bits. The bit field **LEDGx** is not used in the **COLDIAG** register (and as a consequence in the **CF**-bit and at the ERR pin). All bits are sticky (see **Update of the Diagnostics Registers**). The diagnostics are enabled with the **DIAGCFG** register.

DIAG0	Offset	Reset Value
Diagnostics Register for Channel-0 (rh)	08_H	00_H

7	6	5	4	3	2	1	0
RES	RES	LEDGx	SCVx	OCLx	OLAx	OLIx	OTx
r	r	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
RES	7	r	**Reserved** returns 0 if read.
RES	6	r	**Reserved** returns 0 if read.
LEDGx	5	rh	**Gated LED Drive Information of Channel x (Active Mode only)** This bit field indicates that the led of this channel is gated due to overcurrent or over-temperature conditions. 0 : led not gated 1 : led gated
SCVx	4	rh	**Short Circuit to VBB at Channel x (Inactive Mode only)** This bit field indicates that a short circuit to VBB has been detected. 0_B No short circuit to VBB detected. 1_B A short circuit to VBB has been detected.
OCLx	3	rh	**Overcurrent at Channel x (Active Mode only)** This bit field indicates that an overload condition has been detected and that the current is being limited. 0_B No overcurrent detected. 1_B An overcurrent has been detected and limited.
OLAx	2	rh	**Open Load / Wire Break at Channel x (Active Mode)** This bit field indicates that an open load condition has been detected. 0_B No open load detected. 1_B An open load condition has been detected.
OLIx	1	rh	**Open Load / Wire Break at Channel x (Inactive Mode)** This bit field indicates that an open load condition has been detected. 0_B No open load detected. 1_B An open load condition has been detected.
OTx	0	rh	**Over-temperature at Channel x (Active Mode Only)** This bit field indicates that an over-temperature condition has been detected. 0_B No over-temperature detected. 1_B An over-temperature has been detected.

Other Channel Diagnostics Registers

The other channel diagnostics registers in the table below have the same layout as **DIAG0**.
Their names and offset addresses are listed below:

Table 30 Diagnostics Registers for Channel 1-7

Register Short Name	Register Long Name	Offset Address	Reset Value
DIAG1	Diagnostics Register for Channel-1 (rh)	$0A_H$	00_H
DIAG2	Diagnostics Register for Channel-2 (rh)	$0C_H$	00_H
DIAG3	Diagnostics Register for Channel-3 (rh)	$0E_H$	00_H
DIAG4	Diagnostics Register for Channel-4 (rh)	10_H	00_H
DIAG5	Diagnostics Register for Channel-5 (rh)	12_H	00_H
DIAG6	Diagnostics Register for Channel-6 (rh)	14_H	00_H
DIAG7	Diagnostics Register for Channel-7 (rh)	16_H	00_H

Internal Error Register

This register contains the status of internal errors monitored for safe IC operation. The **TE**, **W4P**, **ALLOFF** bits are sticky and routed out to the $\overline{\text{ERR}}$ pin (according to the Table 3). The bits **OTP** and **LAMP** are volatile i.e. are updated every 35 µs. Sticky bits are cleared every time the **INTERR** register is accessed or by every serial access in mode 0 and 1.

INTERR	Offset	Reset Value
Internal Error Register (rh)	18_H	07_H

7	6	5	4	3	2	1	0
RES	OTC	RES	OTP	LAMP	ALLOFF	W4P	TE
r	rh	r	rh	rh	rh	rh	rh

Field	Bits	Type	Description
RES	7	r	**Reserved** returns 0 if read.
OTC	6	rh	**Overtemperature Common (Volatile)** This bit field indicates that an overtemperature or overcurrent condition of at least one of the channels has been detected. Ored **LEDGx**-values. 0_B No overtemperature or overcurrent has been detected. 1_B An overtemperature or overcurrent condition has been detected.
RES	5	r	**Reserved** returns 0 if read.
OTP	4	rh	**Overtemperature Package (Volatile)** This bit field indicates that an overtemperature of the package has been detected. 0_B No package overtemperature detected. 1_B An overtemperature in the package has been detected.
LAMP	3	rh	**Cold Lamp Detected (Volatile)** This bit field indicates that at least a cold lamp behaviour has been detected at one output channel. 0_B No cold lamp behaviour detected. 1_B At least one load at the output channels behaves as a cold lamp.
ALLOFF	2	rh	**All Outputs Channels are Switched Off (Sticky)** This bit field indicates that all the output channels have been switched off due to an internal error, an over-temperature, the ODIS pin or the data of the **DRIVE** (feedback from Power Chip). 0_B The ouput channels are enabled and controlled by the **DRIVE** register. 1_B The ouptut channels are switched off.
W4P	1	rh	**Wait for Power Chip (Sticky)** This bit field indicates that the Power Chip is correctly supplied and ready for operation. 0_B Power Chip is ready. 1_B Power Chip is not ready because of insufficient voltage or long transmission error.

Field	Bits	Type	Description
TE	0	rh	**Transmission Error (Sticky)** This bit field indicates a transmission error over the galvanic isolation detected either from the Process Side or from the µController-Interface 0_B No transmission error is detected. 1_B Transmission error has occured.

Global Configuration Register

This register configures some extended functionalities of the chip.

GLCFG	Offset	Reset Value
Global Configuration Register (rwh)	$1A_H$	00_H

7	6	5	4	3	2	1	0
FRZSC	RESYN	RSTOFF	LEDON	RES	LEDGOFF	OLOFF	SWRST
rw	rw	rw	rw	rw	rw	rw	rwh

Field	Bits	Type	Description
FRZSC	7	rw	**Selection of Isochronous Mode for Diagnostics** This bit field enables the isochronous mode for diagnostics. The entry is totally ignored when RESYN = 1. 0_B Diagnostics are treated independently of SYNC-level 1_B Diagnostics are frozen with falling edge of SYNC and released with rising edge. During SYNC = 0 **DIAG0**,..,**DIAG7** and **COLDIAG** are not updated. But read bits in **COLDIAG** can be reset.
RESYN	6	rw	**Resynchronization of CT-Transmission** This bit field enables the resychronization of CT-transmission. 0_B functionality of SYNC is as defined by bit FRZSC. 1_B SYNC-pin is used for resynchronization of CT-transmission *Note: It is not possible to select RESYN = 1 and to use isochronous mode for drive signals or/and diagnostics at the same time. That means resynchronization and isochronous mode of driver information and diagnostics at the same time is not possible. Edges on SYNC are used solely for resynchronization. In the following the driver information can be only transferred when SYNC = 1 when RESYN is set to "1". A negative pulse on SYNC initializes the resynchronization.*
RSTOFF	5	rw	**HW Reset of ALE Pin Disabled** This bit field disables the external reset. 0_B The HW reset at the ALE pin is enabled (default). 1_B The HW reset is disabled.
LEDON	4	rw	**LED Matrix Enabled** This bit field enables the LED Matrix in serial mode. In this case the HW reset cannot be used (activation of HW Reset is ignored). 0_B The LED matrix is disabled (default). 1_B The LED matrix is enabled in serial mode.
RES	3	rw	**Reserved** **Must be set to "0"**
LEDGOFF	2	rw	**LEDG Report Disabled** This bit field disables the report of the **LEDGx**-information. 0_B The **LEDGx** diagnostic is enabled (default). 1_B The **LEDGx** diagnostic is disabled and not reported in the **DIAG0**,..,**DIAG7** registers.

Field	Bits	Type	Description
OLOFF	1	rw	**Open-Load Diagnostic Disabled** This bit field disables the monitoring of the Open-Load diagnostic **OLAx** and **OLIx**. 0_B The Open-Load diagnostic is enabled and updated in the **DIAG0**,..,**DIAG7** registers (default). 1_B The Open-Load diagnostic is disabled and do not appear in the **DIAG0**,..,**DIAG7** registers.
SWRST	0	rwh	**Soft Reset** This bit field triggers the clear of the user registers and restarts the CT transmission. After setting the soft reset, this bit field will clear itself. 0_B No reset is generated. 1_B A clear of the user registers is generated.

7 Package : Outlines and Marking Pattern

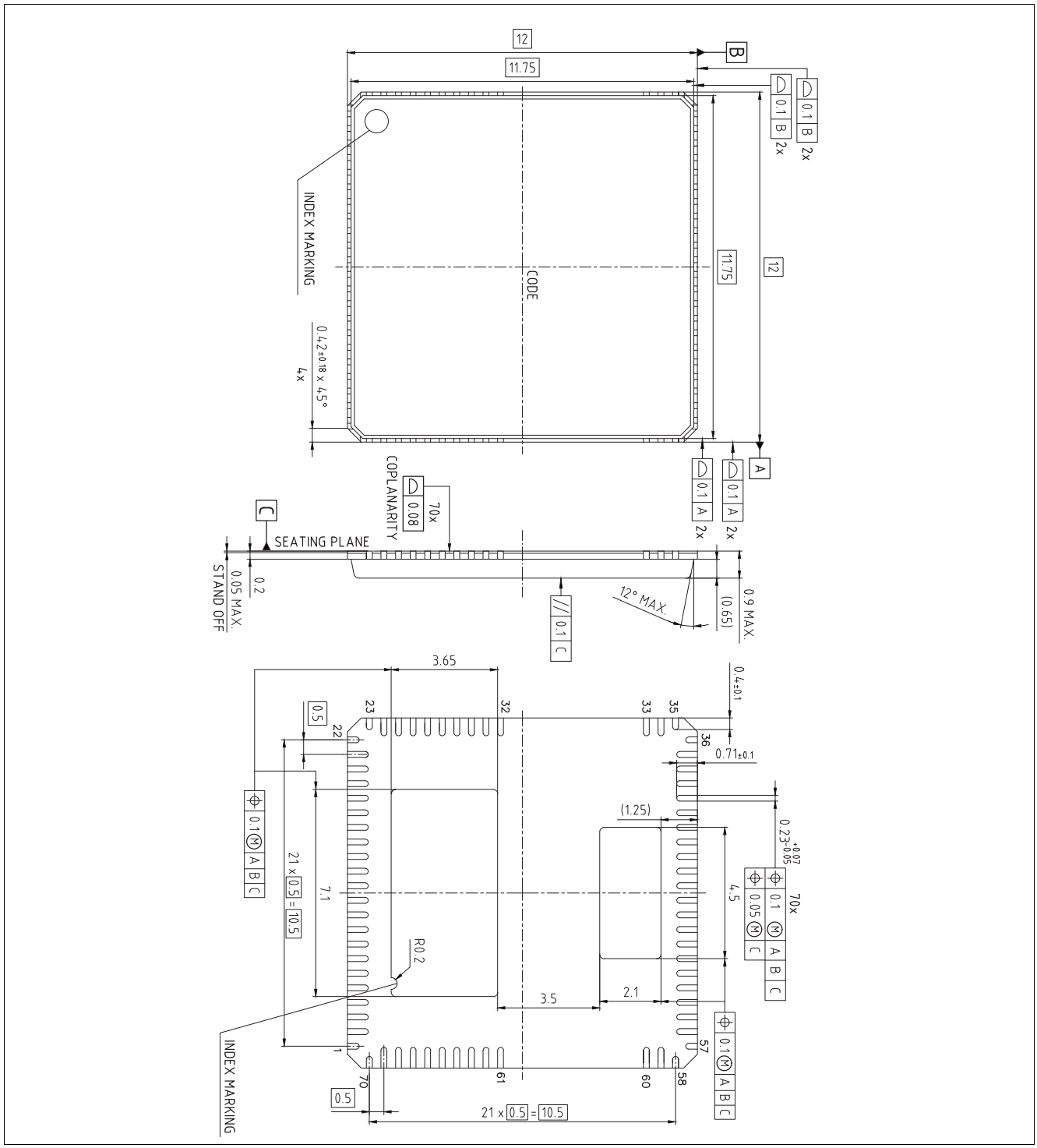


Figure 38 **PG-VQFN-70-2** (Plastic (Green) Very Thin Profile Quad Flat Non Leaded Package)

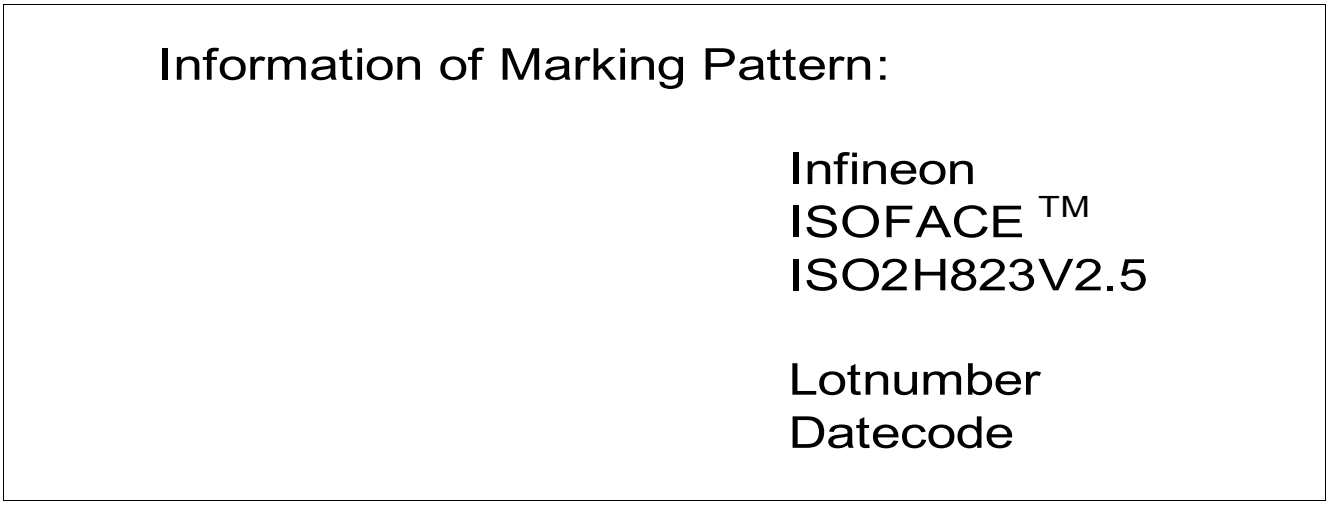


Figure 39 Marking Pattern

For further information on alternative packages, please visit our website:
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Dimensions in mm

w w w . i n f i n e o n . c o m

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