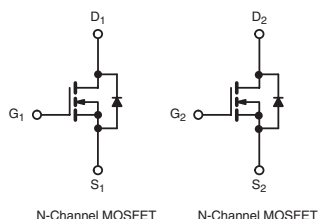
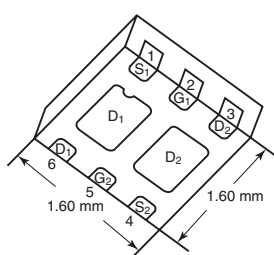


Dual N-Channel 20 V (D-S) MOSFET

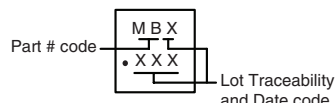
PRODUCT SUMMARY

V_{DS} (V)	20
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.216
$R_{DS(on)}$ (Ω) at $V_{GS} = 2.5$ V	0.268
$R_{DS(on)}$ (Ω) at $V_{GS} = 1.8$ V	0.375
I_D (A) ^a	1.5
Configuration	Dual

PowerPAK SC75-6L-Dual



Marking Code



FEATURES

- High Quality Manufacturing Process Using SMM Process Flow
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package
 - Small Footprint Area
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC
- Find out more about Vishay's Medical Products at: www.vishay.com/medical-mosfets



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATION EXAMPLES

- Medical Implantable Applications Including
 - Drug Delivery Systems
 - Defibrillators
 - Pacemakers
 - Hearing Aids
 - Other Implantable Devices
- Load Switch, PA Switch and Battery Switch for Portable Devices
- DC/DC Converter

ORDERING INFORMATION

Package	PowerPAK SC-75
Lead (Pb)-free and Halogen-free	SMMB912DK-T1-GE3

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C ^a	A
		$T_C = 70$ °C ^a	
		$T_A = 25$ °C ^{b, c}	
		$T_A = 70$ °C ^{b, c}	
Pulsed Drain Current	I_{DM}	5	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C ^a	
		$T_A = 25$ °C ^{b, c}	0.9
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C ^{b, c}	
		$T_A = 70$ °C ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	90	115	°C/W
Junction-to-Case (Drain)	Steady State	R_{thJC}	32	40	

Notes

- a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. $t = 5$ s.
d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 125 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		20	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		-	22	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-	- 2	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		0.4	-	1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 4.5\text{ V}$	$V_{DS} \geq 5\text{ V}$	5	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}$	$I_D = 1.8\text{ A}$	-	0.180	0.216	Ω
		$V_{GS} = 2.5\text{ V}$	$I_D = 1.6\text{ A}$	-	0.223	0.268	
		$V_{GS} = 1.8\text{ V}$	$I_D = 0.3\text{ A}$	-	0.300	0.375	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 1.8\text{ A}$		-	3	-	S
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}$, $f = 1\text{ MHz}$	-	95	-	pF
Output Capacitance	C_{oss}			-	24	-	
Reverse Transfer Capacitance	C_{rss}			-	11	-	
Total Gate Charge	Q_g	$V_{GS} = 8\text{ V}$	$V_{DS} = 10\text{ V}$, $I_D = 1.8\text{ A}$	-	2	3	nC
Gate-Source Charge	Q_{gs}	$V_{GS} = 4.5\text{ V}$	$V_{DS} = 10\text{ V}$, $I_D = 1.8\text{ A}$	-	1.2	1.8	
Gate-Drain Charge	Q_{gd}			-	0.3	-	
Gate Resistance	R_g			-	0.15	-	
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$		0.5	2.5	5	Ω
Rise Time	t_r			-	2.5	5	
Turn-Off Delay Time	$t_{d(off)}$	$V_{DD} = 10\text{ V}$, $R_L = 7.1\text{ }\Omega$ $I_D \cong 1.4\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		-	5	10	ns
Fall Time	t_f			-	10	20	
Turn-On Delay Time	$t_{d(on)}$			-	24	36	
Rise Time	t_r	-	8	16			
Turn-Off Delay Time	$t_{d(off)}$	$V_{DD} = 10\text{ V}$, $R_L = 7.1\text{ }\Omega$ $I_D \cong 1.4\text{ A}$, $V_{GEN} = 8\text{ V}$, $R_g = 1\text{ }\Omega$		-	2	4	
Fall Time	t_f			-	9	18	
Turn-On Delay Time	$t_{d(on)}$			-	8	16	
Rise Time	t_r			-	7	14	
Source-Drain Body Diode Characteristics							
Continuous Source-Drain Diode Current ^c	I_S	$T_C = 25\text{ }^\circ\text{C}$		-	-	1.5	A
Pulse Diode Forward Current	I_{SM}			-	-	5	
Body Diode Voltage	V_{SD}	$I_S = 1.4\text{ A}$, $V_{GS} = 0\text{ V}$		-	0.7	1.2	V

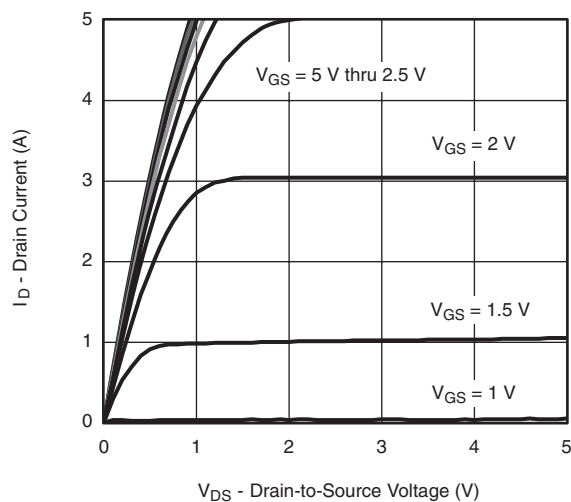
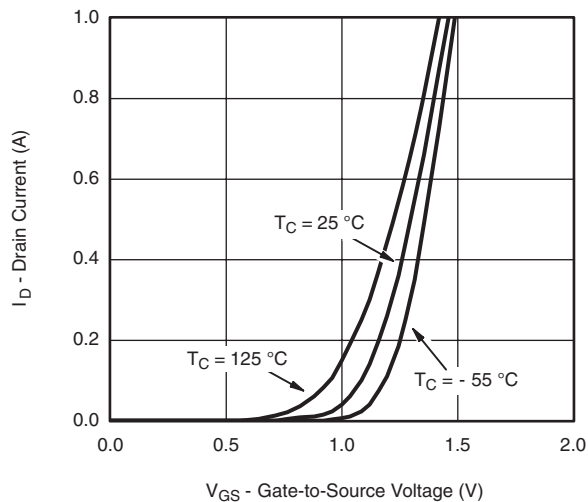
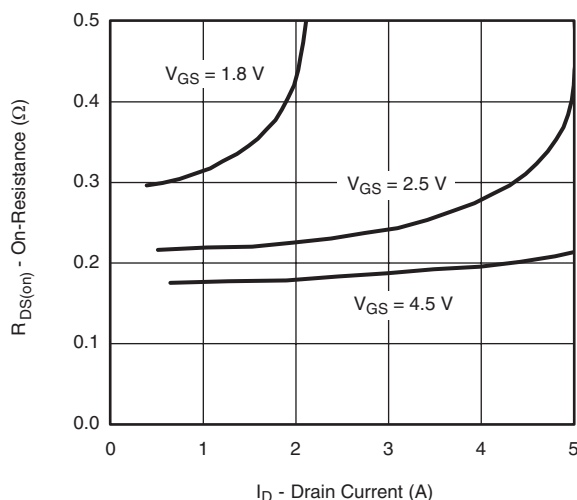
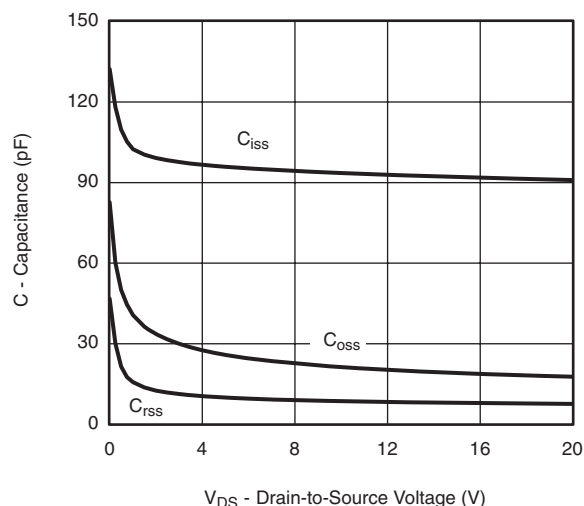
**SPECIFICATIONS** $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

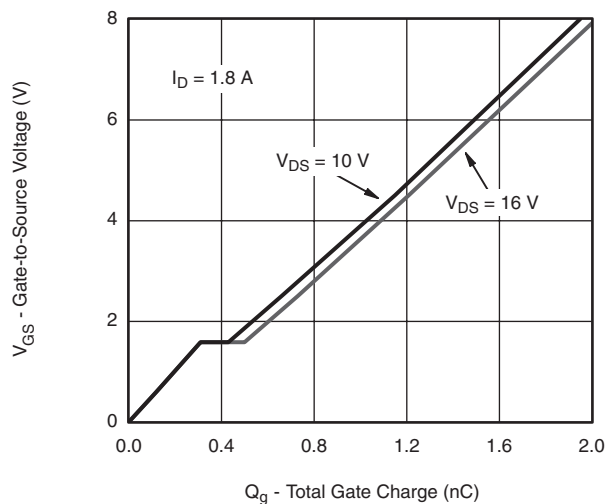
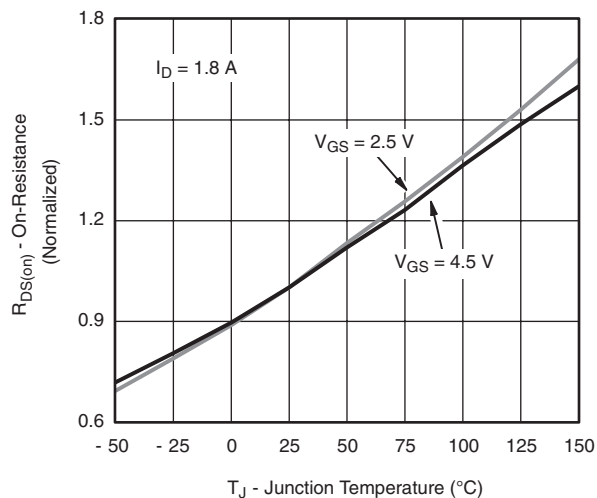
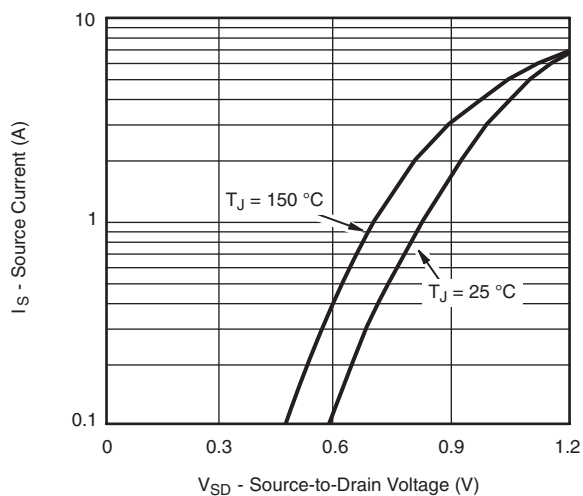
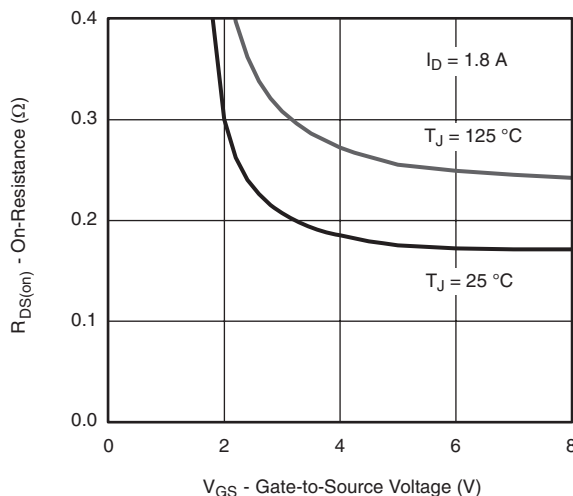
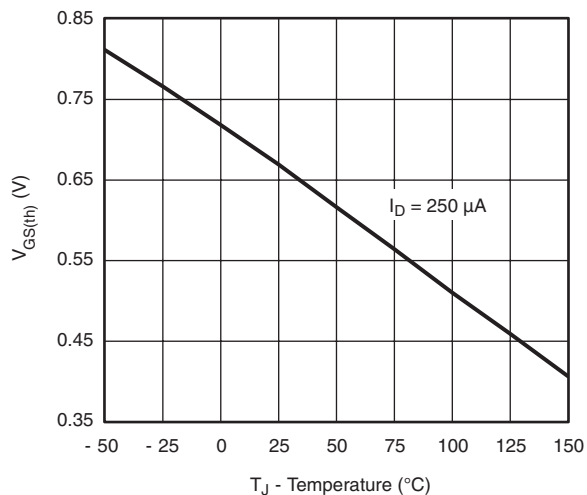
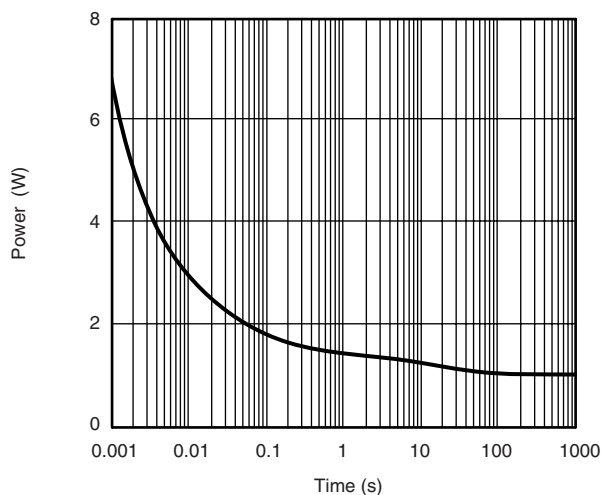
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source-Drain Body Diode Characteristics						
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 1.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	9	18	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3	6	nC
Reverse Recovery Fall Time	t_a		-	6	-	ns
Reverse Recovery Rise Time	t_b		-	3	-	

Notes

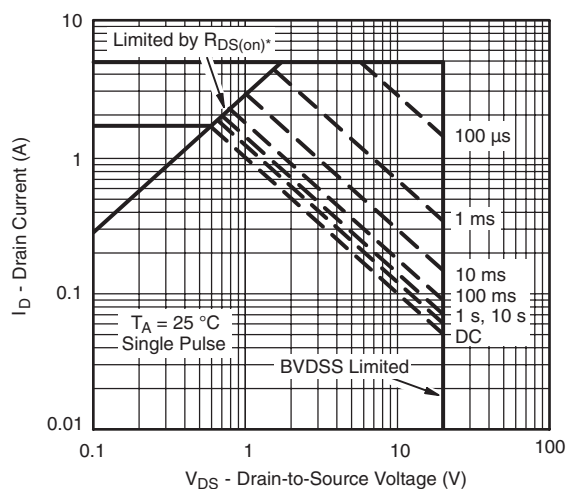
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Package limited.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance**

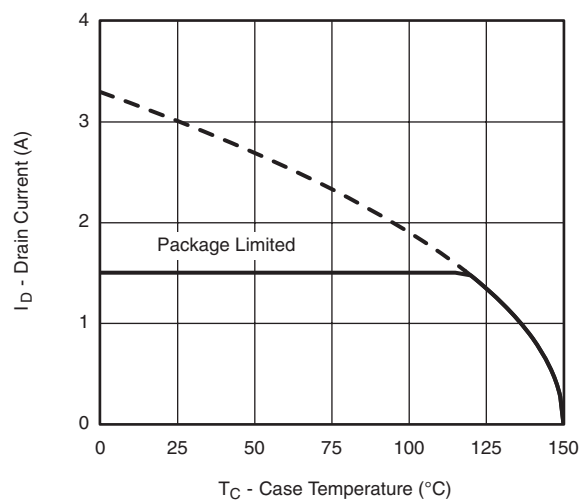
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted**Gate Charge****On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

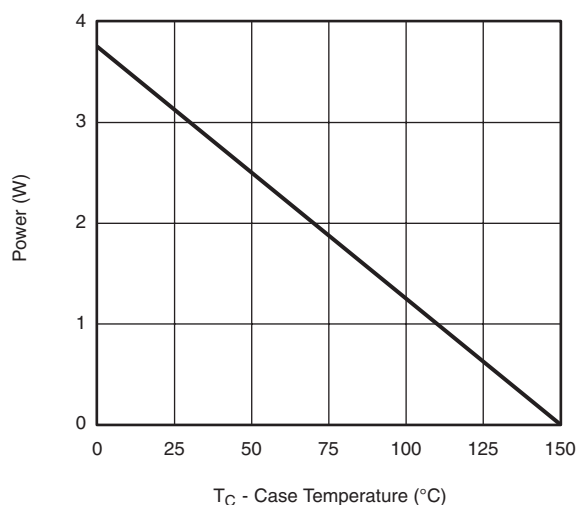


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

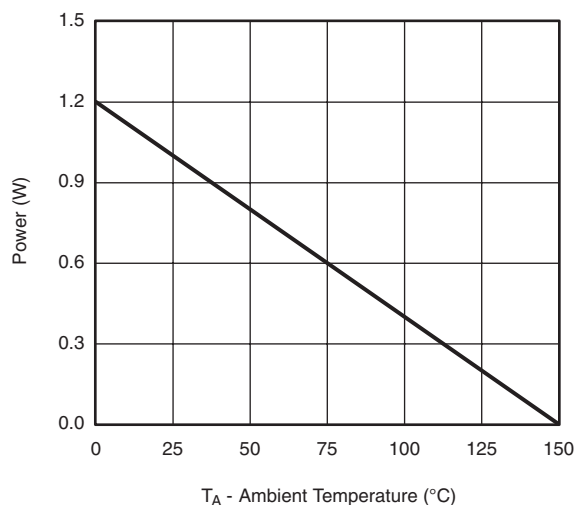
Safe Operating Area, Junction-to-Ambient



Current Derating*

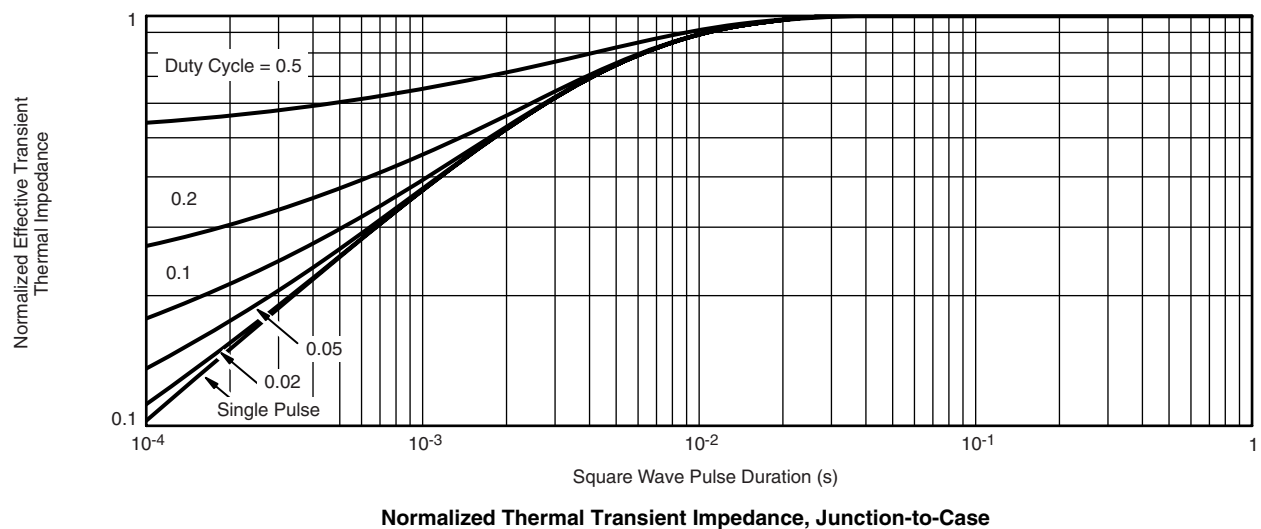
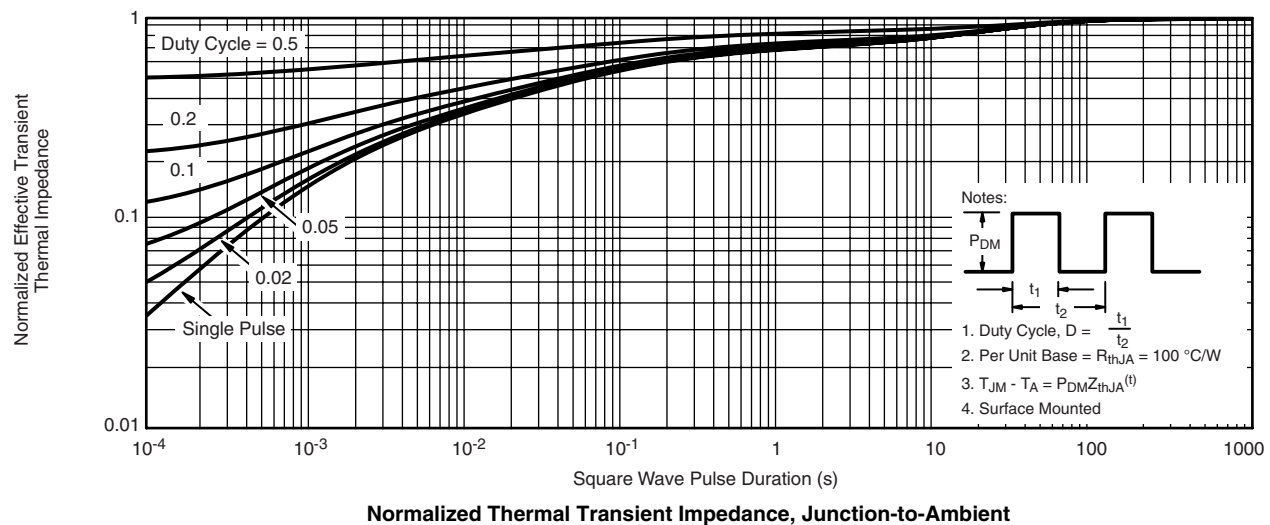


Power Derating, Junction-to-Case



Power Derating, Junction-to-Ambient

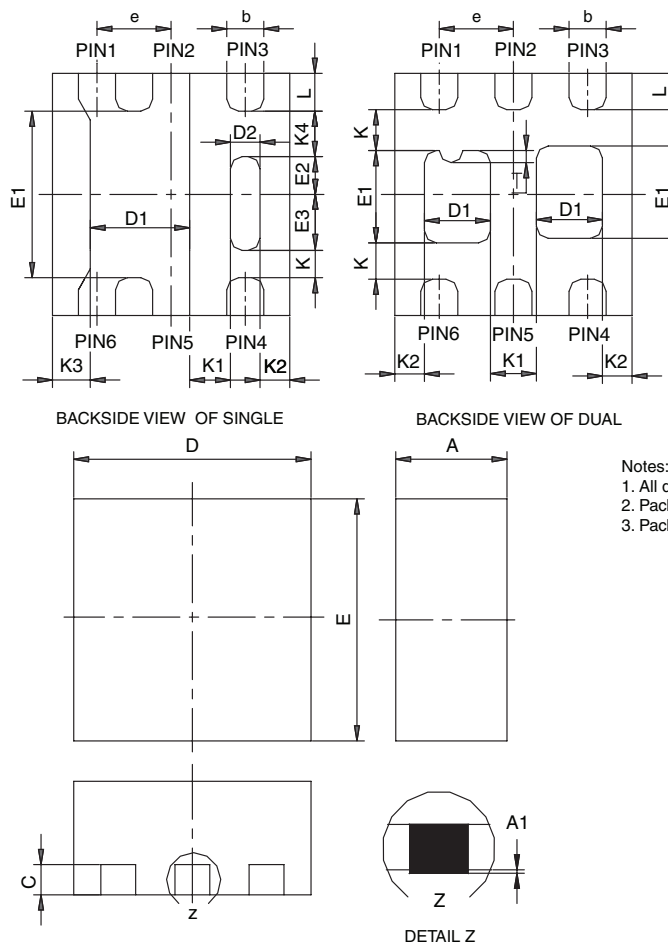
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65459.



PowerPAK® SC75-6L



- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5935

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.