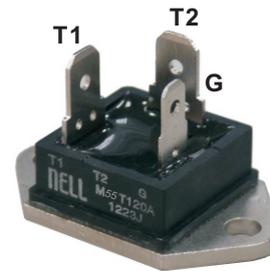


## TRIACs, 55A Sunbberless

### FEATURES

- High current triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated TO-3 package
- High commutation capability
- Packages are RoHS compliant



### APPLICATIONS

Due to their clip assembly technique, they provide a superior performance in surge current handling capabilities.

By using an internal ceramic pad, the M55T series provides voltage insulated tab (rated at 2500VRMS) complying with UL standards.

The snubberless concept offer suppression of RC network and it is suitable for applications such as :

- Static relays
- Solid state switches
- Motor controls
- Light dimmers
- Copy machines
- Microwave ovens
- Heater controls

### MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	55	A
$V_{DRM}/V_{RRM}$	800 to 1600	V
$I_{GT(Q1)}$	10 to 50	mA

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$		$T_c = 90^\circ\text{C}$	55	A
Non repetitive surge peak on-state current (full cycle, $T_j$ initial = $25^\circ\text{C}$ )	$I_{TSM}$	F = 50 Hz	t = 20 ms	550	A
		F = 60 Hz	t = 16.7 ms	600	
$I^2t$ Value for fusing	$I^2t$	$t_p = 10$ ms		1510	$\text{A}^2\text{s}$
Critical rate of rise of on-state current $I_G = 2I_{GT}$ , $t_r \leq 100\text{ns}$	dI/dt	F = 120 Hz	$T_j = 125^\circ\text{C}$	100	$\text{A}/\mu\text{s}$
Peak gate current	$I_{GM}$	$T_p = 20 \mu\text{s}$	$T_j = 125^\circ\text{C}$	8	A
Peak gate power dissipation ( $t_p = 20\mu\text{s}$ )	$P_{GM}$	$T_j = 125^\circ\text{C}$		10	W
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		2	
Storage temperature range	$T_{stg}$			- 40 to + 150	$^\circ\text{C}$
Operating junction temperature range	$T_j$			- 40 to + 125	

© ELECTRICAL CHARACTERISTICS (T<sub>J</sub>= 25 °C unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)					
SYMBOL	TEST CONDITIONS	QUADRANT		Limits	Unit
				BW	
I <sub>GT</sub> <sup>(1)</sup>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 33Ω	I - II - III	MAX.	50	mA
V <sub>GT</sub>		I - II - III		1.3	V
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3KΩ T <sub>j</sub> = 125°C	I - II - III	MIN.	0.2	V
I <sub>H</sub> <sup>(2)</sup>	I <sub>T</sub> = 500 mA		MAX.	80	mA
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	I - III	MAX.	80	mA
		II		160	
dV/dt <sup>(2)</sup>	V <sub>D</sub> = 67% V <sub>DRM</sub> , gate open, T <sub>j</sub> = 125°C		MIN.	1000	V/μs
(dI/dt) <sub>c</sub> <sup>(2)</sup>	Without snubber, T <sub>j</sub> = 125°C			20	A/ms

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V <sub>TM</sub> <sup>(2)</sup>	I <sub>TM</sub> = 82 A, t <sub>p</sub> = 380 μs	T <sub>j</sub> = 25°C	MAX.	1.55	V
V <sub>th</sub> <sup>(2)</sup>	Threshold voltage	T <sub>j</sub> = 125°C	MAX.	0.85	V
R <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125°C	MAX.	10	mΩ
I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>D</sub> = V <sub>DRM</sub> V <sub>R</sub> = V <sub>RRM</sub>	T <sub>j</sub> = 25°C	MAX.	50	μA
		T <sub>j</sub> = 125°C		8	mA

Note 1: Minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE			
SYMBOL		VALUE	UNIT
R <sub>th(j-c)</sub>	Junction to case (AC)	0.50	°C/W
R <sub>th(j-a)</sub>	Junction to ambient	50	

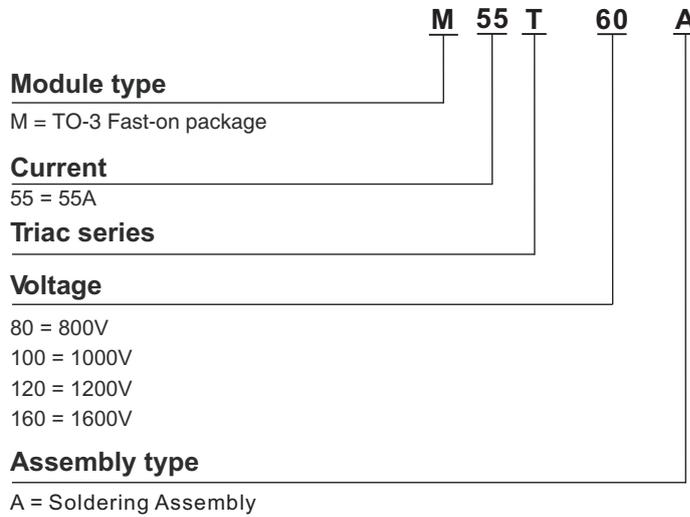
S = Copper surface under tab.

PRODUCT SELECTOR							
PART NUMBER	VOLTAGE (xx)				SENSITIVITY	TYPE	PACKAGE
	800 V	1000 V	1200 V	1600 V			
M55TxxA	V	V	V	V	50 mA	Snubberless	TO-3

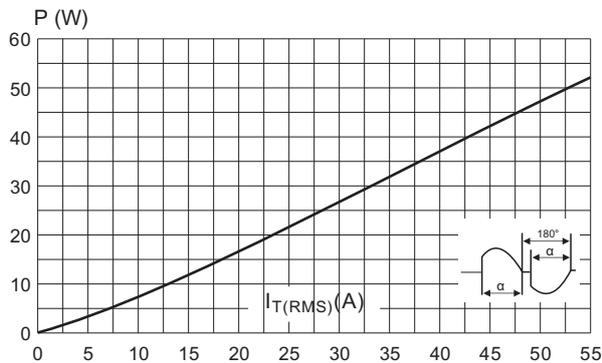
ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
M55TxxA	M55TxxA	TO-3	23g	50	BOX

Note : xx = voltage

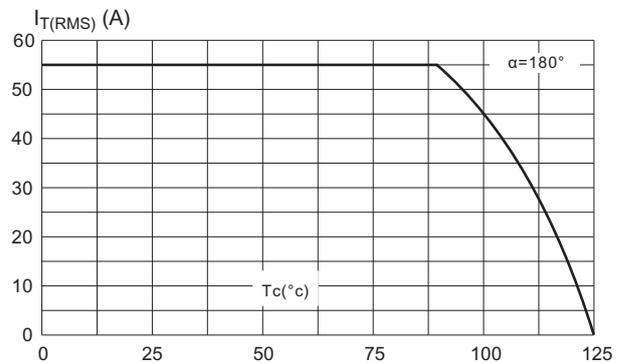
## ORDERING INFORMATION SCHEME



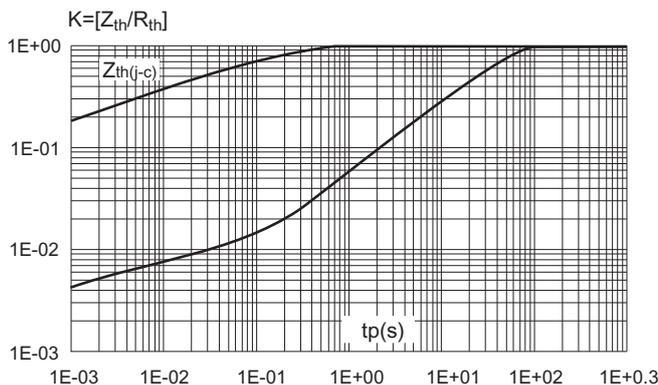
**Fig.1 Maximum power dissipation versus on-state RMS current (full cycle)**



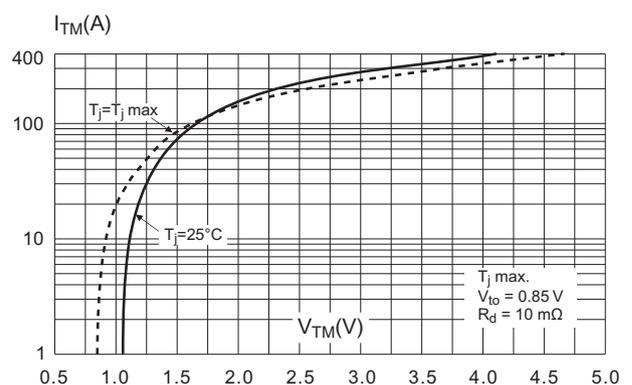
**Fig.2 On-state RMS current versus case temperature (full cycle)**



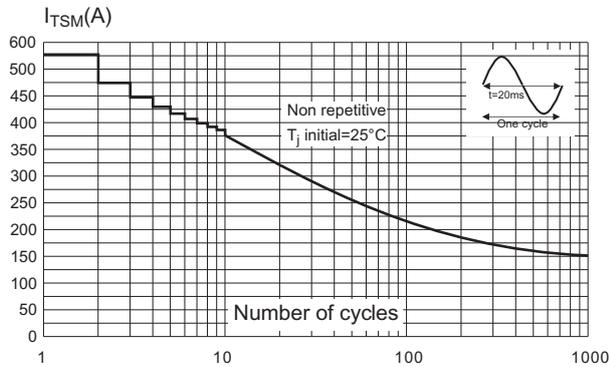
**Fig.3 Relative variation of thermal impedance versus pulse duration.**



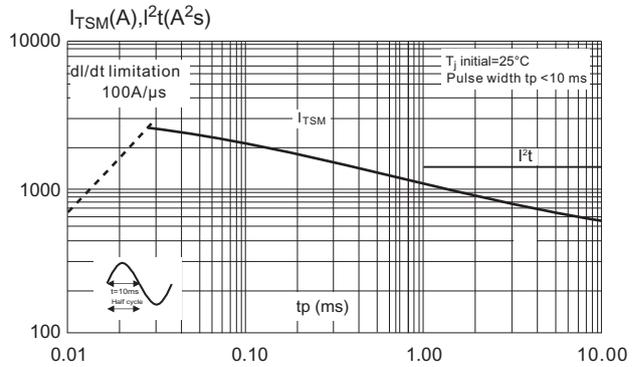
**Fig.4 On-state characteristics (maximum values).**



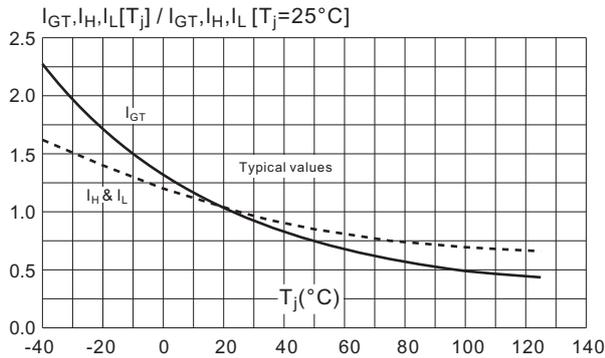
**Fig.5 Surge peak on-state current versus number of cycles.**



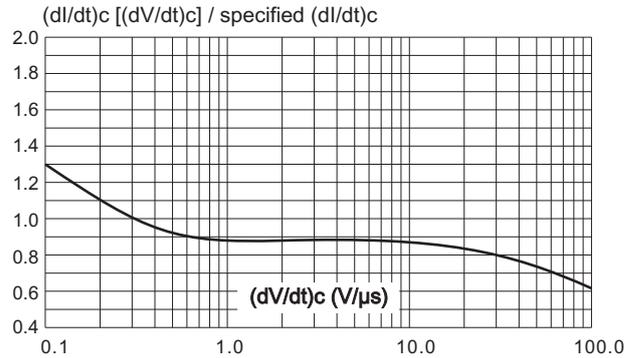
**Fig.6 Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding value of  $I^2t$ .**



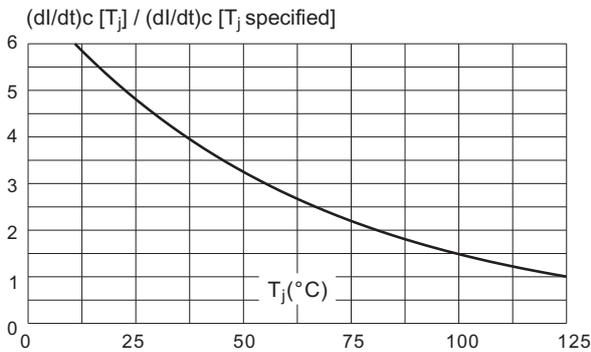
**Fig.7 Relative variation of gate trigger, holding and latching current versus junction temperature.**



**Fig.8 Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$  (typical values).**

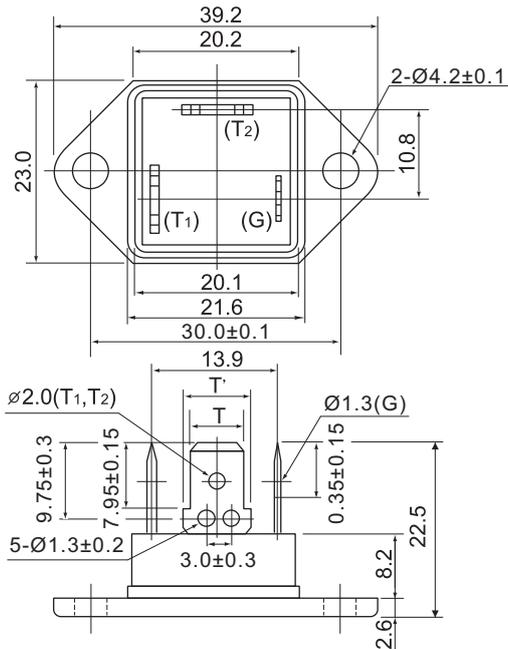


**Fig.9 Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$ .**



**Case Style**

**TO-3**



T<sub>1</sub>:TAB250(T=6.35, T'=8.25, t=0.8)  
 T<sub>2</sub>:TAB250(T=6.35, T'=8.25, t=0.8)  
 G:TAB187(T=4.75, T'=5.7, t=0.5)



All dimensions in millimeters