



Package: Laminate, 16-pin, 3.0mm x 3.0mm x 1.05mm

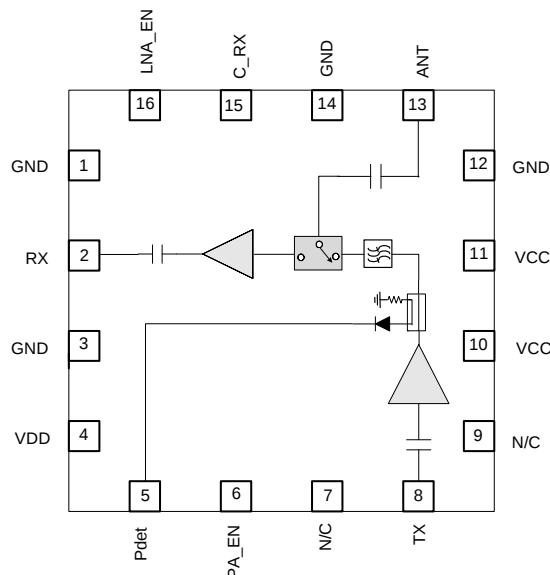


Features

- Single Supply Voltage 3.0V to 4.8V
- Integrated 5GHz Amplifier, SPT2T TX/RX Switch, LNA, and Power Detector Coupler
- $P_{OUT} = 16\text{dBm}$, 11n, 54Mbps at 2% Dynamic EVM
- $P_{OUT} = 16\text{dBm}$, 11ac HT80 MCS9, 1.8% Dynamic EVM

Applications

- IEEE802.11a/n/ac WiFi Applications
- Mobile Devices
- Tablets
- Consumer Electronics
- Gaming
- Netbooks and Notebooks
- TV, Monitors, and Video



Functional Block Diagram

Product Description

The RFFM8500 provides a complete integrated solution in a single Front End Module (FEM) for WiFi 802.11a/n systems. The ultra small form factor and integrated matching minimizes the layout area in the customer's application and greatly reduces the number of external components. This simplifies the total front end solution by reducing the bill of materials, system footprint, and manufacturability cost. The RFFM8500 integrates a Power Amplifier (PA), Single Pole Double Throw switch (SP2T), LNA and a power detector coupler for improved accuracy. The device is provided in a 3mm x 3mm x 1.0mm, 16-pin laminate package. This module meets or exceeds the RF Front End needs of IEEE 802.11a/n WiFi RF systems.

Optimum Technology Matching® Applied

- | | | | |
|---|--------------------------------------|--|-----------------------------------|
| ☐ GaAs HBT | ☐ SiGe BiCMOS | ☒ GaAs pHEMT | ☐ GaN HEMT |
| ☐ GaAs MESFET | ☐ Si BiCMOS | ☐ Si CMOS | ☐ RF MEMS |
| ☒ InGaP HBT | ☐ SiGe HBT | ☐ Si BJT | |

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	6.0	V _{DC}
Maximum TX and RX Input Power (No Damage)	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL3	



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Parameters					Nominal Operating Conditions: V _{CC} = 3.3V to 4.2V; SW Control High: V _{CC} -0.2V; PA_EN = V _{CC} -0.2V; P _{OUT} = 16dBm; Freq=5.18GHz to 5.825GHz; Modulation MCS7 HT20; Temp = -10°C to +70°C; Unless Otherwise Noted
Frequency	5.15		5.85	GHz	
Power Supply V _{CC}	3	3.3	4.8	V	
Switch Control Voltage-high	2.8	3.1	4.6	V	
Switch Control Voltage-Low		0	0.2	V	
PA_EN					
ON	2.8	3.1	4.6	V	PA_EN tracks with V _{CC} . Do not use PA_EN higher than V _{CC} .
OFF		0	0.2	V	
Gain	24	26		dB	V _{CC} = 3.3V; Temp = 25°C; Freq = 5.18GHz to 5.35GHz
	26	28		dB	V _{CC} = 3.3V; Temp = 25°C; Freq = 5.35GHz to 5.825GHz
	23	27		dB	
Dynamic EVM		2	2.5	%	V _{CC} = 3.3V; Temp = 25°C
		2	2.5	%	P _{OUT} = 15.5dBm
			1.8	%	11ac HT80 MCS9; V _{CC} = 3.3V; Temp = 25°C; P _{OUT} = 16dBm (see note)
Quiescent Current		185		mA	RF off; V _{CC} = 3.3V; Temp = 25°C
		185	210	mA	RF off
Operating Current		230	245	mA	V _{CC} = 3.3V; Temp = 25°C
		230	260	mA	
PAEN Current		35	50	μA	
FEM Leakage Current		2	10	μA	RF off; PAEN = OFF ; V _{CC} = "ON"
Second Harmonic		-45	-35	dBm	Fo = 4.9GHz to 5.3GHz: P _{OUT} = 18dBm; RBW = 1MHz
			-43	dBm	Fo = 5.3GHz and 5.85GHz: P _{OUT} = 18dBm; RBW = 1MHz
Third Harmonic		-50	-43	dBm	Fo = 5.15GHz to 5.85GHz: P _{OUT} = 18dBm; RBW = 1MHz
Power Detector					
P _{OUT} at 0dBm	350	375	400	mV	
P _{OUT} at 16dBm	500	600	700	mV	
TX Port Return Loss	9.6	15		dB	at TX input
ANT Port Return Loss	10	15		dB	in TX mode
PA Switching Time- V _{REF} (on<->off)		200	600	ns	
PA Stability					Unconditional into 4:1 VSWR, No spurious above -41.25dBm/MHz

Note: See RFFM8500 Application Note for 11ac applications schematic.

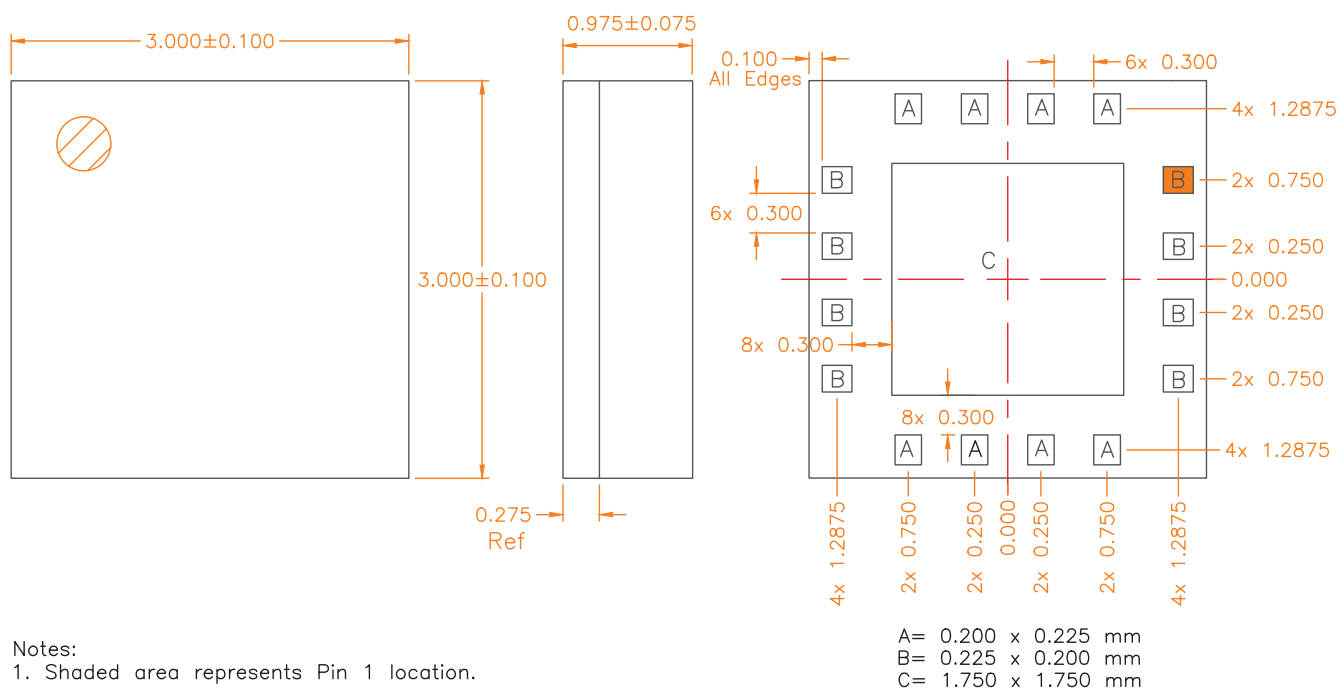
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receive Parameters					Operating Conditions: $V_{DD} = 3.3V$ to $4.2V$; SW Control High: $V_{DD} - 0.2V$; LNA_EN = $2.8V$ to $4.2V$; Freq= $5.18GHz$ to $5.825GHz$; Temp = $-10^{\circ}C$ to $+70^{\circ}C$; Unless Otherwise Noted
Frequency	5.15		5.85	GHz	
LNA Voltage Supply (V_{DD})	3	3.3	4.8	V	
LNA_EN Voltage	2.8	3.1	4.6	V	
Gain	13	15	16	dB	Temp= $25^{\circ}C$; $V_{DD}=3.3v$
	11	15	17	dB	
NF		2.5	2.8	dB	Temp= $25^{\circ}C$; $V_{DD} = 3.3V$
		2.5	3.7	dB	
Rx Port Return Loss	8	15		dB	
ANT Port Return Loss	6	8		dBm	
Input IP3		-3		dBm	
Input P1dB		-13		dBm	
I_{DD}		13	17	mA	
LNAEn Control Current		30	100	μA	
LNA Turn On Time		200	600	ns	
Isolation					
TX-RX	32			dB	Measured from ANT to RX while in Tx mode
Switch Control Current - Each Line		0.5	1	μA	
Switching Speed			100	ns	
ESD					
Human Body Model (HBM)	500			V	EIA/JESD22-114A RF pins
	1000			V	EIA/JESD22-114A DC pins
Charge Device Model	1000			V	JESD22-C101C

Logic Control Table

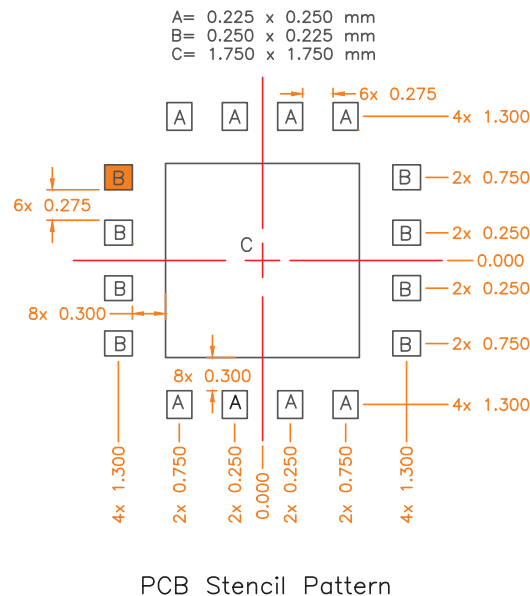
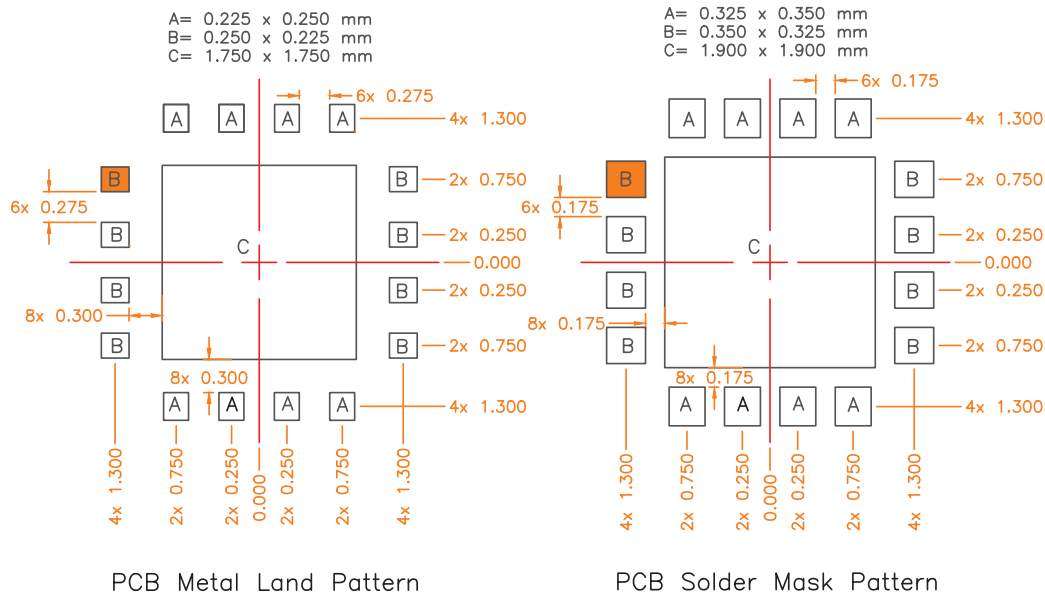
Mode	PA_EN	LNA_EN	C_RX
Standby	Low	Low	Low
802.11a/n TX	High	Low	Low
802.11a/n RX Gain	Low	High	High

Pin	Function	Description
1	GND	Ground connection.
2	RX	RF output port for the 802.11a/n LNA. Input is matched to 50Ω and DC block is provided.
3	GND	Ground connection.
4	VDD	Supply voltage for the LNA. See applications schematic for biasing and bypassing components.
5	PDET	Power detector voltage for TX section. PDET voltage varies with output power. May need external capacitor for noise decoupling.
6	PA_EN	Control voltage for the PA and TX switch. See truth table for proper settings.
7	NC	Not connected.
8	TX	RF input port for the 802.11a/n PA. Input is matched to 50Ω and DC block is provided.
9	NC	Not connected.
10	VCC	Supply voltage for the PA. See applications schematic for biasing and bypassing components.
11	VCC	Supply voltage for the PA. See applications schematic for biasing and bypassing components.
12	GND	Ground connection.
13	ANT	RF bidirectional antenna port matched to 50Ω and is DC blocked internally.
14	GND	Ground connection.
15	C_RX	Receive switch control pin. See switch truth table for proper level.
16	LNA_EN	Control voltage for the LNA.
Pkg Base	GND	Ground connection.

Package Drawing



PCB Patterns



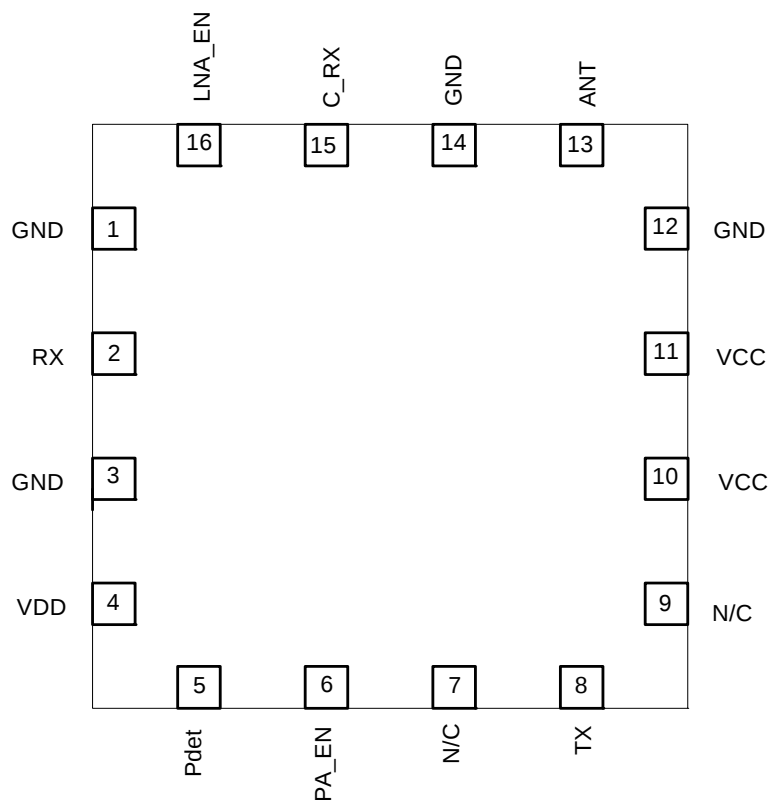
Notes:

1. Shaded area represents Pin 1 location.

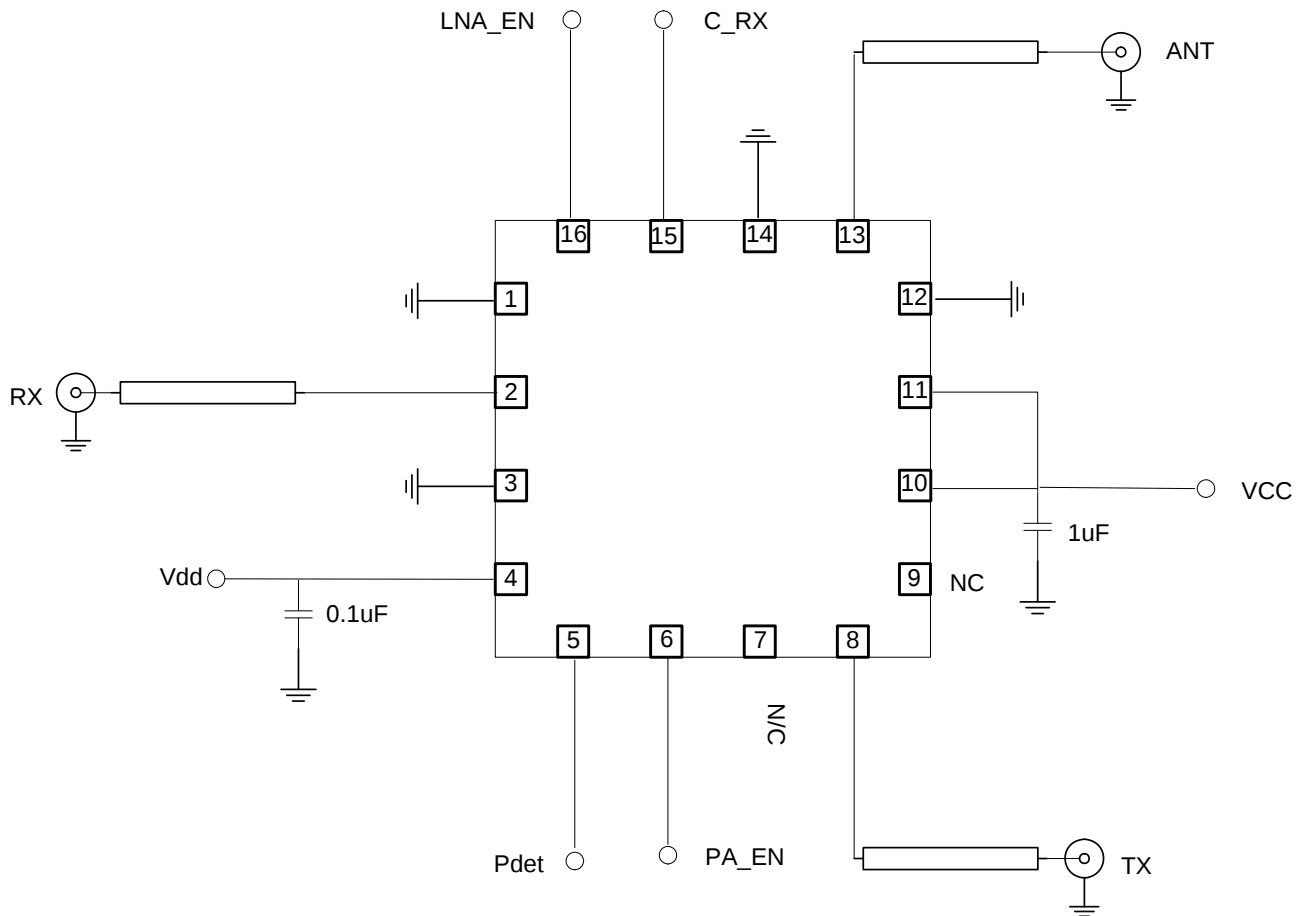
Notes:

1. Shaded area represents Pin 1 location.
2. Thermal vias for center slug "C" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, power dissipation and electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout (gerber files are available upon request).

Pin Out



Applications Schematic

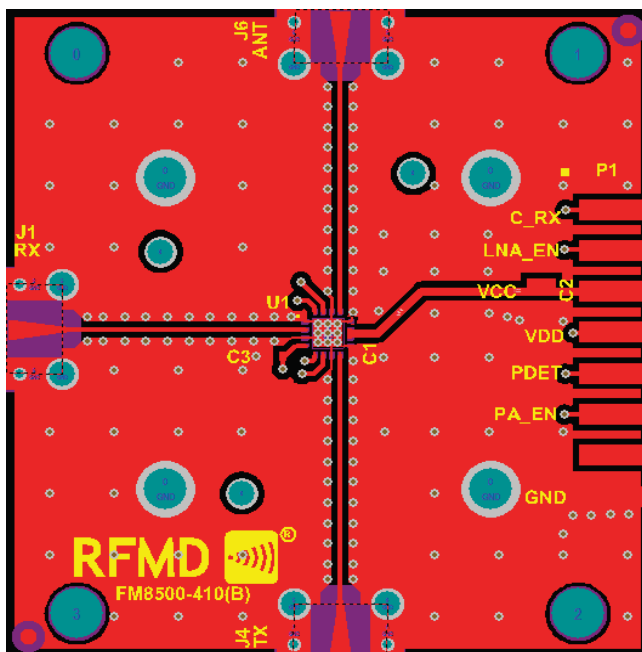


Note:

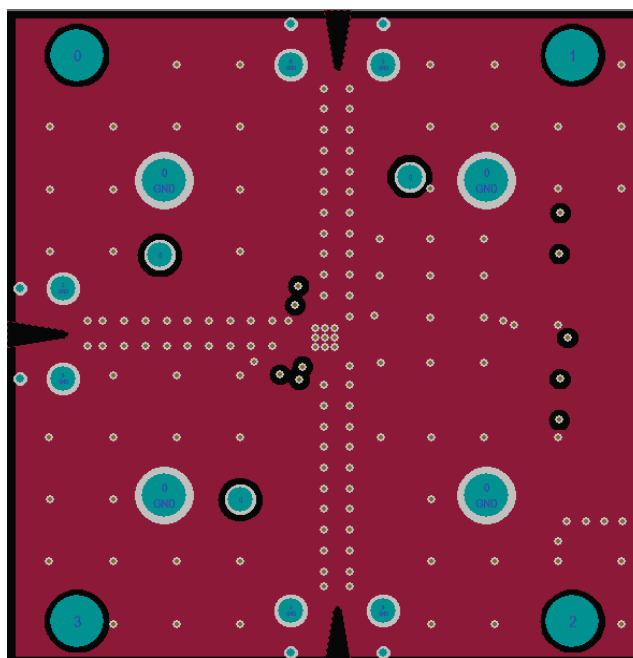
1. Pins 1, 3, 7, 9, 12, and 14 are not connected internally. These pins can be left floating or grounded. It is recommended to follow the RFMD evaluation board layout.

RFFM8500 Evaluation Board Layers

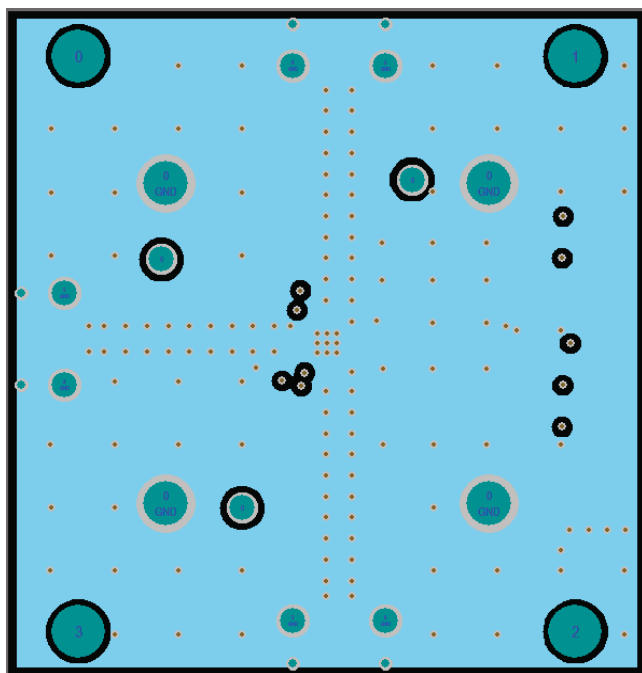
Top Layer



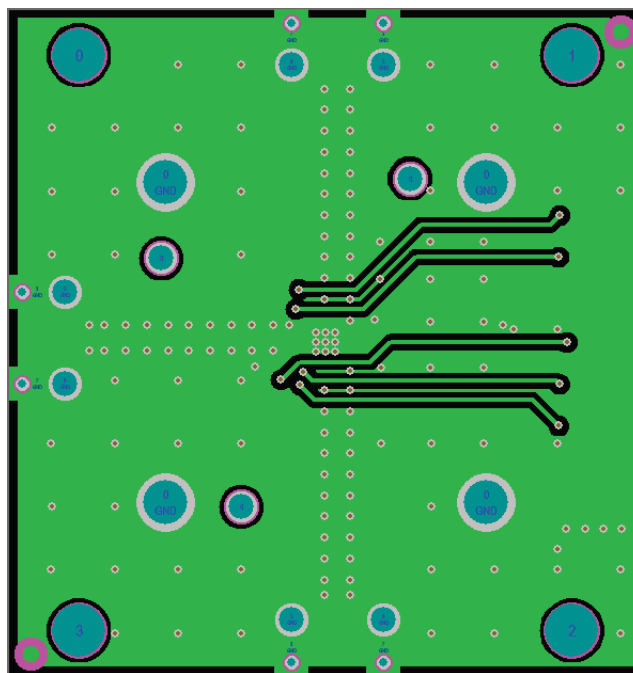
Mid Layer 1



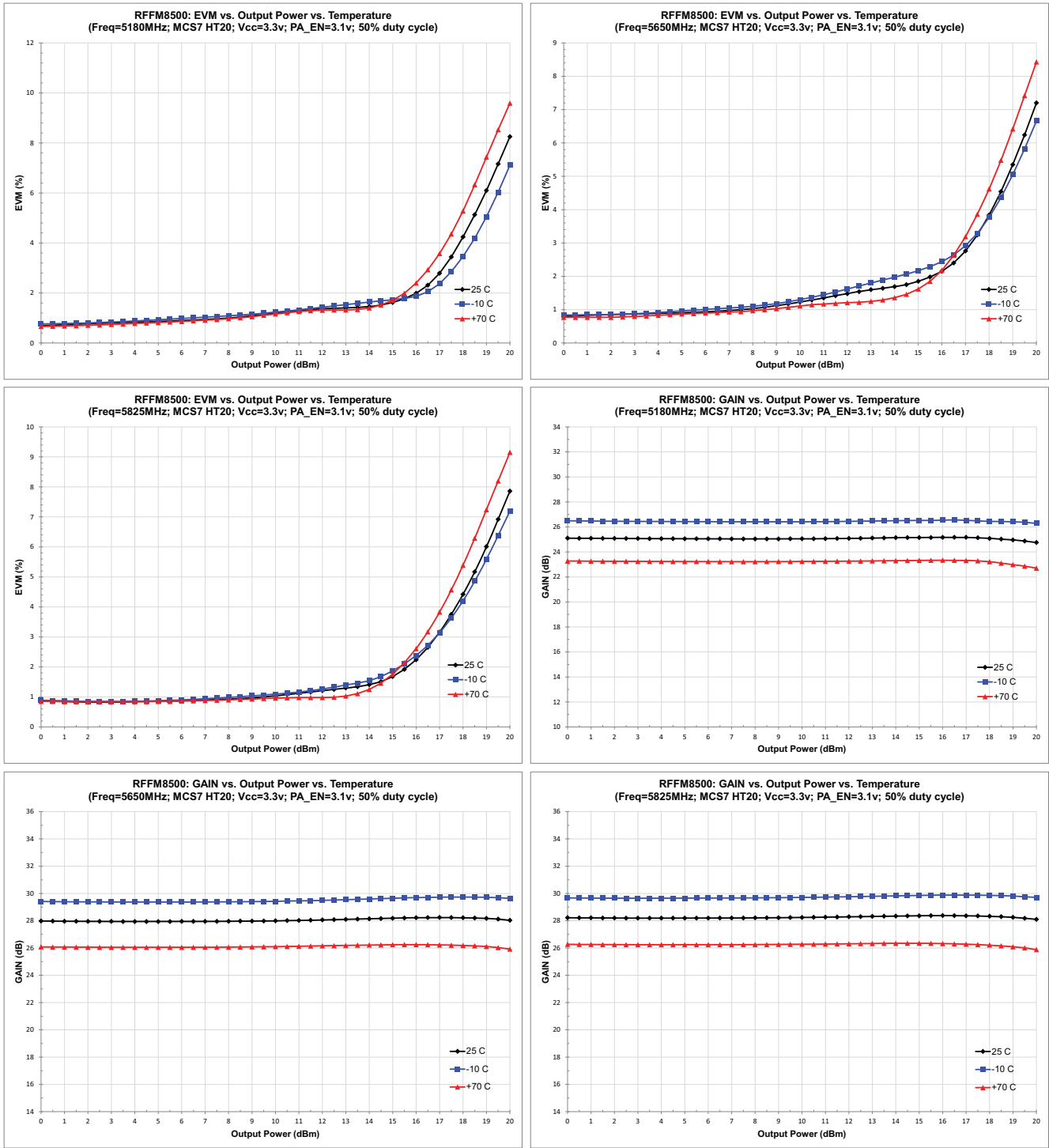
Mid Layer 2



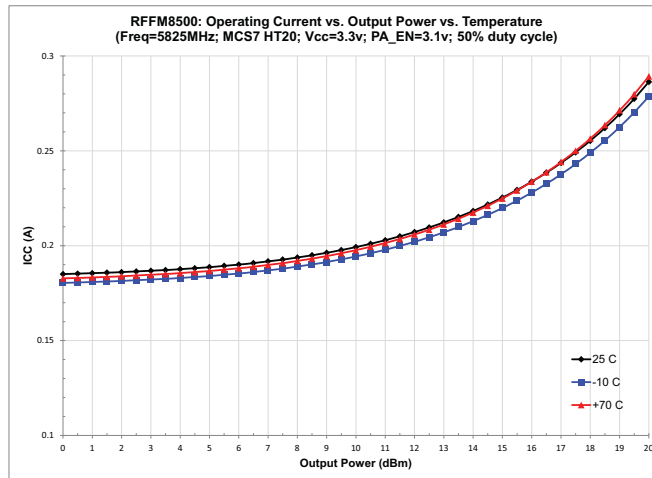
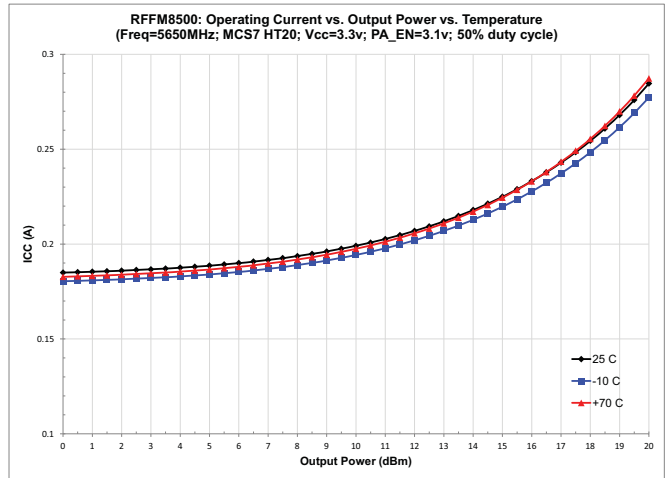
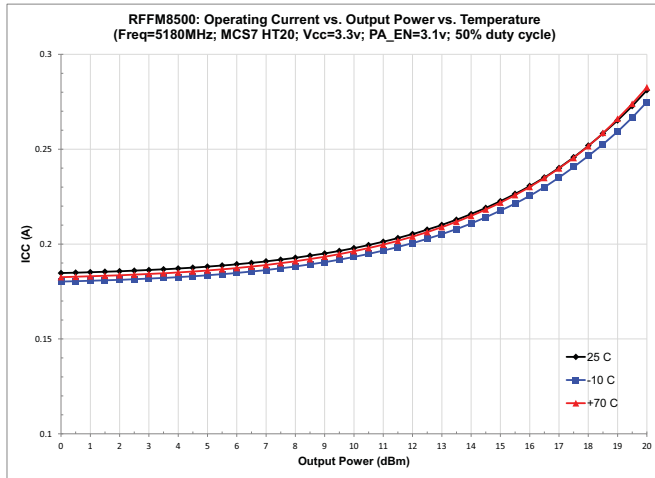
Bottom Layer



RFFM8500 Transmit Performance Plots



RFFM8500 Transmit Performance Plots



RFFM8500 Receive Performance Plots

