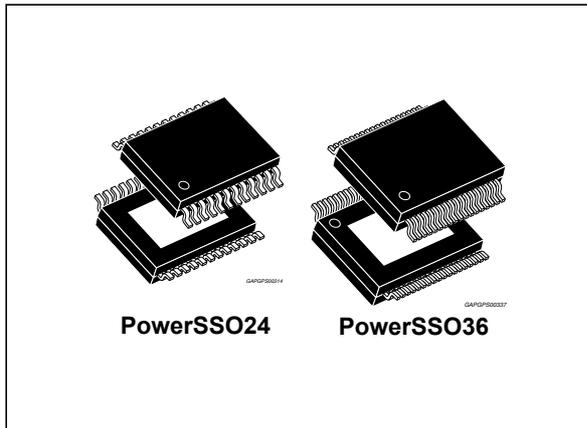


Single and dual PMOS high-side H-bridge

Datasheet - production data



- Current-monitoring with current feedback output signal CF
- SPI-interface for configuration and diagnosis
- Error history in second diagnosis register
- Two independent enable pins: "/ABE" and "DIS"
- Control of power stages by SPI or two input signals, PWM and DIR (configurable via SPI)
- Logic levels 5 V compatible
- Conformity to improved EMC requirements due to smart H-bridge switching

Features

- Full path $R_{DS(ON)}$ less than 540 m Ω
- Continuous load current > 3 A
- Operating battery supply voltage 5 V to 28 V
- Operating V_{DD} supply voltage 4.5 V to 5.5 V
- All ECU internal pins can withstand up to 18 V
- Output switching frequency up to 11 kHz
- Monitoring of V_{DD} supply voltage
- SPI programmable output current limitation from 5 A to 8.6 A (in 3 steps)
- Over temperature and short circuit protection
- Full diagnosis capability
- Fast switch-off open-drain input/output

Description

L9959S/L9959U and L9959T are single and dual integrated H-bridges for resistive and inductive loads featuring output current direction and supervising functions.

The PowerSSO24 houses one full H-Bridge, while the PowerSSO36 houses both two H-Bridges that can work in parallel, through independent input driving commands, and one full H-bridge, by improving PCB footprint design versus different target applications.

Target application ranges from throttle control actuators to exhaust gas recirculation control valves in automotive domain to a more general use to drive DC and Stepper motors.

Table 1. Device summary

| Order code | Package | Packing |
|-------------|------------|-------------|
| L9959S-TR-D | PowerSSO24 | Tape & Reel |
| L9959T-TR-D | PowerSSO36 | Tape & Reel |
| L9959U-TR-D | PowerSSO36 | Tape & Reel |

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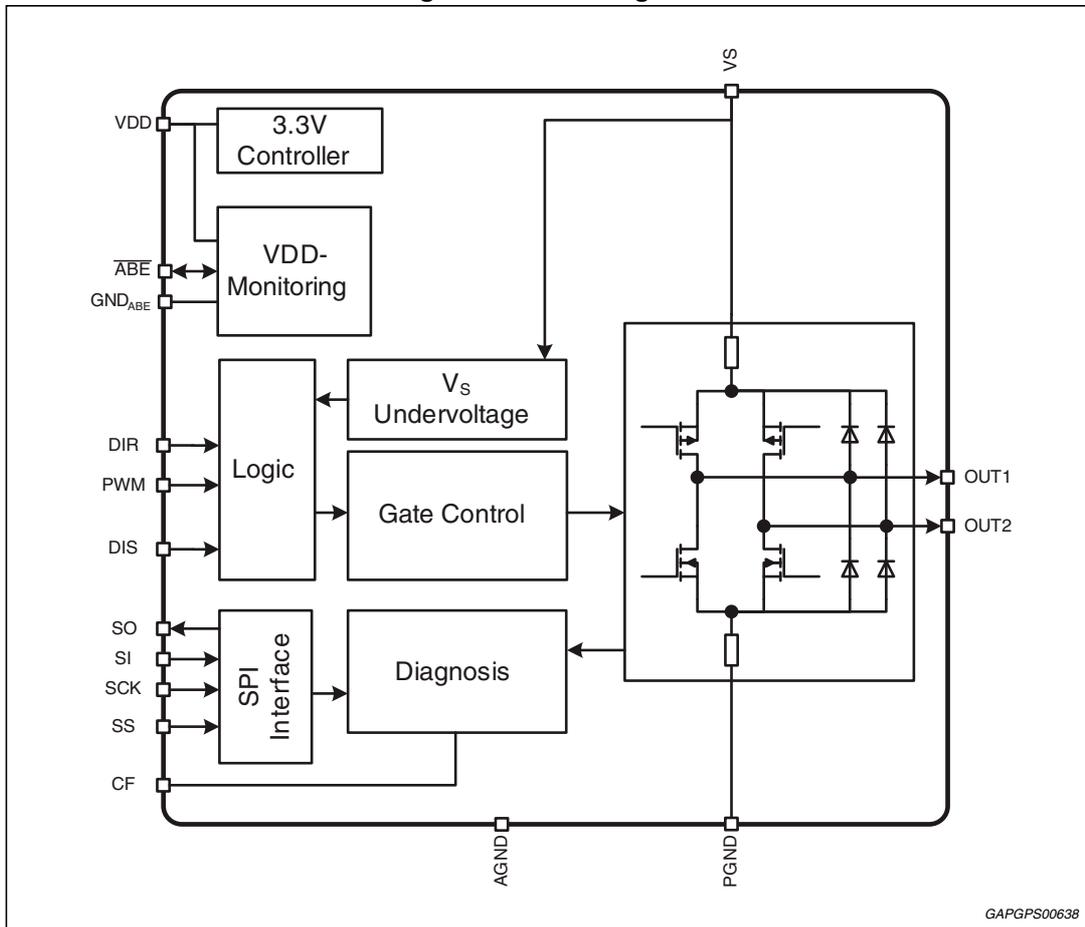
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1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. PSSO24 pin connection (top view)

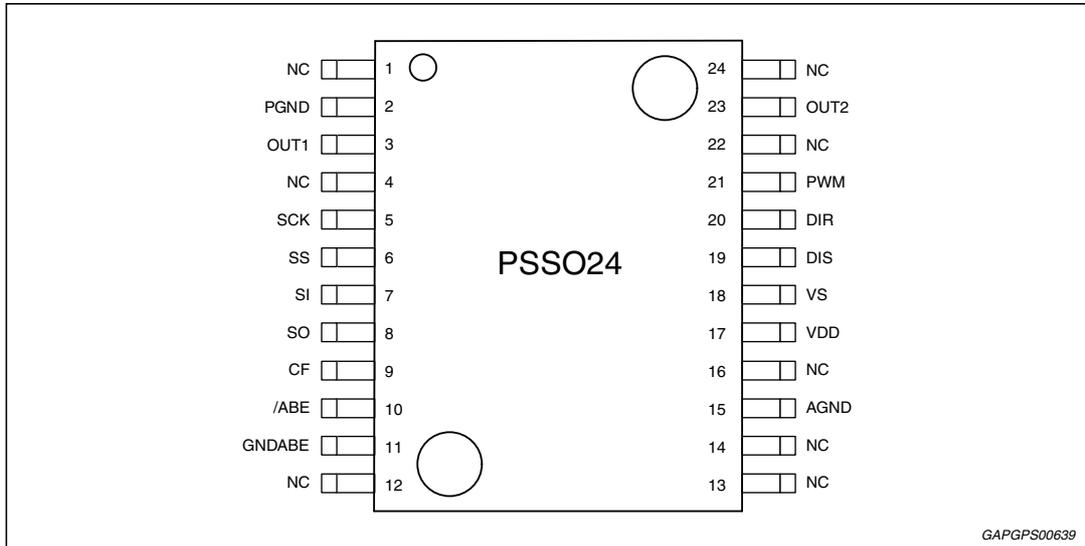


Figure 3. PSSO36 pin connection (top view)

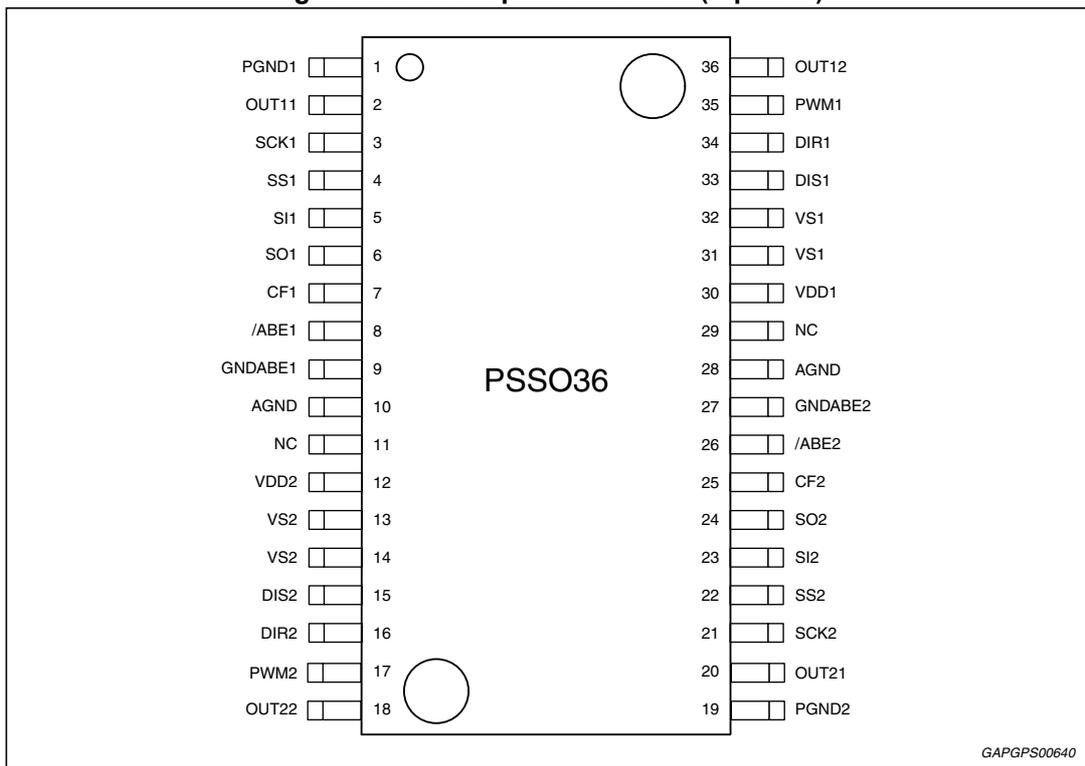
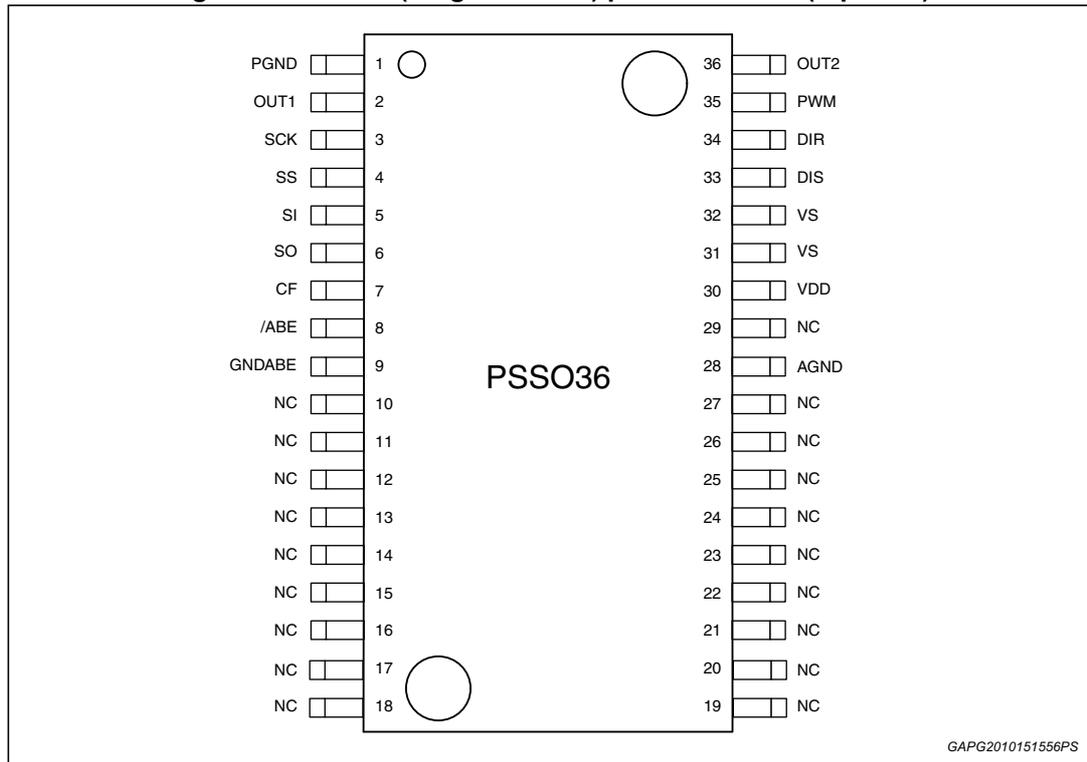


Figure 4. PSSO36 (Single version) pin connection (top view)



2.1 Pin definitions and functions

Table 2. L9959S PSSO24 pin-out

| Pin | Symbol | Function |
|------------------------------|--------|--|
| 1, 4, 12, 13, 14, 16, 22, 24 | NC | To be connected to GND on PCB. |
| 2 | PGND | Power Ground |
| 3 | OUT1 | Bridge output 1 and 2: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. |
| 5 | SCK | Serial clock input: This input controls the internal shift register of the SPI. |
| 6 | SS | Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level. |
| 7 | SI | Slave in (Serial data input): The input receives serial data from the microcontroller. |
| 8 | SO | Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output. |

Table 2. L9959S PSSO24 pin-out (continued)

| Pin | Symbol | Function |
|-----|--------|--|
| 9 | CF | Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current. |
| 10 | /ABE | Bidirectional Ability/Enable Pin: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. |
| 11 | GNDABE | Sense Ground for VDD monitoring |
| 15 | AGND | Device Ground. (Connected to Exposed PAD) |
| 17 | VDD | VDD Supply: 5 V Supply |
| 18 | VS | Power supply voltage for power stage outputs (external reverse protection required) |
| 19 | DIS | Disable input: DIS switches OUT1 and OUT2 to tristate. |
| 20 | DIR | Direction input: The DIR pin controls the switch direction of OUT1 and OUT2. |
| 21 | PWM | PWM input: The PWM input switches OUT1 and OUT2. |
| 23 | OUT2 | Bridge output 1 and 2: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. |
| EP | AGND | Exposed Pad: Connected to AGND. |

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out

| Pin | Symbol | Function |
|-----|----------------------|--|
| 1 | PGND1 ⁽¹⁾ | Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected. |
| 2 | OUT11 | Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22. |
| 3 | SCK1 | Serial clock input: This input controls the internal shift register of the SPI. SCK1 belongs to chip 1 and SCK2 to chip 2. |
| 4 | SS1 | Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level. SS1 belongs to chip 1 and SS2 to chip 2. |
| 5 | SI1 | Slave in (Serial data input): The input receives serial data from the microcontroller. SI1 belongs to chip 1 and SI2 to chip 2. |
| 6 | SO1 | Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output. SO1 belongs to chip 1 and SO2 to chip 2. |

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out (continued)

| Pin | Symbol | Function |
|---------|----------------------|---|
| 7 | CF1 | Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current. CF1 belongs to OUT11 and OUT12, CF2 to OUT21 and OUT22. |
| 8 | /ABE1 | Bidirectional Ability/Enable Pin 1: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. /ABE1 belongs to chip 1. |
| 9 | GNDABE1 | Sense Ground for VDD monitoring |
| 10, 28 | AGND | Device Ground. (Connected to Exposed PAD) |
| 11, 29 | NC | To be connected to GND on PCB. |
| 12 | VDD2 ⁽²⁾ | VDD Supply: 5V Supply. |
| 13, 14, | VS2 ⁽³⁾ | Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected. |
| 15 | DIS2 | Disable input 2: DIS2 switches OUT21 and OUT22 to tristate. |
| 16 | DIR2 | Direction input 2: DIR2 pin controls the switch direction of OUT21 and OUT22. |
| 17 | PWM2 | PWM input 2: PWM1 input switches OUT21 and OUT22. |
| 18 | OUT22 | Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22. |
| 19 | PGND2 ⁽¹⁾ | Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected. |
| 20 | OUT21 | Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22. |
| 21 | SCK2 | Serial clock input: This input controls the internal shift register of the SPI. SCK1 belongs to chip 1 and SCK2 to chip 2. |
| 22 | SS2 | Slave Select input: The serial data transfer between the device and the micro controller is enabled by pulling the input SS to low level. SS1 belongs to chip 1 and SS2 to chip 2. |
| 23 | SI2 | Slave in (Serial data input): The input receives serial data from the microcontroller. SI1 belongs to chip 1 and SI2 to chip 2. |
| 24 | SO2 | Slave Out (Serial data output): The diagnosis data is available via the SPI through this tristate-output. SO1 belongs to chip 1 and SO2 to chip 2. |

Table 3. L9959T (Two H-Bridge drivers in one package) PSSO36 pin-out (continued)

| Pin | Symbol | Function |
|--------|---------------------|---|
| 25 | CF2 | Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current. CF1 belongs to OUT11 and OUT12, CF2 to OUT21 and OUT22. |
| 26 | /ABE2 | Bidirectional Ability/Enable Pin 2: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. /ABE2 belongs to chip 2. |
| 27 | GNDABE2 | Sense Ground for VDD monitoring |
| 30 | VDD1 ⁽²⁾ | VDD Supply: 5V Supply. |
| 31, 32 | VS1 ⁽³⁾ | Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected. |
| 33 | DIS1 | Disable input 1: DIS1 switches OUT11 and OUT12 to tristate |
| 34 | DIR1 | Direction input 1: DIR1 pin controls the switch direction of OUT11 and OUT12. |
| 35 | PWM1 | PWM input 1: PWM1 input switches OUT11 and OUT12. |
| 36 | OUT12 | Bridge output 11, 12, 21, and 22: The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. The bridge outputs of chip 1 are OUT11 and OUT12, of chip 2 OUT21 and OUT22. |
| EP | AGND ⁽⁴⁾ | Exposed PAD: connected to AGND |

1. Pins 1 is referred to die 1, whereas 19 is referred to die 2.
2. Pins 12 is referred to die 2, whereas 30 is referred to die 1.
3. Pins 13 and 14 are referred to die 2, whereas pins 31 and 32 are referred to die1.
4. Pins 10 is referred to die 2, whereas 28 is referred to die 1.

Table 4. L9959U (Single version in PSSO36) pin out

| Pin | Symbol | Function |
|--|--------|---|
| 1 | PGND | Ground: Important: For the capability of driving the full current at the outputs, all ground pins must be externally connected. |
| 2 | OUT1 | The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. |
| 3 | SCK | Serial clock input: This input controls the internal shift register of the SPI. |
| 7 | CF | Current Proportional Feedback output: The CF pin provides in conjunction with an external resistor an output current, which is proportional to the H-Bridge current |
| 8 | /ABE | Bidirectional Ability/Enable Pin: Open-Drain Output, which is pulled low in case of VDD over- and under-voltage. If the input is pulled to low, all output stages are switched off. |
| 9 | GNDABE | Sense Ground for VDD monitoring |
| 10,11, 12,13, 14,15, 16,17, 18,19, 20,21, 22,23, 24,25, 26,27, 29 | NC | To be connected to GND on PCB. |
| 28 | AGND | Device Ground. (Connected to Exposed PAD) |
| 30 | VDD | VDD Supply: 5 V Supply. |
| 31, 32 | VS1 | Power supply voltage for power stage outputs (external reverse protection required): Important: For the capability of driving the full current at the outputs all pins of VS must be externally connected. |
| 33 | DIS | Disable input : DIS switches OUT1 and OUT2 to tristate |
| 34 | DIR | Direction input: DIR pin controls the switch direction of OUT1 and OUT2. |
| 35 | PWM | PWM input: PWM input switches OUT1 and OUT2. |
| 36 | OUT2 | The bridge outputs are built of a high-side p-channel and a low-side N-channel transistor. |

3 Electrical specifications

3.1 Absolute maximum ratings

Warning: Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 5. Absolute maximum ratings

| Symbol | Parameter / Test condition | Value [DC Voltage] | Unit |
|--|---|--------------------|------|
| V_{VS} | DC supply voltage The device is able to sustain load dump as specified in the ISO16750 documentation | -1.0 to +40 | V |
| V_{VDD} | Stabilized supply voltage, logic supply | -0.3 to 18 | V |
| $C_F^{(1)}$ | Current feedback output | -0.3 to 18 | V |
| $V_{SI}, V_{SCK}, V_{SS}, V_{SO}, V_{DIR}, V_{PWM}, V_{DIS}$ | Logic input / output voltage range | -0.3 to 18 | V |
| V_{OUTn} | Output voltage (n = 1,2 or 11,12,21,22); $V_{OUTn} < V_S + 1 V$ | -1.0 to 40 | V |
| | Dynamic pulse / t < 500ms; $V_{OUTn} < V_S + 2 V$ | -2.0 to 40 | V |
| T_j | Operating junction temperature | -40 to 150 | °C |
| | Dynamic junction temperature (1000hrs) | 150 to 175 | °C |
| T_{stg} | Storage temperature | -55 to 150 | °C |

1. It is withstood at $V_S = 18 V$

3.2 ESD protection

Table 6. ESD protection

| Parameter | Value | Unit |
|--|---------------|------|
| All pins versus ground group (AGND, PGND1, PGND2, GND_ABE1, GND_ABE2) | $\pm 2^{(1)}$ | kV |
| VS pin, Power Output Pins: OUT1, OUT2 or OUT11, OUT12, OUT21, OUT22 versus ground group (AGND, PGND1, PGND2, GND_ABE1, GND_ABE2) | $\pm 4^{(2)}$ | kV |

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.

2. HBM with all unzipped pins grounded.

3.3 Thermal data

Table 7. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|---|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-to-case (max) for L9959S, L9959T | 2.0 | °C/W |

3.4 Electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $4.5\text{ V} \leq V_S \leq 18\text{ V}$, $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$; all outputs open; $T_j = -40\text{ °C}$ to 150 °C , unless otherwise specified.

Table 8. Supply

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------------|---|--|------|------|------|------------|
| V_S | Operating voltage range | - | 4.5 | - | 28 | V |
| I_{VS} | V_S current consumption in active mode | $V_{DD} = 5\text{ V}$; $V_S = 5\text{ V}$ and $V_S = 18\text{ V}$; Bridge disabled | - | - | 5 | mA |
| | | $V_{DD} = 5\text{ V}$; $V_S = 5\text{ V}$ and $V_S = 18\text{ V}$; $f_{OUT} = 2\text{ kHz}$; $I_{OUT} = 0\text{ A}$ | - | - | 6 | mA |
| | | $V_{DD} = 5\text{ V}$; $V_S = 5\text{ V}$ and $V_S = 18\text{ V}$; $f_{OUT} = 10\text{ kHz}$; $I_{OUT} = 0\text{ A}$ | - | - | 14 | mA |
| | | $V_{DD} = 5\text{ V}$; $V_S = 28\text{ V}$; $f_{OUT} = 10\text{ kHz}$; $I_{OUT} = 0\text{ A}$ | - | - | 14 | mA |
| $I_{VS(stby)}$ | V_S current consumption in passive mode | $V_{DD} = 0\text{ V}$ | 0 | - | 2.5 | mA |
| $V_{VS_slew}^{(1)}$ | Slew rate on V_S | - | - | - | 100 | V/ μ s |
| $V_{VS_slew}^{(2)}$ | Slew rate on V_S | - | - | - | 20 | V/ μ s |
| V_{DD} | Operating voltage range | - | 4.5 | - | 5.5 | V |
| I_{VDD} | V_{DD} supply current | $V_S = 18\text{ V}$; $V_{DD} = 5\text{ V}$ | - | - | 10 | mA |

1. No change of parameters for VDD-monitoring and in SPI logic
2. No change of parameters

Table 9. Power-on reset

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------|----------------|------|------|------|------|
| V_{DDRES} | Reset active threshold | - | 2.8 | - | 3.4 | V |
| V_{DDPOR} | Power-on reset threshold | - | 3.3 | - | 4 | V |
| $V_{DDPORHYS}$ | Power-on reset hysteresis | - | - | 600 | - | mV |
| t_{POR} | Power-on reset extension time | - | - | - | 1 | ms |

Table 10. V_{DD} monitoring

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------------|--|--|-------------|------|------|-------------------|
| V_{DD} | V_{DD} monitoring voltage range | - | V_{DDPOR} | - | 18 | V |
| V_{DD_THL} | Under voltage threshold | $V_S = 0\text{ V}$ | 4.2 | - | 4.5 | V |
| V_{DD_THH} | Over voltage threshold | $V_S = 0\text{ V}$ | 5.25 | - | 5.5 | V |
| t_{FIL_OFF} | Switch-off filtering time | Guaranteed by scan. | 60 | - | 135 | μs |
| t_{FIL_ON} | Switch-on filtering time | | 60 | - | 135 | μs |
| V_{TEST_THL} | Under voltage test threshold | - | 5.25 | - | 5.5 | V |
| V_{TEST_THH} | Over voltage test threshold | - | 4.2 | - | 4.4 | V |
| V_{DD_MR} | Full V_{DD} supply range | - | -0.3 | - | 18 | V |
| V_{DD_SLEW} | V_{DD} slew | - | - | - | 500 | mV/ μs |
| ΔV_{DD_THX} | Threshold (V_{DD_THH} , V_{DD_THL}) shift during vs. inverse current | - | -0.1 | - | 0.1 | V |
| V_{ABE_INL} | /ABE input low-level | - | -0.3 | - | 1.65 | V |
| V_{ABE_INH} | /ABE input high-level | - | 3.15 | - | 18 | V |
| V_{ABE_INHYS} | /ABE input hysteresis | - | 0.2 | - | 1.0 | V |
| I_{ABE_IN} | /ABE input pull-down current | $0\text{ V} < V_{ABE} < 1.5\text{ V}$ | 0 | - | 60 | μA |
| | | $V_{ABE} = 2.1\text{ V}, 5\text{ V}, 18\text{ V};$ $V_S = 18\text{ V}; V_{DD} = 5\text{ V},$ 18 V | 20 | 40 | 60 | μA |
| V_{ABE_OUTL} | /ABE output low voltage | $2.5\text{ V} < V_{DD} < V_{DD_THL};$ $I_{ABE_OUTL} < 2.5\text{ mA}$ | 0 | - | 1.0 | V |
| V_{ABE_OUTL} | /ABE output low voltage | $V_{DD_THH} < V_{DD} < 18\text{V};$ $I_{ABE_OUTL} < 7.5\text{ mA}$ | 0 | - | 1.2 | V |
| V_{ABE_OUTL} | /ABE output passive low voltage | - | 0 | - | 1.2 | V |
| ΔI_{ABE} | I_{ABE} Change during vs. inverse current | - | -100 | - | 100 | μA |

Table 11. Undervoltage shutdown

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------------|----------------------|----------------------------|------|------|------|---------|
| V_{UV_OFF} | VS UV threshold | VS decreasing | 3.1 | 3.8 | 4.5 | V |
| V_{UV_ON} | VS UV threshold | VS increasing | 3.3 | 4.0 | 4.7 | V |
| V_{UV_HYS} | VS UV hysteresis | $V_{UV_ON} - V_{UV_OFF}$ | 0.1 | - | 1 | V |
| t_{FUV} | VS UV detection time | - | - | - | 1.5 | μ s |

3.5 Outputs OUT1 and OUT2

Table 12. On-resistance ($4.5\text{ V} < V_S < 28\text{ V}$)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------------|--|--|------|------|------|-----------|
| r_{ONVS} OUT1,2 | On-resistance to supply | $V_{DD} = 5\text{ V}; V_S = 10\text{ V},$ $I_{OUT1,2} = 3\text{ A}$ | - | - | 315 | $m\Omega$ |
| r_{ONGND} OUT1,2 | On-resistance to PGND | $V_{DD} = 5\text{ V}; V_S = 10\text{ V},$ $I_{OUT1,2} = 3\text{ A}$ | - | - | 225 | $m\Omega$ |
| I_{LEAK} | Switched-off output current of OUT1,2 | $V_{DD} = 5\text{ V}; V_S = 13\text{ V};$ $V_{OUT} = 0\text{ V}$ | -200 | - | - | μ A |
| | | $V_{DD} = 5\text{ V}; V_S = 13\text{ V};$ $V_{OUT} = V_S$ | - | - | 200 | μ A |

Table 13. Power output switching times ($8\text{ V} < V_S < 18\text{ V}$)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------------------------|--|--|--------------|------|----------|------------|
| $t_{d\ ON}$ | Output delay time driver on | - | - | - | 6 | μ s |
| $t_{d\ OFF}$ | Output delay time driver off | - | - | - | 20 | μ s |
| $t_{d\ dis}^{(1)}$ | Disable delay time | Guaranteed through scan. | - | - | 12.5 | μ s |
| $t_{d\ pwon}$ | Power-on delay time | | - | - | 1 | ms |
| $t_{d\ en}$ | Enable delay time | | - | - | 50 | μ s |
| dl_{OUT}/dt | Current slew rate | - | - | 1.6 | | A/ μ s |
| dV_{OUTHS}/dt (2) | Output rise/fall slew-rate high-side slow selected with bit SR = 0 fast selected with bit SR = 1 | $V_{DD} = 5\text{ V}; V_S = 14\text{ V}$ $R_{LOAD1,2} = 2.6\ \Omega$ (8 V_S), $6\ \Omega$ (18 V_S) | 0.975 2.8 | - | 2.7 8 | V/ μ s |
| dV_{ROUTLS}/dt (2) | Output rise slew-rate low-side valid only after the toggling of DIR input | | 0.975 | - | 2.7 | V/ μ s |
| dV_{fOUTLS}/dt (2) | Output fall slew-rate low-side | | 2.5 | 4 | 8 | V/ μ s |
| f_{pwmmax} | PWM input frequency | - | - | - | 11 | kHz |

1. Driven by /ABE or DIS input.

2. The slew-rates (dV_{OUT}/dt) are defined by dV (voltage difference 20% - 80%) divided by the rise-/fall times (t_r/t_f see [Figure 6: Output rise and fall times](#)).

Figure 5. Output delay times (e.g. low-side output)

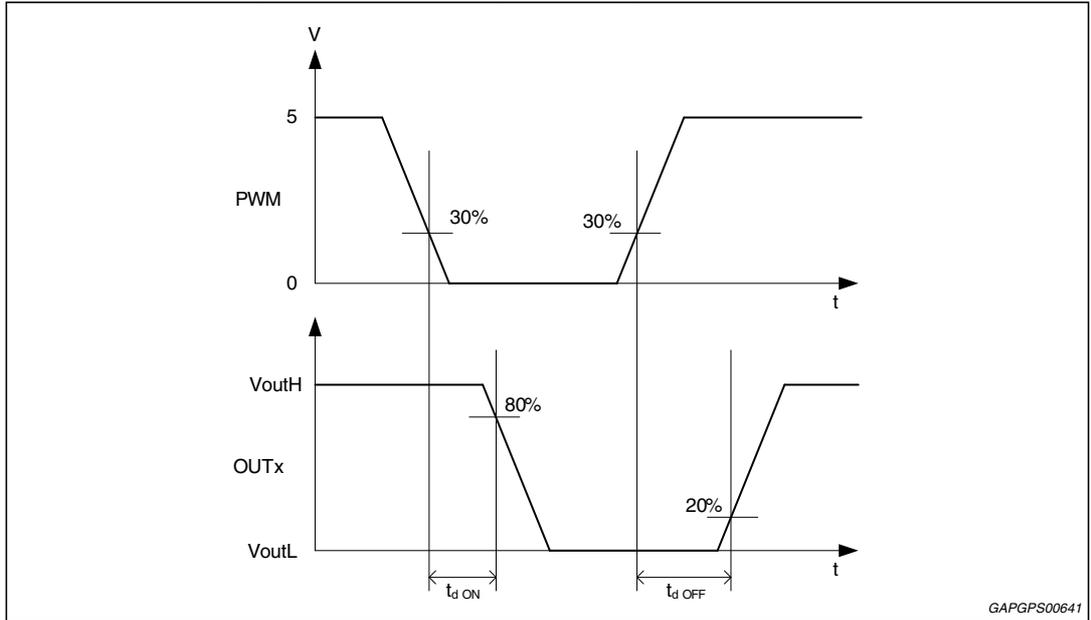


Figure 6. Output rise and fall times

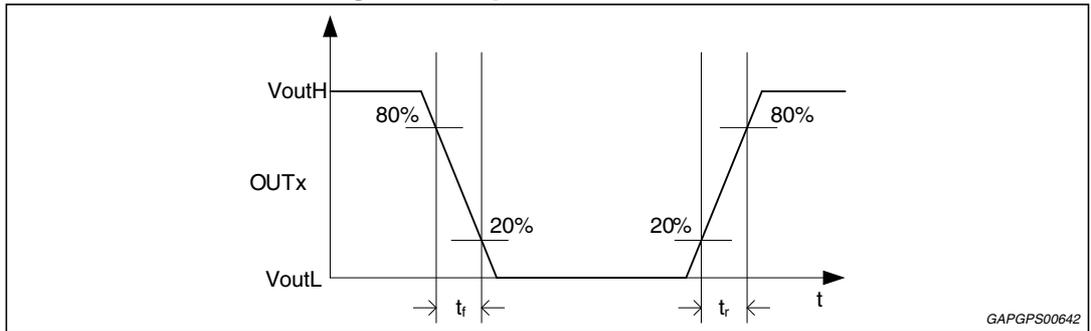


Figure 7. Output disable and enable time (/ABE Input)

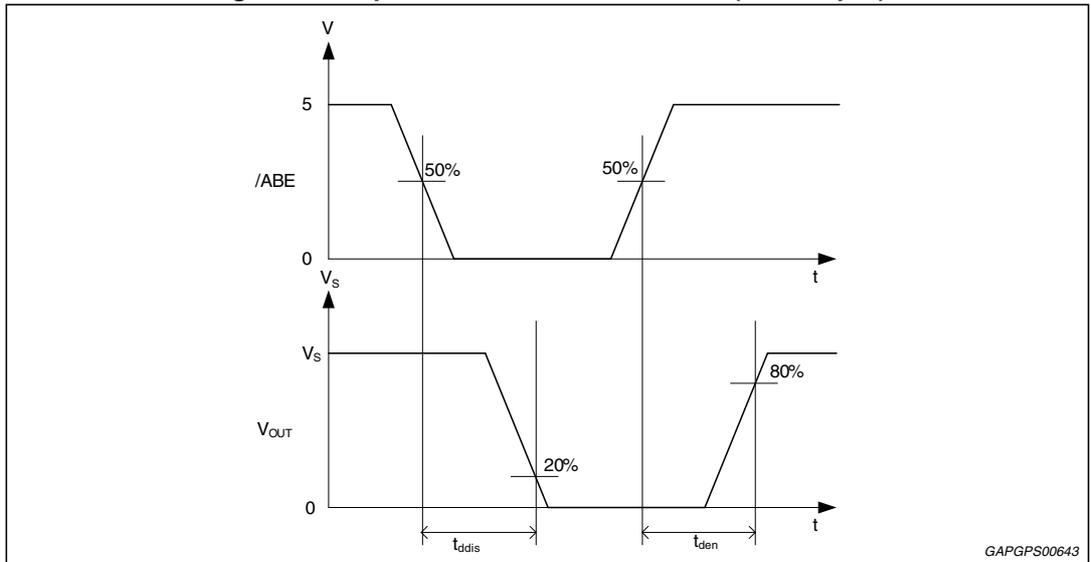
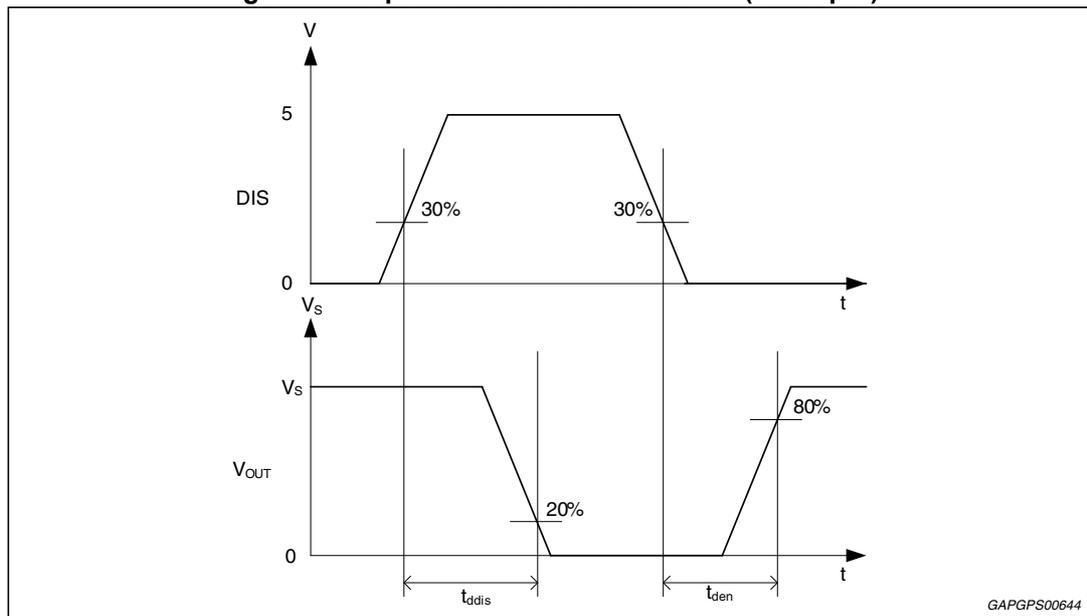


Figure 8. Output disable and enable time (DIS Input)



GAPGPS00644

Table 14. Current feedback (CF)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------------------------|-------------------|--|------|-------|------|------|
| V _{CF} ⁽¹⁾ | CF voltage range | V _S > 6.5 V, OUTx = 0 A, T _J = -40 °C; Current level 2,3,4 | 0.01 | 0.05 | 0.20 | V |
| | | V _S > 6.5 V, OUTx = 250mA, T _J = 130 °C; Current level 2,3,4 | 0.04 | 0.275 | 0.5 | V |
| | | V _S > 6.5 V, OUTx = 0.4 * I _{clx} , T _J = 130 °C; Current level 2,3,4 | 1.71 | 1.80 | 1.89 | V |
| | | V _S > 6.5 V, OUTx = I _{clx} , T _J = -40 °C to 150 °C; Current level 2,3,4 | 3.82 | 4.5 | 5.18 | V |
| R _{CF} ⁽²⁾ | CF resistor range | - | 5.1 | - | kΩ | |
| I _{OFFSET} | CF offset current | - | 10 | - | μA | |

1. Measured at a 5.1k resistor between CF and GND (R_{CF}). Levels see [Table 34](#) Current Level (CONFIG_REG).

2. Defined by design, not tested.

Note: This signal has an individual error ±5 % in each of the three currents levels, at trimming temperature of 130 °C. Additional an individual error ±10 % in each of the three current levels over temperature and aging. So the maximum error is of ±15 % in each of the three current levels. The offset and the gain errors may be different in each current level. The adjustment is done at 130 °C and compensates the error corresponding to 0.4 * I_{clx}

Table 15. Current limiting

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------------|---------------------------------------|--------------------------------|--------------------|------|---------------------|---------------|
| $ I_{CL2} ^{(1)}$ | Current limit ₂ | $R_{CF} = 5.1 \text{ k}\Omega$ | 4.25 | 5 | 5.75 | A |
| $ I_{CL3} ^{(1)}$ | Current limit ₃ | | 5.6 | 6.6 | 7.6 | A |
| $ I_{CL4} ^{(1)}$ | Current limit ₄ | | 7.3 | 8.6 | 9.9 | A |
| $ I_{HYS2-4} ^{(1)}$ | Current limit hysteresis ₁ | - | -5% I_{CL2-4} | - | -10% I_{CL2-4} | A |
| t_b | Blanking time | Guaranteed through scan. | 8 | 11 | 15 | μs |
| t_{trans} | Time between two transient | | 90 | - | 130 | μs |

1. Programmable current levels see [Table 34](#) Current Level (CONFIG_REG). Measured using a 5.1 k Ω resistor between CF and GND (R_{CF}).

Table 16. Over-current detection ($8 \text{ V} < V_S < 18 \text{ V}$)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------------|---|-------------------------|------|------|------|---------------|
| $ I_{OC2_LS} ^{(1)}$ | Low side over current threshold ₂ | $V_{DD} = 5 \text{ V}$ | 4.9 | - | 8.2 | A |
| $ I_{OC3_LS} ^{(1)}$ | Low side over current threshold ₃ | $V_{DD} = 5 \text{ V}$ | 6.7 | - | 11.1 | A |
| $ I_{OC4_LS} ^{(1)}$ | Low side over current threshold ₄ | $V_{DD} = 5 \text{ V}$ | 8.4 | - | 14 | A |
| $ I_{OC2_HS} ^{(1)}$ | High side over current threshold ₂ | $V_{DD} = 5 \text{ V}$ | 5.5 | - | 9.2 | A |
| $ I_{OC3_HS} ^{(1)}$ | High side over current threshold ₃ | $V_{DD} = 5 \text{ V}$ | 6.9 | - | 11.5 | A |
| $ I_{OC4_HS} ^{(1)}$ | High side over current threshold ₄ | $V_{DD} = 5 \text{ V}$ | 8.6 | - | 14.4 | A |
| $I_{TRACK-2}^{(2)}$ | $ I_{OC2} - I_{CL2} $ | $V_{DD} = 5 \text{ V}$ | 0.4 | - | 5.5 | A |
| $I_{TRACK-3}^{(2)}$ | $ I_{OC3} - I_{CL3} $ | $V_{DD} = 5 \text{ V}$ | 0.4 | - | 5.5 | A |
| $I_{TRACK-4}^{(2)}$ | $ I_{OC4} - I_{CL4} $ | $V_{DD} = 5 \text{ V}$ | 0.4 | - | 5.5 | A |
| t_{DF} | Delay time for fault detection | guaranteed by design | 1 | 2 | 4.5 | μs |
| t_{DF_off} | Switch-off delay time | - | | | 6 | μs |
| t_{DF_del} | Delayed switch-off time | - | 20 | | 200 | μs |
| t_{SC} | Short-circuit detection | guaranteed through scan | 292 | 350 | 413 | μs |

1. Programmable current levels see [Table 34](#) Current Level (CONFIG_REG).
2. Tracking values are referred for both LS and HS.

Table 17. Open-load detection

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------|--|--------------------------|------|------|------|------------|
| R_{OL} | Open-load detection threshold | - | 5 | - | 50 | k Ω |
| t_{DIAGOL} | Open-load diagnosis enable delay | Guaranteed through scan. | 100 | - | 150 | ms |
| $t_{DIAGOL1}$ | Open-load diagnosis filter time ₁ | | 2.4 | - | 3.6 | ms |
| $t_{DIAGOL2}$ | Open-load diagnosis filter time ₂ | | 200 | - | 300 | μ s |
| V_{out1_OFF} | Out1 voltage regulator | - | 1.67 | - | 1.97 | V |

Note: If the value of the connected load is below 5 k Ω no Open Load is detected; whereas if the value of the connected load is more than 50 k Ω , Open Load is detected. If the load is in the range between (5 to 50) k Ω , the Open Load diagnosis could be not reliable.

Table 18. Retest delay

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------------------|--|--------------------------|------|------|------|---------|
| $t_{delay\ retest}$ | Retest delay for failures: SCB, SCG, SCL | Guaranteed through scan. | 290 | 350 | 410 | μ s |

3.6 Temperature dependent current reduction

Table 19. Temperature dependent current reduction

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------------|--|--------------------------|------|------|------|--------------|
| $ I_{L_TSD} $ | Current limit at T_{SD} | - | 1.4 | 2.5 | 3.6 | A |
| T_{ILR} | Start of temperature dependent current reduction | - | 150 | 165 | - | $^{\circ}$ C |
| T_{SD} | Thermal shut-down | - | 175 | - | - | $^{\circ}$ C |
| $T_{SD}-T_{ILR}$ | Range of temperature dependent current reduction | - | 20 | 25 | 30 | $^{\circ}$ C |
| T_{fTSD} | Thermo-shut-down detection filter time | Guaranteed through scan. | 6 | - | 18 | μ s |

Note: see also [Figure 17: Temperature dependent current reduction](#).

3.7 Free-wheeling diodes

Table 20. Free-wheel diodes

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|----------------|---|------------------------|------|------|------|------|
| U_D | Free-wheeling diode forward voltage | $I_{OUT} = 3\text{ A}$ | - | - | 2 | V |
| $T_{it}^{(1)}$ | Free-wheeling diode reverse recovery time | - | - | - | 100 | ns |

1. Not subject to production test; specified by design.

3.8 SPI / logic electrical characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $4.5\text{ V} \leq V_S \leq 18\text{ V}$, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$; all outputs open; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$, unless otherwise specified.

Table 21. Inputs: SI, SS, SCK, DIR, DIS and PWM; Output: SO

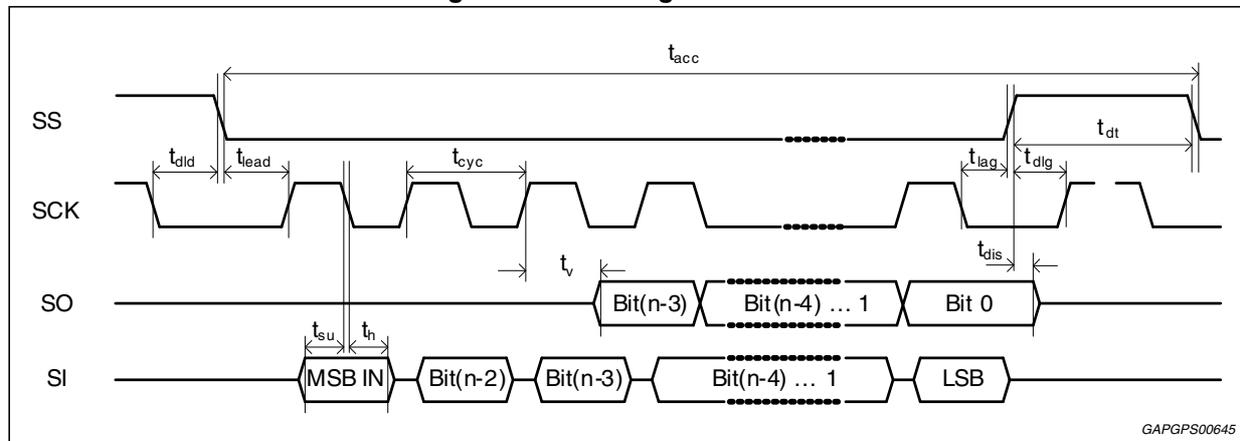
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---------------------------------------|--------------|-----|--------------|---------------|
| Inputs: SI, SS, SCK DIR, PWM | | | | | | |
| V_{IL} | Input voltage low-level | $V_{DD} = 5\text{ V}$ | -0.3 | - | 0.75 | V |
| V_{IH} | Input voltage high-level | $V_{DD} = 5\text{ V}$ | 1.75 | - | $V_{DD}+0.3$ | V |
| V_{IHYS} | Input hysteresis | $V_{DD} = 5\text{ V}$ | 0.2 | - | 1.0 | V |
| R_{PUin} | Input pull-up resistor | $V_{DD} = 5\text{ V}$ | 50 | - | 250 | k Ω |
| I_{INx} | PWM, DIR input current | $V_{INx} > 3.0\text{V}$ | -5 | - | 5 | μA |
| $C_{Slin}^{(1)}$ | SI input capacitance | - | - | - | 10 | pF |
| $C_{SCKin}^{(1)}$ | SCK input capacitance | - | - | - | 10 | pF |
| $C_{SSin}^{(1)}$ | SS Input Capacitance | - | - | - | 15 | pF |
| $C_{DIR,PWM}^{(1)}$ | DIR, PWM input capacitance | - | - | - | 20 | pF |
| Input: DIS | | | | | | |
| R_{DISPU} | Pull-up resistor | $0\text{ V} < V_{DIS} < 2.1\text{ V}$ | 10 | - | 45 | k Ω |
| I_{DISx} | DIS input current | $V_{DIS} > 3\text{ V}$ | -5 | - | 5 | μA |
| $C_{DISin}^{(1)}$ | DIS input capacitance | - | - | - | 20 | pF |
| t_{DIS} | DIS pulse width | - | 0.5 | 1 | 1.5 | μs |
| Input pin disturbance (SI, SS, SCK DIR, PWM,DIS) | | | | | | |
| ΔV_{x_HL} | Change of V_{IH} and V_{IL} during inverse current on V_S | Not subjected to test in production. | -0.1 | - | 0.1 | V |
| ΔI_{Sx} | Change of input current of SPI input pins during inverse current on V_S | | -100 | - | 100 | μA |
| Output: SO | | | | | | |
| V_{SOL} | Output voltage low level | $I_{OL} = 2\text{ mA}$, | 0 | - | 0.4 | V |
| V_{SOH} | Output voltage high level | $I_{OH} = -2\text{ mA}$ | $V_{DD}-0.5$ | - | V_{DD} | V |
| $SR_{SO}^{(1)}$ | Slew rate | $C_{LOAD} = 200\text{ pF}$ | 0.3 | - | 0.6 | V/ns |
| I_{SOLK} | Tristate leakage current | $V_{SS} = V_{DD}$ | -10 | - | 10 | μA |
| $C_{SOout}^{(1)}$ | SO output capacitance | - | - | - | 10 | pF |
| Output pin disturbance (SO) | | | | | | |
| ΔI_{SOLK} | Change of I_{SOLK} during inverse Current on V_S | - | -100 | - | 100 | μA |

1. Not measured in production test. Parameter guaranteed by design.

Table 22. Dynamic characteristics

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|------------|-------------------|--|------|------|------|---------|
| t_{cyc} | Cycle time | - | 490 | - | - | ns |
| t_{lead} | Enable lead time | - | 300 | - | - | ns |
| t_{lag} | Enable lag time | - | 150 | - | - | ns |
| t_v | Data valid | SCK = 2 V; SO = 0.2 V; $C_L = 40$ pF | 40 | - | - | ns |
| | | SCK = 2 V; SO = 0.2 V; $C_L = 200$ pF | 150 | - | - | ns |
| | | SCK = 2 V; SO = 0.2 V; $C_L = 350$ pF | 230 | - | - | ns |
| t_{su} | Data setup time | - | 40 | - | - | ns |
| t_h | Data hold time | - | 40 | - | - | ns |
| t_{dis} | Disable time | - | 0 | - | 100 | ns |
| t_{dt} | Transfer delay | - | 300 | - | - | ns |
| t_{dld} | Disable lead time | - | 250 | - | - | ns |
| t_{dlg} | Disable lag time | - | 250 | - | - | ns |
| t_{acc} | Access time | - | 8.35 | - | - | μ s |

Figure 9. SPI timing information



4 Application information

4.1 Power stage switching behavior

The L9959 output stages can either be controlled by the pins PWM and DIR or by their corresponding SPI registers (SPWM and SDIR: see [Table 33](#) in Configuration Register (CONFIG_REG)). The SPI bit MUX in the configuration register (CONFIG_REG) is used to define the driving control strategy of the H-bridge. If the power stages are disabled by /ABE or DIS, this bit is reset and the pins PWM and DIR control the outputs.

The active free-wheeling, in which the body diode is actively shorted by its associated Power-MOS, can be disabled by the bit **FW** in the configuration register (CONFIG_REG). By default, active free-wheeling is enabled.

The device minimizes electro-magnetic emission by switching the high-side and low-side drivers in a special sequence. Two cases are distinguished: The PWM-mode, during which the current direction does not change and the direction switches using the DIR, which changes the current direction (see [Figure 10](#), [Figure 12](#) and [Figure 13](#)).

4.1.1 PWM mode (same current direction)

The PWM input pin switches the high-/low-side output of the half-bridge, which is selected by the DIR pin.

DIR = '0': OUT1 is switched, DIR = '1': OUT2 is switched.

PWM = '0': Switched low-side is on, PWM = '1': Switched high-side is on.

Figure 10. PWM mode current flow

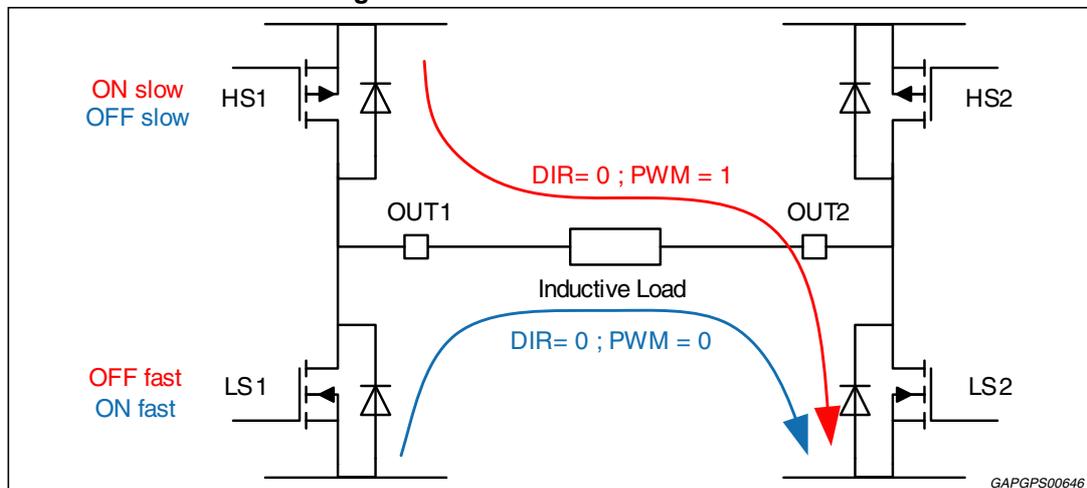
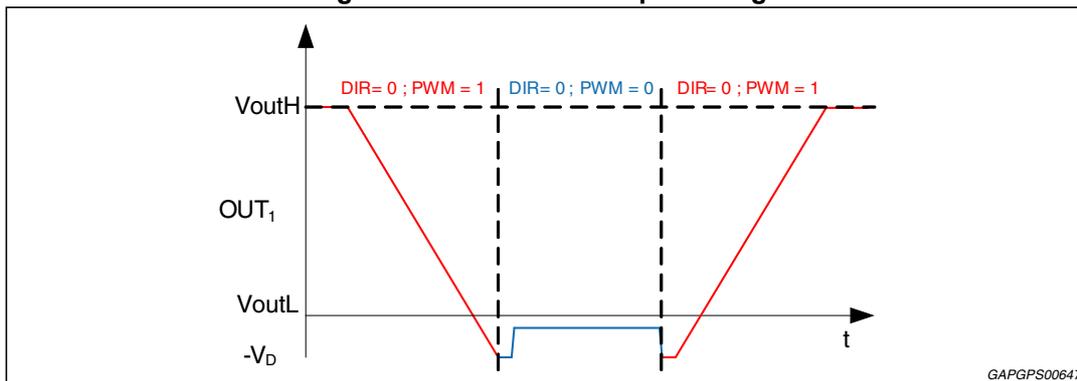


Figure 11. PWM mode output voltage



During PWM mode the high-side (e.g. *Figure 10* HS1) output is switched off with a slow slew rate until it is off and the low-side body-diode has taken over the entire current (passive freewheeling). Then the associated low-side transistor (e.g. *Figure 10* LS1) is turned on with a fast slope to reduce the voltage across the device and to minimize the power.

The output is pulled to high voltage, by first turning off the low-side driver with a fast slew rate and, after it is off, the high-side driver is switched on by a slow one (e.g. *Figure 10* LS1, HS1).

This assures, that the voltage and current change over the body diode is done smoothly, reducing the electromagnetic emission.

4.1.2 DIR-change mode

The first part of the sequence is identical to the PWM-mode (s.a.). After this has been finished and the associated low-side driver is on (e.g. *Figure 12* LS1), in phase 1 the other low-side driver is turned on (e.g. *Figure 12* LS2) to enter passive freewheeling phase. Then in phase 2 the low-side output of OUT2 is switched-off slowly and the current through the load is taken over by the body-diode of the high-side (e.g. *Figure 13* HS2).

Depending on the inductance of the load, the current vanishes more or less quickly. After the low-side driver is turned off, the high-side is switched on with a slow slew-rate.

This assures, that direction switch occurs while the current over the load has vanished, which reduces the electromagnetic emission.

Figure 12. DIR-change (current is changing its direction)

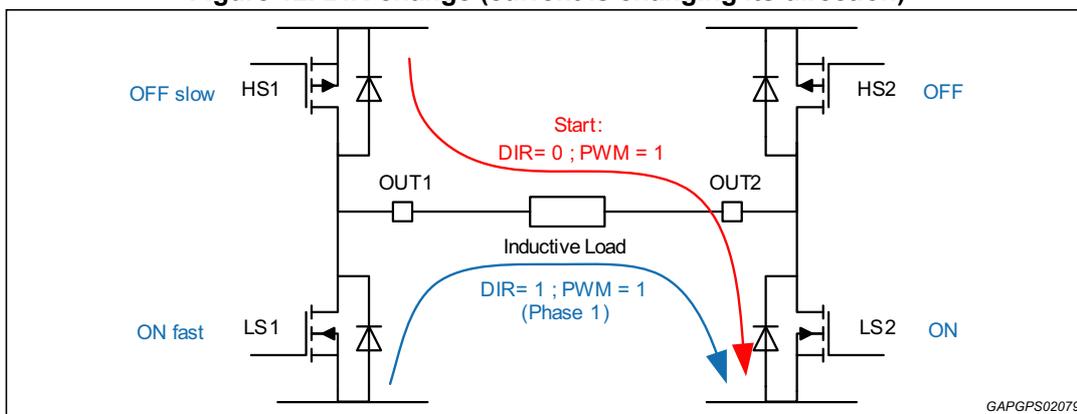


Figure 13. DIR-change current flow phase 2

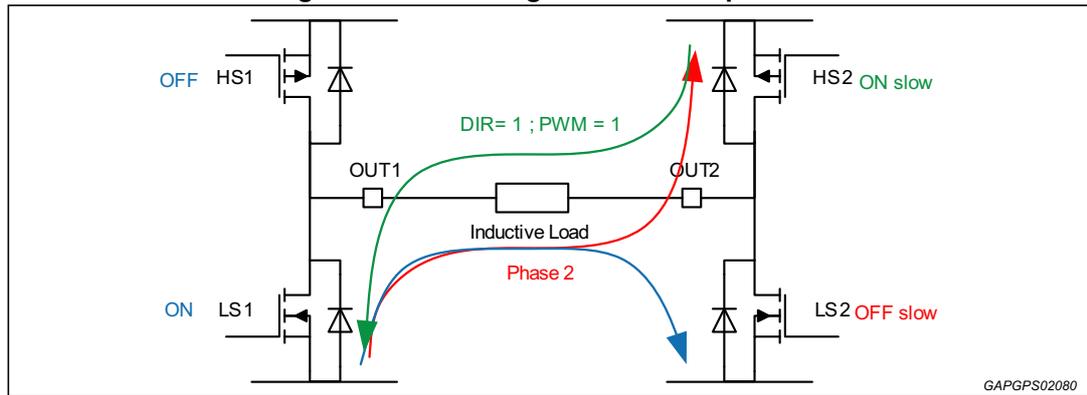
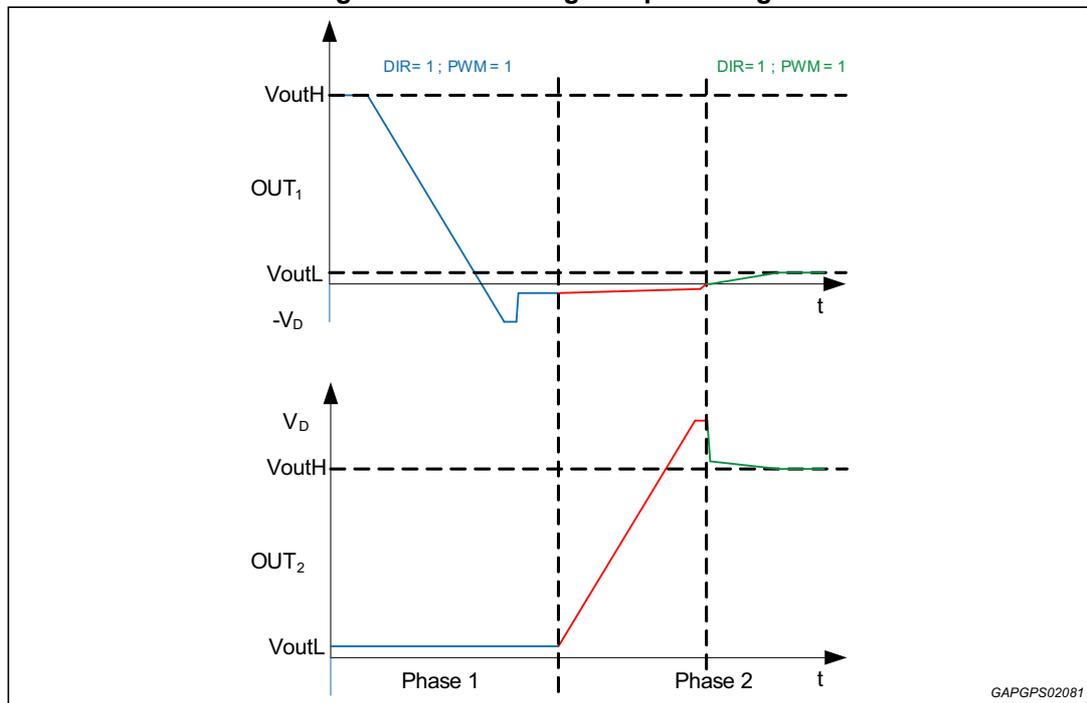


Figure 14. DIR-change output voltage



4.2 Protection and monitoring

A set of failure as Short-circuit to Ground (SCG), Short-circuit to battery (SCB) and Short-circuit to load (SCL) errors (SBC, SCG, SCL) are confirmed after their occurrence by accessing the error condition after time $t_{\text{delay_retest}}$ a second time. Only after the error is confirmed, it is entered into the diagnosis register 1 (DIA_REG1), and the device is disabled and no further diagnosis is run.

The device can be enabled again by the following actions: Power-on reset, disabling and enabling the device using the pins /ABE or DIS (e.g. disabling - enabling sequence). The diagnosis registers can be cleared by sending a reset command by SPI (**STATCON_REG**) to either diagnosis register 1 (**DIA_REG1**) or 2 (**DIA_REG2**). The bit1 (Reset) of the CONFIG_REG if forced to zero resets both the device registers configuration and diagnosis registers to default but is not able to restart the device. In order to restart IC it is necessary

to force a transition **LOW/HIGH/LOW** on DIS pin or a transition **HIGH/LOW/HIGH** on /ABE pin.

The errors in the diagnosis register 1 (DIA_REG1) are transferred to the diagnosis register 2 by setting the bit DIACLR1 in the status and configuration register (STATCON_REG) or by using the enabling -disabling sequence on /ABE or DIS. This will also clear the diagnosis register 1.

4.2.1 Current feedback

A feedback current signal is provided at pin CF (Current Feedback). This current is proportional to the current in the H-Bridge, but does not change its direction. It is measured in the low-side transistor, which is not switched by PWM. This is determined by the input DIR or the SDIR register respectively. Therefore, the direction of the current can be seen from this direction signal.

One current sense monitoring circuit is present and it is connected to the output of the active LS driver (DIR change mode).

After the DIR transition, the LSx reference output is switched only in the phase in which both LS drivers are active for recirculation.

In the time-frame between HS turn-off and the start of active freewheeling, (including dead time and passive freewheeling), the current sense monitors the current flowing in the previous active LS driver.

This time-frame is not fixed but adaptative to real operative conditions (battery and selected slew rate mode).

In *Table 14: Current feedback (CF)* the CF behavior over an external resistor of 5.1k Ohm is specified. The current out of CF consists of a static offset current and a current proportional to the current in the select low-side transistor. The voltage at pin CF scales with the resistor at this pin.

Figure 15. Current feedback and current limiting

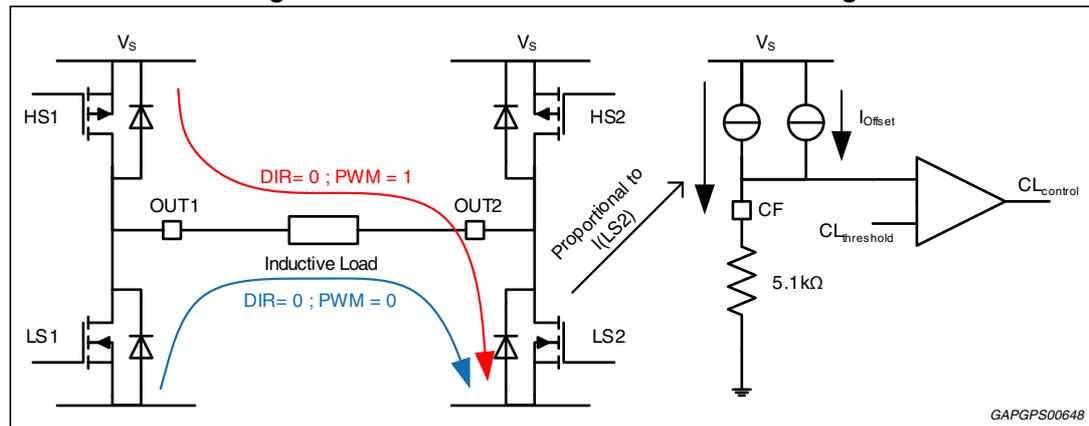


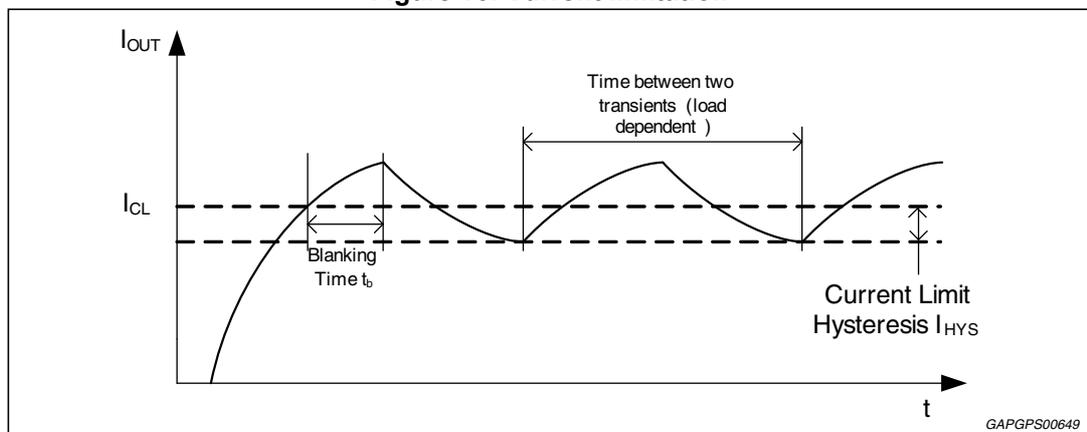
Figure 15 Current Feedback and Current Limiting shows the current feedback in case the OUT1 is controlled by PWM (DIR = 0). In this case, the current is measured through low-side 2. If the direction is inverted, the current is measured through low-side 1.

4.2.2 Current limitation

The H-Bridge output current can be limited to three different values (see [Table 15: Current limiting](#)). If the current reaches the current limiting threshold I_{CL} , the output driver is switched off after the blanking time t_b , and switched on again after the current dropped below the lower current limit hysteresis threshold ($I_{CL} - I_{HYS}$). The current limiting thresholds can be adjusted using the resistor at pin CF. The values in [Table 15](#) refer to a 5.1k Ohm external resistor. The current limiting threshold can be calculated by $(4.5V/R_{CF} - I_{OFFSET}) * (I_{CLX} * 5.1k / 4.45V)$ from [Table 15](#) and $I_{OFFSET} = 10\mu A$ (typical). R_{CF} is the resistor used at pin CF.

The overcurrent threshold is not changed by R_{CF} (see [Table 16](#)). The current limitation is active as long as the output driver is switched on. The information that the device is in current limitation is stored in the diagnosis register 2 (**DIA_REG2**).

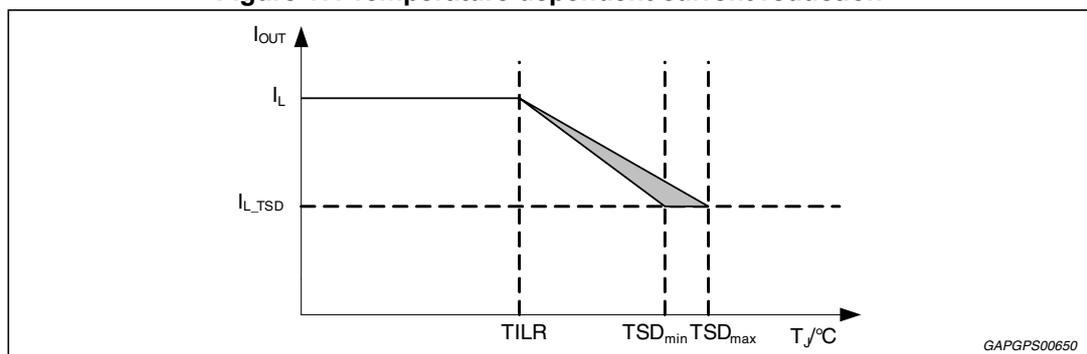
Figure 16. Current limitation



4.2.3 Temperature dependent current reduction

If the device reaches the temperature **TILR**, the current will be reduced (see [Figure 17: Temperature dependent current reduction](#)). If the temperature reaches the temperature shutdown threshold **TSD**, the outputs are switched off. The current limitation information is written into the diagnosis register 2 (**DIA_REG2**).

Figure 17. Temperature dependent current reduction



4.2.4 Short to battery (SCB) and short to Ground (SCG)

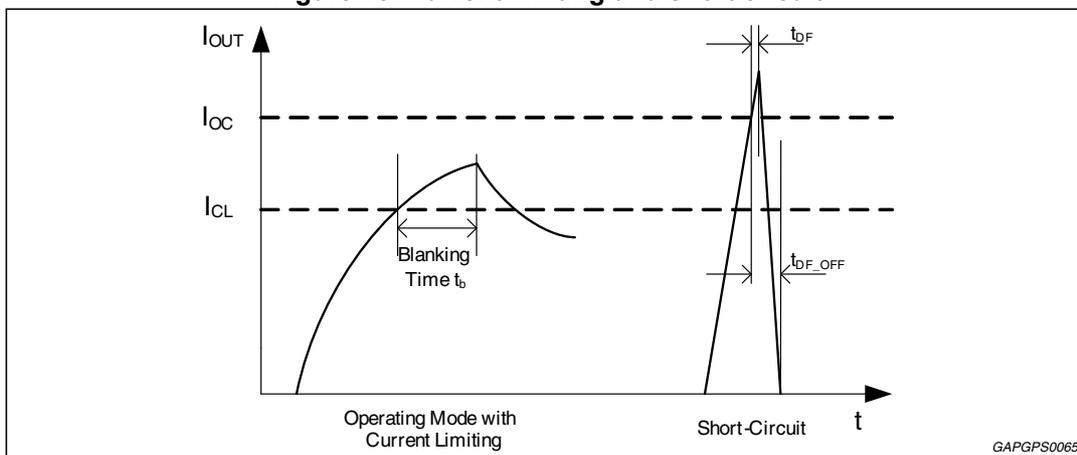
While the power stages are on, the current through them is monitored. If the output current reaches the current limit I_L , the output is switched off after the blanking time t_b . In case the current reaches the limit I_{OC} during this time, a short to battery (SCB) on low-sides or a short to ground (SCG) on high-sides is diagnosed, and the affected output driver is switched off immediately, the not affected one after the time t_{DF_del} .

In order to confirm this error, the outputs are turned on again. If the error is detected for the second time, it is confirmed but it is still not possible to determine to which of the following types belongs to:

- SCB and SCL
- SCG and SCL

To discriminate the fault type, it is necessary to turn outputs on for the third time, and in case the fault is detected, the diagnosis register (DIA_REG1) is updated consequently and the device is disabled. Otherwise, the SCG and SCB faults are confirmed only.

Figure 18. Current limiting and short circuit



The three different over-current limits are related to the programmable current limitation, which can be programmed into the SPI register ([Table 33: Configuration register \(CONFIG_REG\)](#)). The over-current limits are independent of the resistor at pin CF.

Note: SCG: Fault Detection works correctly if the following condition is respected: $Duty (switch\ on\ time) > T_{don} + Slew\ rate + t_{DF}$.

4.2.5 Short circuit over load (SCL)

Short circuit over load (SCL) is diagnosed by a retest sequence after a short to battery (SCB) or a short to ground (SCG) has been detected and confirmed by a retry on the switched-on high-side and low-side driver. Then after the time t_{retest} , the opposite driver is switched off (i.e. the high-side in case of a short to battery on the low-side and vice versa). If the failure then disappears, a short over load (SCL) is detected.

The error is only entered into the diagnosis register and the device is disabled, if it is confirmed.

4.2.6 Open load (OL)

Open load can either be detected in active mode or while the output drivers are in a tri-state condition, disabled by DIS or /ABE. Open load in active mode is enabled by setting the **OLDA** in the configuration register (CONFIG_REG).

Open load in active mode

With OLDA = '1', the open load condition can only be diagnosed if an inductive load is used. In normal operation, the output free wheels via the built-in diodes below ground, if the high-side output driver is switched-off. If the output does not go below ground, an open load is detected. It is possible to enable the filter OLDAFILTER by setting the dedicated bit 4 in SPECIAL_REG (0 or 40ms). With OLDAFILTER = '1', the open-load will be rechecked at the next PWM cycle and if detected again, the failure will be confirmed in DIAG_REG1 (and latched).

In case OLDAFILTER is set at '0' (40ms) the recheck will be executed after the filter time expiration and next PWM pulse. If detected again, the failure will be confirmed (and latched).

Note: For Open-load in active mode L9959 works properly in case the duration of the transient conditions is less than 40msec (Transient condition: function of starting current, ending current, load electrical parameters, DC MOTOR mechanical characteristics...).

Open load in inactive mode

In inactive mode the open load is independent from the OLDAFILTER status (don't care condition) and it is detected by applying a pull-down current (I_{PD}) to both outputs.

A pull-up current is generated at one output to compensate these two output currents.

If the pull-up current is in the range of one pull-down current, an open load is diagnosed.

If the load is connected, the pull up current is in the range of the sum of both pull-down currents.

An open load is detected, if the load resistance is above the open load resistance threshold; no open load is detected, if it is below this threshold (R_{OL}).

After the outputs are disabled, it takes the time t_{DIAGOL} until the open load diagnostic can be enabled. The open load settling time to reach the correct pull up current is $t_{diagOL1}$, the open load filter time is $t_{diagOL2}$.

4.3 VS-undervoltage

VS is monitored for under-voltage. If VS goes below the VS-undervoltage threshold, the outputs are switched to tristate after the time t_{FUV} .

4.4 Inverse current at V_S

An inverse current of maximum 5 A, which decreases during a period of max 250 ms out of the device at VS does not lead to any destruction. After the exposure to such an inverse current the device returns to the specified functionality.

4.5 /ABE pin

/ABE (Ability/Enable) is a bidirectional pin, with an open-drain output. In normal operating condition, this pin is pulled up by an external resistor. If /ABE is set to low, the outputs enter tristate mode.

/ABE can be used to switch off the outputs quickly by an external signal. It is possible to connect the /ABE pins of several devices together, so all of them can be disabled in case one detects an error, which is flagged by the /ABE pin.

4.6 VDD-monitor

V_{DD} is monitored for under- and over-voltage referenced to GND_{ABE} .

If V_{DD} goes below V_{DD_THL} or above V_{DD_THH} , /ABE is pulled to low and the outputs enter tristate mode after the time t_{FIL_OFF} . The VDD-monitoring state is stored into the status and control register (STACON_REG).

If VDD increases above V_{DD_THL} , /ABE is pulled to high after the filter time t_{FIL_ON} . The SPI remains functional as long as V_{DD} is above the power-on reset threshold.

The behavior of the pin /ABE and the output stages after VDD goes below V_{DD_THH} from VDD-over-voltage is determined by bit CONFIG 0 in the status and configuration register (STATCON):

CONFIG0 = 1: /ABE is latched and the outputs remain in tristate

CONFIG0 = 0: /ABE goes to inactive and the output stages are enabled after the filtering time t_{FIL_ON} .

4.7 VDD-monitor test

VDD-Monitor blocks can be tested in the application via SPI. During this test, the output stages are still switched off in case of over- and under-voltage.

Upper threshold

The over-voltage threshold can be reduced using the configuration registers 1 and 2 (CONFIG1 and CONFIG2) in the status and control register (STACON_REG) to V_{TEST_THH} (see [Table 35: Status and configuration register \(STATCON_REG\)](#)). Since V_{TEST_THH} is below the normal VDD voltage, the status bit STATUS0 shows a VDD over-voltage.

Lower threshold

The under-voltage threshold can be increased to V_{TEST_THL} using CONFIG1 and CONFIG2 in the STATCON register. Since the VDD voltage is below V_{TEST_THL} , the resulting VDD-undervoltage resets STATUS0.

After leaving the VDD-monitor test mode, the bits in the STACON register return to their normal state.

4.8 Power-on reset

At power-on, while VDD increases, the internal registers are cleared and the outputs are set to tristate at the reset-active voltage V_{DDRES} . Above the power-on reset threshold V_{DDPOR} the device starts to operate after the time t_{POR} . If VDD drops below V_{DDPOR} , the device enters its reset state, i.e. all internal registers are cleared and the outputs are set to tristate.

Table 23. Device states with respect to supply voltage

| V_S [V] | V_{DD} [V] | Functional state |
|------------------|--------------------|--|
| 28 – 40 | 0 – 18 | No damage to the device, no functional behavior guaranteed |
| 4.5 – 6.5 | 4.5 – 5.5 | Device functional, Current Feedback accuracy reduced |
| 6.5 – 28 | 4.5 – 5.5 | Device functional |
| 4.5 – 28 | 4.0 – 4.5 5.5 - 18 | Device functional, but power-outputs tristate by V_{DD} -monitor, /ABE pulled to low, SPI functional |
| 0 – 4.5 4.5 – 28 | V_{DDPOR} – 4.5 | Device in reset mode, SPI functional, power-outputs tristate, /ABE pulled to low |
| 0 – 4.5 4.5 – 28 | 2.5 - V_{DDPOR} | Device in reset mode, SPI reset, power-outputs tristate, /ABE tristate |
| 0 – 4.5 | 4.5 – 5.5 | Device functional, outputs are tristate by V_S -undervoltage |
| 0 – 4.5 | 4.0 – 4.5 5.5 - 18 | Device functional, outputs are tristate by V_S -undervoltage and V_{DD} -monitor, /ABE pulled to low |

Note: All voltages are nominal. Please refer to [Section 3: Electrical specifications](#) for their specified values.

5 SPI functional description

5.1 General description

The SPI communication is based on a Serial Peripheral Interface structure using SS (SPI Select), SI (Serial Data In), SO (Serial Data Out) and SCK (Serial Clock) signal lines. The first data at pin SI is latched into the device with the first falling edge of the clock SCK after the clock has changed from low to high, which is the second edge after SPI-Select has been pulled to low.

5.1.1 SPI select (SS)

The SS input pin is used to select the serial interface of this device. When SS is high, the output pin (SO) is in high impedance state. A low signal starts the serial communication. A communication frame is the time between the falling edge of SS and its rising edge.

5.1.2 Serial data In (SI)

The SI input pin is used to transfer data serially into the device. The data applied to the SI is sampled at the falling edge of the SCK signal.

5.1.3 Serial clock (SCK)

The Data Input (SI) is latched at the falling edge of Serial Clock SCK. Data on Serial Data Out (SO) is shifted out at the rising edge of the serial clock (SCK). The serial clock SCK must be active only during a frame (SS low).

5.1.4 Serial out (SO)

The content of the selected status or control register is transferred out of the device using the SO pin on the rising edge of SCK. Each subsequent rising edge of the SCK will shift the next bit out.

5.1.5 SPI communication flow

The SPI communication is started by sending an SPI instruction to the device beginning with the MSB. The first two bits of this instruction are used as a device identifier (see [Table 24: SPI instruction byte](#)). Whether the transfer is a read or a write access is determined by the SPI command (see [Table 26: Command overview](#)). The SPI data is transmitted from the device at the same time as the data is received, although on different SCK edges. While the 8-bit instruction is sent, the device responds with the check byte. Since the first two bits of the instruction are used as a device identifier, the first two bits of the check byte are tristate. This avoids bus conflicts on the SO line. During a write access, the 8-bit data byte is received after the instruction byte. The device responds with **00_H**. In a read cycle the device sends the 8-bit data, while the receive data bits are ignored (see [Figure 19: Write access](#) and [Figure 20: Read access](#)). If an invalid instruction is detected, the register of the device are not modified and the data byte **FF_H** is transmitted instead of the data or **00_H** respectively. The bit **TRANS_F** in the check byte is set in case of an invalid instruction and transmitted during the next SPI-access. An instruction is invalid, if an unused instruction code is detected, the previous transmission has not been completed or the number of clocks is not equal to 16.

Figure 19. Write access

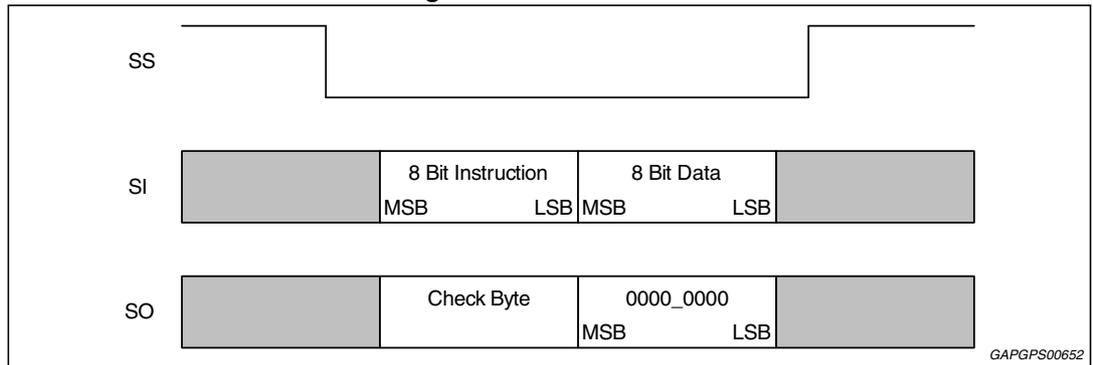
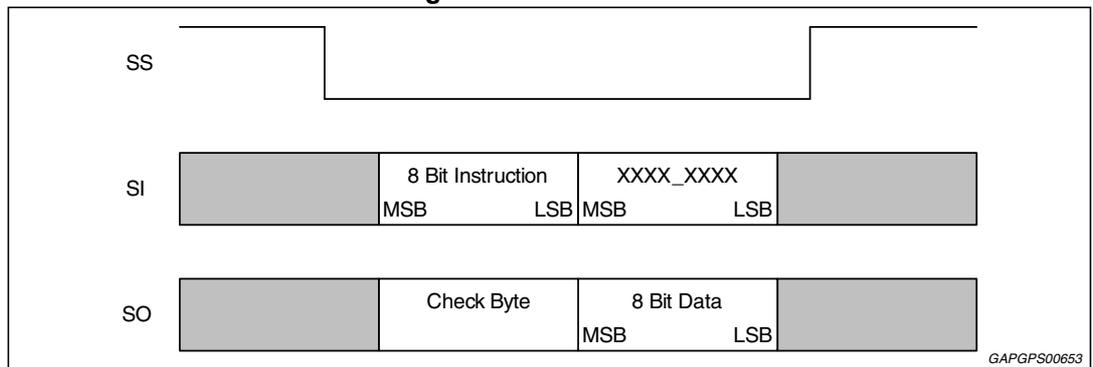


Figure 20. Read access



5.2 SPI-instruction

Table 24. SPI instruction byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----------|------------------------------|---------|---------|---------|---------|---------|---------|
| Name | CPAD1 | CPAD0 | INST<5> | INST<4> | INST<3> | INST<2> | INST<1> | INST<0> |
| Bit | Name | Content | | | | | | |
| 7 | CPAD1 | Chip Address: 0 | | | | | | |
| 6 | CPAD0 | Chip Address: 0 | | | | | | |
| 5 | INST<5> | Read/Write: Read: 0 Write: 1 | | | | | | |
| 4:0 | INST<4:0> | SPI Instruction | | | | | | |

Table 25. Check byte

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|--|---|---|---|---|---|---------|
| Name | Tristate | Tristate | 1 | 0 | 1 | 0 | 1 | TRANS_F |
| Bit | Name | Content | | | | | | |
| 7:6 | Tristate | Tristate | | | | | | |
| 6:1 | | Fix Content: 10101 | | | | | | |
| 0 | TRANS_F | Transfer-Failure Invalid instruction TRANS_F = 1 | | | | | | |

5.3 Device register map

Table 26. Command overview

| Command | INST<5:0> | Content |
|------------|-----------|--|
| RD_ID | 00_0100 | Read Device ID |
| RD_REV | 00_0110 | Read Device Revision |
| RD_DIA1 | 01_0000 | Read Diagnostic Information Register 1 |
| RD_DIA2 | 01_1000 | Read Diagnostic Information Register 2 |
| RD_CONFIG | 00_1000 | Read Configuration |
| RD_STATCON | 00_1100 | Read VDD Monitoring Status |
| RD_SPECIAL | 00_1110 | Read information from SPECIAL |
| WR_DIA1 | 11_0000 | Write to Diagnostic Information Register 1 |
| WR_DIA2 | 11_1000 | Write to Diagnostic Information Register 2 |
| WR_CONFIG | 10_1000 | Write Configuration |
| WR_STATCON | 10_1100 | Write VDD Monitoring Status |
| WR_SPECIAL | 10_1110 | Write information to SPECIAL |
| All Other | - | Invalid Command: TRANS_F: 1 |

5.4 SPI - control and status registers

Table 27. Device identifier (ID)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------|-----------------------|-------|-------|-------|-------|-------|-------|
| Name | ID<7> | ID<6> | ID<5> | ID<4> | ID<3> | ID<2> | ID<1> | ID<0> |
| Bit | Name | Content | | | | | | |
| 7:0 | ID<7:0> | Device ID: DFH | | | | | | |

Table 28. Revision register (REV)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------|--|--------|--------|--------|--------|--------|--------|
| Name | SWR<3> | SWR<2> | SWR<1> | SWR<0> | MSR<3> | MSR<2> | MSR<1> | MSR<0> |
| Bit | Name | Content | | | | | | |
| 7:4 | SWR<3:0> | Software Revision: 0H | | | | | | |
| 3:0 | MSR<3:0> | Mask Set Revision: 06H ⁽¹⁾ | | | | | | |

1. Here below the Mask set revision:

00H - AA
 01H - BA
 02H - CA
 03H - CB
 04H - DA
 05H - DB
 06H - DC

Table 29. DIA_REG1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|------------|--|-----|-----|-------|-------|-------|-------|
| Name | /ABE / DIS | OT | Res | Res | DIA21 | DIA20 | DIA11 | DIA10 |
| Bit | Name | Content | | | | | | |
| 7 | /ABE / DIS | H-bridge Disable: 0, if /ABE = 0 or DIS = 1 | | | | | | |
| 6 | OT | Over temperature: 0:OT, 1: no OT | | | | | | |
| 5:4 | Reserved | 0 | | | | | | |
| 3 | DIA21 | Diagnose Bits (<i>Table 30: Diagnosis bits (DIA_REG1)</i>) | | | | | | |
| 2 | DIA20 | | | | | | | |
| 1 | DIA11 | | | | | | | |
| 0 | DIA10 | | | | | | | |
| Reset ^(5.4.1) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POR | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| SPIR | X | 1 | X | X | 1 | 1 | 1 | 1 |
| ENDISR | X | 1 | X | X | 1 | 1 | 1 | 1 |
| RDR | X | X | X | X | X | X | X | X |
| DIACL1 | X | 1 | X | X | 1 | 1 | 1 | 1 |

Table 30. Diagnosis bits (DIA_REG1)

| DIA21 | DIA20 | DIA11 | DIA10 | Description | Remark |
|-------|-------|-------|-------|---|-------------|
| 0 | 0 | 0 | 1 | Short Circuit to Ground at OUT1 (SCG1) | Latched |
| 0 | 0 | 1 | 0 | Short Circuit to Ground at OUT2 (SCG2) | Latched |
| 0 | 1 | 0 | 1 | Short Circuit to Battery at OUT1 (SCB1) | Latched |
| 0 | 1 | 1 | 0 | Short Circuit to Battery at OUT2 (SCB2) | Latched |
| 0 | 1 | 1 | 1 | Short Circuit over Load (SCL) | Latched |
| 1 | 0 | 0 | 0 | Short Circuit to Battery at Disabled Output | Latched |
| 1 | 0 | 0 | 1 | Short Circuit to Ground at Disabled Output | Latched |
| 1 | 0 | 1 | 0 | Open Load at disabled or active Output (OL) | Latched |
| 1 | 1 | 0 | 1 | Under Voltage at VS | Not Latched |
| 1 | 1 | 1 | 1 | No Failure | - |

Note: Reading this register does not reset the bits. Writing STACON_REG.DIACLR1 = 0 transfers all latched errors to DIA_REG2 and resets DIA_REG1 afterwards, if there is no VS-undervoltage.

Table 31. Diagnosis register 2 (DIA_REG2)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---------|--|----|-----|-------|-------|-------|-------|
| Name | CurrRed | CurrLim | OT | Res | DIA21 | DIA20 | DIA11 | DIA10 |
| Bit | Name | Content | | | | | | |
| 7 | CurrRed | Current Reduction: 0, if temperature dependent current reduction is active This information bit is reset after each read access | | | | | | |
| 6 | CurrLim | Current Limitation: 0, if current limitation is active This information bit is reset after each read access | | | | | | |
| 5 | OT | Over temperature 1 no over-temperature 0 over-temperature | | | | | | |
| 4 | Res | Reserved, 0 | | | | | | |
| 3 | DIA21 | Diagnosis Bits (see Table 32: Diagnosis bits (DIA_REG2)) | | | | | | |
| 2 | DIA20 | | | | | | | |
| 1 | DIA11 | | | | | | | |
| 0 | DIA10 | | | | | | | |
| Reset ^(5.4.1) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POR | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| SPIR | 1 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| ENDISR | 1 | 1 | X | X | X | X | X | X |
| RDR | 1 | 1 | X | X | X | X | X | X |
| DIACLR2 | 1 | 1 | 1 | X | 1 | 1 | 1 | 1 |

Table 32. Diagnosis bits (DIA_REG2)

| DIA21 | DIA20 | DIA11 | DIA10 | Description | Remark |
|-------|-------|-------|-------|---|---------|
| 0 | 0 | 0 | 1 | Short Circuit to Ground at OUT1 (SCG1) | Latched |
| 0 | 0 | 1 | 0 | Short Circuit to Ground at OUT2 (SCG2) | Latched |
| 0 | 1 | 0 | 1 | Short Circuit to Battery at OUT1 (SCB1) | Latched |
| 0 | 1 | 1 | 0 | Short Circuit to Battery at OUT2 (SCB2) | Latched |
| 0 | 1 | 1 | 1 | Short Circuit over Load (SCL) | Latched |
| 1 | 0 | 0 | 0 | Short Circuit to Battery at Disabled Output | Latched |
| 1 | 0 | 0 | 1 | Short Circuit to Ground at Disabled Output | Latched |
| 1 | 0 | 1 | 0 | Open Load at disabled or active Output (OL) | Latched |
| 1 | 1 | 1 | 1 | No Failure | - |

Table 33. Configuration register (CONFIG_REG)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|-------|--|------|------|-----|-----|-------|------|
| Name | FW | MUX | SPWM | SDIR | CL1 | CL2 | RESET | OLDA |
| Bit | Name | Content | | | | | | |
| 7 | FW | Free-Wheeling mode selection 0: FW via Body Diode; 1: FW with active short of Body Diode | | | | | | |
| 6 | MUX | Multiplex Bit for H-bridge control strategy: 0: control by bits SPWM and SDIR; 1: Control by inputs PWM and DIR | | | | | | |
| 5 | SDIR | SPI control for Direction: Same as input DIR | | | | | | |
| 4 | SPWM | SPI control for PWM: Same as input PWM | | | | | | |
| 3 | CL1 | See Table 34: Current Level (CONFIG_REG) . | | | | | | |
| 2 | CL2 | | | | | | | |
| 1 | RESET | Reset: 0: Reset of device configuration to default; 1: No change | | | | | | |
| 0 | OLDA | Open-Load Diagnosis in active mode: 1: OLD A is enabled; 0: OLD A is disabled | | | | | | |
| Reset ^(5.4.1) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POR | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| SPIR | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| ENDISR | X | X | X | X | X | X | 1 | X |
| RDR | X | X | X | X | X | X | 1 | X |

Table 34. Current Level (CONFIG_REG)

| CL1 | CL2 | Current Level | Typical Current |
|-----|-----|-------------------|-----------------|
| 0 | 0 | No Change | No Change |
| 0 | 1 | 2 | 5.0 A |
| 1 | 0 | 3 (default value) | 6.6 A |
| 1 | 1 | 4 | 8.6 A |

Table 35. Status and configuration register (STATCON_REG)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---------|---|---------|---------|---------|---------|---------|---------|
| Name | CONFIG2 | CONFIG1 | CONFIG0 | DIACLR2 | DIACLR1 | STATUS2 | STATUS1 | STATUS0 |
| Bit | Name | Content | | | | | | |
| 7 | CONFIG2 | VDD Test Threshold: 0: VDD Threshold Test is on 1: VDD Threshold test is off | | | | | | |
| 6 | CONFIG1 | VDD Test Threshold: 1: Lower VDD Test Threshold is lifted 0:Upper VDD Test Threshold is lowered | | | | | | |
| 5 | CONFIG0 | VDD Over-Voltage Latch: 0: Latch is disabled 1: Latch is enabled | | | | | | |
| 4 | DIACLR2 | Reset DIA_REG2: 0: Reset errors in DIA_REG2 1: No action (Reading this bit always returns „1.) | | | | | | |
| 3 | DIACLR1 | Transfer Errors: 0: All latched errors of DIA_REG1 are transferred to DIA_REG2. DIA21,DIA20, DIA11, DIA10are set to “1111”. During VS-Undervoltage DIACLR1 is disabled 1: No action (Reading this bit always returns „1.) | | | | | | |
| 2 | STATUS2 | Logic Level at Pin /ABE | | | | | | |
| 1 | STATUS1 | VDD Under-Voltage: 0: Under-Voltage 1: No Under-Voltage | | | | | | |
| 0 | STATUS0 | VDD Over-Voltage: 0: Over-Voltage 1: No Over-Voltage This information is not reset during VS-Undervoltage. It will be reset by CONFIG0, SPI reset or internal VDD reset | | | | | | |
| Reset ^(5.4.1) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POR | 1 | 1 | 0 | 1 | 1 | X | X | X |
| SPIR | 1 | 1 | 0 | 1 | 1 | X | X | X |
| ENDISR | X | X | X | 1 | 1 | X | X | X |
| RDR | X | X | X | 1 | 1 | X | X | X |

Note: Only the bits ‘CONFIG’ and ‘DIACLR’ in this register can be written, all other bits are ‘read-only’

Table 36. Special register (SPECIAL_REG)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---------------|--|---|------------|---------------|----|---------------|----------|
| Name | Not specified | | | OLDAFILTER | Not specified | SR | Not specified | SPRCSPEC |
| Controller access: write-access: WR_SPECIAL read-access: RD_SPECIAL | | | | | | | | |
| Bit | Name | Content | | | | | | |
| 7 | Not specified | - | | | | | | |
| 6 | Not specified | - | | | | | | |
| 5 | Not specified | - | | | | | | |
| 4 | OLDAFILTER | Open-load filter in active mode only. OLDAFILTER is a don't care in case of Off state 1: open-load in on detected after one retry 0: openload in on detected after 40 ms | | | | | | |
| 3 | Not specified | - | | | | | | |
| 2 | SR | Voltage SR selection 1: fast slew rate 0: slow slew rate | | | | | | |
| 1 | Not specified | - | | | | | | |
| 0 | SPRCSPEC | SPREADSPECTRUM mode selection 1: spread spectrum = active 0: spread spectrum = disabled Spread spectrum = active provides the internal state machine with slightly jittering clock. Spread spectrum = disabled. The internal state machine runs with constant clock frequency. | | | | | | |
| Reset (5.4.1) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POR | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| SPIR | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| ENDISR | X | X | X | X | X | X | X | X |
| RDR | X | X | X | X | X | X | X | X |

5.4.1 Reset sources

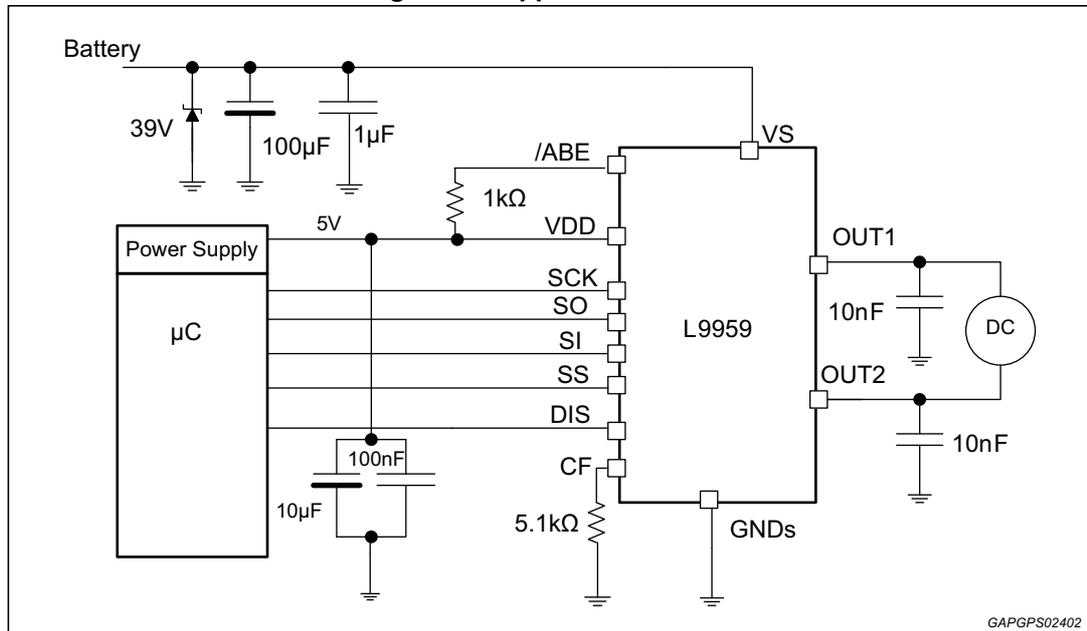
- POR: Reset due to a VDD power up on VDD (Power-Up Reset)
- ENDISR: Reset caused by an enable or disable of the power stages (DIS or /ABE edge triggered) (Enable-/Disable Reset)

5.4.2 Configuration registers reset sources

- POR: Reset due to a VDD power up on VDD (Power-Up Reset)
- SPIR: Reset by setting bit **RESET** in the configuration register (CONFIG_REG) (SPIReset)
- RDIR: Reset caused by a read access to the corresponding register (Read Register)
- DIACLR1: Reset by setting bit DIACLR1 in the Status and Configuration Register STATCON (Diagnosis Reset 1)
- DIACLR2: Reset by setting bit DIACLR2 in the Status and Configuration Register STATCON (Diagnosis Reset 2)

6 Application circuit

Figure 21. Application circuit



GAPGPS02402

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

7.1 PowerSSO-24 (exposed pad) package information

Figure 22. PowerSSO-24 (exposed pad) package outline

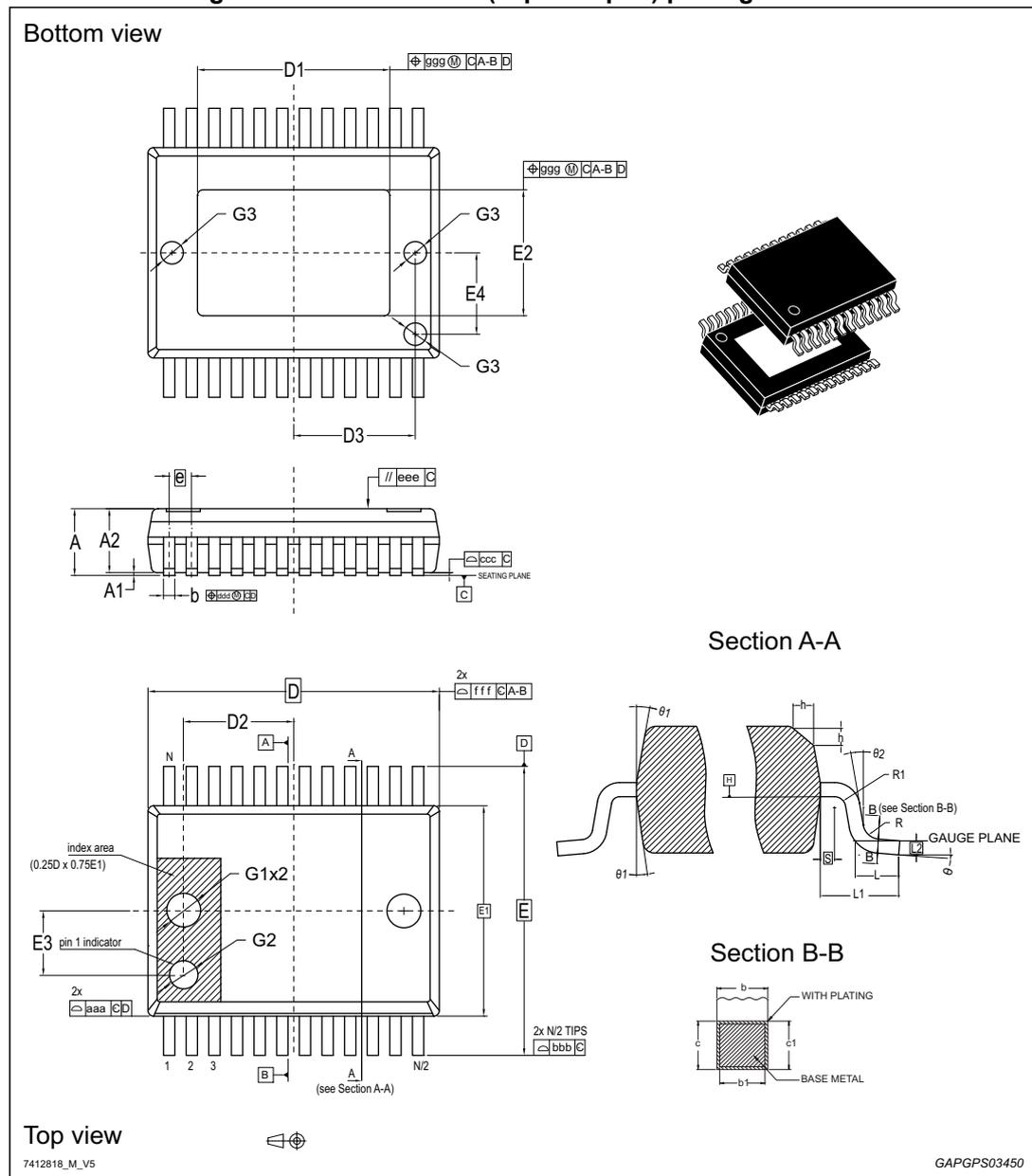


Table 37. PowerSSO-24 (exposed pad) package mechanical data

| Ref | Dimensions | | | | | |
|-------------------|-------------|------|------|-----------------------|--------|--------|
| | Millimeters | | | Inches ⁽¹⁾ | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| Θ | 0° | - | 8° | 0° | - | 8° |
| Θ1 | 5° | - | 10° | 5° | - | 10° |
| Θ2 | 0° | - | - | 0° | - | - |
| A | - | - | 2.45 | - | - | 0.0965 |
| A1 | 0.0 | - | 0.1 | 0.0 | - | 0.0039 |
| A2 | 2.15 | - | 2.35 | 0.0846 | - | 0.0925 |
| b | 0.33 | - | 0.51 | 0.013 | - | 0.0201 |
| b1 | 0.28 | 0.40 | 0.48 | 0.011 | 0.0157 | 0.0189 |
| c | 0.23 | - | 0.32 | 0.0091 | - | 0.0126 |
| c1 | 0.20 | 0.20 | 0.30 | 0.0079 | 0.0079 | 0.0118 |
| D ⁽²⁾ | 10.30 BSC | | | 0.4055 BSC | | |
| D1 | VARIATION | | | | | |
| D2 | - | 3.65 | - | - | 0.1437 | - |
| D3 | - | 4.30 | - | - | 0.1693 | - |
| e | 0.80 BSC | | | 0.0315 BSC | | |
| E | 10.30 BSC | | | 0.4055 BSC | | |
| E1 ⁽²⁾ | 7.50 BSC | | | 0.2953 BSC | | |
| E2 | VARIATION | | | | | |
| E3 | - | 2.30 | - | - | 0.0906 | - |
| E4 | - | 2.90 | - | - | 0.1142 | - |
| G1 | - | 1.20 | - | - | 0.0472 | - |
| G2 | - | 1.0 | - | - | 0.0394 | - |
| G3 | - | 0.80 | - | - | 0.0315 | - |
| h | 0.30 | - | 0.40 | 0.0118 | - | 0.0157 |
| L | 0.55 | 0.70 | 0.85 | 0.0217 | - | 0.0335 |
| L1 | 1.40 REF | | | 0.0551 REF | | |
| L2 | 0.25 BSC | | | 0.0098 BSC | | |
| N | 24 (# lead) | | | | | |
| R | 0.30 | - | - | 0.0118 | - | - |
| R1 | 0.20 | - | - | 0.0079 | - | - |
| S | 0.25 | - | - | 0.0098 | - | - |

Table 37. PowerSSO-24 (exposed pad) package mechanical data (continued)

| Ref | Dimensions | | | | | |
|---------------------------------------|-------------|------|------|-----------------------|------|--------|
| | Millimeters | | | Inches ⁽¹⁾ | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| Tolerance of form and position | | | | | | |
| aaa | 0.20 | | | 0.0079 | | |
| bbb | 0.20 | | | 0.0079 | | |
| ccc | 0.10 | | | 0.0039 | | |
| ddd | 0.20 | | | 0.0079 | | |
| eee | 0.10 | | | 0.0039 | | |
| fff | 0.20 | | | 0.0079 | | |
| ggg | 0.15 | | | 0.0059 | | |
| VARIATIONS | | | | | | |
| Option A | | | | | | |
| D1 | 6.5 | - | 7.1 | 0.2559 | - | 0.2795 |
| E2 | 4.1 | - | 4.7 | 0.1614 | - | 0.1850 |
| Option B | | | | | | |
| D1 | 4.9 | - | 5.5 | 0.1929 | - | 0.2165 |
| E2 | 4.1 | - | 4.7 | 0.1614 | - | 0.1850 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

Table 38. PowerSSO-36 (exposed pad) package mechanical data (continued)

| Ref | Dimensions | | | | | |
|---------------------------------------|------------------|------|------|-----------------------|--------|--------|
| | Millimeters | | | Inches ⁽¹⁾ | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A1 | 0.0 | - | 0.1 | 0.0 | - | 0.0039 |
| A2 | 2.15 | - | 2.35 | 0.0846 | - | 0.0925 |
| b | 0.18 | - | 0.32 | 0.0071 | - | 0.0126 |
| b1 | 0.13 | 0.25 | 0.3 | 0.0051 | 0.0098 | 0.0118 |
| c | 0.23 | - | 0.32 | 0.0091 | - | 0.0126 |
| c1 | 0.2 | 0.2 | 0.3 | 0.0079 | 0.0079 | 0.0118 |
| D ⁽²⁾ | 10.30 BSC | | | 0.4055 BSC | | |
| D1 | VARIATION | | | | | |
| D2 | - | 3.65 | - | - | 0.1437 | - |
| D3 | - | 4.3 | - | - | 0.1693 | - |
| e | 0.50 BSC | | | 0.0197 BSC | | |
| E | 10.30 BSC | | | 0.4055 BSC | | |
| E1 ⁽²⁾ | 7.50 BSC | | | 0.2953 BSC | | |
| E2 | VARIATION | | | | | |
| E3 | - | 2.3 | - | - | 0.0906 | - |
| E4 | - | 2.9 | - | - | 0.1142 | - |
| G1 | - | 1.2 | - | - | 0.0472 | - |
| G2 | - | 1 | - | - | 0.0394 | - |
| G3 | - | 0.8 | - | - | 0.0315 | - |
| h | 0.3 | - | 0.4 | 0.0118 | - | 0.0157 |
| L | 0.55 | 0.7 | 0.85 | 0.0217 | - | 0.0335 |
| L1 | 1.40 REF | | | 0.0551 REF | | |
| L2 | 0.25 BSC | | | 0.0098 BSC | | |
| N | 36 | | | 1.4173 | | |
| R | 0.3 | - | - | 0.0118 | - | - |
| R1 | 0.2 | - | - | 0.0079 | - | - |
| S | 0.25 | - | - | 0.0098 | - | - |
| Tolerance of form and position | | | | | | |
| aaa | 0.2 | | | 0.0079 | | |
| bbb | 0.2 | | | 0.0079 | | |
| ccc | 0.1 | | | 0.0039 | | |
| ddd | 0.2 | | | 0.0079 | | |

Table 38. PowerSSO-36 (exposed pad) package mechanical data (continued)

| Ref | Dimensions | | | | | |
|-------------------|-------------|------|------|-----------------------|------|--------|
| | Millimeters | | | Inches ⁽¹⁾ | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| eee | 0.1 | | | 0.0039 | | |
| fff | 0.2 | | | 0.0079 | | |
| ggg | 0.15 | | | 0.0059 | | |
| VARIATIONS | | | | | | |
| Option A | | | | | | |
| D1 | 6.5 | - | 7.1 | 0.2559 | - | 0.2795 |
| E2 | 4.1 | - | 4.7 | 0.1614 | - | 0.1850 |
| Option B | | | | | | |
| D1 | 4.9 | - | 5.5 | 0.1929 | - | 0.2165 |
| E2 | 4.1 | - | 4.7 | 0.1614 | - | 0.1850 |
| Option C | | | | | | |
| D1 | 6.9 | - | 7.5 | 0.2717 | - | 0.2953 |
| E2 | 4.3 | - | 5.2 | 0.1693 | - | 0.2047 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

8 Revision history

Table 39. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 27-Jul-2015 | 1 | Initial release. |
| 28-Oct-2015 | 2 | Added: – New commercial part number in <i>Table 1: Device summary on page 1</i> ; – <i>Figure 4: PSSO36 (Single version) pin connection (top view) on page 8</i> ; – <i>Table 4: L9959U (Single version in PSSO36) pin out on page 12</i> . Corrected in <i>Table 10: VDD monitoring on page 15</i> the test conditions of V_{ABE_OUTL} . Updated <i>Description on page 1</i> . |
| 25-Feb-2016 | 3 | Corrected typo in the <i>Table 10: VDD monitoring on page 15</i> (Test condition column of the ' V_{ABE_OUTL} ' parameter). |

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